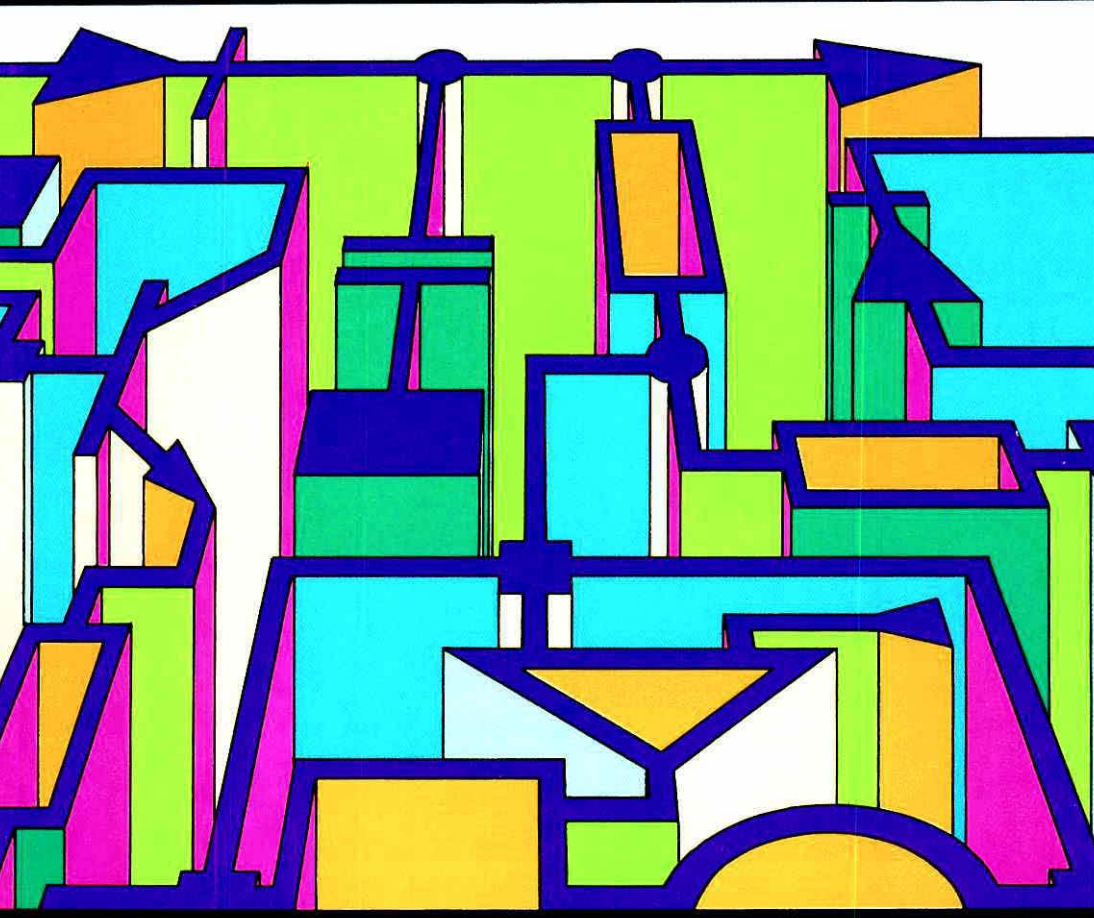
VIDEO PRODUCTS

APPLICATION MANUAL

1st EDITION



SGS-THOMSON
MICROELECTRONICS

VIDEO PRODUCTS

APPLICATION MANUAL

1st EDITION

JULY 1991

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SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

SGS-THOMSON's dedicated video product range is now so extensive that it has been necessary to divide the databook into two volumes: one for power devices and graphic circuits and one for signal devices. Application notes for video products have been gathered together in the video products Application Manual.

Volume 1, Signal Processing Products, covers chroma and video ICs, single-chip processors, video switch matrices and other signal level parts. In this area the company specializes in offering complete solutions all of the ICs needed for a specific TV or monitor chassis type and gives special attention to the basic solutions. Much of the knowhow in this field has been gained in the demanding Asia/Pacific market for the cost effective aspect, and in western Europe for PAL/SECAM multistandard design, placing SGS-THOMSON in a very strong position in the emergent East European market the new frontier in consumer electronics.

Volume 2, Power & Graphics Products, covers power ICs such as deflection boosters and sound channels, plus other ICs for graphics monitor deflection applications. In the monitor market SGS-THOMSON is the recognized world leader; in fact today 7 out of 10 monitors produced in the world include SGS-THOMSON ICs. Power ICs in general are a traditional specialty of the company, which began producing monolithic power amplifiers in the 60's and has remained at the forefront of power technology development ever since.

With these two volumes SGS-THOMSON Microelectronics proposes a dedicated video product range that satisfies virtually every need in television, monitor, VCR and related applications. And if you don't find the product you are looking for in these volumes contact the nearest SGS-THOMSON office; it may be that the product you want is included in other books covering micros, memories, standard ICs or discretes.

The Video Products Application Manual is part of the comprehensive technical support offered by SGS-THOMSON's Video Division to make application design fast and productive. This support also includes PC design aids and evaluation boards.

ALPHANUMERICAL INDEX

APPLICATION NOTES

VERTICAL DEFLECTION CIRCUITS FOR TV & MONITOR

by Alessandro MESSI

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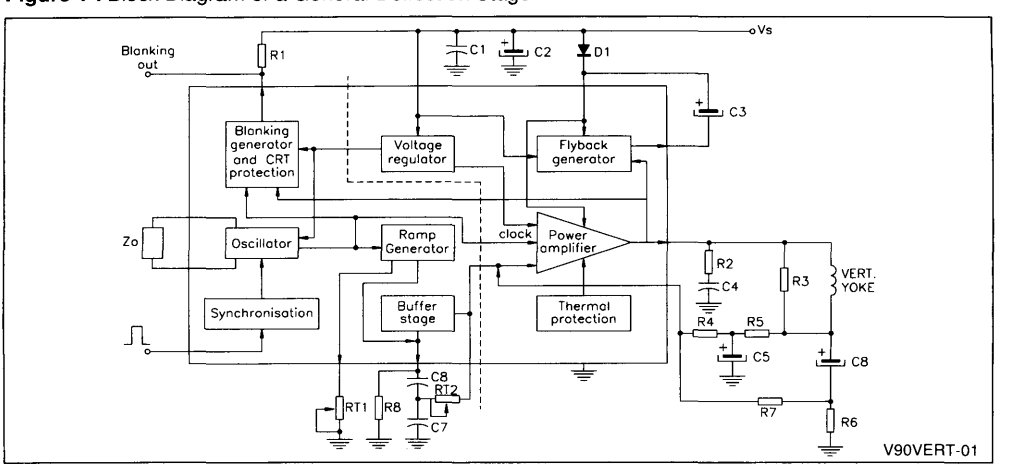
1. INTRODUCTION

In a general way we can define vertical stages circuits able to deliver a current ramp suitable to drive the vertical deflection yoke.

In Figure 1 is represented the more general possible block diagram of a device performing the vertical deflection.

Figure 1 : Block Diagram of a General Deflection Stage.

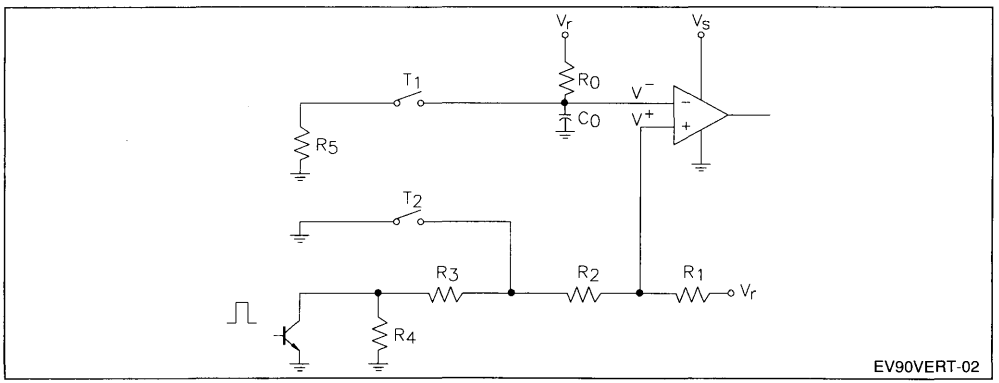


Such a device will be called "complete vertical stage" because it can be simply driven by a synchronization pulse and it comprises all the circuitry necessary to perform the vertical deflection that is : oscillator, voltage ramp generator, blanking genetor, output power and flyback generator.
At the right side of the dotted line in Figure 1 is represented the circuitry characterizing a "vertical output stage". This kind of device comprises only the power stages and it has to be driven by a voltage sawtooth generated by a previous circuit (for example a horizontal and vertical synchronization stage.
In the first class there are the following devices : TDA1170D, TDA1170N, TDA1170S, TDA1175, TDA1670A, TDA1675, TDA1770A, TDA1872A, TDA8176.
In the second class there are : TDA2170, TDA2270, TDA8170, TDA8172, TDA8173, TDA8175, TDA8178, TDA8179.
There is also a third class of vertical stages comprising the voltage ramp generator but without the oscillator; these circuits must be driven by an already synchronized pulse. In this third class there are : TDA1771 and TDA8174.

2. OSCILLATOR

There are two different kinds of oscillator stages used in SGS-THOMSON complete vertical deflections, one is used in TDA1170D, TDA1170N, TDA1170S, TDA1175 and TDA8176, the other in TDA1670A, TDA1675, TDA1170A and TDA1872A.
The principle of the first kind of oscillator is represented in Figure 2.
The following explanations will be the more general possible; we shall inform the reader when we refer to a particular device.

Figure 2 : First Kind of Oscillator Stage.

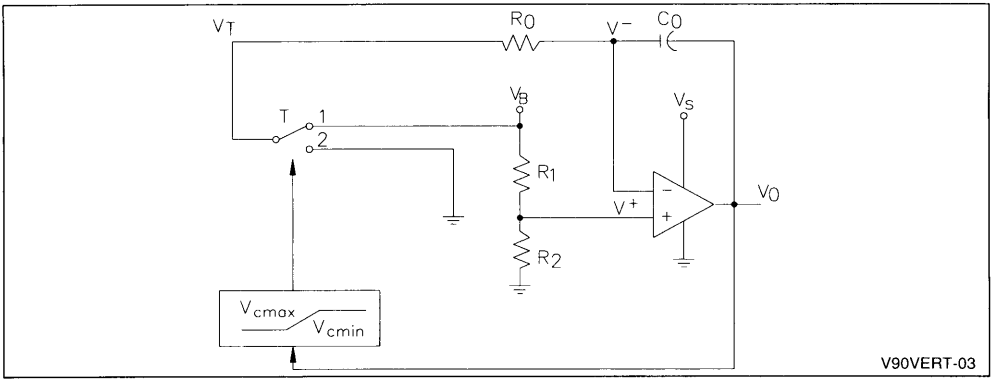


When the switches T_1 and T_2 are opened the C_O capacitor charges exponentially through R_O to the value $V^+_{(MAX)}$ determined by the integrated resistors R_1, R_2, R_3 and R_4. At this point the switches are closed, short-circuiting R_3 and R_4, so the voltage at the non-inverting input becomes $V^+_{(MIN)}$. The capacitor C_O discharges to this value through the integrated resistor R_5.
The free running frequency can be easily calculated resulting in :

$$T_O = R_O \cdot C_O \cdot \log \frac{V_R - V^+_{(MIN)}}{V_R - V^+_{(MAX)}} + R_5 \cdot C_O \cdot \log \frac{V^+_{(MAX)}}{V^+_{(MIN)}} \qquad (1) \qquad f_O = \frac{1}{T_O}$$

with R_O = 360 kΩ and C_O = 100 nF, it results in 43.7 Hz.
The oscillator synchronization is obtained reducing the superior threshold $V^+_{(MAX)}$ short-circuiting the R_4 resistor when a vertical synchronization pulse occurs.
The second kind of oscillator is represented in Figure 3.

Figure 3 : Second Kind of Oscillator Stage.



When the switch T is in position 2, a constant current $I_{CO} = V^- / R_O$ flows through C_O charging it with a voltage ramp. When the voltage V_O reaches $V_{O(MAX)}$, T passes in position 1, so a constant current $I_{CO} = (V_B - V^-) / R_O$ discharges the capacitor causing the inversion of the voltage ramp slope at the output V_O (t). The discharges stops when V_O reaches the value $V_{O(MIN)}$ and the cycle takes place again.

It is possible to calculate the free running frequency f_O with the following formula :

$$T_O = \frac{(V_{O(MAX)} - V_{O(MIN)}) \cdot R_O \cdot C_O}{V^-} + \frac{(V_{O(MAX)} - V_{O(MIN)}) \cdot R_O \cdot C_O}{V_B - V^-} \qquad (2)$$

with $V_{O(MAX)} - V_{O(MIN)} = 3.9V$, $V_B = 6.5V$, $V^- = 0.445V$, $R_O = 7.5k\Omega$ and $C_O = 330nF$ it results in : $f_O = 43.8Hz$.

The oscillator synchronization is still obtained in the above mentioned way.

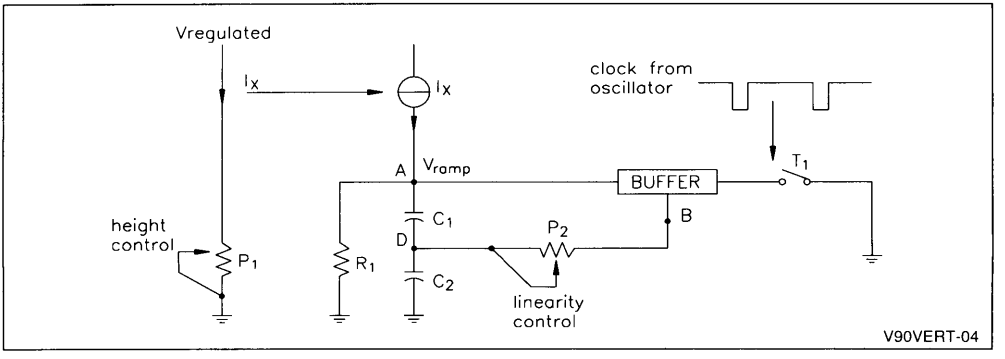
In order to guarantee a minimum pull-in range of 14Hz the threshold value has been chosen in $V_P = 4.3V$.

The spread of the free running frequency in this kind of oscillator is very low because it mainly depends from the threshold values $V_{O(MAX)}$, $V_{O(MIN)}$ and V^- that are determined by resistor rates that can be done very precise.

3. RAMP GENERATOR

The ramp generator is conceptually represented in Figure 4.

Figure 4 : Ramp Generator.



The Voltage ramp is obtained charging the group R_1, C_1 and C_2 with a constant current I_X.

It is easy to calculate the voltage V_{RAMP} That results in :

$$V_{RAMP}(t) = (V_{(MIN)} - R_1 \cdot I_X)\ e^{-\frac{t}{R_1 \cdot C}} + R_1 \cdot I_X \qquad (3)$$

where $V_{(MIN)}$ is the voltage in A when the charge starts and C is the series of C_1 and C_2.
The resistor R_1 is necessary to give a "C correction" to the voltage ramp. The ramp amplitude is determined by $I_X = V_{REG} / P_1$,so the potentiometer P_1 is necessary to perform the height control.
The voltage ramp is then transferred on a low impedence in B through a buffer stage.
Te P2 potentiometer connected between D and B performs the ramp linearity control or "S correction" that is necessary to have a correct reproduction of the images on the TV set.
The voltage ramp in B grows up until the switch T_1 is closed by a clock pulse coming from the oscillator; in this way the capacitors discharge fastly to $V_{(MIN)}$ that is dependent upon the saturation voltage of the transistor that realizes the switch.
At this point the exponential charge takes place again.

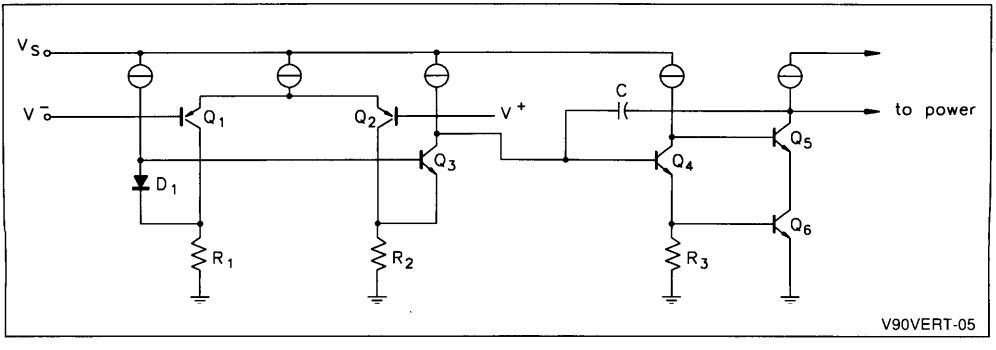
4. BLANKING GENERATOR AND CRT PROTECTION

This circuit senses the presence of the clock pulse coming from the oscillator stage and the flyback pulse on the yoke. If both of them are present a blanking pulse is generated able to blank the CRT during the retrace period. The duration of this pulse is the same of the one coming from the oscillator.
If for any reason the vertical deflection would fail, for instance for a short circuit or an open circuit of the yoke, the absence of the flyback pulse puts the circuit in such a condition that a continuous vertical blanking is generated in order to protect the CRT against eventual damages.
This circuit is available only in the following devices : TDA1670A, TDA1675, TDA1770A and TDA1872A.
The stages we will consider starting from this point are common both to complete vertical stages and vertical output stages.

5. POWER AMPLIFIER STAGE

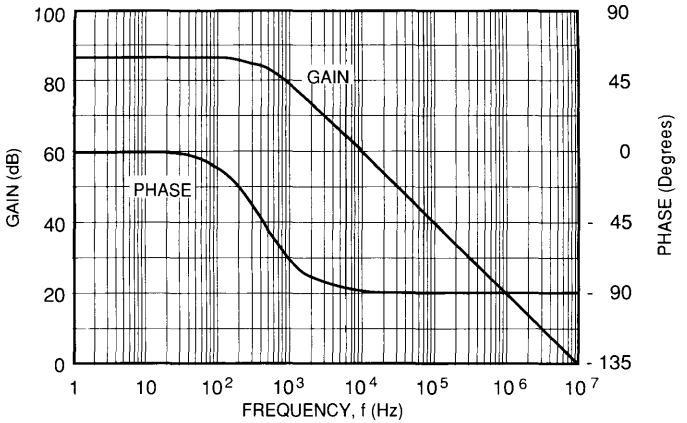
This stage can be divided into two distinct parts : the amplifier circuit and the output power.
The amplifier is realized with a differential circuit; a schematic diagram is represented in Figure 5.

Figure 5 : Amplifier Stage.



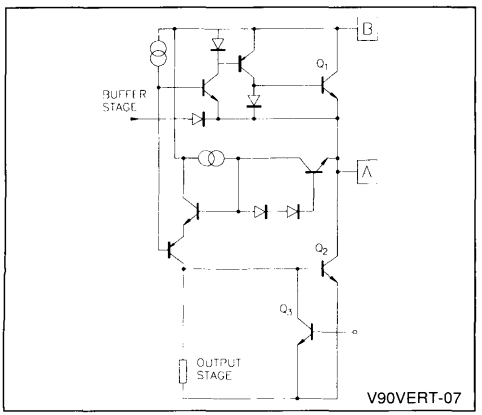
The open-loop gain of the circuit is variable from 60dB to 90dB for the different integrated circuits.
The compensation capacitor C determines the dominant pole of the amplifier. In order to obtain a dominant pole in the range of 400Hz, the capacitor must be of about 10pF.
As an example in Figure 6 is represented the boole diagram of the amplifier open loop gain for TDA8172.

Figure 6 : Amplifier Open Loop Gain and Phase.



The output power stage is designed in order to deliver to the yoke a vertical deflection current from 1 to 2 Apeak, depending upon the different devices, and able to support flyback voltages up to 60V. A typical output stage is depicted in Figure 7.

Figure 7 : Power Stage.



The upper power transistor Q_1 conducts during the first part of the scanning period when the vertical deflection current is flowing from the supply voltage into the yoke; when the current becomes negative, that is it comes out of the yoke, it flows through the lower power transistor Q_2.The circuit connected between the two output transistors is necessary to avoid distortion of the current at the crossing of zero, when Q_1 is turned off and Q_2 is turned on. When the flyback begins, Q_2 is switched-off by Q_3 in order to make it able to support the high voltage of the flyback pulse.
The circuit behaviour during flyback is explained in chapter 7.

6. THERMAL PROTECTION

The thermal protection is available in all the devices except the TDA1170 family and the TDA8176.
This circuit is usefull to avoid damages at the integrated circuit due to a too high junction temperature caused by an incorrect working condition.
It is possible to sense the silicon temperature because the transistor V_{BE} varies of - 2 mV/ °C, so a temperature variation can be reconducted to a voltage variation.
If the temperature increases and it is reaching 150°C, the integrated circuit output is shut down by putting off the current sources of the power stage.

7. FLYBACK BEHAVIOUR

In order to obtain sufficiently short flyback times, a voltage greather than the scanning voltage must be applied to the deflection yoke.
By using a flyback generator, the yoke is only supplied with a voltage close to double the supply during flyback.
Thus, the power dissipated is reduced to approximately one third and the flyback time is halfed.

The flyback circuit is shown in Figure 8 together with the power stage.

Figure 8 : Output Power and Flyback stages.

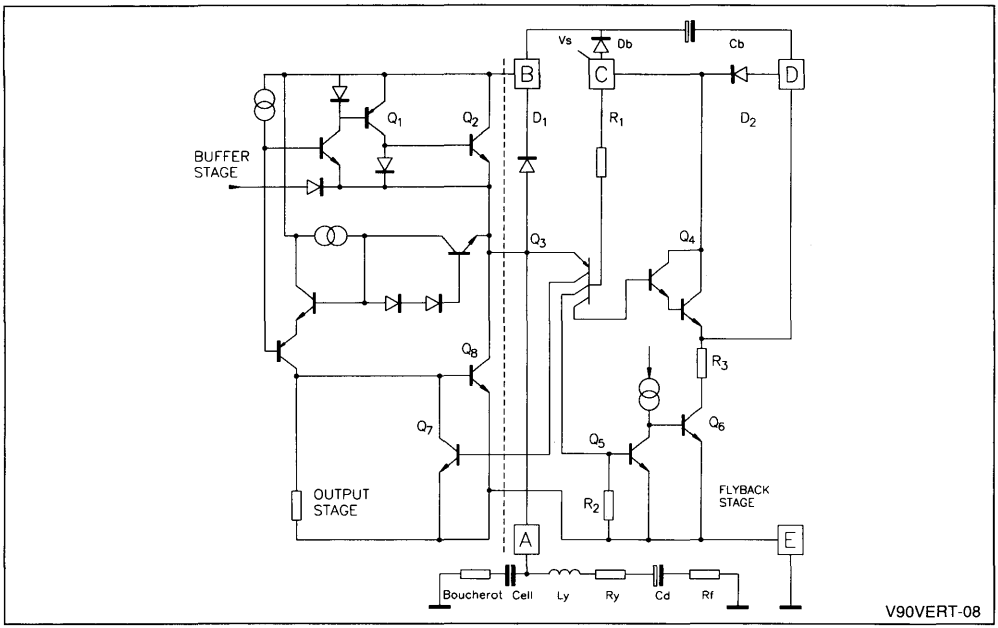
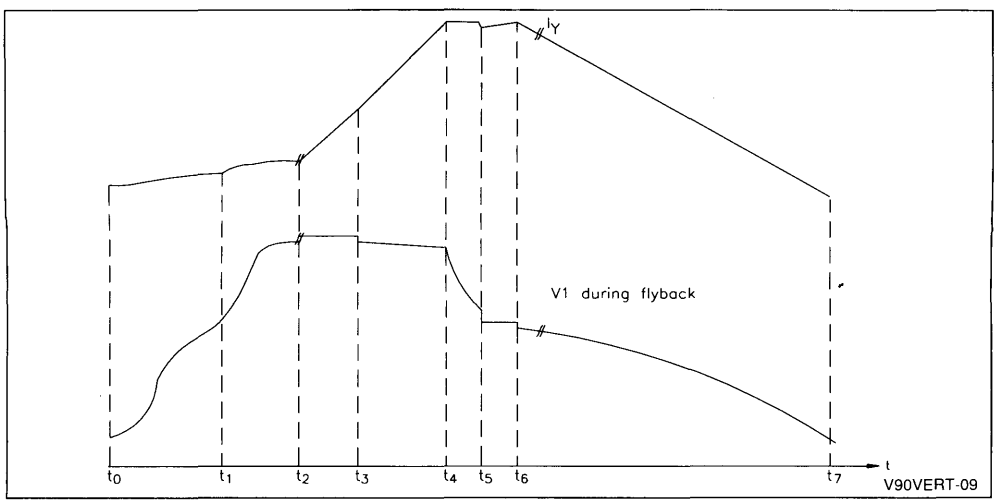


Figure 9 shows the circuit behaviuor, to show operation clearly. The graphs are not drawn to scale. Certain approximations are made in the analysis in order to eliminate electrical parameters that do not significantly influence circuit operations.

Figure 9 : Current in the Yoke and Voltage Drop on the Yoke during Vertical Deflection.



a) Scan period (t_6 - t_7) : Figure 10

During scanning Q_3, Q_4 and Q_5 are off and this causes Q_6 to *saturate*.

A current from the voltage supply to ground flows through D_B, C_B and Q_6 charging the C_B capacitor up to :

$VC_B = V_S - VD_B - VQ_{6SAT}$ (4)

At the end of this period the scan current has reached its peak value (I_P) and it is flowing from the yoke to the device. At the same time V_A has reached its minimum value.

In Figures 11 and 12 are depicted the voltage drop on the yoke and the currents flowing through D_B and the yoke.

Figure 10 : Circuit Involved during Scan Period.

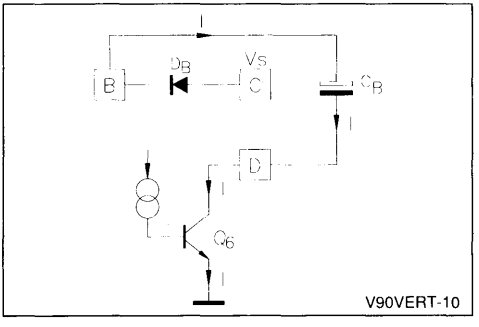


Figure 11 : Voltage Drop on the Yoke and Current Flowing through D_B.
V = 10V/div.
I = 0.5A/div.
t = 2ms/div.

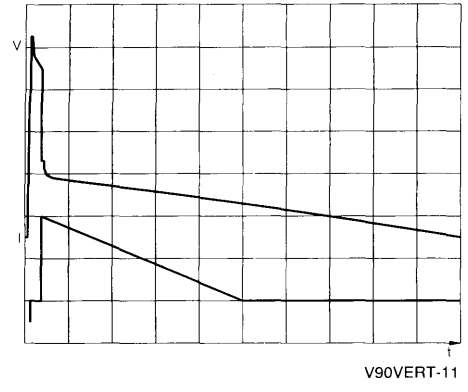


Figure 12 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 1A/div.
t = 5ms/div.

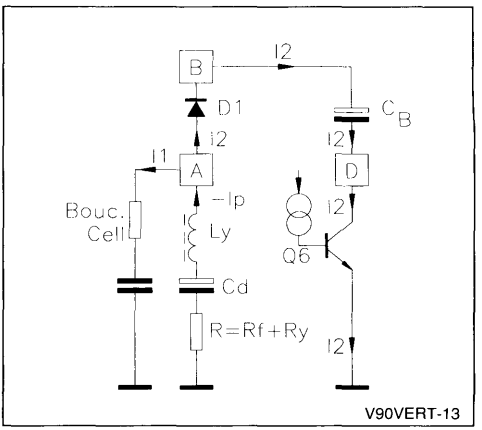
b) Flyback starting (t_0 - t_1) : Figure 13

Q_8, that was conducting the - I_P current, is turned off by the buffer stage.

The yoke, charged to I_P, now forces this current to flow partially through the Boucherot cell (I_1) and partially through D_1, C_B and Q_6 (I_2).

In Figures 14, 15 and 16 are represented the currents flowing through the yoke, the Boucherot cell and D_1.

Figure 13 : Circuit Involved during Flyback Starting.



c) Flyback starting (t_1 - t_2)

When the voltage drop at pin A rises over V_S, Q_3 turns on and this causes Q_4 and Q_5 to saturate. Consequently Q_6 turns off.

During this period the voltage at pin D is forced to :

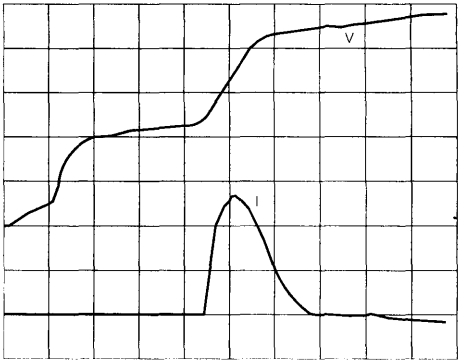
$$V_D = V_S - VQ_{4SAT} \quad (5)$$

Therefore the voltage at pin B becomes :

$$V_B = V_{CB} + V_D \quad (6)$$

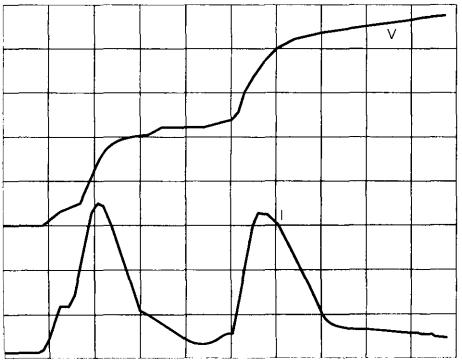
The yoke current flows in the Boucherot cell added to another current peak flowing from V_S via Q_4 and C_B (Figures 14 and 15).

Figure 15 : Voltage Drop on the Yoke and Current Flowing through D_1.
V = 10V/div.
I = 1A/div.
t = 1µs/div.



V90VERT-15

Figure 14 : Voltage Drop on the Yoke and Current Flowing through the Boucherot Cell.
V = 10V/div.
I = 1A/div.
t = 1µs/div.



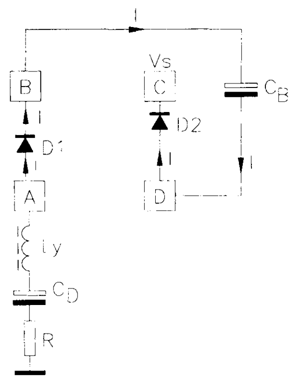
V90VERT-14

Figure 16 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 100mA/div.
t = 1µs/div.

V90VERT-16

d) Negative current rise (t_2 - t_3) : Figure 17

Figure 17 : *Circuit Involved* during the Negative Current Rise.



V90VERT-17

During this period, the voltage applied at pin A is :

$$V_A = V_B + V_{D1},$$
$$V_A = V_{CB} + V_D + V_{D1},$$
$$V_A = V_S - V_{DB} - VQ_{6SAT} + V_S + V_{D2} + V_{D1},$$
$$V_A = 2 \cdot V_S + V_{D1} + V_{D2} - V_{DB} - VQ_{6SAT} \qquad (7)$$

It is possible to calculate the current solving the following equation :

$$V_A = L_Y \frac{di}{dt} + \frac{1}{C_D} \int i \cdot dt + R \cdot i \qquad (8)$$

where $R = R_F + R_Y$

Because the voltage at pin A is approximatively constant (error less than 2%) we can simplify the (8) in the following equation :

$$\frac{d^2 i}{dt^2} + \frac{R}{L_Y} \frac{di}{dt} + \frac{1}{L_Y C_D} i = 0 \qquad (9)$$

It results in :

$$i(t) = \frac{I_P}{e^{2\beta \Delta T_1} - 1} e^{(-\alpha + \beta) t} - \frac{I_P}{1 - e^{-2\beta \Delta T_1}} e^{(-\alpha - \beta) t} \qquad (10)$$

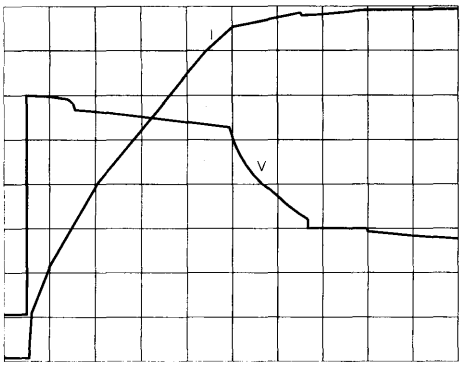
where :

$$\alpha = \frac{R}{2 L_Y} \qquad \beta = \sqrt{\frac{R^2}{4 \cdot L_Y^2} - \frac{1}{L_Y C_D}} \qquad \Delta T_1 = t_3 - t_2$$

Because of ΔT_1 is two orders of magnitude lower than the scan time, we can apply an exponential sum to obtain the following equation :

$$i(t) = I_P \frac{\alpha \cosh(2\beta \Delta T_1) + \beta \sinh(2\beta \Delta T_1) - \alpha}{\cosh(2\beta \Delta T_1) - 1} t - I_P \qquad (11)$$

Figure 18 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 250mA/div.
t = 100µs/div.



V90VERT-18

Simplifying :

$$i(t) = I_P \left(\alpha + \frac{1}{\Delta T_1} \right) t - I_P \qquad (12)$$

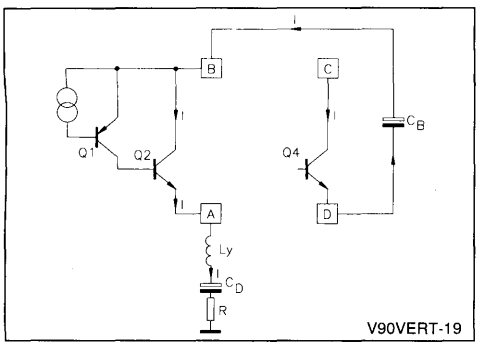
The slope of the current is therefore :

$$\frac{di}{dt} = \left(\frac{R}{2\,L_Y} + \frac{1}{\Delta T_1} \right) I_P \quad (A/s) \qquad (13)$$

The current flows from the yoke to V_S through D_1, C_B and D_2, and it is depicted in Figure 18.

e) Positive current rise (t_3 - t_4) : Figure 19

Figure 19 : Circuit Involved during the Positive Current Rise.



V90VERT-19

When the current becomes zero, D_1 turns off and Q_2 saturates; so the pin A voltage becames :

$$V_A = V_B - VQ_{2SAT}$$
$$V_A = 2 \cdot V_S - V_{DB} - VQ_{6SAT} - VQ_{4SAT} - VQ_{2SAT} \qquad (14)$$

The current flows from $+V_S$ into the yoke through Q_4, C_B and Q_2 and rises from zero to I_P as it can be seen in Figure 18.
By using the previous procedure explained in section d), we can obtain the slope of the current :

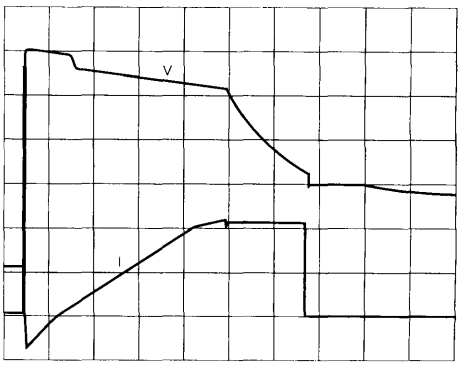
$$\frac{di}{dt} = \left(\frac{R}{2\,L_Y} + \frac{1}{\Delta T_2} \right) I_P \quad (A/s) \qquad (15)$$

where $\Delta T_2 = t_4 - t_3$

f) Flyback decay (t_4 - t_5)

When the yoke current reaches its maximum peak, Q_2 desaturates and conducts the maximum peak current flowing from V_S via Q_4 and C_B into L_Y; the current flowing through C_B is depicted in Figure 20.

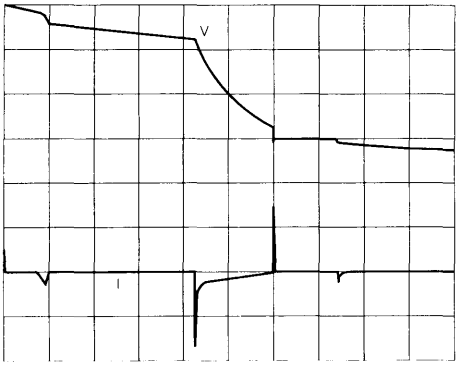
Figure 20 : Voltage Drop on the Yoke and Current Flowing through C_B.
V = 10V/div.
I = 0.5A/div.
t = 100µs/div.



V90VERT-20

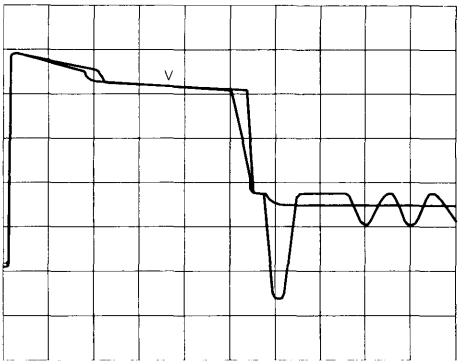
An eventual antiringing parallel resistor modify the linear decay slope in an exponential one, as it can be seen in Figure 22.
This continues until the buffer stage turns Q_2 on.
The effect of the Boucherot cell during this periode is negligible (see Figure 21).

Figure 21 : Voltage Drop on the Yoke and Current Flowing through the Boucherot Cell.
V = 10V/div.
I = 100mA/div.
t = 100µs/div.



V90VERT-21

Figure 22 : Effect of the Resistor in Parallel connected to the yoke.
V = 10V/div.



V90VERT-22

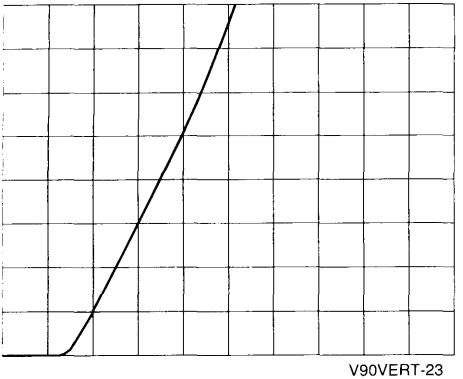
g) V_A pedestal (t_5 - t_6)

When V_A reaches the value V_S of the supply voltage, the flyback generator stops its function.
Q_3 is turned off and turns off Q_4 that open the connection between pin D and V_S.
Therefore V_B drops to V_S - V_{DB} while : $V_A = V_S - V_{DB} - VQ_{2CE\ on}$
At this point the normal scan takes place.

8. CURRENT-VOLTAGE CHARACTERISTICS OF THE RECIRCULATING DIODES.

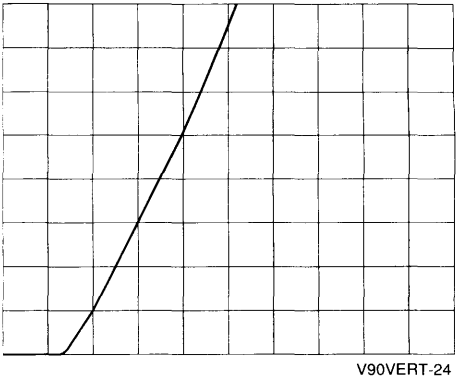
The following Figures 23 and 24 reproduce the I - V characteristics of the integrated recirculating diodes D_1 and D_2 (see Figure 8).

Figure 23 : I - V Characteristic of the Diode D_1.
V = 500mV/div.
I = 200mA/div.



V90VERT-23

Figure 24 : I - V Characteristic of the Diode D_2.
V = 500mV/div.
I = 200mA/div.



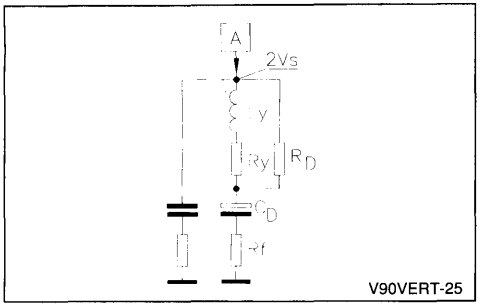
V90VERT-24

These characteristics are useful in order to calculate the maximum voltage reached at pin A with the formula (7) explained in chapter 7.

9. CALCULATION PROCEDURE OF THE FLY-BACK DURATION

The flyback duration can be calculated using the following procedure (referring to Figure 25).

Figure 25 : Circuit Involved in the Calculation of Flyback Duration.



During the flyback period the voltage applied at pin A is about 2 V_S, as previously explained in chapter 7. The voltage drop across C_D is approximatively a constant voltage little less than V_S /2. The voltage on the feedback resistor R_F is :

$VR_F(t) = R_F\ I_Y(t)$

so in the period which we are considering it is negligible respect to $V_S/2$.

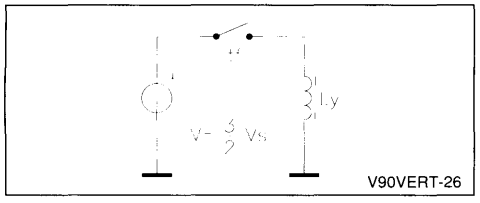
The effect of the Boucherot cell during this period is not sensible as it can be seen in Figure 21; while R_D acts principally during the flyback decay time (Figure 9 : t_4 - t_5) reducing its slope and the resulting oscillations but doesn't influence the total flyback time as shown in Figure 22. So their influences are also negligible.

Now the effective voltage drop across the yoke can be approximated to :

$$2 \cdot V_S - \frac{V_S}{2} = \frac{3}{2} V_S$$

Figure 25 can be simplified as shown in Figure 26.

Figure 26 : Simplified Circuit for the Calculation of Flyback Duration.



The voltage charges the coil with a linear current that can be calculated in the following way :

$$i(t) = \frac{1}{L_Y} \int V \cdot dt = \frac{1}{L_Y} \int \frac{3}{2} V_S \cdot dt \quad (16)$$

$$i(t) = \frac{1}{L_Y} \frac{3}{2} V_S \cdot t + K$$

K is calculated imposing that the current at the beginning of the flyback is - I_P.

$$i(0) = -I_P \qquad K = -I_P$$

$$i(t) = \frac{3}{2} \frac{V_S}{L_Y} t - I_P \quad (17)$$

At the end of the flyback period the current will be + I_P, so we can write :

$$I_P = \frac{3}{2} \frac{V_S}{L_Y} t_F - I_P$$

The duration of the flyback period is then :

$$t_F = \frac{4}{3} \frac{I_P L_Y}{V_S} = \frac{2}{3} \frac{I_Y L_Y}{V_S} \quad (18)$$

10. APPLICATION INFORMATION

The vertical deflection stages producted by SGS-THOMSON are able to cover the complete range of applications that the market need for color television and high/very high resolution monitors.

Television and monitor applications are not very different but in monitor field, in addition to the linearity and interlacing problems, we have to pay attention to the flyback time that must be very short for very high resolution models.

In television applications the most important requirement is to choose the lowest supply voltage possible in order to minimize the power dissipation in the integrated circuit, reducing the dimension of the heatsink, and the power dissipation from the voltage supplier.

These results can be reached very easily with SGS-THOMSON deflection stages because of the high efficiency of the flyback generator circuit used.

In high resolution monitors one of the main problems is to reach the very short flyback time requested; the flyback generator, together with the high current and power dissipation capabilities, solve all the problems in a simple way.

In Figures 27, 28 and 29 are depicted three typical application circuits for the different kinds of integrated circuits available.

Figure 27 : Application Circuit for TDA1170.

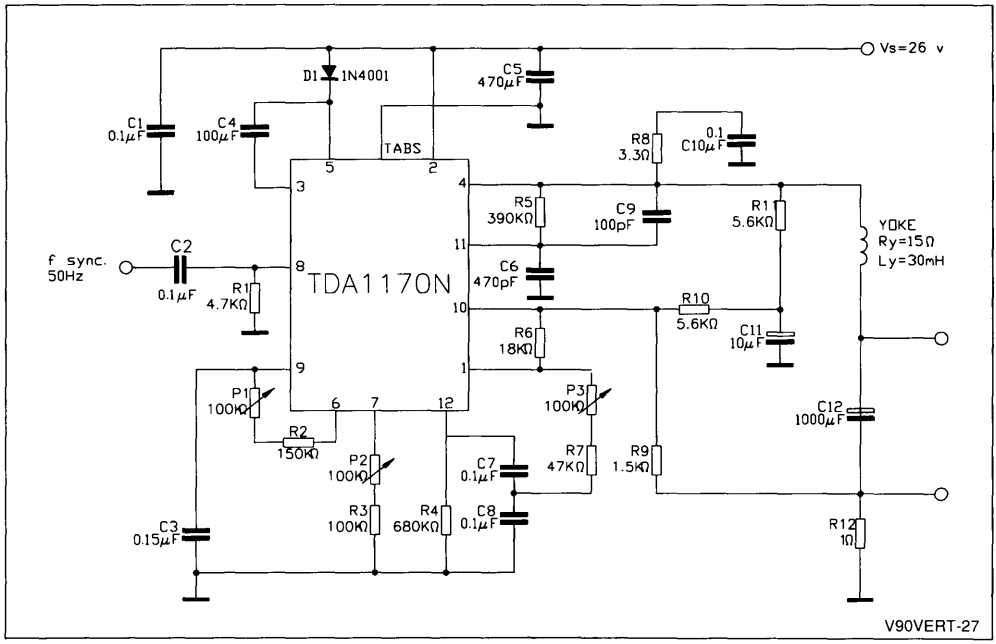
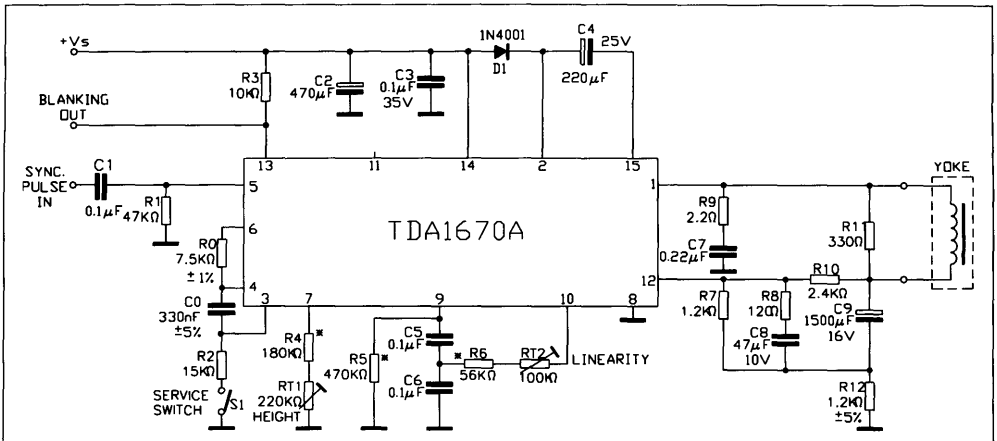
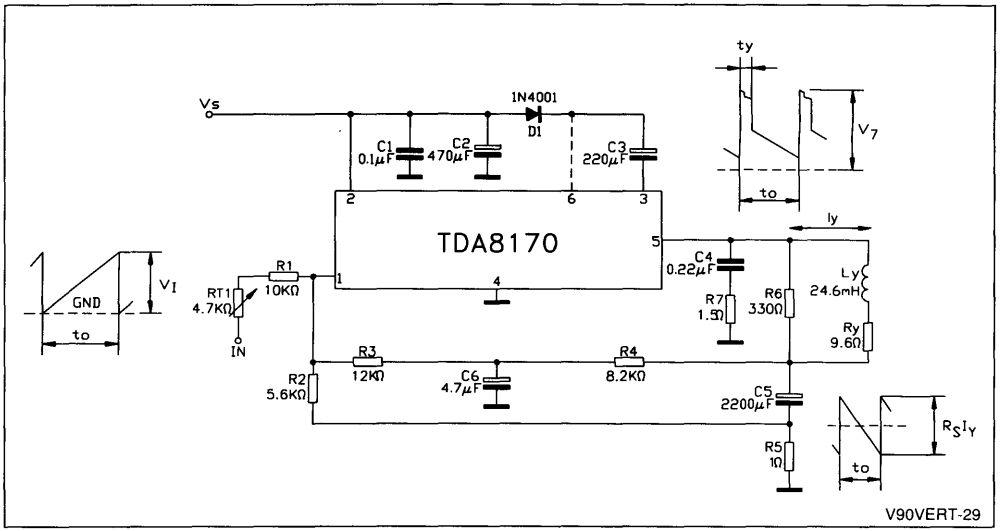


Figure 28 : Application Circuit for TDA1670A.



* The value depends on the characteristics of the CRT. The value shown is indicative only.

Figure 29 : Application Circuit for TDA8170.



In the following chapters we shall do the calculation for television and monitor in order to choose the right voltage supply and external network for the yoke used and the current requirements.

11. SUPPLY VOLTAGE CALCULATION

For television applications we shall calculate the minimum supply voltage necessary to have vertical scanning knowing the yoke characteristics and the current required for the given application.
Figure 30 shows the terms used in this section, while the circuit part involved in the following calculations is depicted in Figure 31.

Figure 30 : Parameters Used in the Calculation of the Supply Voltage.

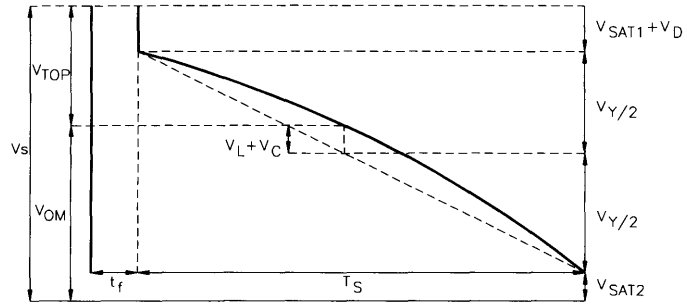
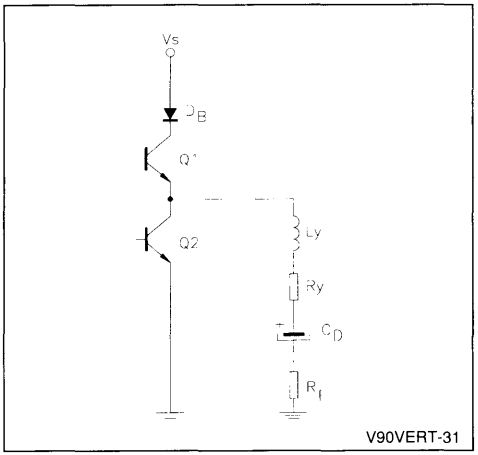


Figure 31 : Circuit Involved in the Calculation of the Supply Voltage.



V_S = supply voltage.
V_Y = nominal voltage required to produce the scanning current including the feedback resistance and the 20% increasing for temperature variations in the yoke current;

$$V_Y = (1.2\, R_Y + R_F)\, I_Y \qquad (19)$$

V_{SAT1} = nominal output saturation voltage due to the upper power transistor Q_1 (see Figure 32);
V_{SAT2} = nominal output saturation voltage due to the lower power transistor Q_2 (see Figure 33);
V_{OM} = nominal quiescent voltage (midpoint) on the output power transistors;
V_C = voltage peak due to the charge of C_D capacitor;

$$V_C = \frac{I_Y \cdot t_S}{8 \cdot C_D} \qquad (20)$$

V_L = voltage drop due to the yoke inductance L_Y;

$$V_L = \frac{L_Y \cdot I_Y}{t_S} \qquad (21)$$

Figure 32 : Saturation characteristic of the Upper Power Transistor.

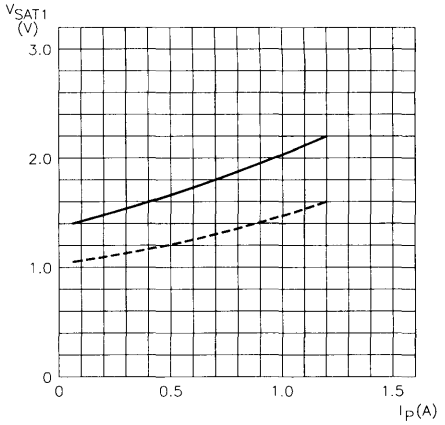
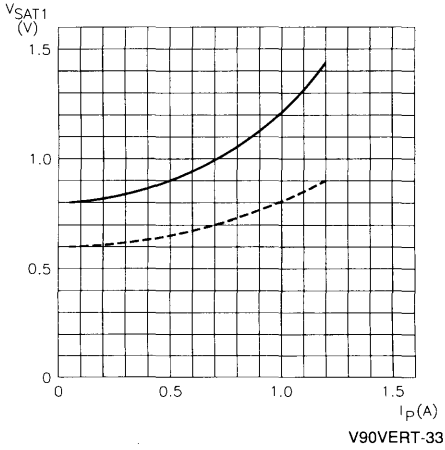


Figure 33 : Saturation characteristic of the Lower Power Transistor.



V_D = nominal voltage drop on D_B diode in series with the supply;
T = vertical scan period;
t_F = flyback time;

$$t_F = \frac{2}{3} \frac{I_Y \cdot L_Y}{V_S}$$

t_S = scanning time;

$$t_S = T - t_F$$

I_Y = peak to peak deflection current;
R_Y = nominal yoke resistance;
L_Y = nominal yoke inductance;
R_F = feedback resistor.

Referring to Figure 30 it is easy to see that the minimum supply voltage is given by :

$$V_S = V_{OM} + V_{TOP} \qquad (22)$$

where :

$$V_{OM} = \frac{V_Y}{2} + V_{SAT2} + V_C + V_L \qquad (23)$$

and :

$$V_{TOP} = \frac{V_Y}{2} + V_D + V_{SAT1} - V_L - V_C \qquad (24)$$

So we obtain :

$$V_S = V_Y + V_D + V_{SAT1} + V_{SAT2} \qquad (25)$$

The (25) gives the minimum voltage supply if we do not consider the tolerances of the integrated circuit and of the external components, but the calculation, even if it was not realistic, it was useful in order to understand the procedure.
Now we shall do the same thing considering all the possible spreads; we can in this way obtain the real minimum supply voltage.
We shall follow the statistical composition of spreads because it is never possible that all of them are present at the same time with the same sign.

We must consider the following spreads :

- ΔV_Y due to the variation of yoke and feedback resistance and yoke current, supposing a 10% of regulation range in scanning current and a precision of 7% for resistors;

$$\Delta V_Y = (1.2\, R_Y + R_F)\ 1.07\ (1.1\, I_Y) - V_Y \qquad (26)$$

- ΔV_C due to the tolerance of C_D and yoke current regulation;

$$\Delta V_C = \frac{1.1\, I_Y\, t_S}{8\, C_{D(MIN)}} - V_C \qquad (27)$$

- ΔV_L due to the tolerance of L_Y (± 10%) and yoke current regulation;

$$\Delta V_L = \frac{1.1\, I_Y\ 1.1\, L_Y}{t_S} - V_L \qquad (28)$$

$$\Delta V_{SAT1} = V_{SAT1(MAX)} - V_{SAT1}$$
$$\Delta V_{SAT2} = V_{SAT2(MAX)} - V_{SAT2}$$

For each parameter, it is necessary to calculate the factor ρ, expressing the percentual influence of every parameter variation on the nominal supply voltage, with the following formulas :

for V_{OM} :

$$\rho = \frac{\Delta V}{V_{OM}}$$

for V_{TOP} :

$$\rho = \frac{\Delta V}{V_{TOP}}$$

We have then to calculate the square mean root of the spreads expressed as :

$$\sqrt{\Sigma\ \rho^2}$$

So if we call :

$$V_{OM1} = V_{OM}\left(1 + \sqrt{\Sigma\ \rho^2}\right)$$

and :

$$V_{TOP1} = V_{TOP}\left(1 + \sqrt{\Sigma\ \rho^2}\right)$$

We can write :

$$V_S = V_{OM1} + V_{TOP1} \qquad (29)$$

An example of calculation will better explain the procedure. We shall consider a 26", 110°, neck 29.1mm *tube whose* characteristics are :
I_Y = 1.2 App;
R_Y = 9.6Ω ± 7%;
L_Y = 24.6mH ± 10%.

We shall use a coupling capacitance C_D of 1500µF with + 50% and - 10% tolerance and a feedback resistance R_F of 1.2Ω.

a) Nominal minimum supply voltage :

$$V_Y = (1.2\,R_Y + R_F)\,I_Y = 15.264\ V$$

$$V_C = \frac{I_Y \cdot t_S}{8 \cdot C_D} = 2\ V$$

$$V_L = \frac{L_Y \cdot I_Y}{t_S} = 1.476\ V$$

V_{SAT1} = 1.25 V V_{SAT2} = 0.68 V
V_D = 1 V
V_{OM} = 11.788 V V_{TOP} = 6.406 V

We obtain : V_S = 18.2V

b) Statistical minimum supply voltage :

ΔV_C = 2.702V

$$\rho V_{YM} = \frac{V_{Y/2}}{V_{OM}} \qquad \rho^2_{V_{YM}} = 1.313 \cdot 10^{-2}$$

$$\rho V_{YT} = \frac{V_{Y/2}}{V_{TOP}} \qquad \rho^2_{V_{YT}} = 4.447 \cdot 10^{-2}$$

ΔV_C = 0.445 V $\rho^2_{V_{CM}} = 1.421 \cdot 10^{-3}$
$\rho^2_{V_{CT}} = 4.813 \cdot 10^{-3}$

ΔV_L = 0.31 V $\rho^2_{V_{LM}} = 6.914 \cdot 10^{-4}$
$\rho^2_{V_{LT}} = 2.341 \cdot 10^{-3}$

ΔV_{SAT1} = 0.45 V $\rho^2_{V_{SAT1T}} = 4.935 \cdot 10^{-3}$

ΔV_{SAT2} = 0.27 V $\rho^2_{V_{SAT2M}} = 5.246 \cdot 10^{-4}$

$$V_{OM1} = V_{OM}\left(1 + \sqrt{\Sigma\ \rho^2}\right) = 13.268\ V$$

$$V_{TOP1} = V_{TOP}\left(1 + \sqrt{\Sigma\ \rho^2}\right) = 7.930\ V$$

$V_S = V_{OM1} + V_{TOP1}$ = 21.2 V

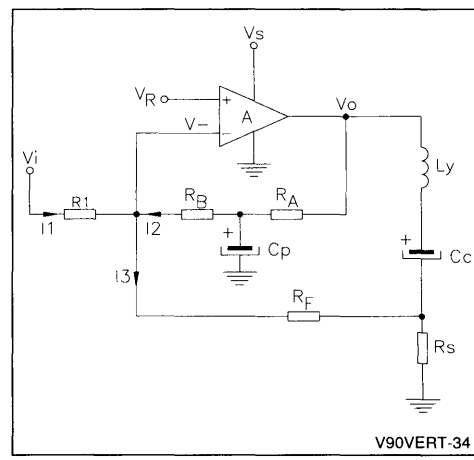
This is a real value for the minimum supply voltage needed by the above mentioned application.
In this case we obtain a flyback duration of about :

$$t_F = \frac{2}{3}\,\frac{I_Y \cdot L_Y}{V_S} \approx 900\ \mu s$$

12. CALCULATION OF MIDPOINT AND GAIN

For the calculation of the output midpoint voltage, it is necessary to consider the different feedback network for the applications of the various integrated circuits.
We shall first consider the TDA1170 family, the TDA1175, TDA2170, TDA2270, TDA8170, TDA8172, TDA8173, TDA8175 and TDA8176.
The equivalent circuit of the output stage is represented in Figure 34.

Figure 34 : Circuit Utilized for the Calculation of midpoint and gain for TDA1170, TDA1175, TDA8176, TDA2170, TDA2270, TDA8170, TDA8172, TDA8173 and TDA8175.



For DC considerations we shall consider the two capacitors as open circuits. Because of the very high gain of the amplifier we can suppose :
$V^- = V_R$.
We can so write :

$$I_1 + I_2 = I_3 \qquad (30)$$

where :

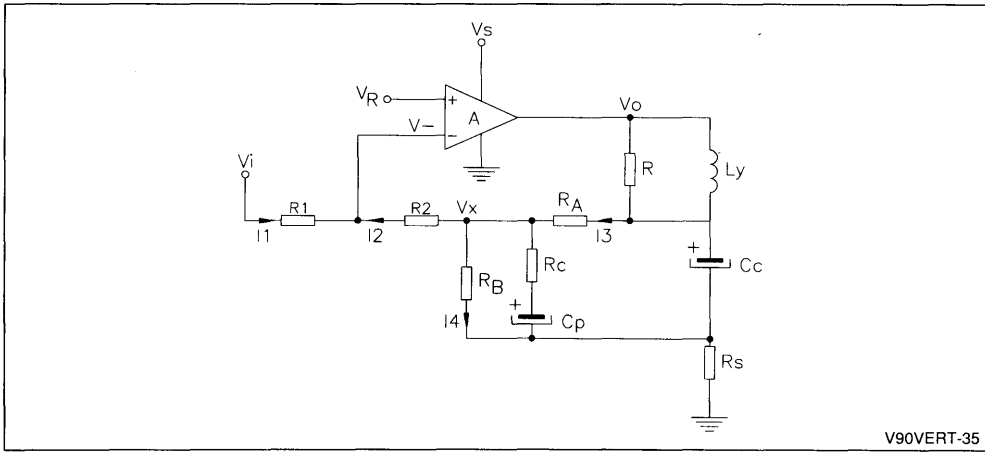
$$I_1 = \frac{V_i - V_R}{R_1} \qquad I_2 = \frac{V_O - V_R}{R_A + R_B} \qquad I_3 = \frac{V_R}{R_F + R_S}$$

Substituting into the (30) we obtain :

$$V_O = V_R \left(1 + \frac{R_A + R_B}{R_F + R_S}\right) - (V_i - V_R)\frac{R_A + R_B}{R_1} \qquad (31)$$

Let's consider now TDA1670A, TDA1675, TDA1770A, TDA1771, TDA1872A and TDA8174. The equivalent output circuit is depicted in Figure 35.

Figure 35 : Circuit Utilized for the Calculation of Midpoint and Gain for TDA1670A, TDA1675,TDA1770A, TDA1771, TDA1872A and TDA8174.



We can write :

$$I_1 = I_2 \qquad (32)$$

$$I_2 + I_3 = I_4 \qquad (33)$$

where :

$$I_1 = \frac{V_i - V_R}{R_1} \qquad I_2 = \frac{V_R - V_X}{R_2} \qquad I_3 = \frac{V_O - V_X}{R_A} \qquad I_4 = \frac{V_X}{R_B + R_S}$$

with the (32) and (33) we can calculate the DC output voltage. It results in :

$$V_O = V_R \left(1 + \frac{R_A + R_2}{R_1} + \frac{R_A (R_1 + R_2)}{R_1 (R_B + R_S)}\right) - V_i \left(\frac{R_A + R_2}{R_1} + \frac{R_A \cdot R_2}{R_1 (R_B + R_S)}\right) \qquad (34)$$

Referring to Figures 34 and 35, it is possible to calculate the transconductance gain of the power amplifier. For this calculation we shall do the following approximations :

- the capacitors are practically short circuits;
- the gain A of the amplifier is very high ($A \rightarrow \infty$).

For the circuit represented in Figure 34 we obtain :

$$I_Y = \frac{R_F}{R_1 \cdot R_S} V_i \qquad (36)$$

Using the (31), (34), (35) and (36) it is possible to calculate the external feedback network for every

while for the application in Figure 35 the yoke current results in :

$$I_Y = \frac{R_2 + R_A // R_B // R_C}{R_1 \cdot R_S} V_i \qquad (37)$$

different yoke known the scanning current and the midpoint output voltage.

Figure 36 : Open Loop Gain and Phase for the Application Circuit in Figure 27.

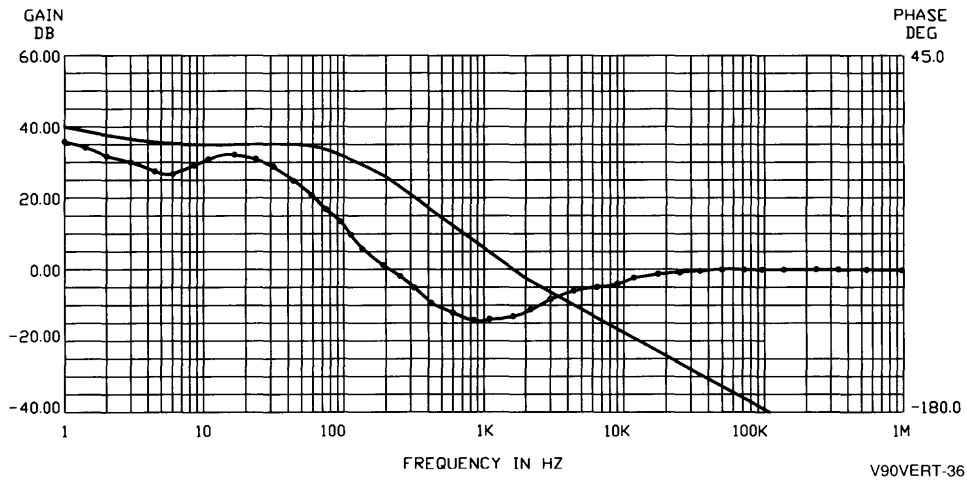
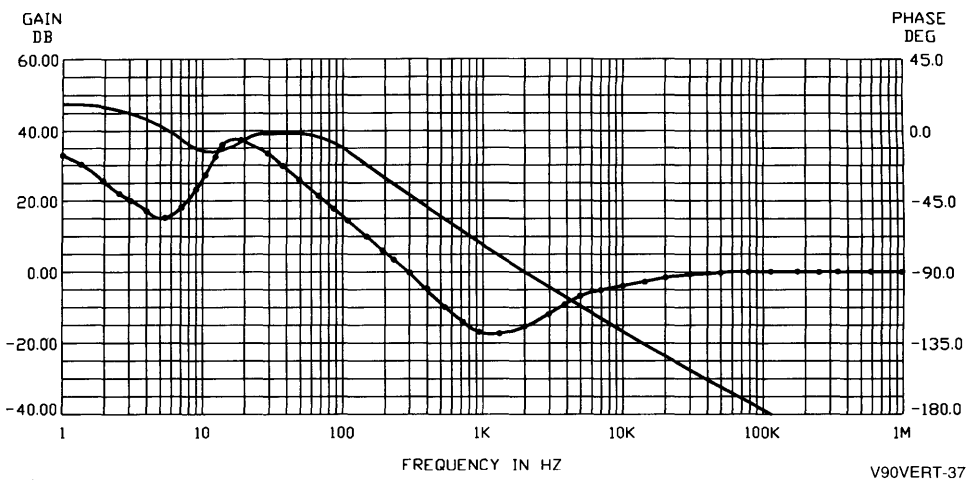
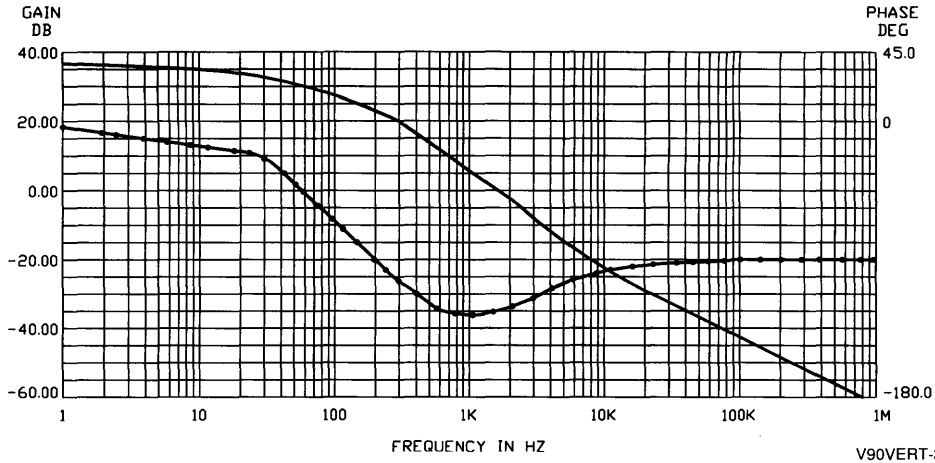


Figure 37 : Open Loop Gain and Phase for the Application Circuit in Figure 28.



We can now consider the open loop gain of the whole system amplifier plus external feedback network. This calculation is useful in order to verify that no oscillations can occur at any frequency.

Figure 38 : Open Loop Gain and Phase for the Application Circuit in Figure 29.



We shall consider some typical applications; the results are reported in Figures 36, 37 and 38.
It is easy to verify that in all cases, when the gain reaches 0dB, the phase margin is about 60°, so the stability of the system is assured.

13. MONITOR APPLICATIONS

In monitor applications the flyback time needed could be very smaller than the one we get using the minimum supply voltage calculation.

It is possible to reduce the flyback time in two different ways :
a) increasing the supply voltage, when the nominal value calculated is lower than the integrated circuit limit;
b) choosing a yoke with lower values in inductance and resistance and by supplying the circuit with the voltage needed for getting the right flyback time.

In both cases we have to calculate the biasing and the gain conditions using the nominal voltage and then we fix the supply voltage for the flyback time requested with the formula (18) :

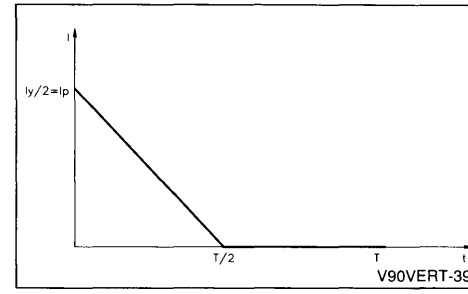
$$V_S = \frac{2}{3} \frac{I_Y \cdot L_Y}{t_F}$$

The calculation procedure for monitors is so the same as the one we have explained in the previous chapters for television applications.

14. POWER DISSIPATION

We shall now examine the power dissipation of the integrated circuit and the dimensions of the heatsink.
To calculate the power dissipated we must consider the maximum scanning current required to drive the yoke $I_{Y(MAX)}$ and the maximum supply voltage $V_{S(MAX)}$ because we have to dimension the heatsink for the worst case.
The current absorbed from the power supply is depicted in Figure 39.

Figure 39 : Current Absorbed from the Power Supply during Scanning.



The equation of the curve is :

$$i(t) = \frac{I_Y}{2} - \frac{I_Y}{T}\,t \qquad \text{for } 0 < t \leq T/2$$

$$i(t) = 0 \qquad \text{for } T/2 < t \leq T \qquad (37)$$

To the previous one we have to sum the DC current necessary to supply the other parts of the circuit (quiescent current).

The power absorbed by the deflection circuit is then :

$$P_A = \int_0^{T/2} V_{S(MAX)} \cdot i(t) \cdot dt + V_{S(MAX)} \cdot I_{DC}$$

$$= V_{S(MAX)} \int_0^{T/2} \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right) dt + V_{S(MAX)} \cdot I_{DC}$$

The solution is :

$$P_A = V_{S(MAX)} \left(\frac{I_{Y(MAX)}}{8} + I_{DC} \right) \qquad (38)$$

The power dissipated outside the integrated circuit is formed by the three following fundamental components : the scanning power dissipated in the yoke for which the minimum resistance of yoke $R_{Y(MIN)}$ and the maximum scanning current $I_{Y(MAX)}$ must be considered, the power dissipated in the feedback resistance R_F and that one dissipated in the diode for recovery of flyback.

The power dissipated outside the integrated circuit is then :

$$P_Y = \int_0^T (R_{Y(MIN)} + R_f)\, i^2(t) \cdot dt + \int_0^{T/2} V_D\, i(t) \cdot dt$$

$$= (R_{Y(MIN)} + R_f) \int_0^T \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right)^2 dt + V_D \int_0^{T/2} \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right) dt$$

The solution is :

$$P_Y = \frac{I^2_{Y(MAX)}\,(R_{Y(MIN)} + R_f)}{12} + \frac{I_{Y(MAX)} \cdot V_D}{8} \qquad (39)$$

The power dissipated inside the integrated circuit is :

$$P_D = P_A - P_Y \qquad (40)$$

The thermal resistance of the heatsink to be used with the integrated circuit depends upon the maximum junction temperature $T_{J(MAX)}$, the maximum ambient temperature T_{AMB} and the thermal resistance between junction and tab $R_{TH\ (J\text{-}TAB)}$ that is different for the various packages used. The thermal resistance of the heatsink is expressed by the following formula :

$$R_{TH\,J\text{-}AMB} = \frac{T_{J(MAX)} - T_{AMB(MAX)}}{P_{D(MAX)}} - R_{TH\,J\text{-}TAB} \qquad (41)$$

As an example we can calculate the dissipated power and the thermal resistance of the heatsink for the 26", 110°, neck 29.1mm tube for which we calculated the minimum supply voltage in chapter 11.

We shall consider the integrated circuit TDA1670A and we can suppose a maximum supply voltage of 25V.
The power absorbed from the supply is :

$$P_A = 25 \left(\frac{1.2}{8} + 0.04 \right) = 4.75\ W$$

The power dissipated outside the integrated circuit is :

$$P_Y = \frac{1.2^2 (9.6 \cdot 0.93 + 1.2)}{12} + \frac{1.21}{8} = 1.37\ W$$

therefore the power dissipated by the integrated circuit is :

$$P_D = 4.75 - 1.37 = 3.38\ W$$

The thermal resistance of the heatsink, considering the $R_{TH\ J\text{-}TAB}$ for the multiwatt package of 3°C/W, a maximum junction temperature of 120°C and a maximum ambient temperature of 60°C is :

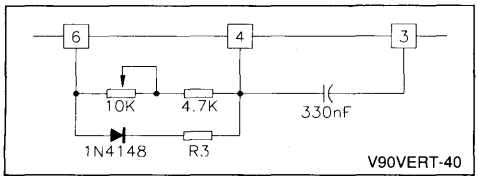
$$R_{TH\ H\text{-}AMB} = \frac{120 - 60}{3.38} - 3 = 15°C/W$$

For the same application with TDA1170S we have a thermal resistance for the heatsink of about 8°C/W.

15. BLANKING PULSE DURATION ADJUSTMENT

For the devices that have the blanking generator it is possible to adjust the blanking pulse duration. We shall consider as an example the TDA1670A; the circuit arrangement is depicted in Figure 40.

Figure 40 : Circuit Arrangement for Blanking Pulse Duration Adjustment.



By adjusting R_3 the blanking pulse duration will be adapted to the flyback time used and the picture tube protection will be ready to work properly.

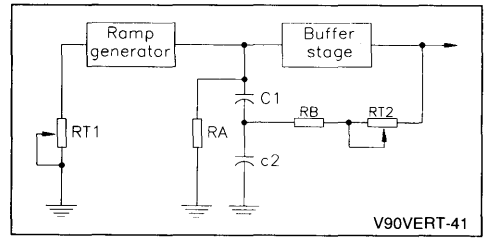
When necessary, it is possible to use a trimmer system to adjust it very carefully.

16. LINEARITY ADJUSTMENT

The complete vertical stages have the possibility to control the linearity of the vertical deflection ramp. There are two different methods to obtain the above mentioned performance.

a) For the first method we shall refer to Figure 41.

Figure 41 : Circuitry for Ramp Linearity Regulation.



The linearity regulation is obtained by means of R_A, R_B and R_{T2}.

In order to choose the right values of this components we suggest to follow the following procedure :
1 - Set the amplitude regulation potentiometer R_{T1} for the nominal raster size;
2 - Disconnect the R_A resistance;
3 - Adjust the linearity control potentiometer R_{T2} in order to obtain the top and the bottom of the raster with the same amplitude;
4 - In this condiotion the center of the raster must be narrower then the top and the bottom. If with R_A

disconnected the center is larger than the top and the bottom it is necessary to act on the feedback network. Referring to Figures 27, 28 and 29 it is necessary to increase the capacitors C_{11}, C_8 or C_6;
5 - After increasing the capacitors it is necessary to repeat the linearity adjustment (R_{12} potentiometer) in order to get the top and the bottom with the same amplitude again;
6 - Connect the R_A resistor and repeat the linearity adjustment (point 3 regulation);
7 - Check the top and the bottom amplitude comparing it with the center. If the center amplitude is still narrower it is necessary to reduce R_A. If the center amplitude becomes larger it is necessary to increase R_A.

Note : Every time the linearity conditions are changed (for adjusting or setting) before checking the linearity status, the point 3 adjustment must be repeated.

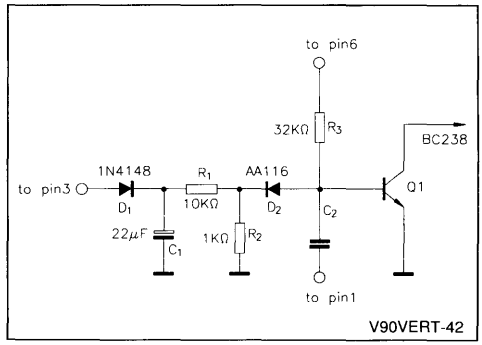
b) For the second method we shall refer to Figure 28.
In this case the linearity regulation is obtained acting directly on the feedback network, that is substituting the R_8 resistance with a potentiometer. This solution is cheaper than the first one, because it is possible to save the resistors R_A, R_B (see Figure 41), the potentiometer R_{T2} and to use only a capacitor instead of the series C_1 and C_2.
On the other hand a disadvantage is due to the fact that the resistance R_8 influences not only the linearity of the ramp but also the gain of the amplifier, as it can be seen in the equation (36). So to perform a linearity adjustment it is necessary to act at the same time on the potentiometer in the feedback loop and on the potentiometer R_{T1} (see Figure 41) in order to correct the vertical amplitude variations. On the contrary, in the method a) the linearity control network doesn't influence any other parameters. this is the reason why the a) method is generally adopted by all television set producers.

17. FACILITIES AND IMPROVEMENTS

In this section we shall briefly examine some facilities which may be useful to improve operations of the television set.

a) Blanking generator and CRT protection for TDA1170 family.
At pin 3 a pulse is available which has the same duration and phase as the flyback and amplitude equal to the supply voltage.
If the retrace duration is not sufficient for carrying out correct vertical blanking, for instance in the presence of text and teletext signals the circuit of Figure 42 can be used.
The true blanking generator is formed by Q_1,R_3 and C_2 and the blanking duration is dependent upon the values of R_3 and C_2. The other components are used for picture tube protection in the event of loss of vertical deflection current. If for any reason there is no flyback, the transistor Q_1 is permanently inhibited and provides continuous switch off which eliminates the white line at the center of the screen. Thermal stability and stability with the supply voltage is good in relation to the simplicity of the application.

Figure 42 : Blanking Generator and CRT Protection for TDA1170.



b) Vertical deflection current compensation to maintain picture size with beam current variations.

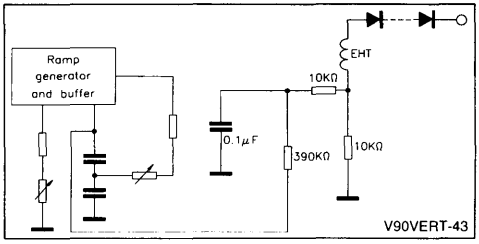
Changes in the supply voltage or the brightness and contrast controls will bring out changes of the beam current, thus causing EHT and picture size variations.
The rate of change of the picture size is mainly dependent upon the EHT internal resistance.
In order to avoid variations of the vertical picture size it is necessary to track the scanning current to the beam current. Because the tracking ratio :

$$\frac{\Delta I_{YOKE}}{\Delta I_{BEAM}} \cdot 100 \qquad (42)$$

varies from one chassis design to another, three suggested tracking circuits are shown in Figures 43, 44 and 45.

The circuit in Figure 43 adopts the straight forward technique of linking the vertical scanning current directly to the beam current .Its drawback lies in the fact that a long wire connection is required between the EHT transformer and the vertical circuit, and the layout of this connection could be critical for flashover.

Figure 43 : Circuit for Vertical Scanning Current Variation according with the Beam Current.



The circuit of Figure 44, which links the vertical scanning current directly to the supply voltage, is the simplest one. Its drawback could be incorrect tracking ratio and ripple on the supply voltage.To overcome the drawbacks of the preceding circuit it is usefull to filter out the supply voltage ripple and adjust the tracking ratio by transferring the supply voltage to a lower level by means of a Zener diode as shown in Figure 45. Tracking ratio is adjusted by choosing a suitable Zener voltage value.

Figure 44 : Circuit for Vertical Scanning Current Variation according with the Supply Voltage.

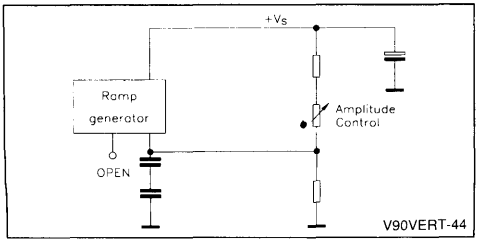
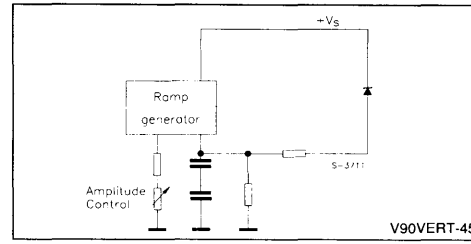


Figure 45 : Circuit for Vertical Scanning Current Variation according with the Supply Voltage.



18. GENERAL APPLICATION AND LAYOUT HINTS

In order to avoid possible oscillations induced by the layout it is very important to do a good choice of the Boucherot cell position and ground placing. The Boucherot cell must be placed the most possible closed to the vertical deflection output of the integrated circuit, while the ground of the sensing resistor in series connected with the yoke must be the same as the one of the integrated circuit and different from the one of other power stages. Particular care must be taken in the layout design in order to protect the integrated circuit against flashover of the CRT. For instance the ground of the filter capacitor connected to the power supply must be near the integrated circuit ground.

19. REFERENCES

1) Television Deflection Systems - A. Boekhorst, J. Stolk - Philips Technical library.
2) TV Vertical Deflection System TDA1170S - SGS-THOMSON Application Notes.
3) TDA1670A Technical Note - SGS-THOMSON Technical Note.
4) TV and Monitor Vertical Deflection using TDA1670A - O. Cossutta, F. Gatti SGS-THOMSON Application Notes.
5) TDA1670A Flyback Stage Behaviour - A. Messi, G. Nardini - SGS-THOMSON Application Notes.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TDA8102A

by Fabio GRILLI

TECHNICAL INFORMATION

APPLICATION INFORMATION

TECHNICAL INFORMATION

1. ABSTRACT

The system evolution in the monitor field leads to develop suitable I.C.'s whose performances and characteristics are mainly monitors oriented rather than TV oriented. The automatic frequencies raster preset of the monitor by computer and optical equipments leads to the adoption of Digital to Analog converters in order to set the different parameters, and consequently all regulation must be DC compatible.

High scanning frequency and low jitter are additional factors that characterize the quality and the resolution of the monitor. In this note new circuit solutions on silicon, concerning the monitor field, are described. In a single I.C., making use of TTL compatible synchro pulses, horizontal and vertical processing functions and vertical ramp generation are implemented.

INTRODUCTION

In Fig.1 is shown the block diagram of TDA8102A.

Horizontal frequency and phase as well as vertical frequency, amplitude and linearity are all DC adjustable on different terminals.The horizontal phase adjustment within ± 45° is implemented on first PLL (sync-oscillator) rather than on the second PLL (flyback-oscillator) allowing the raster to be centered in case of no standard phase sync position.

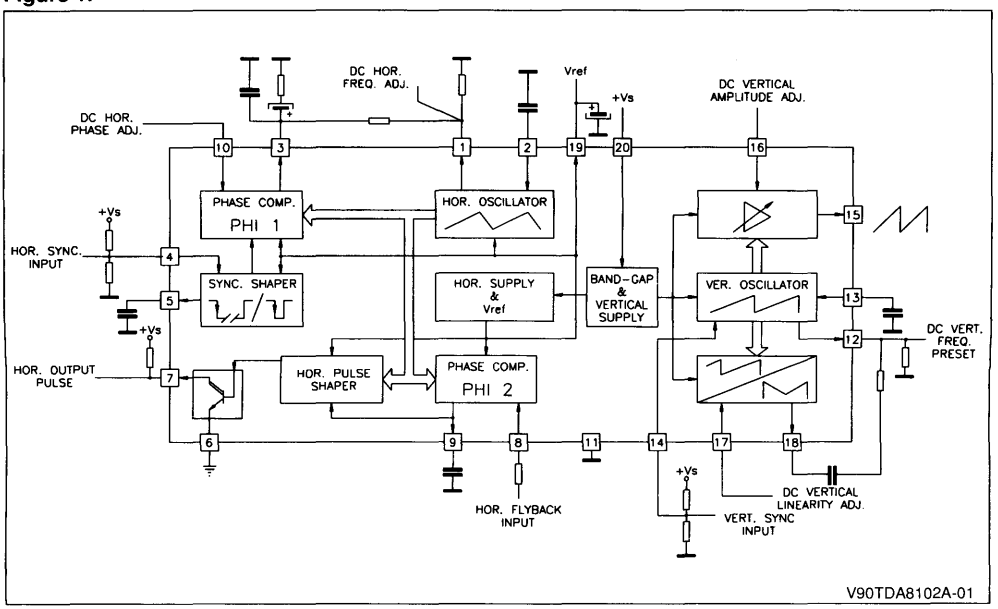
An additional feature makes the raster phase independent by the duty-cycle of the input synchronizing pulse thanks to an internal shaper circuit generating a standard sync pulse starting from the leading edge of input signal.

The vertical amplitude changes depending on a voltage amplifier whose gain is set on Pin 16 ; the peak to peak voltage of the sawtooth does not influence its average value which is maintained constant.

The current capability of the horizontal output stage (Pin 7) is such to directly drive an external darlington used as line power switch.

Since part of the jitter effect is due to the internal voltage reference circuits, an external pin connected to the V_{CO} supply voltage is got available for noise filtering (Pin 19).

Figure 1.



3. FUNCTIONAL DESCRIPTION

Here following are briefly described all the functional blocks of TDA8102A.

3.1 Horizontal oscillator

The circuit in Fig.2 is a Current Controlled Oscillator, it works charging and discharging the capacitor at pin 2 between two thresholds V_{S1} = 2.5V and V_{S2} = 6.5V coming from an internal resistor divider. This one is also used to provide a voltage reference at pin 1 (V_1 = 3.5V) by means of a unity gain amplifier.

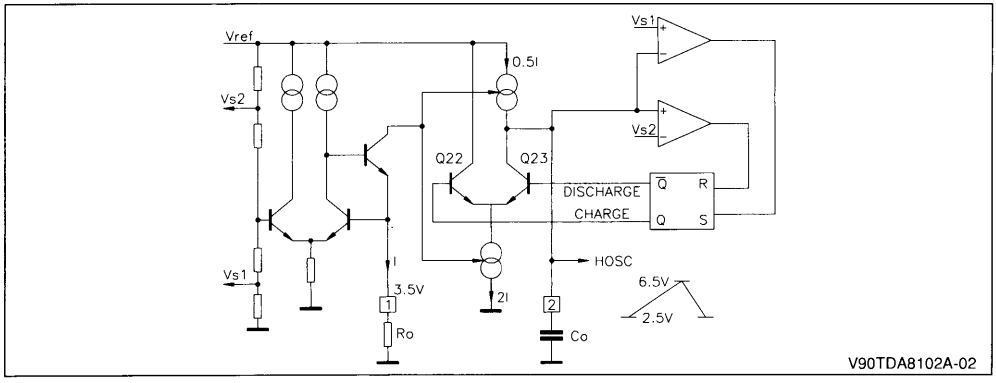
An external resistor connected between Pin 1 and ground sets the current reference.

This current is mirrored with 0.5 : 1 ratio to charge the capacitor C_O at Pin 2, and with 2 : 1 ratio to discharge C_O.

The charging and discharging time ratio will result in 3 : 1.

The differential switch Q_{22}-Q_{23} is driven by a S-R flip-flop, which changes its state every time that the peak of the triangular waveform reaches one of the two thresholds V_{S1} or V_{S2}.

Figure 2.



3.2 Horizontal synchronism shaper circuit

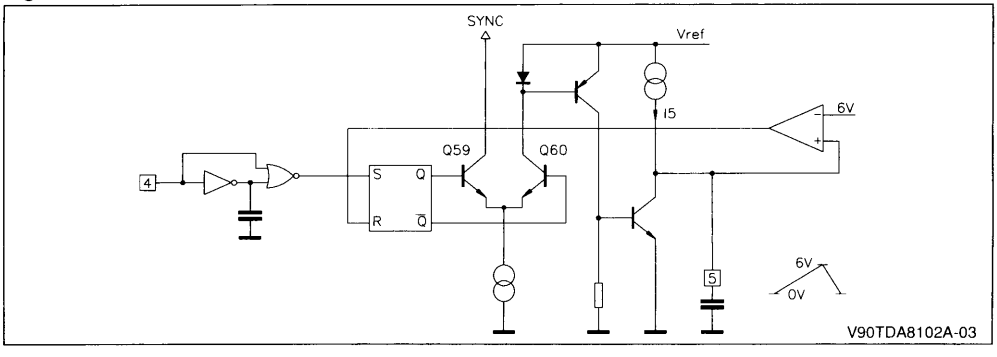
The electric diagram shown in Fig.3 can be divided in three stages. The first of which is a negative edge detector able to set the S-R flip-flop each time that a negative edge of the sync pulse is applied to the input (Pin 4).

The second one is a differential stage that feeds the first phase comparator (φ 1).

The third stage uses an external capacitor to produce a ramp on the Pin 5. As soon as the peak of the ramp reaches the internal threshold (6V) the external capacitor is suddenly discharged and the flip-flop is reset.

The horizonal sync pulse width on the collector of Q_{59} will depend on the value of the capacitor at Pin 5.

Figure 3.



3.3 First phase comparator (φ 1) and phase adjustment interface circuit

In the circuit of Fig.4, a comparator squares the horizontal waveform using as voltage reference Vref1 which represents the output of the phase adjustment interface circuit.

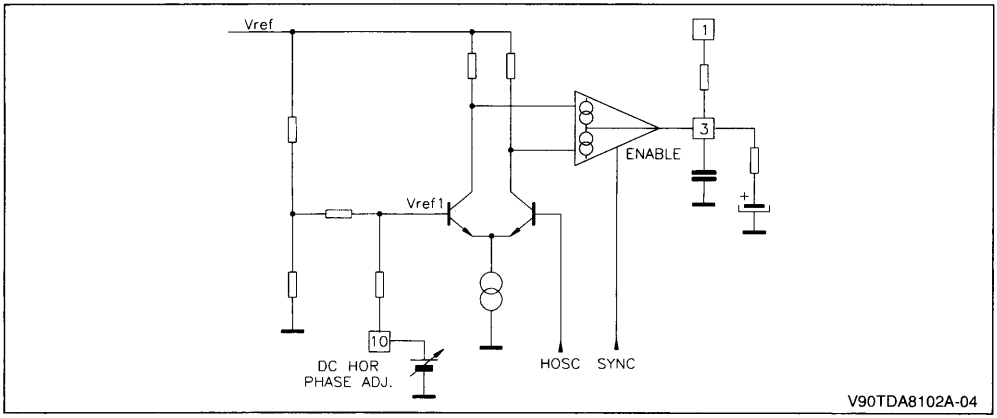
If the voltage at Pin 10 changes in the range from 0.5V to 4.5V, the phase will shift of ± 45° between the sync and the flyback pulse.

The rectangular waveforms that are the outputs of first differential amplifier are applied to another differential stage which is activated only during the horizontal sync pulse coming from the horizontal sync shaper circuit.

The product in terms of current of the sync signal and the oscillator signal is available at Pin 3.

Two clamp limit the maximum voltage range of Pin 3 (from 1V to 6V) and consequently the hold in range of the CCO.

Figure 4.



3.4 Second phase comparator (φ 2) between flyback and oscillator

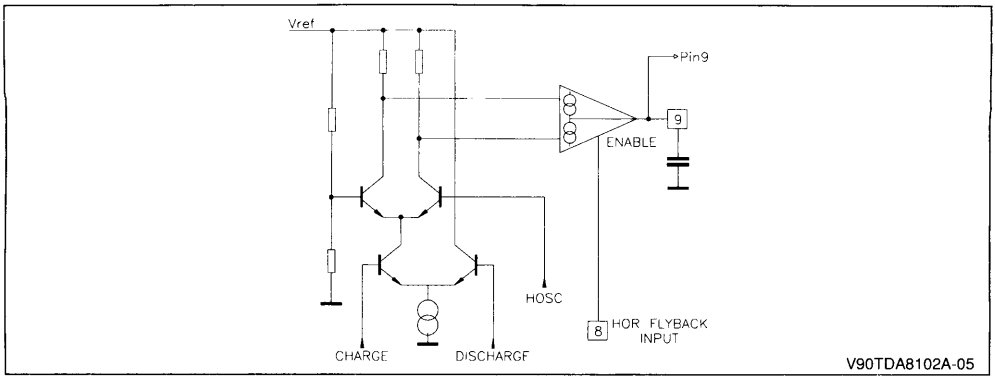
This circuit recovers dynamically the deflection delay of line output transistor.

The flyback pulse applied to Pin 8 (see Fig.5) is detected and clamped at a voltage level of 0.7V.

This circuit is similar to φ 1, the substantial differences are two, the input pulse is the flyback pulse instead of sync pulse and the first differential stage is activated by S-R flip-flop of horizontal oscillator.

The φ 2 output acts on the horizontal output stage in order to shift the output pulse to recover the deflection delay.

Figure 5.



3.5 Phase shifter, output stage and start up circuit

The storage time t_S of the line output transistor is recovered by advancing the leading edge of the output pulse of ts with respect to the phase of the sync reference.

The triangular oscillator waveform (Fig.6a) is compared with internal threshold S_1 and S_2 whose voltages depend upon the voltage level present at the output of phase comparator φ 2.

The voltage difference S_1-S_2 is constant and this value fixes the duty-cycle of the horizontal output pulse present at Pin 7.

During the positive slope of the oscillator the output pulse (Pin 7) is low when the triangular waveform voltage is in the voltage range established by S_1 and S_2; whereas during the negative slope of the oscillator the output pulse is always at high level thanks to a comparator drived by S-R flip-flop of horizontal oscillator.

As shown in Fig.6a, a transistor insures that the output pulse is low when the flyback pulse is present.

At the switch on, the horizontal output stage (Pin 7) is inhibited until the power supply does not overcome 8 V.

Figure 6a.

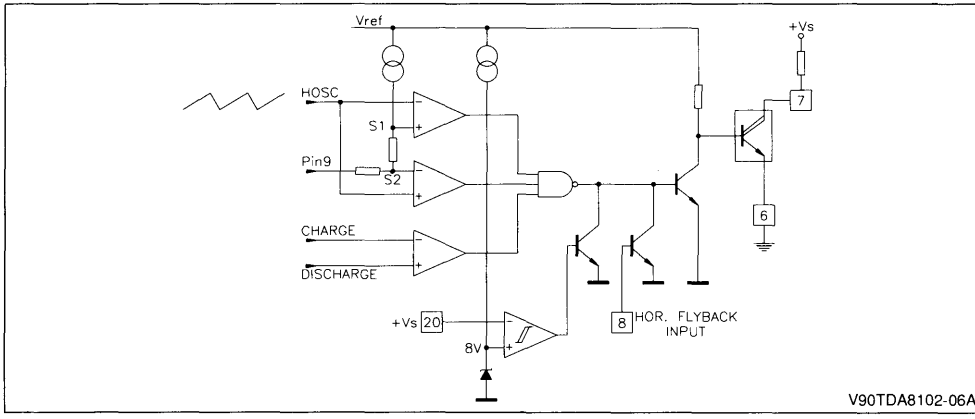
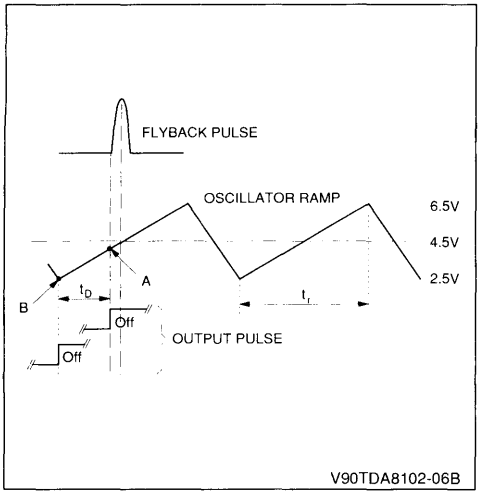


Figure 6b.



About the maximun allowable delay, it depends on the flyback time and the working frequency (see Fig.6b).

The PLL2 works in such a way to maintain the middle of the flyback exactly in correspondence between the crossing of the V_{REF} = 4.5V and the oscillator ramp.

Then if you suppose to have zero delay time, the switch-off edge of the output pulse will rise at point "A" now if the delay time increases the switch-off edge will move to point "B" to recover the delay.

The equation to calculate the t_D with a good approximation is the following :

Maximum Allowable Delay :

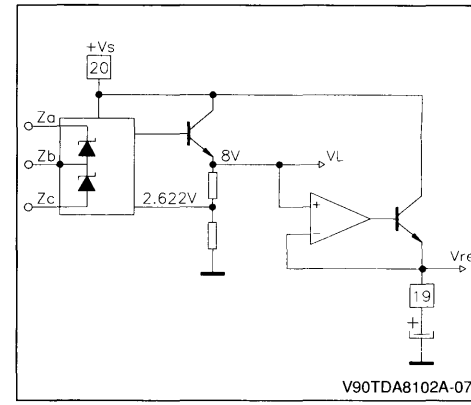
$$t_D = \frac{t_r}{2} - \frac{t_{FLY}}{2}$$

where t_R is the rise time of the horizontal ramp = 3/4 T and t_{FLY} is the flyback time.

3.6 Voltage regulator 8 V

The voltage reference, Fig.7, is a band-gap circuit that allows on the output a voltage reference equal to 2.622V that means a voltage V_L = 8V.
By means of zener zap is possible to adjust, during the testing, the voltage reference from ± 6% into a ± 2% range.
V_L feeds all the circuits of the vertical side and, by means of a unity gain amplifier, provides a voltage reference (V_{REF}) at Pin 19 to supply all the circuits of the horizontal side.
The unity gain amplifier is necessary to avoid all the possible interactions between the horizontal and vertical sections.
Moreover, to minimize jitter on the horizontal oscillator, is possible to connect an external capacitor between Pin 19 and ground.

Figure 7.



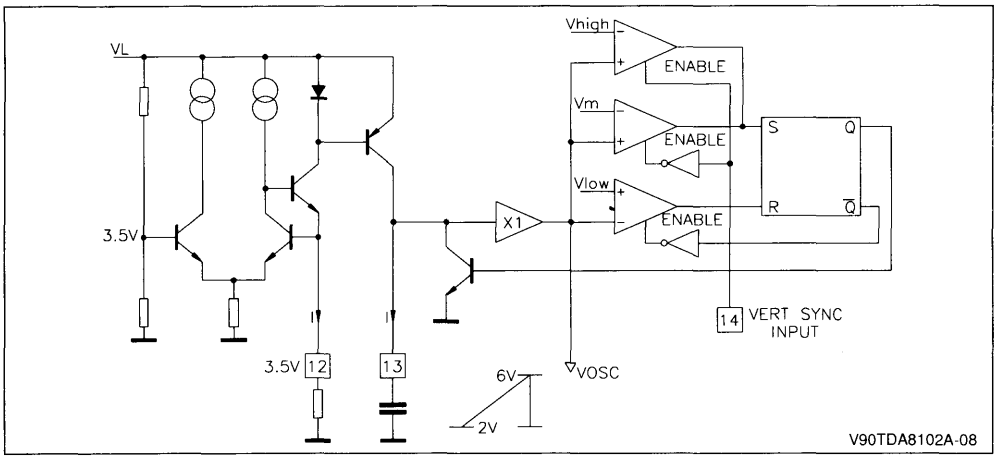
3.7 Vertical oscillator

A new concept of vertical oscillator is implemented in this I.C. whose resistor divider, used to set the lower and higher thresholds (V_{low} = 2V ; V_{high} = 6.8V), is not commutated .
The circuit shown in Fig.8 works charging an external capacitor connected at Pin 13 with a current set at Pin 12 and reflectd to Pin 13 through a current mirror.
As soon as the ramp gets V_m or V_{high} the capacitor is quickly discharged by a darlington, the voltage on the capacitor will fall down till to get the lower threshold; at this point the darlington will be driven off and the current will charge again the capacitor.
A buffer is used to decouple the ramp generator from other circuits (like linearity correction and amplitude regulation circuits).
The lower threshold is detected by a differential stage whose current generator is only activated during the discharge phase.
A comparator detects the higher threshold corresponding to the free running frequency; if no sync pulse (negative edge) is applied on Pin 14, this stage is continually fed and the capacitor at Pin 13 is discharged when the vertical ramp reaches V_{high}.
If the sync pulse is present the previous comparator will be inhibited and another comparator, which has the threshold at 5.2V (V_m), will be activated.
This last comparator, when it is set going, is able to cause the discharge of the capacitor at Pin 13 if the vertical ramp is between the thresholds Vm and V_{high}.
In this way the vertical synchronization is established.
To guarantee that the vertical oscillator is locked in the middle of the pull-in range is necessary to adjust the current at Pin 12 until the peak of the vertical sawtooth, in locking condition, reaches the voltage equal to:

$$V_P = \frac{V_m + V_{high}}{2} = 6\ V$$

that means V_{pp} = 4V.

Figure 8.



3.8 S Correction circuit and DC linearity adjustment

The circuit which is used to realize a new concept of vertical linearity regulation is shown in Fig.9.

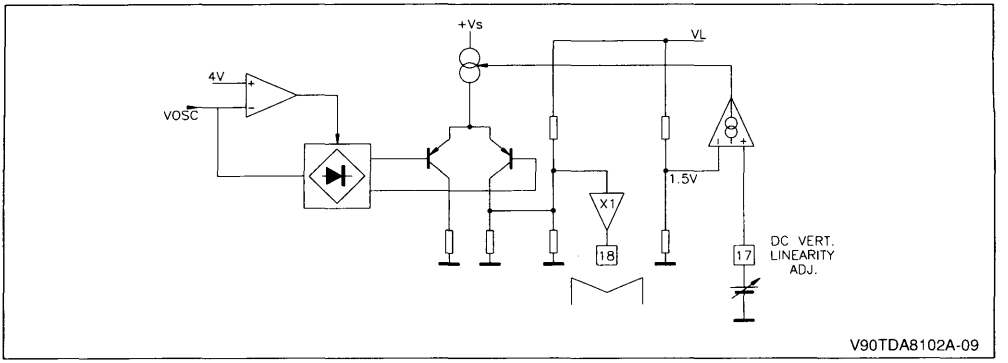
A comparator squares the vertical sawtooth using as voltage reference a fixed value (4V) that is the average value of sawtooth.

This squared signal is used to drive a particular configuration of differential stage in order to obtain, in terms of current, a triangular waveform which inverts its slope just when the original sawtooth crosses the voltage reference.

This current signal is converted in voltage by a resistor divider and transferred on Pin 18 through a buffer.

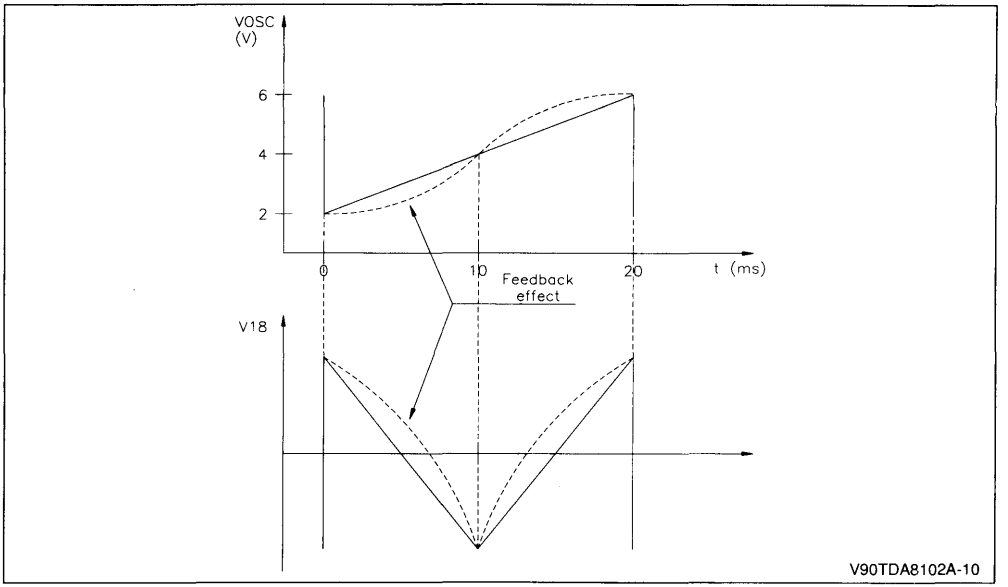
The peak to peak voltage on this pin depends on the maximum current that the output differential stage is able to handle, the value of this current can be externally regulated by means of Pin 17 through a transconductance amplifier.

Figure 9.



An external feedback resistor in series to a capacitor (to avoid any DC offset) must be connected between Pins 18 and 12 in order to obtain the proper S correction as shown in Fig.10.

Figure 10.



3.9 Vertical amplitude regulation circuit

This function has been implemented using the circuit configuration that can be seen in Fig.11.

It consists of an Op-Amp in non inverting input configuration and of a variable gain OTA whose gain can be set by means of the Pin 16 through a transconductance amplifier.

Both the inputs of the two circuit handle the vertical ramp and the output of the multiplier is fed back to the inverting input.

The control circuit is a transconductance amplifier that modulates the current of the variable gain OTA depending on the DC voltage applied on Pin 16.

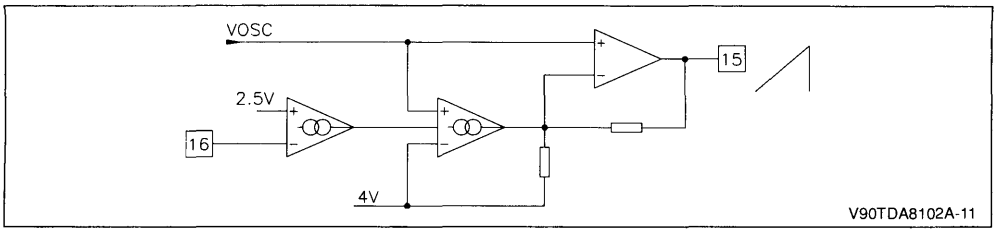
This circuit guarantees a gain adjustment of ± 20% around the nominal value.

4. CONCLUSION

This new I.C. can be considered as a first step towards a new generation of serial bus compatible LSI circuits in which additional logic function can be implemented and all the D/A converters can be included.

It is assembled in 20 pins DIL plastic package able to dissipate the 0.7W required by a typical application.

Figure 11.



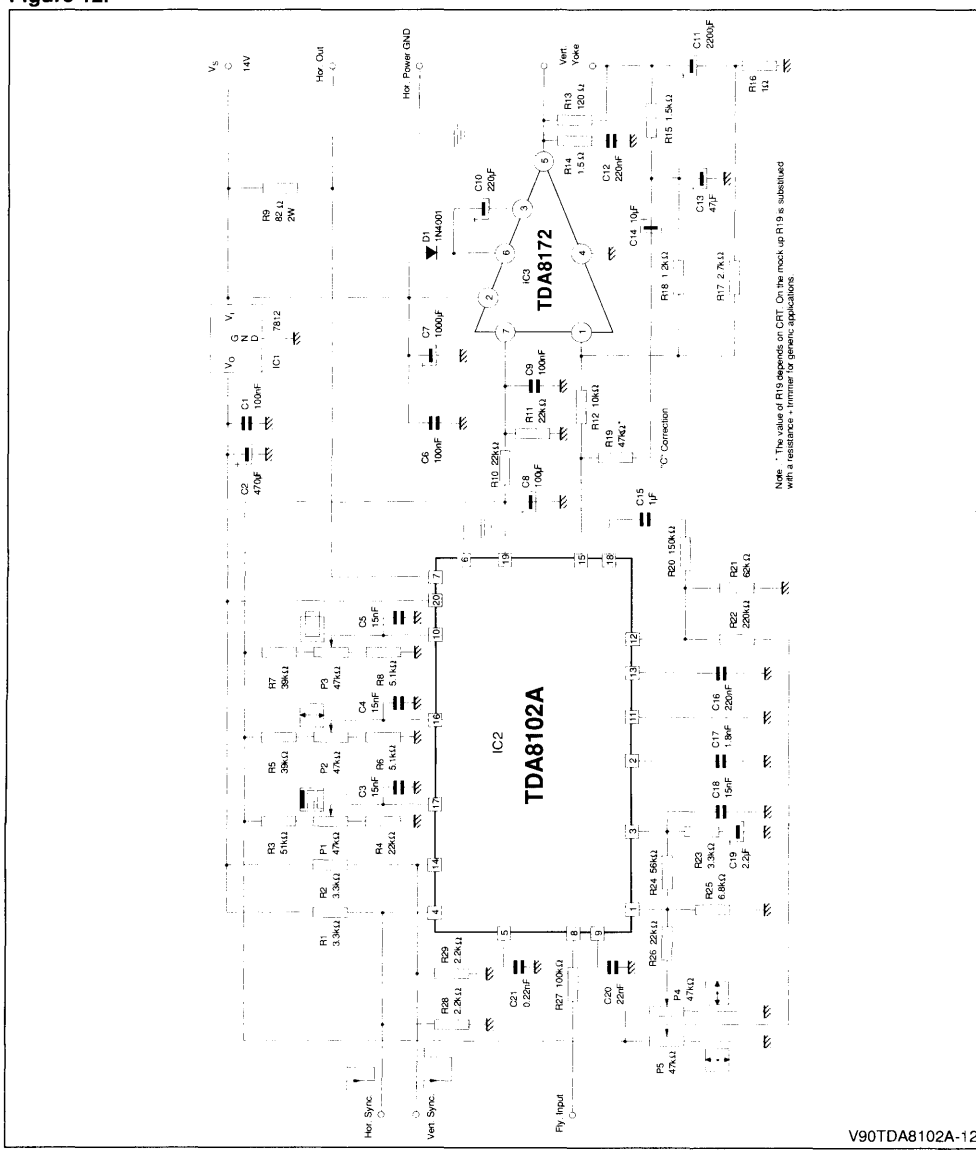
APPLICATION INFORMATION

In Fig.12 is shown a typical application of the TDA8102 A *with the TDA*8172, which is a vertical booster; for further information regarding TDA8172 consult the note :

SGS-THOMSON "Vertical Deflection Stages for TV and Monitor" by A. MESSI

All the information is referred to the above mentioned figure.

Figure 12.



5. HORIZONTAL SECTION

5.1 Frequency

The device is able to work from 15 KHz to 100 KHz. The free running frequency is fixed by the resistor at Pin 1 (R_{25}) and by the capacitor at Pin 2 (C_{17}) with the following formula:

$$f_O = \frac{1}{K_O \times R_{25} \times C_{17}}$$

where K_O is typically 3.0476 ± 5% (see data-sheet). In the aplication of Fig.12, using R_{25} = 6.8kΩ and C_{17} = 1.8nF, we obtain:

$$f_O = \frac{10^6}{3.0476 \times 6.8 \times 1.8} = 26.808\text{kHz}$$

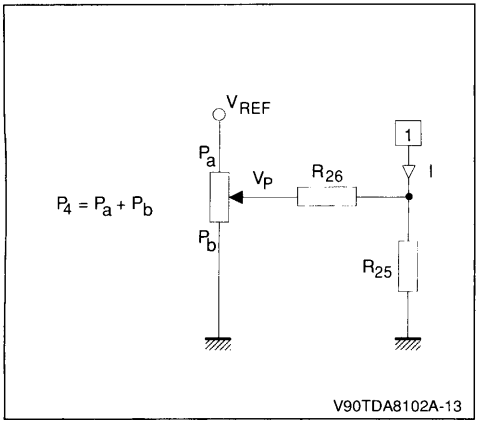
The maximum available current at Pin 1 is 1mA, so it must be $\frac{V_1}{R_{25}} \leq 1\text{mA}$.

By means of trimmer P_4 , it is possible to adjust the horizontal free running frequency, that changes accordingly with the following formula:

$$f_H = f_O \left\{ 1 - \frac{(V_p - V_1) / R_{26}}{V_1 / R_{25}} \right\}$$

where $0 \leq V_p \leq 8V$ is the voltage at the central point of the trimmer (see Fig.13).

Figure 13.



5.2 Pull-in range

This range is determined by the ability of the first comparator (φ 1) to correct the difference between the sync frequency and the free running frequency and it is set by R_{24} and R_{25}.

$$f_{pull\text{-}in} = f_O \frac{|V_3 - V_1| / R_{24}}{V_1 / R_{25}}$$

$|V_3 - V_1|$ is typically 2.5V, while V_1 = 3.5V.

This is the theoretical value calculated if the frequency adjustment is disconnected.

In the application inf Fig.12 we have:

$$f_{pull\text{-}in} = 26808 \frac{2.5}{3.5} \frac{6800}{56000} = \pm 2.3\text{kHz}$$

When the frequency adjustment is connected the pull-in range changes due to the fact that in parallel with R_{25} are connected R_{26} + P_b (see Fig.13).

When the device is synchronized and perfectly tuned, $V_3 = V_1$ and the φ 1 will work in the best way.

C_{17}, on the contrary of R_{25}, is influential only for the free running frequency of the horizontal oscillator; it has no effect on the pull-in range, which doesn't change in percentage with respect to the free running frequency.

If you change the horizontal frequency changing R_{25} the pull-in range changes accordingly with the previous formula.

5.3 Internal sync. width

The internal sync. pulse is made by current generator (I_5) that charges an external capacitor at Pin 5 (C_{21}) up to the trigger threshold V_5 = 6V.

$$t_5 = \frac{C_{21} \times V_5}{I_5}$$

$t_5 = 1 / (12 \times f_O)$ is recommended.

5.4 Phase adjustment range

The voltage range accepted at Pin 10 is from 0.5V to 4.5V, so the resistor divider must be dimensioned to supply these values.

In our application we have :

$$V_{10\,min} \begin{cases} = \dfrac{V_{19}}{R_7 + P_3 + R_8} R_8 \\ = \dfrac{8}{39 + 47 + 5.1} 5.1 \\ = 0.447V \end{cases}$$

$$V_{10\,max} \begin{cases} = \dfrac{V_{19}}{R_7 + P_3 + R_8} (P_3 + R_8) \\ = \dfrac{8}{39 + 47 + 5.1} 52.1 \\ = 4.575V \end{cases}$$

5.5 Flyback input

The resistor in series at Pin 8 (R_{27}) must be dimensioned in order to have an input current included between 0.7mA and 2mA (typ 1mA), according with the following formula:

$$R_{27} = \frac{V_{fly} - 0.6V}{1mA}$$

6. VERTICAL SECTION

6.1 Frequency

The device is able to work form 30Hz to 120Hz.
The free running frequency is fixed by R_{21} and C_{16}.
The formula to calculate the free running frequency is the following:

$$f_v = \frac{I_C}{(V_{high} - V_{low}) \times C_{16}}$$

but

$$I_C = I = \frac{V_{12}}{R_{21}} \leq 0.5mA$$

then

$$f_v = \frac{V_{12}}{(V_{high} - V_{low}) \times C_{16} \times R_{21}}$$

where $V_{12} = 3.5V$, $V_{high} = 6.8V$ and $V_{low} = 2V$.
In the application proposed the free running frequency is:

$$f_v = \frac{3.5 \times 10^6}{(6.8 - 2) \times 220 \times 62} = 53.4Hz$$

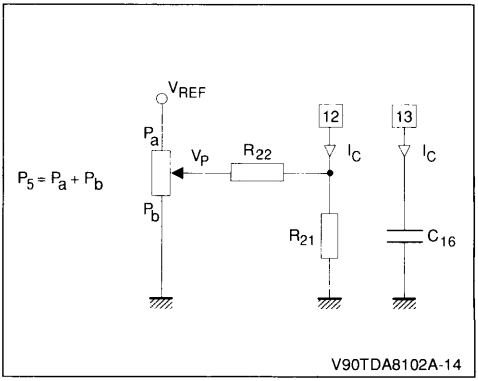
With the trimmer P_5 is possible to change the current that charges C_{16} and consequently to change the free running frequency.

The current in C_{16} due to this correction become:

$$I_C = \frac{V_{12}}{R_{21}} - \frac{V_P - V_{12}}{R_{22}}$$

where $0 \leq V_P \leq 8V$ is the voltage at the central point of the trimmer (see Fig.14).

Figure 14.



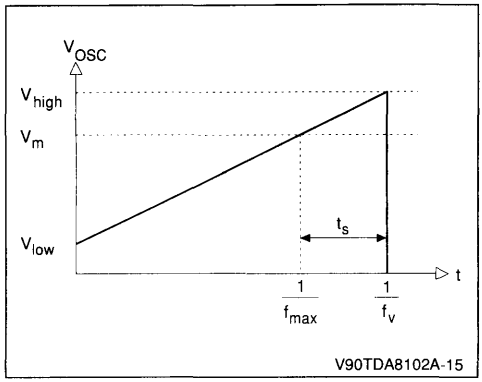
It is easy to substitute the new I_C in the formula in order to obtain the new free running frequency.

6.2 Pull-in range

The vertical pull-in range is fixed by internal thresholds.

With reference to figure 15 :

Figure 15.



we can write :

$f_{pull\ -\ in} = f_{max} - f_v$

$$f_{max} = \frac{1}{t_v - t_s}$$

$$t_s = \frac{(V_{high} - V_m)}{(V_{high} - V_{low})} \times t_v = K_{14} \times t_v$$

the value of K_{14} is 0.333 (see data-sheet).

6.3 Amplitude adjustment range

The voltage range accepted at pin 16 is from 0.5V to 4.5V.

So the resistor divider must be dimensioned to supply these values.

In our application we have:

$$V_{16min} \left| \begin{array}{l} = \frac{V_{19}}{R_5 + P_2 + R_6} R_6 \\ = \frac{8}{39 + 47 + 5.1} 5.1 \\ = 0.447V \end{array} \right.$$

$$V_{16max} \left| \begin{array}{l} = \frac{V_{19}}{R_5 + P_2 + R_6} (P_2 + R_6) \\ = \frac{8}{39 + 47 + 5.1} 52.1 \\ = 4.575V \end{array} \right.$$

This system allows a vertical ramp amplitude variation of ± 20% around the nominal value; the value of amplitude of vertical ramp at Pin 15 can be determined with the following formula:

$$V_{15\ pp} = [K_{16} (V_{16} - 2.5) + K_{15}] V_{13pp}$$

Where K_{15} is typically 1 and K_{16} is typically 0.1 (as you can see on the data-sheet).

6.4 Vertical DC reference

The average value of the vertical ramp at Pin 15 is the half of V_{19}, then with a resistive divider this DC voltage can be used as reference for the vertical booster as shown in Fig.12.

For a best noise immunity we suggest to filter V_{19} with an electrolytic capacitor.

6.5 Linearity correction

The "S" correction is performed with the new concept described in chapter 3.8.

The adjustment is obtained varying the DC voltage at Pin 17 from 1.5 to 4.5V, then the resistor divider (R3, P1 and R4) must be dimensioned for obtaining this range of values.

In our application we have:

$$V_{17min} \left| \begin{array}{l} = \frac{V_{19}}{R_3 + P_1 + R_4} R_4 \\ = \frac{8}{51 + 47 + 22} 22 \\ = 1.466V \end{array} \right.$$

$$V_{17max} \begin{cases} = \dfrac{V_{19}}{R_3 + P_1 + R_4} (P_1 + R_4) \\ = \dfrac{8}{51 + 47 + 22} 69 \\ = 4.6V \end{cases}$$

The "S" correction is not performed when the voltage at Pin 17 is 1.5V, while it is maximum when the Pin 17 voltage is 4.5V.
You can verify this using the following formula:

$$V_{18pp} = K_{18} (V_{17} - 1.5)$$

where K_{18} is typically 1.
If the CRT requires a higher "S" correction, it is possible to obtain it reducing the value of R_{20}; however take care that C_{15} in series with R_{20} is a high-pass filter with the purpose to cut only the D_C.
In our application we have:

$$f_t \begin{cases} = \dfrac{1}{6.28 \times R_{20} \times C_{15}} \\ = \dfrac{10^3}{6.28 \times 150 \times 1} \\ = 1.06 \text{ Hz} \end{cases}$$

The "C" correction is obtained with a resistor in series to a capacitor connected between Pin 15 and the central point of the vertical DC feedback of vertical booster (R_{19} and C_{14}).
The value of R_{19} is strictly dependent on CRT used.

7. LAY-OUT SUGGESTIONS

It is necessary to take care not to connect the horizontal output ground (Pin 6) directly to Pin 11, to avoid horizontal interference on vertical stages.
The 15nF capacitors connected on Pins 10, 16 and 17 have the only aim to filter the DC control voltage against horizontal noise, so they must be connected as close as possible to the above mentioned pins.

8. ADJUSTING PROCEDURE

Here following it is shortly described the procedure to adjust horizontal and vertical frequencies, vertical amplitude, linearity and horizontal phase.
Before starting these operations take care that the horizontal and vertical synchronization pulses are properly applied to the device inputs.

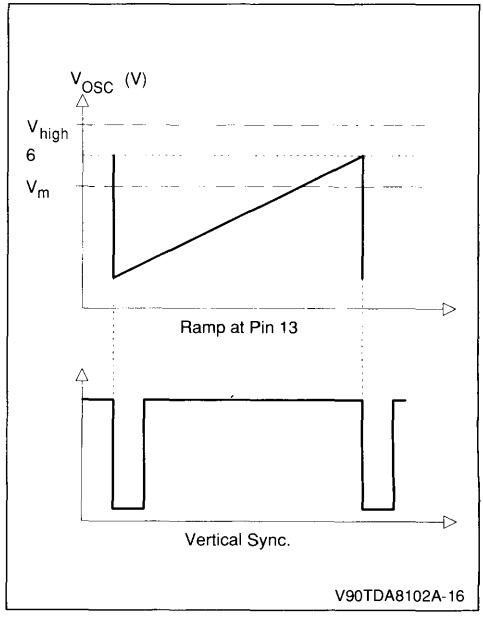
8.1 Horizontal frequency

Adjust P_4 in order to obtain $V_3 = V_1$; in this way the horizontal synchronisation is perfect, and the pull-in range is maximum in both directions.

8.2 Vertical frequency

Adjust the vertical ramp amplitude using P_5 in order to have $4V_{pp}$; in this way the vertical frequency value is in the middle of the synchronization range; as shown in Fig.16.

Figure 16.



This operation is important because some internal circuits are dimensioned for a $4V_{pp}$ ramp.

8.3 Vertical amplitude and horizontal phase

Looking at the display correct P_2 for the right vertical amplitude and adjust P_3 in order to have the correct horizontal phase.

8.4 Vertical linearity

If the vertical ramp at Pin 13 is correctly set the central point of the "M" waveform at Pin 18 will be at the center of the scan; in other case, using P_5, lead the central point of "M" in correspondence of the scan center (see Fig.17).

where : t_S = scan time
$t_V = 1/f_V$ = vertical period
t_{SC} = scan centre
t_C = period centre

In this way the S linearity correction has a uniform behaviour on the top and bottom sides of the CRT. Now looking at the display, adjust P_1 to obtain a right S correction and select R_{19} value to optimise the C correction.

Figure 17.

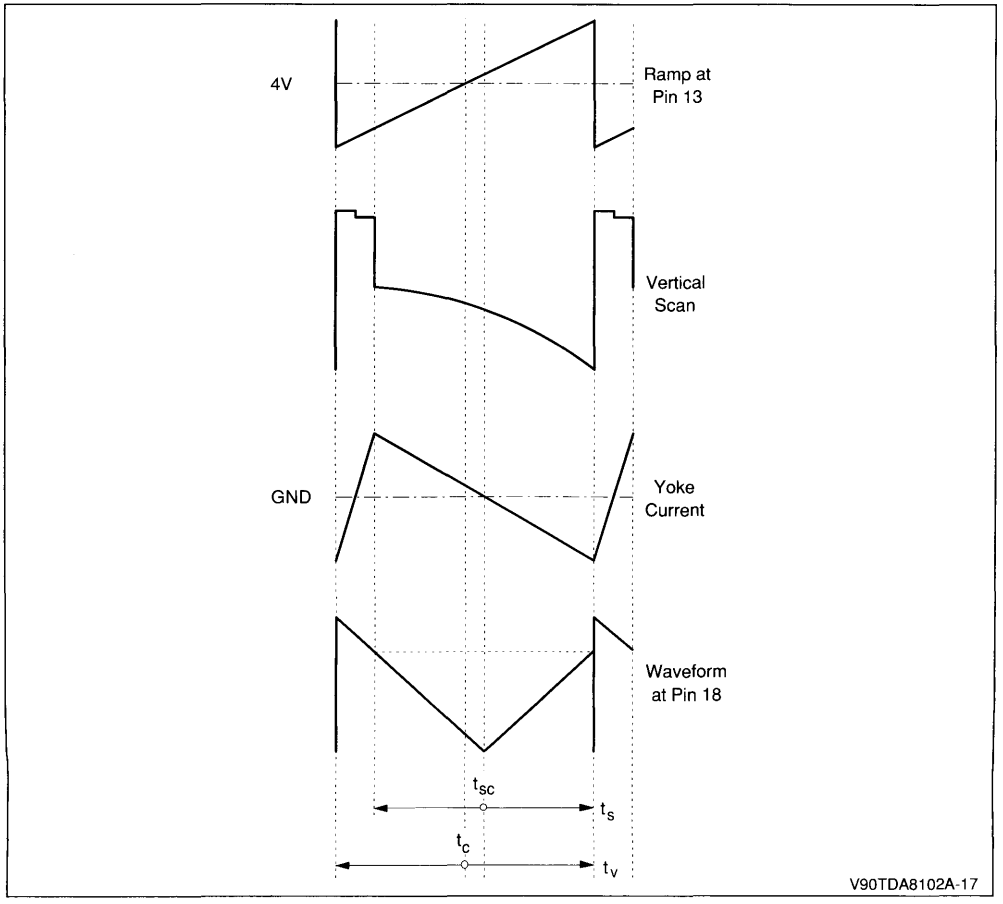
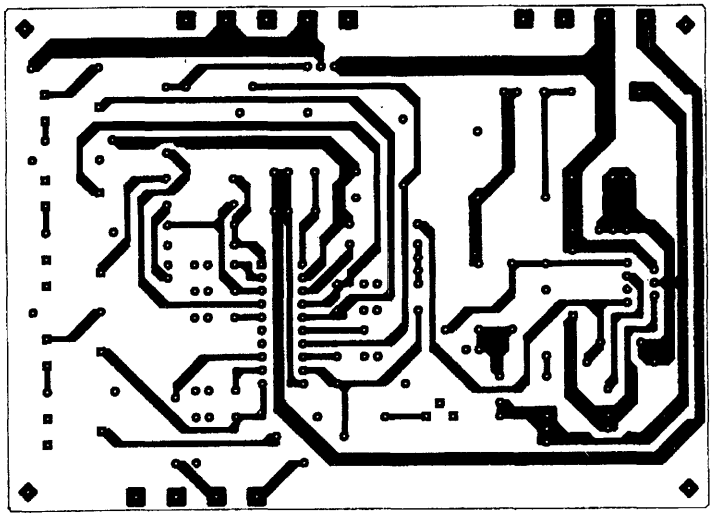
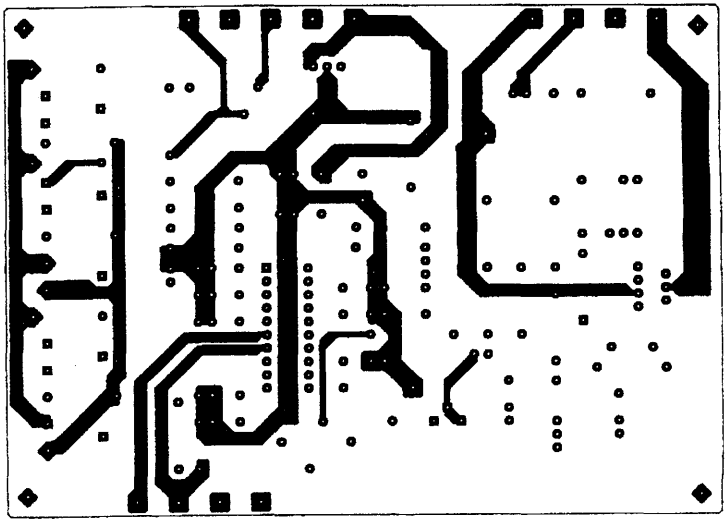


Figure 18 : Solder Side.



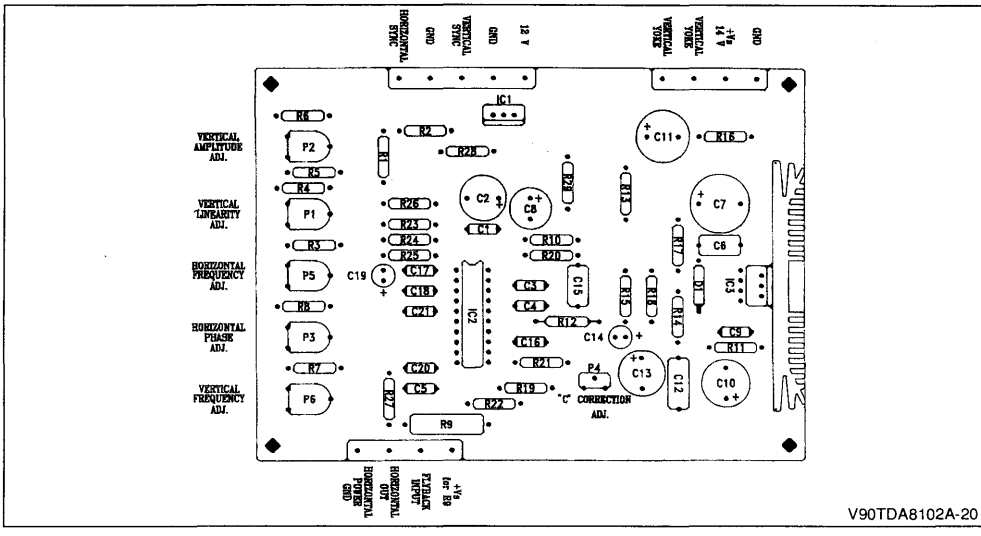
V90TDA8102A-18

Figure 19 : Component Side.



V90TDA8102A-19

Figure 20 : PCB Layout.



9. COMPONENT LIST

Component	Value	Component	Value	Component	Value
R_1, R_2, R_{23}	3.3kΩ	R_{20}	150kΩ	C_{10}	220µF / 25V
R_3	51kΩ	R_{21}	62kΩ	C_{11}	2200µF / 16V
R_4, R_{10}, R_{11}, R_{26}	22kΩ	R_{22}	220kΩ	C_{12}, C_{16}	220nF
R_5, R_7	39kΩ	R_{24}	56kΩ	C_{14}	10µF / 63V
R_6, R_8	5.1kΩ	R_{25}	6.8kΩ	C_{15}	1µF
R_9	82Ω / 2W	R_{27}	100kΩ	C_{17}	1.8nF
R_{12}	10kΩ	R_{28}, R_{29}	2.2kΩ	C_{19}	2.2µF / 63V
R_{13}	120Ω	P_1, P_2, P_3, P_5, P_6	47kΩ hor.	C_{20}	22nF
R_{14}	1.5Ω	P_4	47kΩ ver.	C_{21}	220pF
R_{15}	1.5kΩ	C_1, C_6, C_9	100nF	D_1	1N4001
R_{16}	1Ω	C_2, C_{13}	470µF / 16V	IC_1	L7812
R_{17}	2.7kΩ	C_3, C_4, C_5, C_{18}	15nF	IC_2	TDA8102A
R_{18}	1.2kΩ	C_7	1000µF / 25V	IC_3	TDA8172
R_{19}	33kΩ	C_8	100µF / 16V		

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2260 / TEA2261
HIGH PERFORMANCE DRIVER CIRCUITS FOR S.M.P.S.

SUMMARY

SUMMARY (continued)

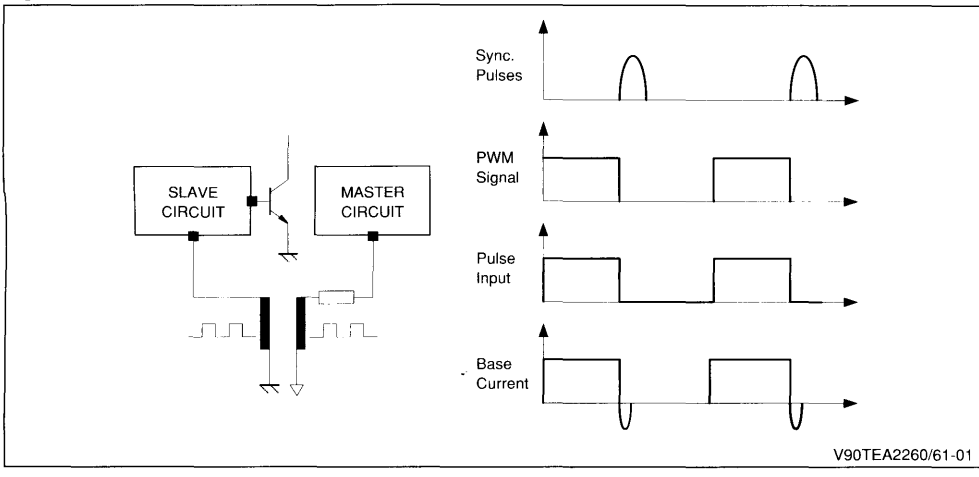
I. INTRODUCTION

The TEA2260/61 is an integrated circuit able to drive a bipolar transistor directly with an output base current up to 1.2A.
So the TEA 2260/61 covers a wide range of application from 80W to more than 200W with all safety requirements respected.
The high performances of the regulation loop provide a very low output power due to an automatic burst mode.
The TEA 2260/61 can be used in a MASTER SLAVE STRUCTURE, in a PRIMARY REGULATION or a SECONDARY REGULATION.
The TEA 2260/61 is very flexible and high performance device with a very large applications field.
The only difference between TEA2260 and TEA2261 concerns security functions (see paragraph II.8)

I.1. MASTER SLAVE MODE (fig.1)

In this configuration the master circuit located on the secondary side, generates PWM pulses used for output voltage regulation. These pulses are sent via a feedback transformer to the slave circuit (Fig.1).
In this mode of operation, the falling edge of the PWM Signal may be synchronized with an external signal. By this way the switching off time of the power transistor, which generates lot of parasites, can be synchronized on the line flyback signal in TV applications.
An other advantage of the MASTER SLAVE STRUCTURE is to have a very good regulation not depending of the coupling between transformer primary and secondary windings, which allows the use of low cost switch mode transformers.

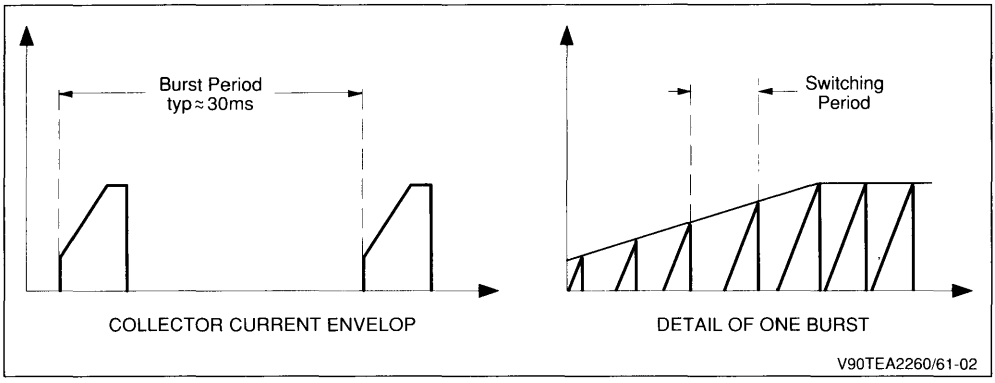
Figure 1.



I.2 BURST MODE (fig.2)

During start-up and stand-by phases, no regulation pulses are provided by the master circuit to the slave circuit.
The slave circuit operates in primary regulation mode. When the output power is very low the burst mode is automatically used.
This operating mode of the SMPS effectively provides a very low output power with a high efficiency. The TEA2260/61 generates bursts with a period varying as a function of the output power.
Thus the output power in burst mode can varied in a wide range from 1W to more than 30W.

Figure 2 : Burst Mode Operation.



I.3. OPERATION OF MASTER SLAVE POWER SUPPLY IN TV APPLICATION

The system architecture generally employed is depicted in Fig.3. On the secondary side a micro controller is connected to the remote control receiver which generates control signal for the stand-by and normal modes of operation (Fig.4).

- In stand-by mode, the device power consumption is very low (few watts). The master circuit does not send pulses and hence the slave circuit works in primary regulation and burst mode.
- In the normal mode, the master circuit provides the PWM signal required for regulation purposes. This is called MASTER SLAVE MODE. The master circuit can be simultaneously synchronized with the line flyback signal.
- Power supply start-up. As soon as the V_{CC}(start) threshold is reached, the slave circuit starts in continuous mode and primary regulation as long as the nominal output voltages are not reached. After this start-up phase the microcontroller holds the TV Set in stand-by mode or either in normal mode.

Figure 3 : TV Application System Diagram.

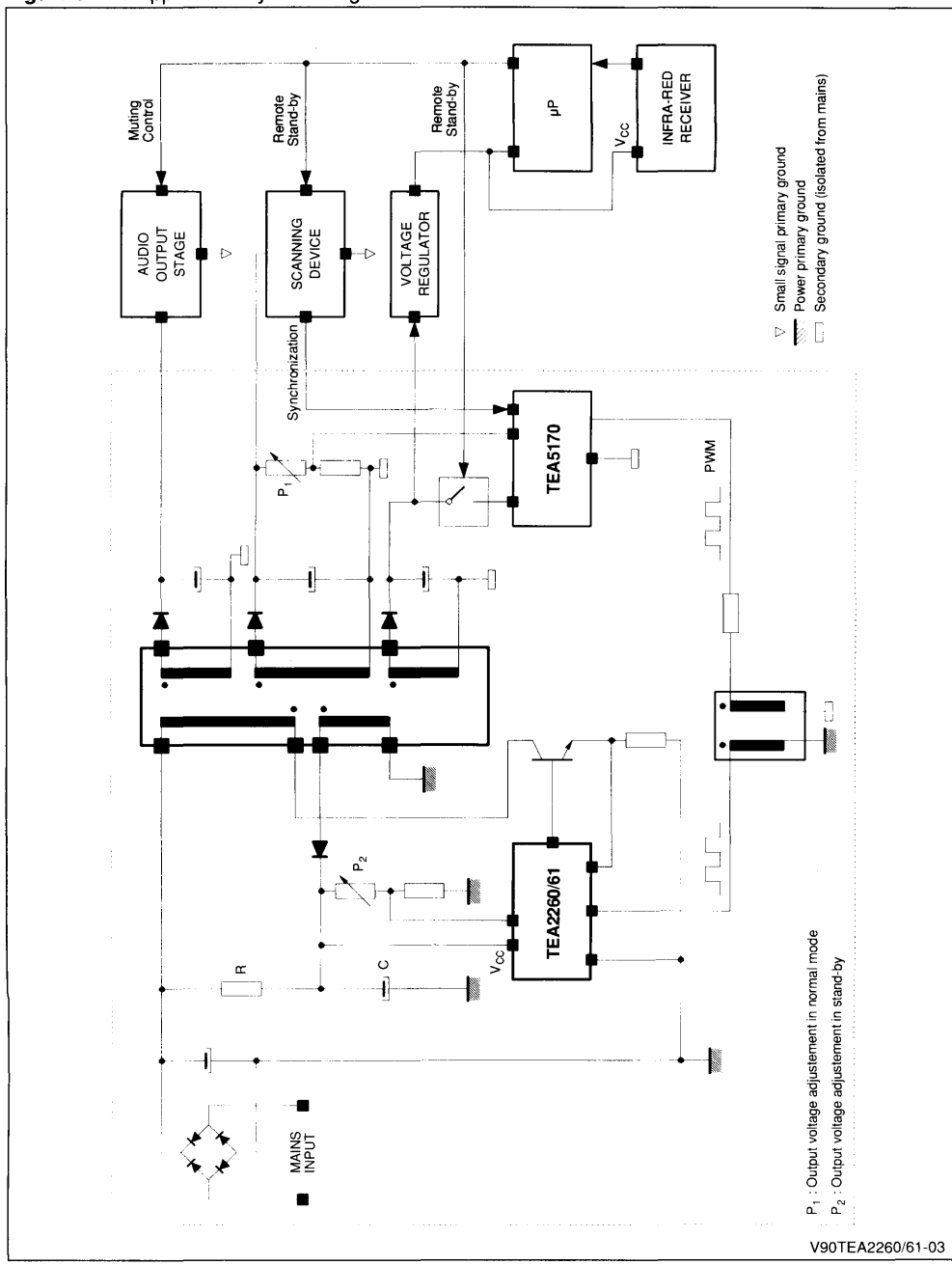
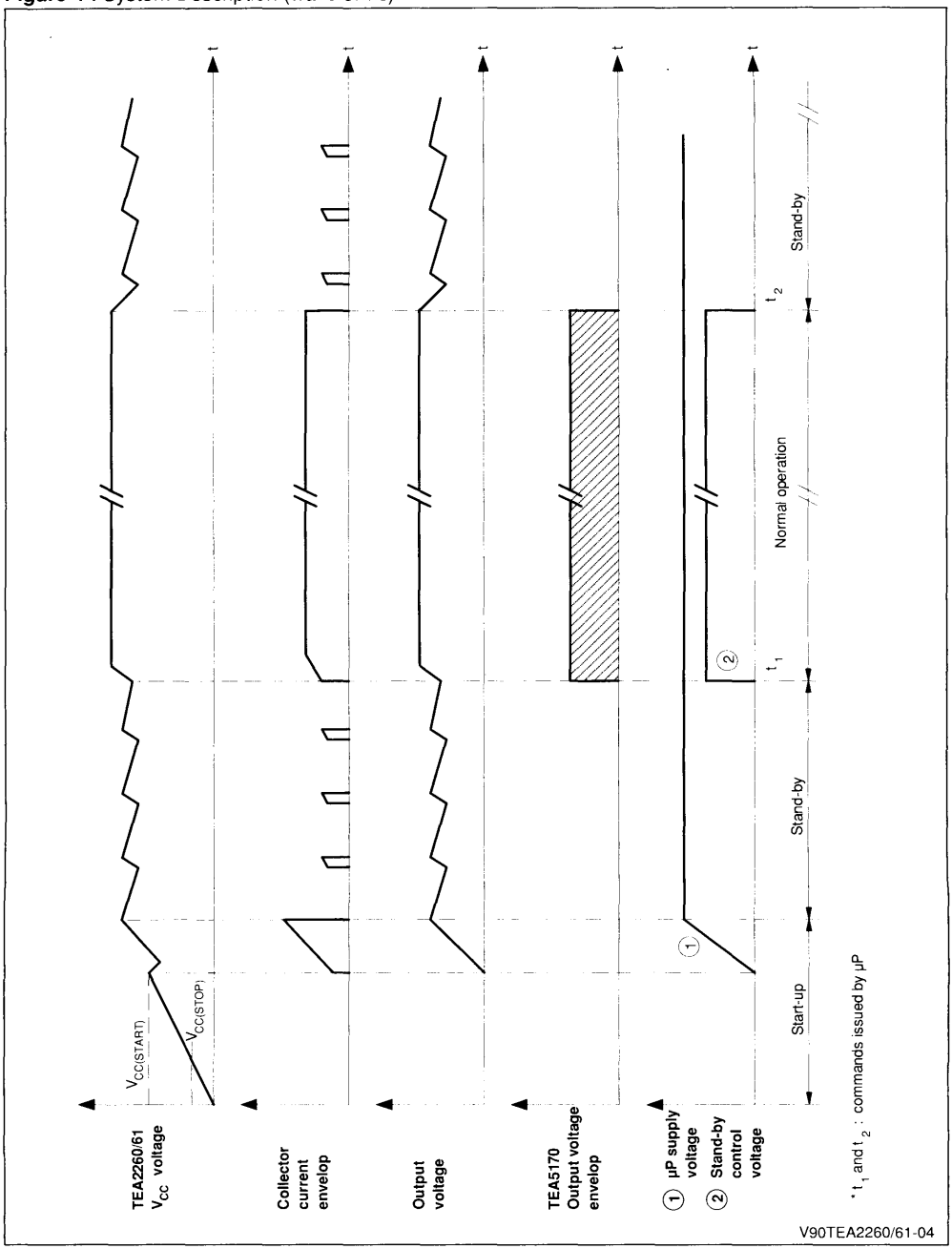


Figure 4 : System Description (waveforms).



I.4. SECONDARY REGULATION (fig.5, 6)

In this configuration the TEA2260/61 provides the regulation through an optocoupler to ensure good accuracy.

The advantage of this configuration is the avaibility of a large range of output power variation (e.g 1W to 110W).

This feature is due to the automatic burst mode (see paragraph II.6).

The structure in a TV Set is simpler than the MASTER SLAVE STRUCTURE because the power supply switches from normal mode to burst mode automatically as a function of the output power.

Figure 5 : TV Application System Diagram.

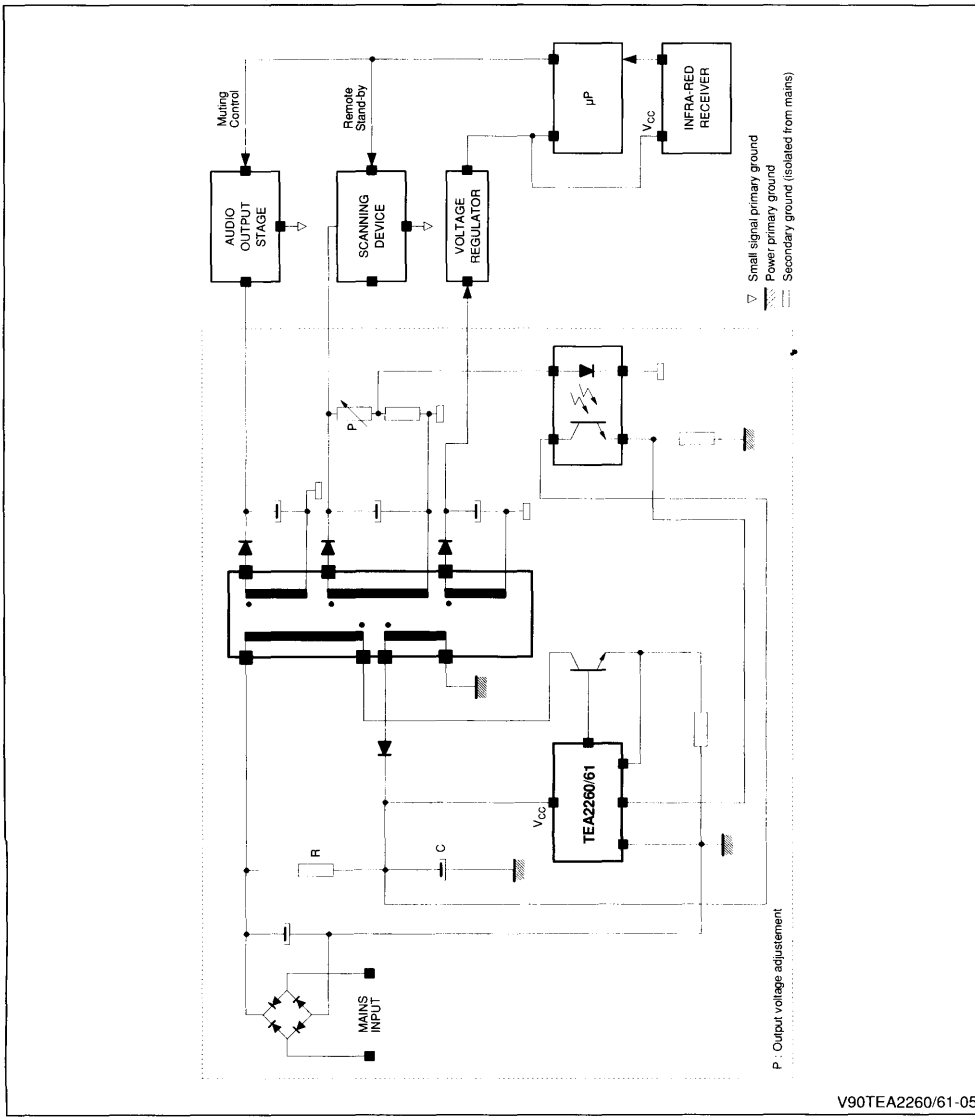
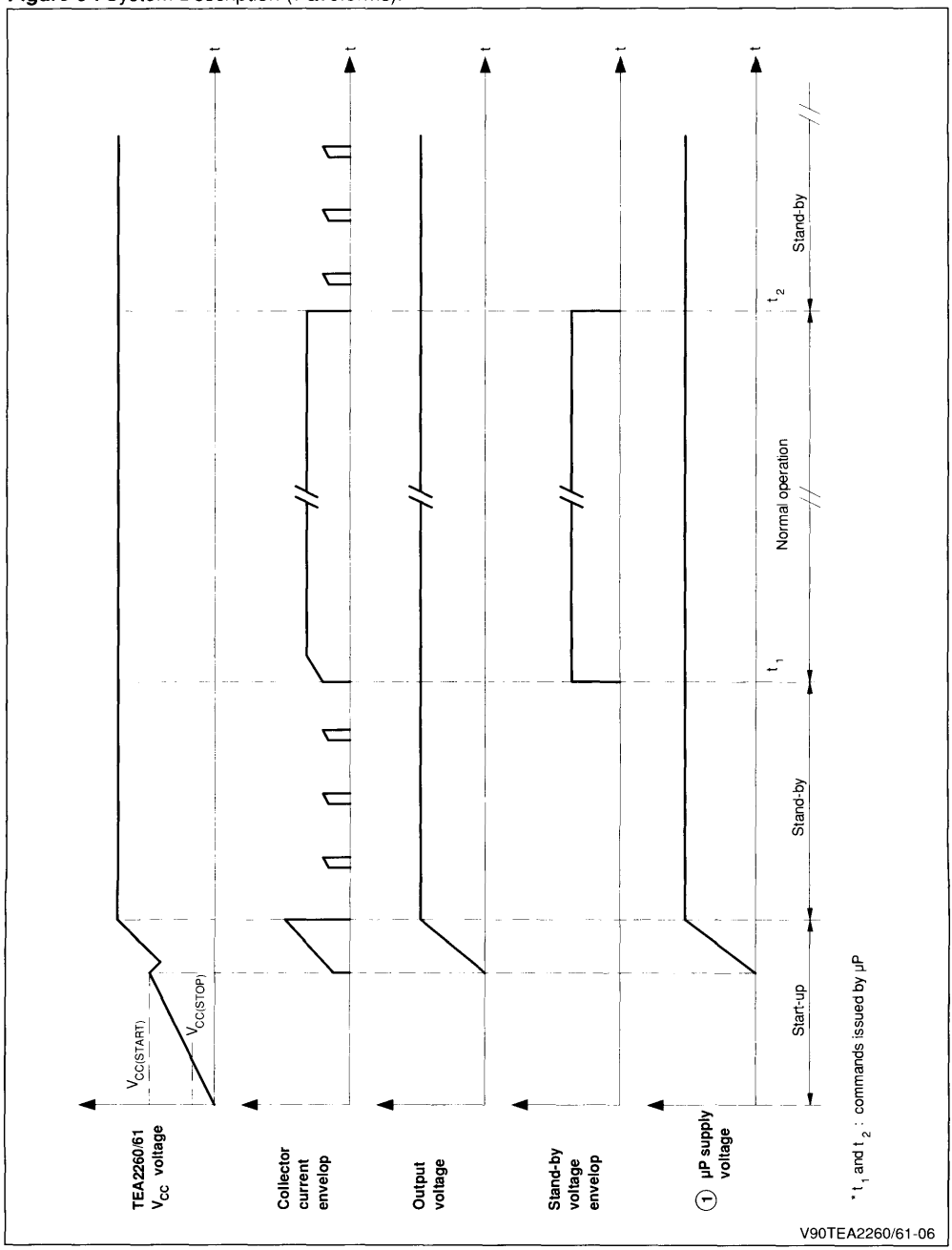


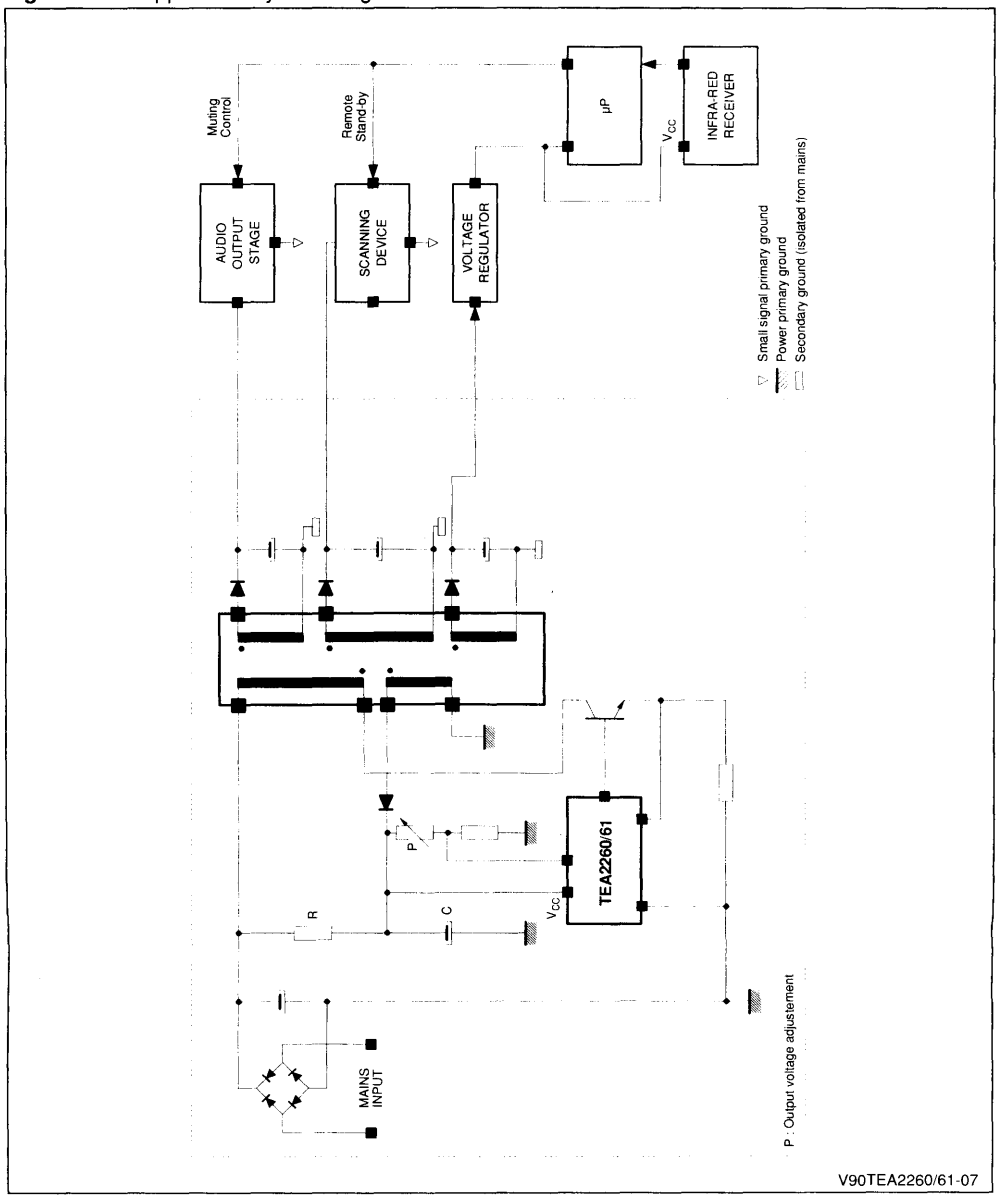
Figure 6 : System Description (waveforms).



I.5. PRIMARY REGULATION (fig.7)

In this configuration the TEA2260/61 provides the regulation through an auxilliary winding.
This structure is very simple but the accuracy depends on the coupling between the transformer primary and secondary winding.
Due to the automatic burst mode the output power can vary in a large range.

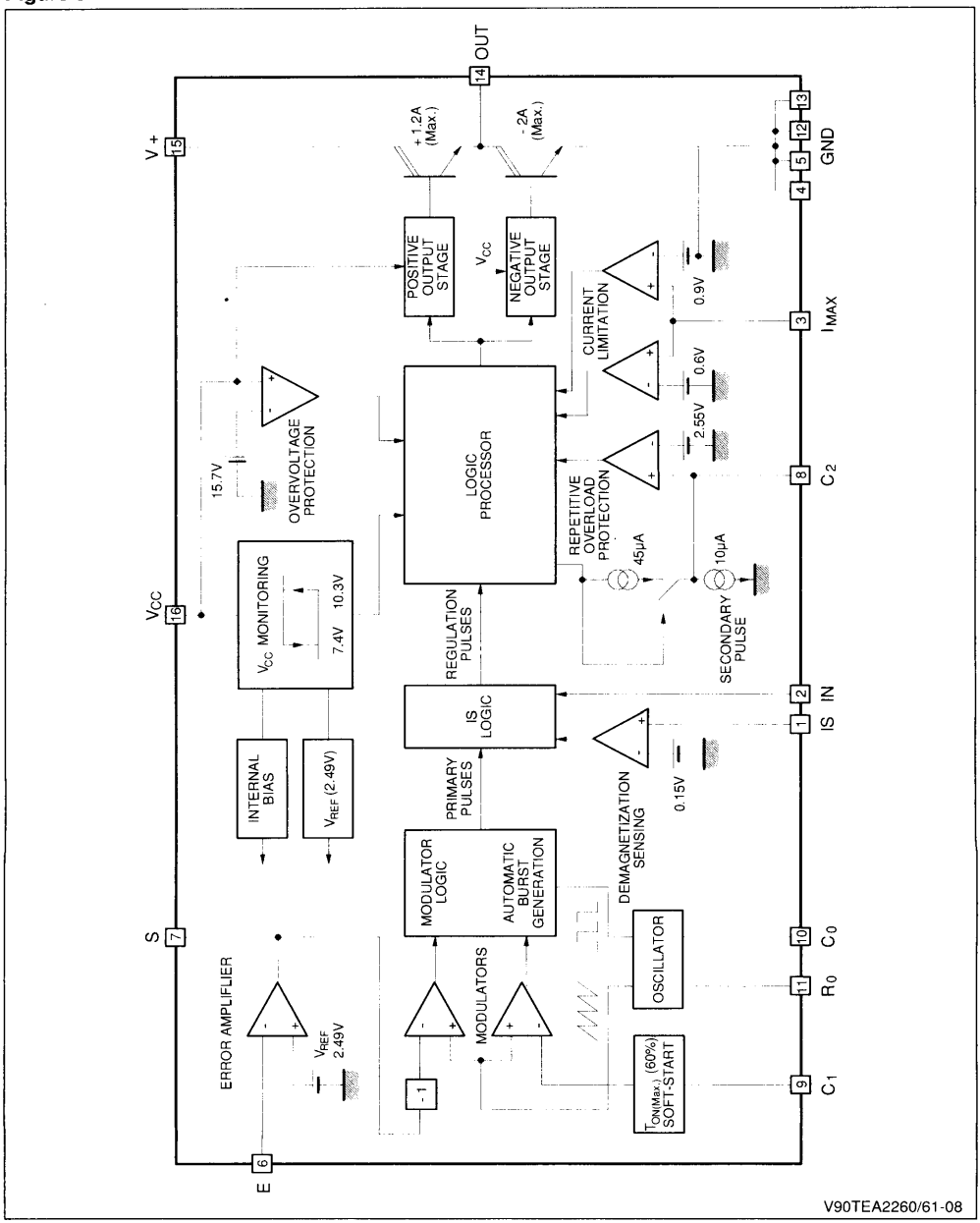
Figure 7 : TV Application System Diagram.



II. CIRCUIT DESCRIPTION

Figure 8 shows the integrated functions.

Figure 8.



The circuit contains 8 blocks :

- Voltage reference and internal V_{CC} generation.
- RC oscillator
- Error amplifier
- Pulse width modulator (PWM)
- "Is logic" for transformer demagnetization checking.
- Current limitation sub-unit (IMAX)
- Logical block.
- Output stage.

II.1. VOLTAGE REFERENCE AND INTERNAL V_{CC} GENERATION (fig.9)

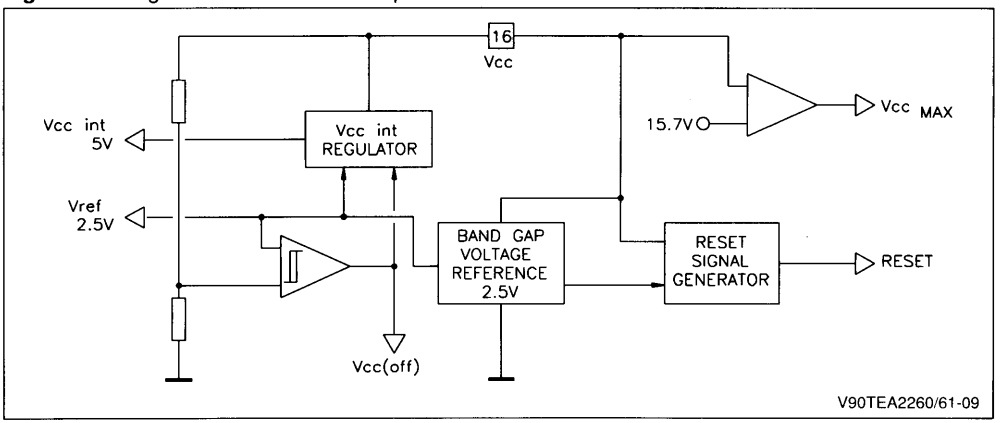
This block generates a 2.5 V typ. voltage reference valid as soon as V_{CC} exceeds 4V. It is not directly accessible externally but is transmitted to other blocks of the circuit.

This block also generates an internal regulated V_{CC}, $V_{CC(int)}$, the nominal value of which is 5V. $V_{CC(int)}$ supplies the circuit when Vcc is higher than $V_{CC(start)}$ (10.3V typ.).

This allows the circuit to achieve a good external V_{CC} rejection, and to provide high performance even with large V_{CC} supply voltage variations.

This block also generates initialization and control signals for the logical block. It also contains the $V_{CC(Max.)}$ comparator (typ threshold 15.7V).

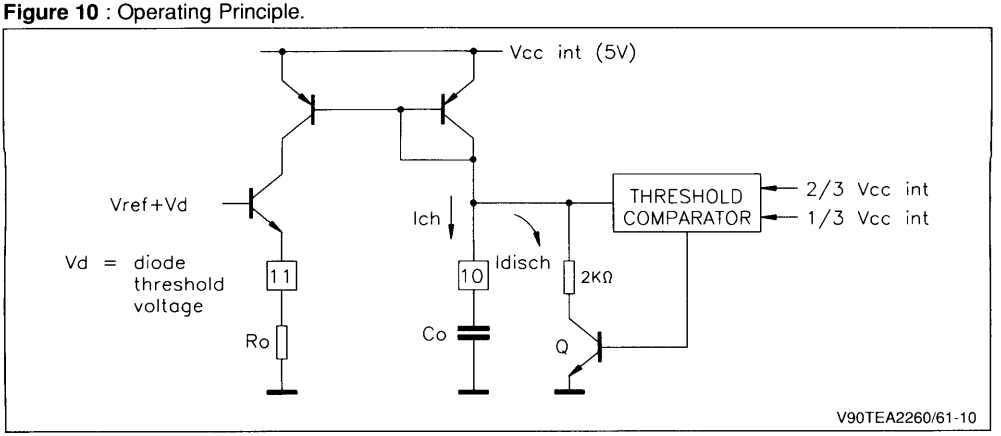
Figure 9 :Voltage Reference Block Principle.



II.2. OSCILLATOR (fig 10,11)

The oscillator determines the switching frequency in primary regulation mode. Two external components are required : a resistor R_O and a capacitor C_O. The oscillator generates a sawtooth signal, which is available on pin 10.

Figure 10 : Operating Principle.

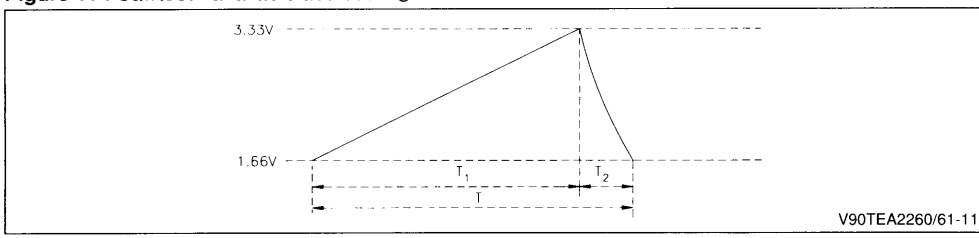


C_O capacitor is charged with a constant current. The current is fixed by R_O which is supplied by voltage Vref.

$$I_{ch} = \frac{2.5}{R_O}$$

When the voltage across C_O reaches $\frac{2}{3}$ x V_{CCint} (typ 3.33V), Q Transistor conducts and C_O is quickly discharged into an 2kΩ (typ) internal resistor. When the voltage reaches 1/3 x $V_{CC\text{-}int}$ (typ 1.66V), the discharge is stopped, and the linear charge starts again.

Figure 11 : Sawtooth available accross C_O.



Theoretical values of T, T_1 and T_2 as function of R_O and C_O :

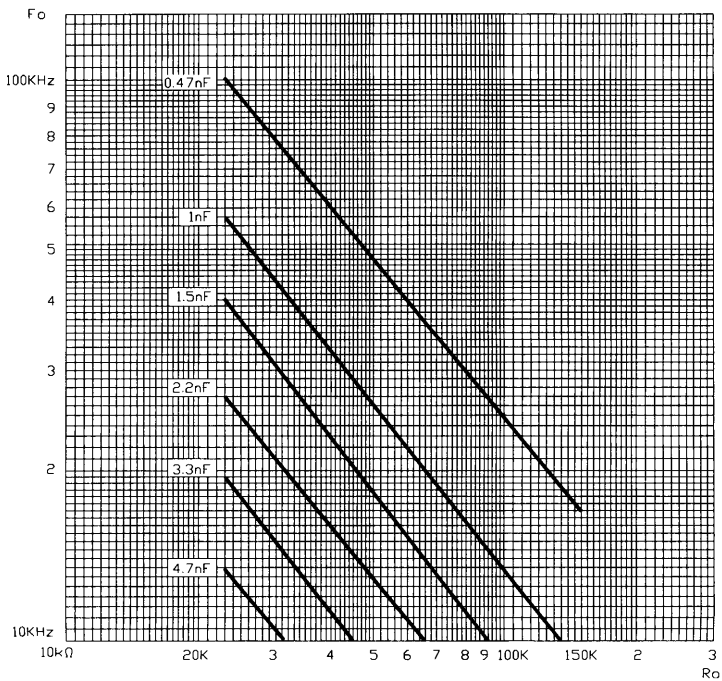
$T = C_O (0.69 \times R_O + 1380)$

$T_1 = R_O \times C_O \times 0.69$

$T_2 = C_O \times 2000 \times 0.69 = C_O \times 1380$

Due to the time response of comparators and normal spread on thresholds values, the real values of T_1 and T_2 may be slightly different, compared with these theoretical values. (see following curves).

Figure 12 : Frequency as a Function of R_O and C_O.



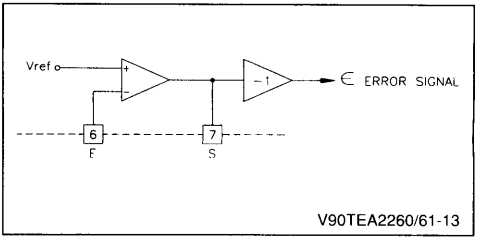
II.3. ERROR AMPLIFIER (fig.13)

It is made of an operational amplifier. The open loop gain is typically 75dB. The unity gain frequency is 550kHz (typ). An internal protection limits the output current (pin 7) at 2mA in case of shorted to ground.

Output and inverting input are accessible thus giving high flexibility in use. The non-inverting input is not accessible and is internally connected to V_{REF} (or 0.9 V_{REF} in burst mode - see paragraph II.6)

Before driving the pulse width modulator (PWM) and in order to get the appropriate phase, the error amplifier is followed by an inverter.

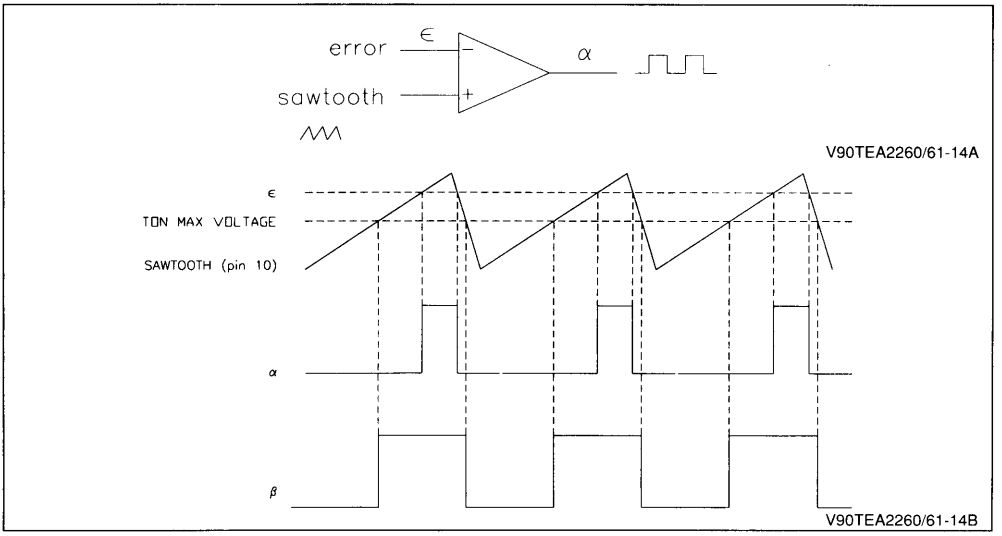
Figure 13 .



II.4. PULSE WIDTH MODULATOR(PWM)(fig.14)

The pulse width modulator consists of a comparator fed by the output signal of the error amplifier and the oscillator output. Its output is used to generate conduction signal.

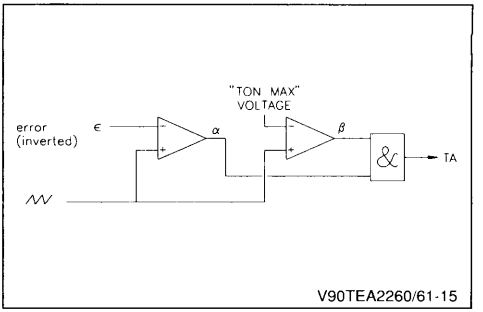
Figure 14 .



The TEA2260/61 actually integrates two PWM :

- A main PWM generates a regulation signal ($\propto$) by comparing the error signal (inverted) and the sawtooth.
- An auxiliary PWM generates a maximum duty cycle conduction signal (β), by comparing the sawtooth with an internal fixed voltage. Furthermore, during the starting phase of the SMPS, in association with an external capacitor, this PWM generates increasing duty cycle, thus allowing a "soft" start-up.
- A logic "AND" between signals ($\propto$) and (β) provides the primary regulator output signal T_A.

Figure 15.

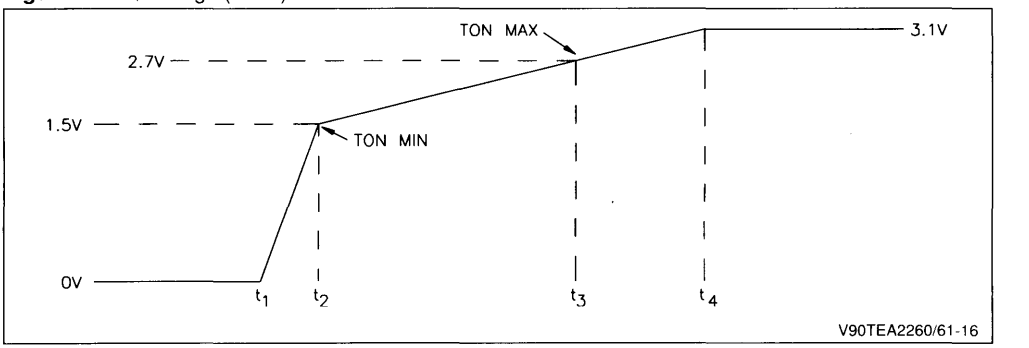


II.5. SOFT START OPERATION (fig.16)

From t_1 to t_2, there is no output pulse (pin 14) and C_1 is charged by a 180µA current (typically). When C_1 voltage reaches 1.5V (typically), output pulses appear and the charge current of C_1 is divided by 20 (9µA typically), then the duty cycle increases progressively. When C_1 voltage reaches 2.7V (typically), the soft-starting device ceases to limit the duty cycle, which may reach 60%

Under established conditions C_1 voltage is charged to 3.1V (typically)

Figure 16 : C_1 Voltage (Pin 9).



II.6. BURST GENERATION IN STAND BY (primary regulation mode)

When the SMPS output power becomes very low, the duty cycle of the switching transistor conduction becomes also very low. In order to transmit a low average power, while ensuring correct switching conditions to the power transistor, a "burst" system is used for energy transmission in stand by mode.

Principle :

For a medium output power (e.g. more than 10W), the voltage reference is applied to the non- inverting input of the error amplifier. When output power decreases as the minimum conducting time of the power transistor is reached, the output voltage tends to increase. Consequently the error signal applied to the PWM becomes higher than the sawtooth. This is detected by a special logic and the voltage applied to the non inverting input becomes Vref = 0.9 x 2.5 = 2.25V typically.

Consequently the regulation loop is in an overvoltage equivalent state and the output pulses disappear. The output voltage decreases and when it reaches a value near 0.9 times the normal regulation value , the voltage applied to the non inverting input is switched again to the normal value V_{REF} = 2.5V. Pulses applied to the power transistor reappear, the output voltage increases again, and so on... A relaxation operation is obtained, generating the burst.

Futhermore, to avoid a current peak at the beginning of each burst, the soft-start is used at this instant.

Advantages of this method :

- improved power supply efficiency compared with traditional systems, for low power transmission.
- automatic burst-mode continuous mode transition, as a function of the output power.
- high stand-by power range.
- burst frequency and duty cycle adjustable with external components to the circuit.

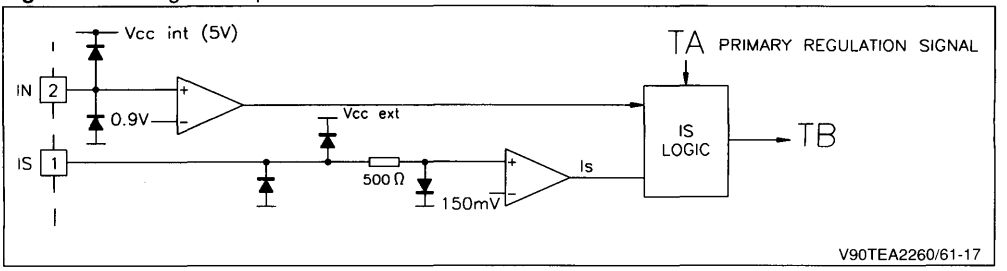
II.7. IS LOGIC (fig.17)

During the transition from the "stand-by" mode to the "normal operating" mode, conduction pulses generated by the secondary regulator occur concurrently with those from the primary regulator.

These pulses are non-synchronous and this may be dangerous for the switching transistor. For example if the transistor is switched-on again during the overvoltage phase, just after switching-off, the FBSOA may not be respected and the transistor damaged.

To solve this problem a special arrangement checking the magnetization state of the power transformer is used.

Figure 17 : IS Logic Principle Schematic.

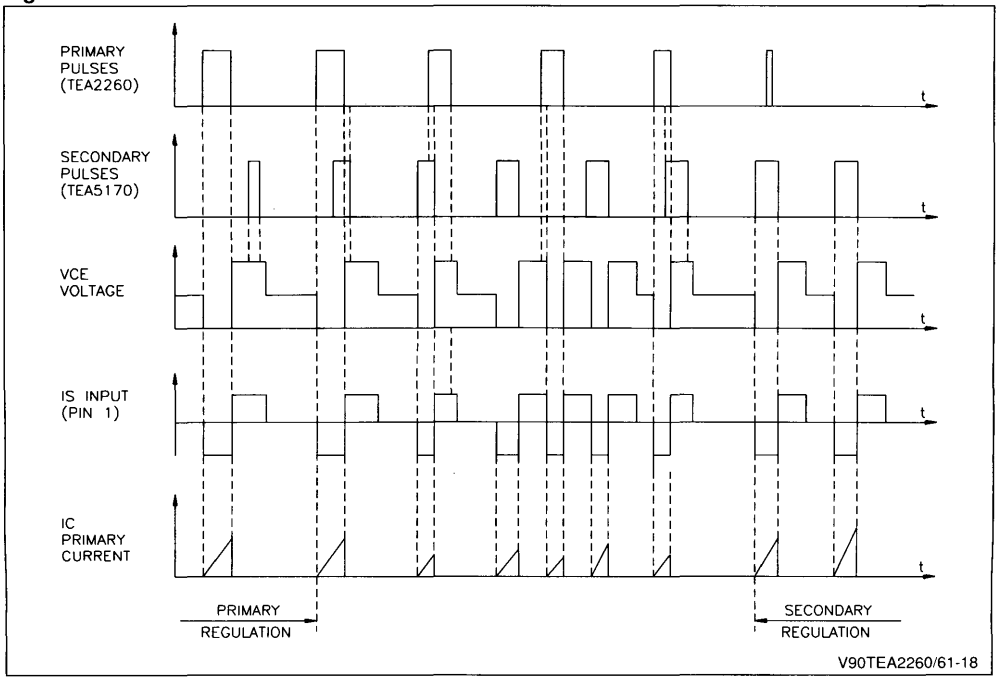


The aim of the IS Logic is therefore to monitor the primary regulation pulses (TA) and the secondary regulation pulses (pin 2), and to deliver a signal TB compatible with the power transistor safety requirements.

The IS Logic block comprises mainly two D flip-flops.

When a conduction signal arrives, the corresponding flip-flop is set in order to inhibit a conduction signal coming from the other regulation loop. Both flip-flops are reset by the negative edge of the signal applied to the demagnetization sensing input (Is Pin 1).

Figure 18.



Note : The demagnetization checking device just described is only active when there are concurrently primary and secondary pulses, which in practice only occurs during the transient phase from Stand-by mode to normal mode.

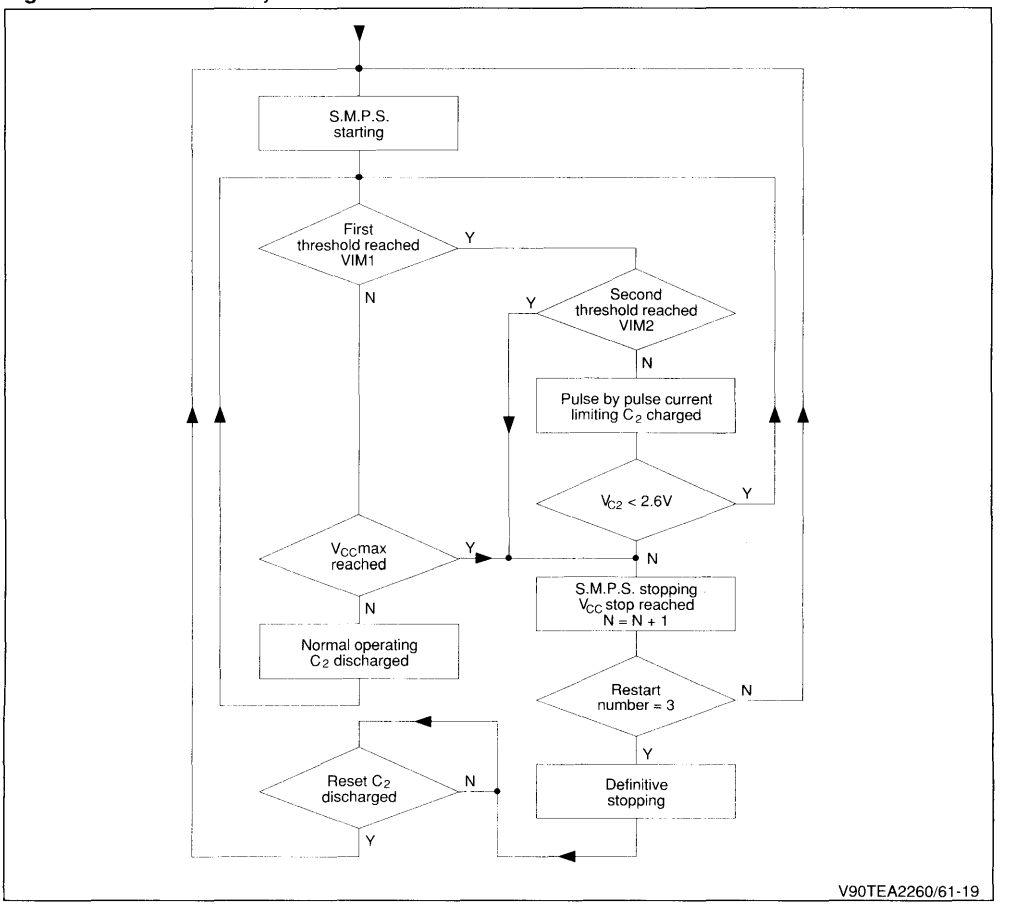
When the power supply is in primary regulation mode **or** in secondary regulation mode, the demagnetization checking function is not activated.

II.8. SAFETY FUNCTIONS : Differences between TEA2260 and TEA2261

TEA2260 :

Concerning the safety functions, V_{CC}(max) (overvoltage detection) VIM1, VIM2 (overcurrent detection) the TEA2260 uses an internal counter which is incremented each time V_{CC}stop is reached (after fault detection) and try to restart. After 3 restarts with fault detection the power supply stops. But in certain cases where the TV set is supplied for a long time, without swich off, the power supply could stop (cases of tube flashes). In this case it is necessary to switch off the TV set and swich on again to reset the internal counter.

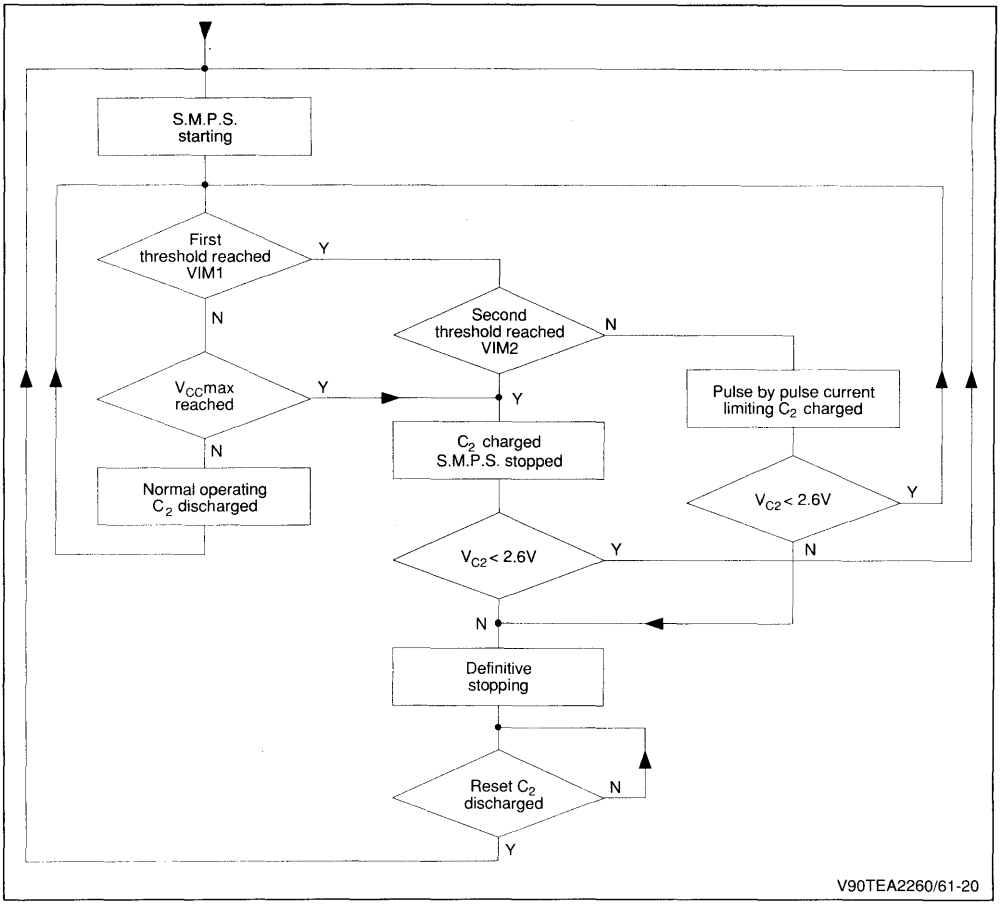
Figure 19 : TEA2260 Safety Functions Flowchart.



TEA2261:

The safety detections are similar to TEA2260 for V_{CC}(max) (overvoltage detection) VIM1, VIM2 (overcurrent detection), but each time a fault detection is operating the C_2 capacitor is loaded step by step up to 2.6V, (case of long duration fault detection) and the power supply stpos. To discharge C_2 capacitor it is necessary to switch off the TV set and to switch on again and the power supply starts up.

Figure 20 : TEA2261 Safety Functions Flowchart.

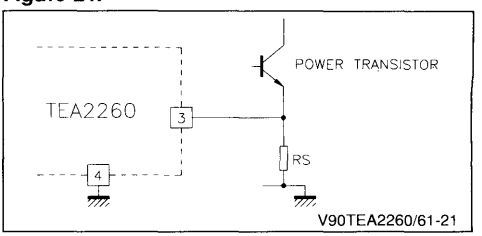


II.8.1. I MAX (power transistor current limitation)

The current is measured by means of a resistor inserted in the emitter of the power transistor. The voltage obtained is applied on pin 3 of the TEA2260/61.

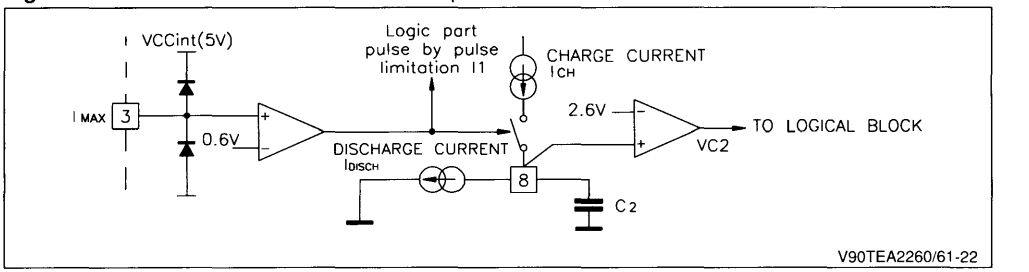
The current limitation device of the TEA2260/61 is a double threshold device. For the first threshold, there is no difference between the two devices, only for the second threshold.

Figure 21.



II.8.1.1. First threshold : VIM1 (typical value)

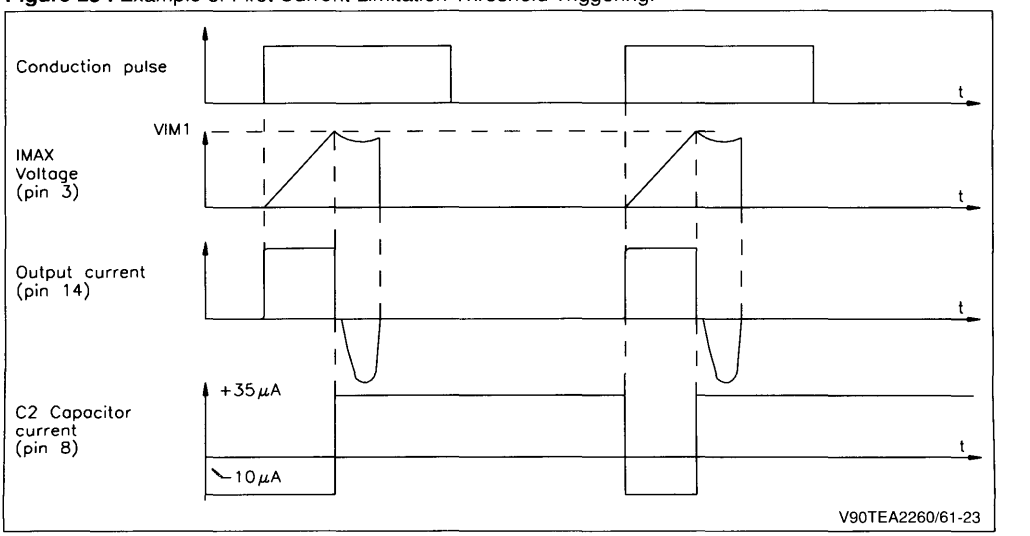
Figure 22 : *Current Limitation* Schematic Principle. First Threshold Part.



Two actions are carried out when the first threshold is reached

- The power transistor is switched-off (pulse by pulse limitation). A new conduction pulse is necessary to switch-on again.
- The C_2 capacitor, which is continuously discharged by Idisch current (10µA typically), is charged by the current
  Ich - I disch (45µA - 10µA = 35µA typically), until the next conduction pulse.

Figure 23 : Example of First Current Limitation Threshold Triggering.



The capacitor C_2 is charged as long as an output overload is triggering the first current limitation threshold. When the voltage across C_2 reaches the threshold V_{C2} (typically 2.55V), output pulses (pin 14) are inhibited and the SMPS is stopped.
A restart may be obtained by decreasing Vcc under the $V_{CC(stop)}$ threshold to reset the IC.

If the output overload disappears before the voltage across C_2 reaches V_{C2}, the capacitor is discharged and the power supply is not turned off.
Due to this feature, a transient output overload is tolerated, depending on the value of C_2 (see III.2.5).

II.8.1.2. Second current limitation threshold (VIM2) for TEA2260

In case of hard overload or short circuit, despite the pulse by pulse current limitation operation, the current in the power transistor continues to increase. If the second threshold VIM2 is reached, the power supply is immediately turned off and the internal counter is incremented. After 3 restarts, the power supply is definitively stopped. Restart is obtained by decreasing V_{CC} below $V_{CC(stop)}$, as in the case of stopping due to the repetitive overload protection triggering.

II.8.1.3. Second current limitation threshold (VIM2) for TEA2261

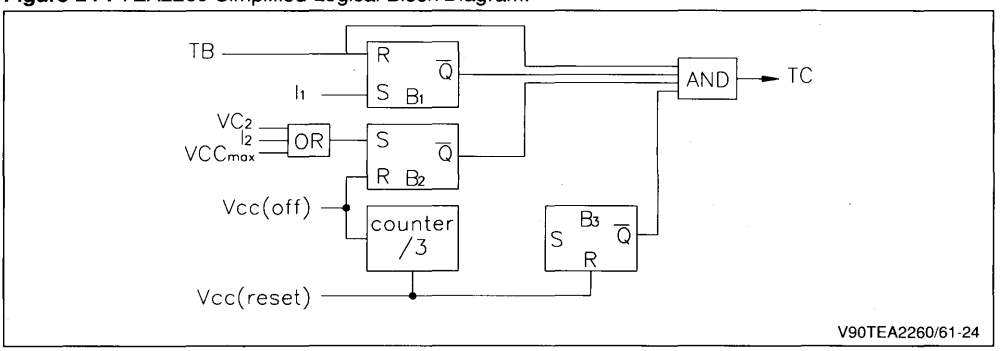
For this device, if the second threshold is reached, the power supply is turned off, C_2 is charged and a new start-up is authorized only if $V_{C2} < 2.6V$.

II.8.2. LOGICAL BLOCK :

This block receives the safety signals coming from different blocks and inhibits the conduction signals when necessary.

II.8.2.1. Logical block for TEA2260

Figure 24 : TEA2260 Simplified Logical Block Diagram.



TB is the conduction signal (primary or secondary)coming from the Is logical block.

TC is the conduction signal transmitted to the output stage.

I_1 is the output signal of the first current limitation threshold comparator. It is memorized by the flip-flop B_1.

I_2 is the output signal of the second current limitation threshold comparator

V_{C2} is the output signal of the comparator checking the voltage across C_2.

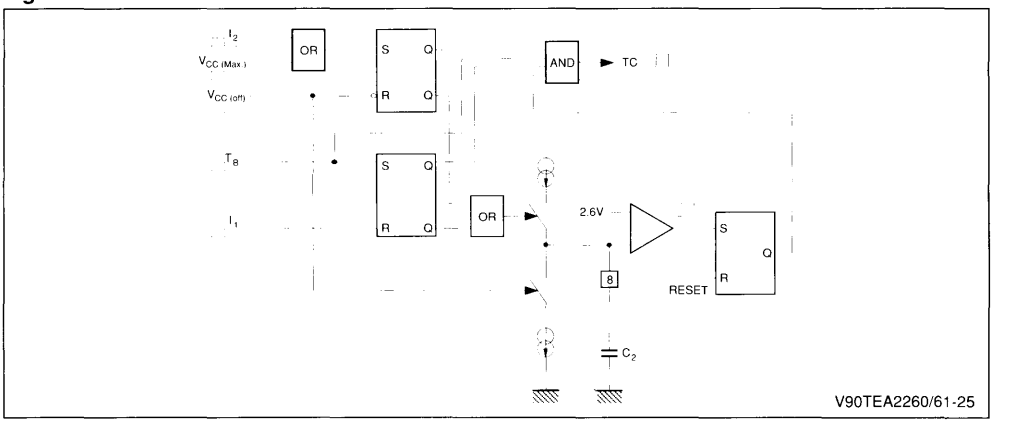
$V_{CC(Max.)}$ is the signal coming from V_{CC} checking comparator.

These three signals V_{C2}, I_2, $V_{CC(Max.)}$ are memorized by B_2.
In case of B_2 flip-flop setting (I_2 or V_{C2} or $V_{CC(Max.)}$ defect) the current consumption on V_{CC} increases. This function allows to decrease the V_{CC} voltage until $V_{CC(stop)}$. After this the current consumption on Vcc decreases to $I_{CC(start)}$ and a new start up is enabled.

The $V_{CC(Off)}$ signal comes from the comparator checking V_{CC}. A counter counts the number of $V_{CC(off)}$ establishment. After four attempted starts of the power supply the output of the circuit is inhibited. To reset the circuit it is necessary to decrease V_{CC} below 5.5V typically. In practice this means that the power supply has to be disconnected from the mains.

II.8.2.2.Logical block for TEA2261

Figure 25.

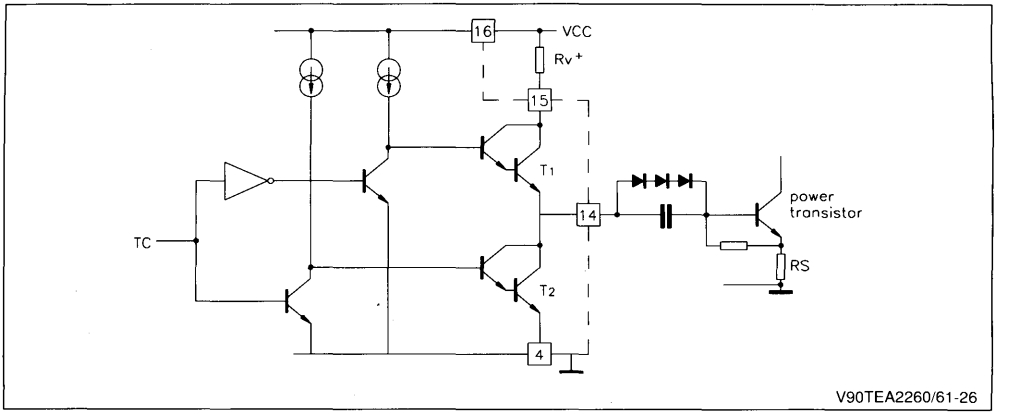


V_{CC}(off) is a signal coming from a comparator checking V_{CC}. When V_{CC} > V_{CC}(stop),V_{CE}(off) is high.
V_{CC}(max) is a signal coming from a comparator checking V_{CC}. When V_{CC} > V_{CC}(max),V_{CC}(max) is high.
I_1 is a signal coming from the first current limitation threshold comparator.
When I_{max} x R_{SHUNT} > VIM1, I_1 is high.
I_2 is a signal coming from the second current limitation threshold comparator.
When I_{max} x R_{SHUNT} > VIM2,I_2 is high.
TB is the conduction signal coming from the error ampliflier system.
TC is the output signal transmitted to the output stage.

II.9. OUTPUT STAGE

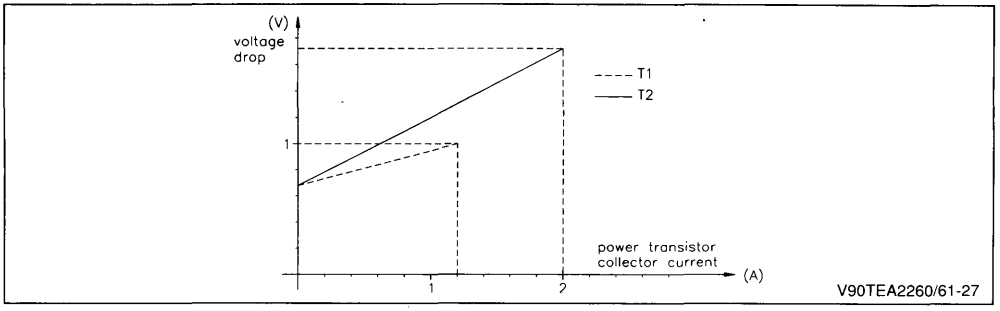
The output stage is made of a push-pull configuration : the upper transistor is used for power transistor conduction and the lower transistor for power transistor switch-off.

Figure 26.



A capacitive coupling is recommanded in order to provide a sufficient negative base current through the power transistor .

Figure 27 : Typical Voltage Drops of Output Transistor versus Current.



Important remark : Due to the internal output stage structure, the output voltage (Pin 14) must never exceed 5V. This condition is respected when a bipolar transistor is driven.
Note that Power-MOS transistor drive is not possible with the TEA2260/61.

III. TV APPLICATION 120W - 220 VAC - 16 kHZ SYNCHRONIZED ON HORIZONTAL DEFLECTION FREQUENCY

General structure and operational features of this power supply were outlined in section I.
The details covered below apply to a power supply application using the master circuit TEA5170.
(refer to TEA5170 data sheet and TEA5170 application note "AN088" for further details).

III.1. CHARACTERISTICS OF APPLICATION

- Discontinuous mode Flyback SMPS
- Standby function using the burst mode of TEA2260/61
- Switching Frequency
  - Normal mode : 15.625 kHz (synchronized on
  - horizontal deflection frequency)
  - Standby mode : about 16 kHz
- Nominal mains voltage : 220 VAC
- Mains voltage range : 170 VAC to 270 VAC
- Nominal output power : 120W
- Output power range in normal mode $14W < P_O < 120W$
- Output power range in standby mode $1W < P_O < 25W$
- Efficiency
  - Normal mode : 85% (under nominal conditions)
  - Stand by mode : 45%
- Regulation performance on high voltage output : 140 VDC
  - ± 0.3% versus mains variations of 170 VAC to 270 VAC (P_{OUT} : 120W)
  - ± 0.5% versus load variations of 14W to 120W (V_{in} = 220 VAC)
- Overload protection and complete shut down after a predetermined time interval.
- Short circuit protection.
- Open load protection by output overvoltage detection
- Complete power supply shut-down after 3 restarts resulting in the detection of a fault condition for TEA2260.
- Complete power supply shut-down when V_{C2} reaches 2.6V for TEA2261.

III.2. CALCULATION OF EXTERNAL COMPONENTS

Also refer to TEA5170 application note "AN408/0591" for calculation methods applicable to other power supply components.

The external components to TEA2260/61 determine the following parameters :

- Operating Frequency in primary regulation
- Minimum conduction time in primary regulation
- Soft start duration
- overload duration
- Error amplifier gain and stand-by output voltage
- Base drive of the switching transistor
- Primary current limitation

Ideal values :

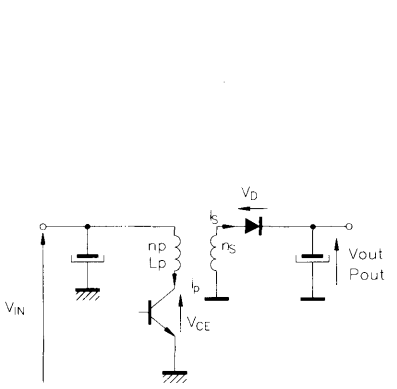
- Free running Frequency in stand-by mode : 16kHz
- $Ton_{(min)}$ duration : 1µs
- Soft start duration : 30ms
- Maximum overload duration : 40ms
- Error amplifier Gain : 15
- Maximum primary current depends on the transformer specifications

III.2.1. Transformer calculation

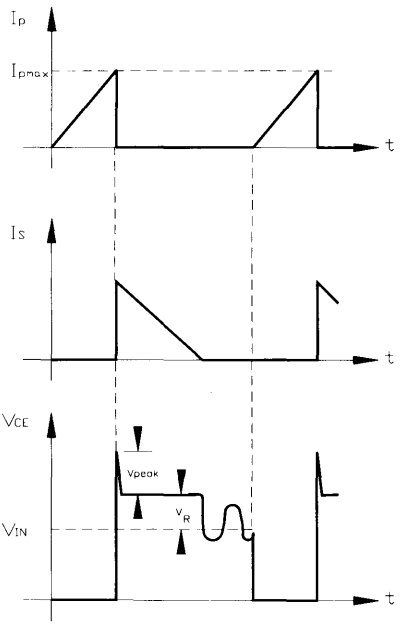
The following important features must be considered to calculate the specifications of the transformer :

- Maximum output power : 120W
- Minimum input voltage :
- 220 VAC - 20% → Vin(min) = 210 VDC with 40V ripple on the high voltage filtering capacitor
- Switching Frequency : 15.625kHz
- Maximum duty cycle : 0.45
- Output voltages :
  + 140V - 0.6A
  + 14V - 0.5A
  + 25V - 1A
  + 7.5V - 0.6A
  + 13V - 0.3A

Figure 28.



V90TEA2260/61-28A



V90TEA2260/61-28B

Maximum primary current

$$I_{P(max)} = 2 \times \frac{P_{OUT}}{\eta \times V_{IN(min)} \times \frac{T_{ON(max)}}{T}}$$

η : efficiency of the power supply $0.80 < \eta < 0.85$

Primary inductance of the transformer

$$L_P = \frac{V_{IN(min)}}{I_{P(max)}} \times T_{ON(max)}$$

Transformer ratio

$$\frac{ns}{np} = \frac{(V_{OUT} + V_D) \times T_{DM}}{V_{IN(min)} \times T_{ON(max)}}$$

Reflected voltage

$$V_R = \frac{1}{\frac{T}{T_{ON(max)}} - 1} \times V_{IN(min)}$$

Overvoltage due to the leakage inductance

$$V_{PEAK} = \frac{I_{P(max)}}{2} \times \sqrt{\frac{L_f}{C}}$$

with : Lf = leakage inductance of the transformer
$0.04 \times Lp < Lf < 0.10 \times Lp$
C = capacitor of the snubber network (see III.2.2.2)

Numerical application

To determine the specifications of the transformer, it is necessary to make a compromise between a maximum primary current and a maximum voltage on the transistor :

- To minimize the maximum primary current

with $0.4 < \frac{T_{ON(max)}}{T} < 0.5$

- To minimize the maximum voltage on the transistor during the demagnetization phase.

$0.3 < \frac{T_{ON(max)}}{T} < 0.4$

When the output power of the power supply is greater than 100W it is better to minimize the maximum primary current because the current gain $B_f = I_C / I_B$ of bipolar transistor is $1.5 < B_f < 6$

Choice : $\frac{T_{ON(max)}}{T} < 0.45$

$$I_{P(MAX)} = \frac{2 \times P_{OUT}}{\eta \times V_{IN(MIN)} \times \frac{T_{ON(MAX)}}{T}} = \frac{2 \times 120}{0.85 \times 210 \times 0.45} = 3A$$

$$L_P = \frac{V_{IN(MIN)}}{I_{P(MAX)}} \times T_{ON(MAX)} = \frac{210}{3} \times 0.45 \times 64\ 10^{-6} = 1.95mH$$

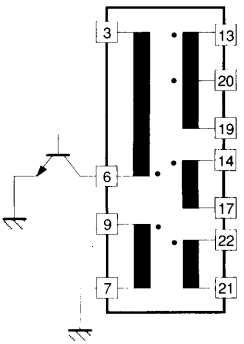
$$V_R = \frac{1}{\frac{T}{T_{ON(MAX)}} - 1} \times V_{IN(MIN)} = \frac{1}{\frac{1}{0.45} - 1} \times 210 = 172V$$

V_{PEAK} will be calculated with the snubber network determination (see II.2.2.2.1)

III.2.1.1 Transformer specification

- Reference : OREGA - SMT5 - G4467-03
- Mechanical Data :
  - Ferrite : B50
  - 2 cores : 53 x 18 x 18 (mm) THOMSON-LCC
  - Airgap : 1.7 mm
- Electrical Data :

Figure 29.



Winding	Pin	Inductance
n_P	3-6	1.95µH
n_{AUX}	7-9	8.1µH
n2	19-13	770µH
n3	19-20	8.2µH
n4	14-17	4.2µH
n5	22-21	31.7µH

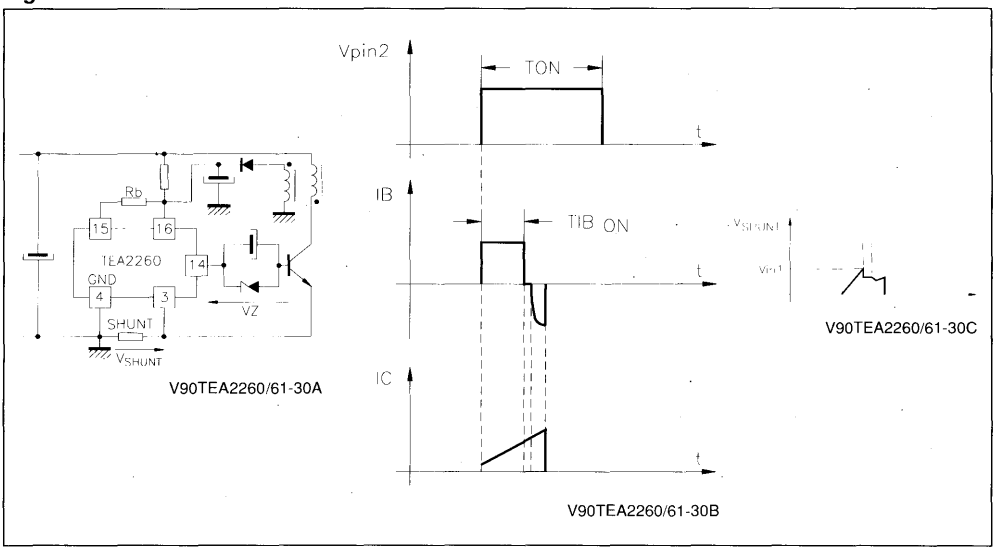
V90TEA2260/61-29

III.2.2. Switching transistor and its base drive

III.2.2.1. First current limitation

Note : in current limitation TIBon < T_{ON}

Figure 30 : Current Limitation.



The current measurement is $I_E = I_B + I_C$

The maximum collector current calculated in III.2.1 is $I_{C(Max.)}$ = 3A (a switching transistor SGSF344 may be chosen)

The current gain is: $B_f = \frac{I_C}{I_{B+}} = 3.5$

The current limitation is :

$$I_{E(max)} = I_{P(max)} - (T_S \times \frac{V_{IN(min)}}{L_P}) + I_{B+}$$

with : T_S = storage time of the switching transistor (typ 3µs) and VIM1 = first threshold of current measurement (typ 0.6 v)

$$R_{SHUNT} = \frac{V_{IM1}}{I_{E(max)}}$$

Numerical application

$$I_{E(max)} = I_{P(max)} - (T_S \times \frac{V_{IN(min)}}{L_P}) + I_{B+}$$

$$I_{E(max)} = 3 - (3\ \ 10^{-6} \times \frac{210}{1.95\ \ 10^{-3}}) + 0.85 = 3.52A$$

$$R_{SHUNT} = \frac{V_{IM1}}{I_{E(max)}} = \frac{0.6}{3.52} = 0.169\Omega$$

III.2.2.2 Snubber network

A R.D.C network is used to limit the overvoltage on the transistor during the switching off time.

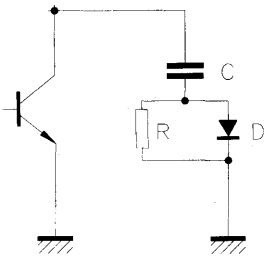
When the transistor is switched off, the capacitor is charged directly through the diode.

When the transistor is switched on, the capacitor is discharged through a resistor.

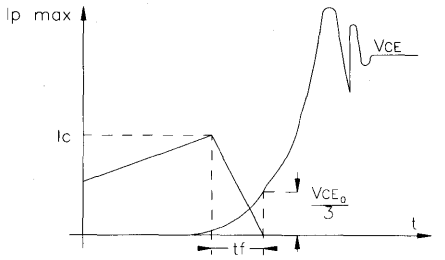
- $C = \frac{I_{P(max)} \times t_f}{2 \times \frac{VCE_O}{3}}$
- $3 \times R \times C = T_{on(min)}$ (to discharge the the capacitor C by the correct amount)
- Maximum power dissipated in R :

$$P = \frac{1}{2} \times C \times (V_{IN(max)} + V_R)^2 \times F$$

Figure 31.



V90TEA2260/61-31A



V90TEA2260/61-31B

Numerical application (with SGSF 344 transistor) with :

$I_{P(Max.)} = 3A$ - $V_{IN(Max.)} = 370$ VDC
$t_f = 0.3\mu s$ - $V_R = 172V$
$V_{CEO} = 600V$ - $F = 16kHz$
$T_{ON(Min.)} = 4\mu s$

$$C = \frac{I_{P(max)} \times t_f}{2 \times \frac{VCE_O}{3}} = \frac{3 \times 0.3\ 10^{-6}}{2 \times \frac{600}{3}} = 2.25nF$$

$$R = \frac{T_{ON(min)}}{3 \times C} = \frac{4\ 10^{-6}}{3 \times 2.25\ 10^{-9}} = 560\Omega$$

$$P = \frac{1}{2} \times C \times V_{IN(max)} + V_R)^2 \times F$$

$$P = \frac{1}{2} \times 2.25 \cdot 10^9 \times (370 + 172)^2 \times 16 \cdot 10^3 = 5.29W$$

In the final application a value of 2.7nF is chosen to decrease the overvoltage on the transistor in short circuit condition.

III.2.2.2.1 Overvoltage due to the leakage inductance

(See. III.2.1)

The capacitor C of the snubber network influences the overvoltage due to the leakage inductance.

$$V_{peak} = \frac{I_{C(max)}}{2} \sqrt{\frac{L_f}{C}}$$

Numerical application

with : $L_f = 0.08 \times L_p = 0.08 \times 1.9\ 10^{-3} = 152\mu H$

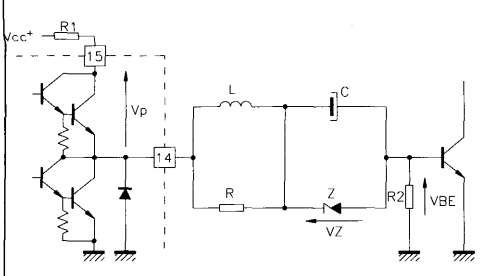
$$V_{peak} \frac{3}{2} \times \sqrt{\frac{152\ 10^6}{2.25\ 10^9}} = 390V$$

so $V_{CE(Max.)} = V_{IN(Max.)} + V_R + V_{peak} =$
$V_{CE(Max.)} = 370 + 172 + 390 \cong 930V$

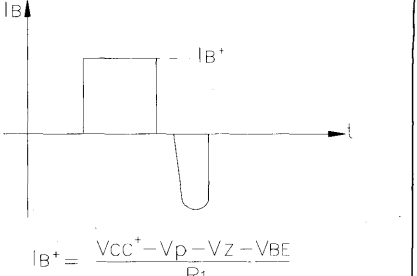
III.2.2.3. Base drive

The output stage of the TEA2260/61 works in saturation mode and hence the internal power dissipation is very low.

Figure 32.



V90TEE2260/61-32A



V90TEE2260/61-32B

$$R_1 = \frac{V_{CC+} - V_P - V_Z - V_{BE}}{I_{B+}}$$

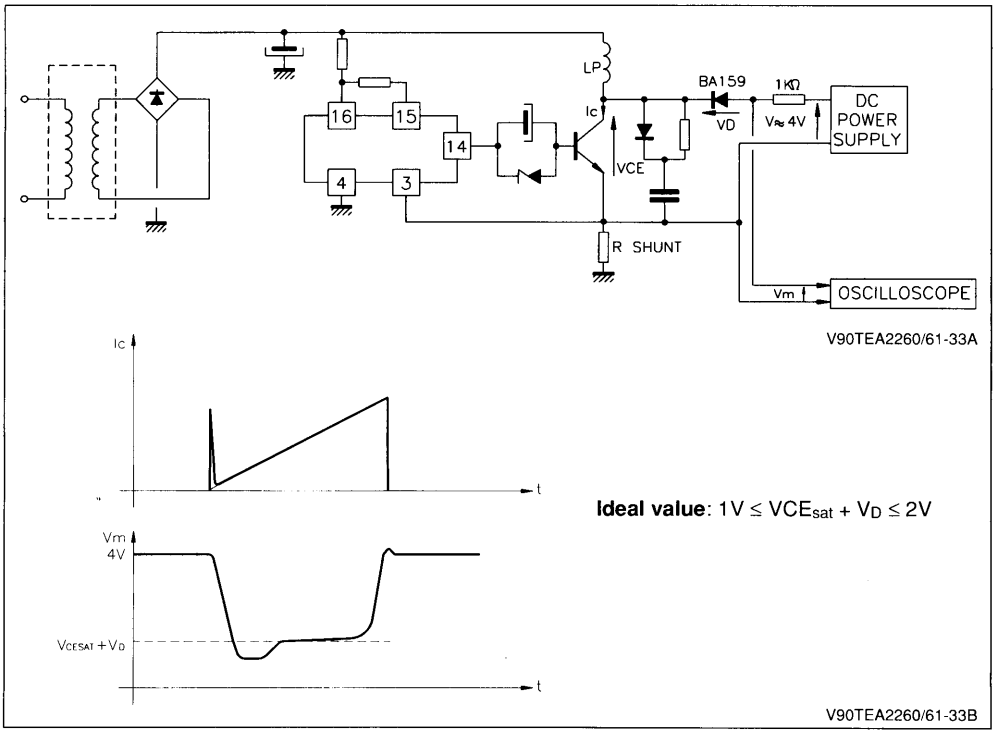
Numerical application

$$R_1 = \frac{13 - 0.9 - 3 - 0.6}{0.85} \cong 10\Omega$$

in this case the current gain,

$B_F = \frac{I_C}{I_B} = \frac{3}{0.85} = 3.5$ but it is recommanded to verify the V_{CE} sat dynamic behaviour on the transistor as follows:

Figure 33.



Remark :The mains of the TEA2260/61 must be provided through an isolation transformer for this measurement

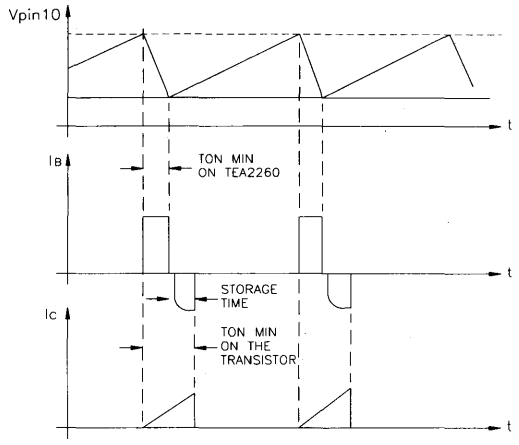
III.2.3. Oscillator frequency

The free running frequency is given on II.2.

The typical value of minimum conduction time $T_{ON(Min.)}$ on the output of the TEA2260/61 is given by: $T_{ON(Min.)} = 1040 \times C_O$

Note : the minimum conduction time $T_{ON(Min.)}$ on the transistor is longer due to the storage time.

Figure 34.



V90TEA2260/61-34

Numerical application

F_O = 16kHz

C_O is chosen at 1nF

so T_{ON} min on the TEA2260/61 = 1µs

$$R_O = \frac{1}{F_O \times C_O \times 0.66} - 1.57 \cdot 10^3$$

$$R_O = \frac{1}{16\ 10^3 \times 1\ 10^{-9} \times 0.66} - 1.57 \cdot 10^3$$

R_O = 93kΩ

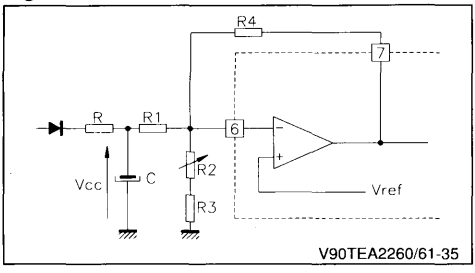
R_O = 100kΩ is chosen.

Note : F_O is chosen relatively low to avoid magnetization of the transformer during the start-up phase.

III.2.4. Regulation loop

In stand by mode the error amplifier of the TEA2260/61 carries out the regulation.

Figure 35.



V90TEA2260/61-35

- The R.C. filter is necessary to avoid the peak voltage due to the leakage inductance. The time constant τ = RC is about 30µs < R.C. < 150µs as a function of the transformer technology.
- To achieve a stable behaviour of the regulation loop and to decrease the ripple on the output voltage in stand by mode the time constant should be approximately :

$$(R_1 + R_2 + R_3) \times C \cong \frac{R_{OUT} \times C_{OUT}}{15}$$

with : C_{OUT} (filtering output capacitor) and R_{OUT} (load resistor on the output in stand by mode)

- To ensure a stable behaviour in stand-by mode the amplifier gain is choosen to :

$$G = \frac{R_4}{R_2 + R_3} \cong 15$$

Calculation of R, R_1, R_2, R_3, R_4

a) The resistor R is given by

$$R = \frac{\tau}{C}$$

C choosen between 1µF < C < 10µF

τ = 80µs is chosen

C = 2.2µF is chosen

Numerical application

$$So\ R = \frac{\tau}{C} = \frac{80\ 10^{-6}}{2.2\ 10^{-6}} = 36\Omega$$

b) The resistors R_1, R_2, R_3 are given by

$$R_1 + R_2 + R_3 \cong \frac{C_{OUT} \times R_{OUT}}{15 \times C}$$

with :
V_{REF} : reference voltage of the error amplifier
$V_{REF} = 2.5V$
V_{CC}(stand-by) : Vcc voltage in stand by mode.
V_{CC}(stand-by) = 0.9 x V_{CC} (in normal mode)

Numerical application

with :
$V_{CC} = 13V$
$V_{REF} = 2.5V$
$R_{OUT} = 2k\Omega$ on output 135V
$C_{OUT} = 100\mu F$ on output 135V
$C = 2.2\mu F$

$$R_1 + R_2 + R_3 \cong \frac{C_{OUT} \times R_{OUT}}{15 \times C}$$

$$= \frac{100\ 10^{-6} \times 2\ 10^{3}}{15 \times 2.2\ 10^{-6}} = 6k\Omega$$

$$R_2 + R_3 = (R_1 + R_2 + R_3) \times \frac{V_{REF}}{V_{CC}(\text{stand by})}$$

$$R_2 + R_3 = 6 \cdot 10^{3} \times \frac{2.5}{0.9 \times 13} = 1.28k\Omega$$

values choosen :
R_2 potentiometer resistor of 1kΩ
R_3 fixed resistor 1kΩ
$R_1 = (R_1 + R_2 + R_3) - (R_2 + R_3)$
$R_1 = 6k - 1.28k = 4.7k\Omega$

c) The resistor R_4 is given by $R_4 \cong 15 \times (R_2 + R_3)$

Numerical application

$R_4 \cong 15 \times (R_2 + R_3) \cong 15 \times (1.28\ 10^{3}) \cong 18k\Omega$

III.2.5. Overload capacitor

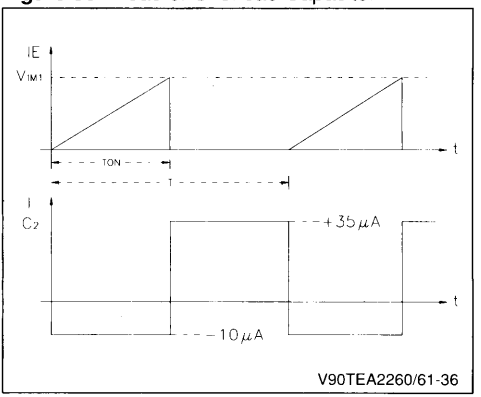
When an overload is detected with the first threshold VIM1 the capacitor C_2 (pin 8) is charged until the end of the period as shown in figure 36.
So the average load current is given by :

$$I_{C2} = \frac{T - T_{ON}}{T} \times I_{CH} - I_{DISCH}$$

the threshold to cut off the TEA2260/61 power supply is 2.5V typically and hence the delay time before overload detection is given by :

$$T_{overload} = \frac{2.5 \times C_2}{(\frac{T - T_{ON}}{T} \times I_{CH}) - I_{DISCH}}$$

Figure 36 : Load of Overload Capacitor.



Numerical application

with : maximum overload time = 40ms
the longer delay time is obtained when
$T_{ON} = T_{ON(Max.)}$

$$C_2 = ((\frac{T - T_{ON(Max.)}}{T} \times I_{CH}) - I_{DISCH}) \times \frac{T_{overload}}{2.5}$$

$$C_2 = (0.55 \times 45 \times 10^{-6} - 10 \times 10^{-6} \frac{40 \cdot 10^{-3}}{2.5} \cong 220nF$$

Note : in practice, the overload capacitor value must be greater than the soft start capacitor ($C_2 \geq C_1$) to ensure a correct start up phase of the power supply.

III.2.6 Soft start capacitor

Refer to paragraph II.5 for the soft start function explanation.
The soft start duration is given by :

$$T_{SOFTSTART} = \frac{(2.7 - 1.5) \times C_1}{9 \cdot 10^{-6}}$$

$$C_1 = 7.5 \cdot 10^{-6} \times T_{SOFT\ START}$$

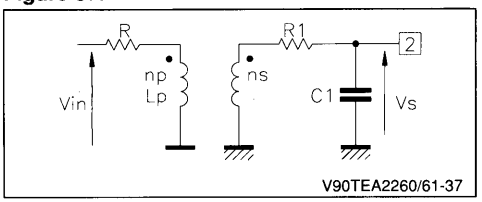
Numerical application

with : Tsoft start = 30ms
$C_1 = 7.5\ 10^{-6} \times 30\ 10^{-3} = 220nF$

III.2.7. Feed back voltage transformer

A feedback voltage transformer is used to send information from the secondary circuit (master circuit) to the primary circuit (slave circuit).
This transformer is needed to provide an electric insulation between primary and secondary side.

Figure 37.



The feedback input of TEA2260/61 is fed with logic level (threshold 0.9V)
It is necessary to have the same waveform on the primary side as on the secondary side.
For this reason the time constant must be higher than the maximum conduction time in normal mode.
Hence the primary inductance Lp must be calculated as follows :

$L_P > 3.R.T_{ON(Max.)}$

Numerical application

with :

$T_{ON(Max.)} = 28\mu s$

$R = 270\Omega$

$L_P > 3 \times 270 \times 28\ 10^{-6} = 22mH$

a) When the TEA5170 is used VIN = 7V

$$\frac{ns}{np} = \frac{V_{S(min)}}{V_{IN} \times (1 - \frac{T_{ON(max)}}{T})}$$

$$\frac{ns}{np} = \frac{1.5}{7 \times (1 - 0.45)} = 0.389$$

b) When the TEA 2028 is used VIN = 12V

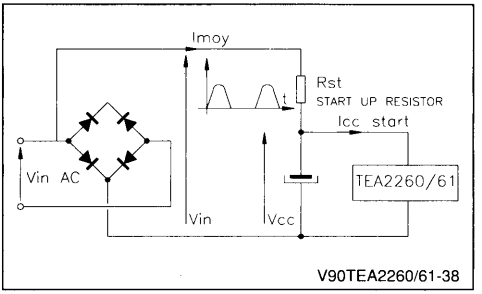
$$\frac{ns}{np} = \frac{1.5}{12 \times (1 - 0.45)} = 0.227$$

Note : The $R_1.C_1$ filter is used to damp oscillation on the secondary side of the feedback transformer. The time constant $R_1 \times C_1 \cong 0.1\mu s$.

III.2.8. Start up resistor

After switching on the power supply the filtering capacitor on V_{CC} of TEA2260/61 is charged through a resistor connected to the mains input voltage. Do not connect this resistor to the high voltage filtering capacitor because there is enough energy in this capacitor to cause three attempted restarts and to cut off the TEA2260/61 on fault detection when the power supply is switched off. Hence it is recommended to connect the start-up resistor as follows:

Figure 38.



Start-up delay time

$$I_{MOY} = \frac{\sqrt{2} \times V_{IN\ AC(min)}}{\pi \times R_{ST}}$$

$$\text{Start-up delay time} = Tst = \frac{V_{CC\ START}}{I_{MOY} - I_{CC\ START}} \times C$$

$$R_{ST} = \frac{\sqrt{2} \times V_{IN\ AC(min)}}{\pi \times \left((C \times \frac{V_{CC\ START}}{Tst}) + I_{CC\ START} \right)}$$

Power dissipated in start-up resistor

$$P = \frac{V_{IN\ AC(max)}2}{2\ .\ R_{ST}}$$

Numerical application

with :

start-up delay time = 1s

$V_{IN(max)} = 370V$ DC ($V_{IN\ AC(max)} = 265V$)

$V_{IN\ AC(min)} = 175V$

$V_{CCstart} = 10.3V$

$I_{CCstart} = 0.7mA$

$C = 220\mu F$

$$R_{ST} = \frac{2 \times 175}{\pi \times (220\ 10^{-6} \times 10.3 + 0.7\ 10^{-3})} = 26k\Omega$$

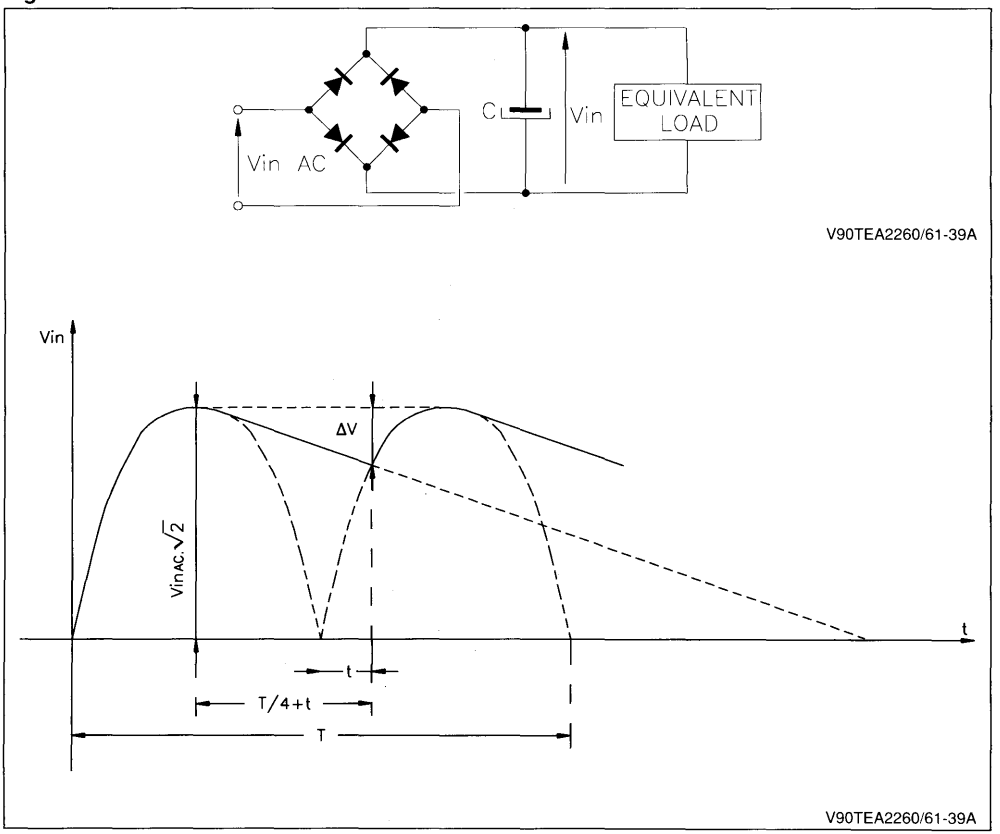
Value choosen = 22kΩ

Power dissipated

$$P = \frac{(265)^2}{2 \times 22\ 10^3} = 1.6W$$

III.2.9. Determination of high voltage filtering capacitor

Figure 39.



Hypothesis :

ΔV : ripple on the filtering voltage
$V_{IN.AC(min)}$: minimal value of A.C. input voltage
T : period of the mains voltage
P_{OUT} : output power of the power supply
η : efficiency of the power supply

$$C = \frac{T}{2\pi} \times \frac{\frac{\pi}{2} + \text{ArcSin}\left(1 - \frac{\Delta V}{V_{IN\,AC(min)} \times \sqrt{2}}\right)}{\Delta V \times V_{IN\,AC(min)} \times \sqrt{2}} \times \frac{P_{OUT}}{\eta}$$

Numerical application

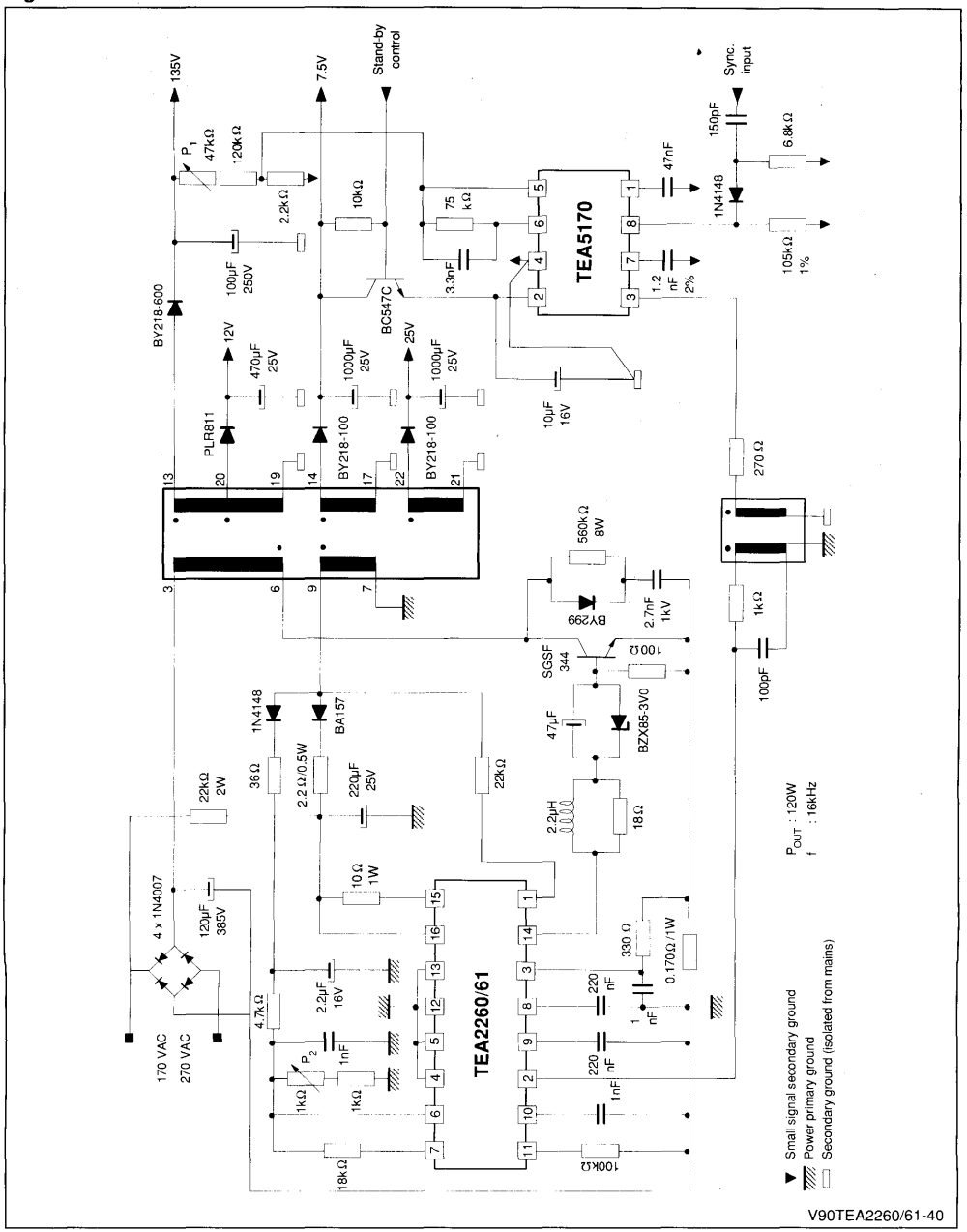
ΔV = 40V
$V_{IN\,AC(min)}$ = 170 VAC
T = 20ms
P_{OUT} = 120W
η = 0.85

$$C = \frac{20\,10^{-3}}{2\pi} \times \frac{\frac{\pi}{2} + \text{ArcSin}\left(1 - \frac{40}{250}\right)}{40 \times 250} \times \frac{120}{0.85} = 115\mu F$$

value choosen : C = 120µF

III.3. ELECTRICAL DIAGRAM

Figure 40.



IV. TV APPLICATION 140W - 220 VAC - 32kHZ SYNCHRONIZABLE

All details concerning the determination of external components are described in section III.

IV.1. APPLICATION CHARACTERISTICS.

- Discontinuous mode flyback SMPS
- Stand-by function using the burst mode of TEA2260.
- Switching frequency in burst mode : 16kHz
- Switching frequency in normal mode : 32kHz
- Nominal mains voltage : 220 VAC
- Mains voltage range : 170 VAC to 270 VAC
- Output power range in normal mode $25W < P_O < 140W$
- Output power range in stand-by mode $2W < P_O < 45W$
- Efficiency at full load > 80%
- Efficiency in stand-by mode (Po = 7W) > 50%
- Short circuit protection
- Long duration overload protection
- Complete shut down after 3 restarts with fault detection for TEA2260
- Complete shut down when V_{C2} reaches 2.6V for TEA2261

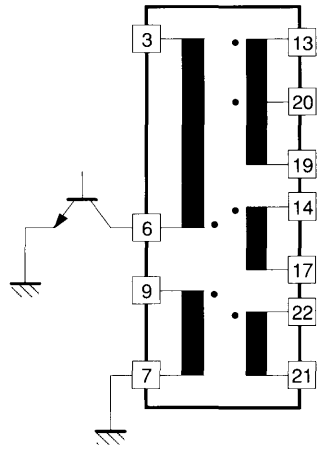
Load regulation **(VDC = 310V)**
Output 135V (± 0.18%) → (I_{135} : 0.01A to 0.8A; I_{25} = 1A)
Output 25V (± 2%) → (I_{135} : 0.8A; I_{25} = 0.5A to 1A)

Line regulation **(I_{135} : 0.8A; I_{25} : 1A)**
Output 135V (± 0.13%)→ (210V < VDC < 370V)
Output 25V (± 0.17%)

IV.2. TRANSFORMER CHARACTERISTICS

- Reference : OREGA.SMT5. G4576-03
- Electrical Data :

Figure 41.

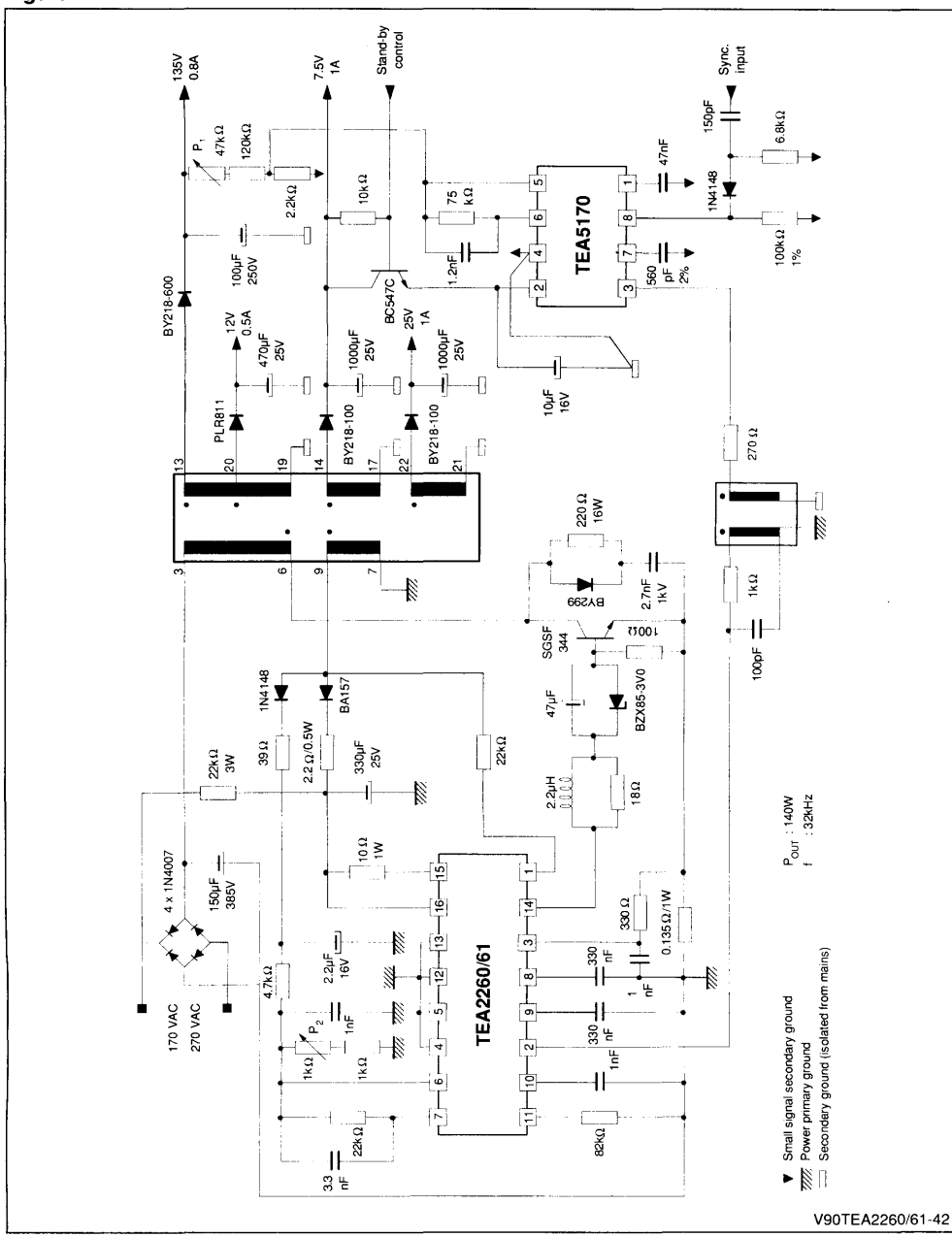


V90TEA2260/61-41

Winding	Pin	Inductance
n_p	3-6	790µH
n_{aux}	7-9	5.4µH
n2	19-13	338µH
n3	19-20	4.8µH
n4	14-17	3.4µH
n5	22-21	13µH

IV.3. ELECTRICAL DIAGRAM

Figure 42.



V. TV APPLICATION 110W -220 VAC - 40kHz REGULATED WITH OPTOCOUPLER

This application works in asynchronous mode. The regulation characteristics are very attractive (output power variation range from 1W to 110W due to automatic burst mode (see II.6). In this configuration higher is the regulation loop gain, lower is the output voltage ripple in burst mode (e.g. ouput voltage ripple 0.8% with a loop gain of 15).

V.1. FREQUENCY SOFT START

The nominal switching frequency is 40kHz but during the start-up phase the switching frequency is shifted to 10kHz in order to avoid the magnetization of the transformer.
Otherwise the second current limitation will be reached at high input voltage and hence the power supply will not start.

V.2. APPLICATION CHARACTERISTICS

- Discontinous mode Flyback SMPS
- Switching frequency : 40kHz
- Nominal mains voltage : 220 VAC
- Mains voltage range : 170 VAC to 220 VAC
- Output power in normal mode : 30W < P_O < 110 W
- Output power in burst mode : 1W < P_O < 30W. The transient phase between normal mode and burst mode is determinated automatically as a function of the output power. Hence the regulation of the output voltage is effective for an output power variation of 1W < P_O < 110W
- Efficiency as full load > 80%
- Efficiency in burst mode (P_O = 8W) > 50%
- Short circuit protection
- Open load protection
- Long duration overload protection
- Complete shutdown after 3 restarts with fault detection for TEA2260
- Complete shut down when V_{C2} reaches 2.6V for TEA2261

Load regulation *(VDC = 310V)*
Output 135V (± 0.15%) → (I_{135} : 0.05A to 0.6A; I_{25} = 1A)
Output 25V (± 2.5%) →(I_{135} = 0.6A; I_{25} : 0.25 to 1A)

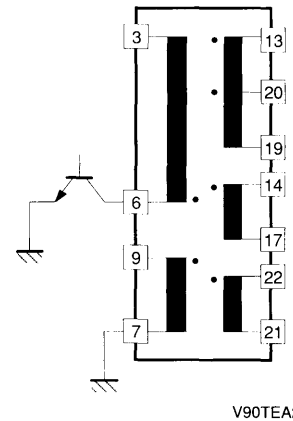
Line regulation *(I_{135} : 0.6A; I_{25} : 1A)*
Output 135V (± 0.30%) → (210V < VDC <, 370V)
Output 25V (± 0.30%)

Influence of the audio output on the video output
Output 135V (± 0.1%) →(I_{135} = 0.6A; I_{25} : 0 →1A)
Output 135V (± 0.05%) →(I_{135} = 0.3A; I_{25} : 0 →1A)

V.3. TRANSFORMER SPECIFICATION

- Reference : OREGA.SMT5. G4576-02
- Mechanical Data :
  - Ferrite : B50
  - 2 cores : 53 x 18 x 18 (mm) THOMSON LCC
- Electrical Data :

Figure 43.

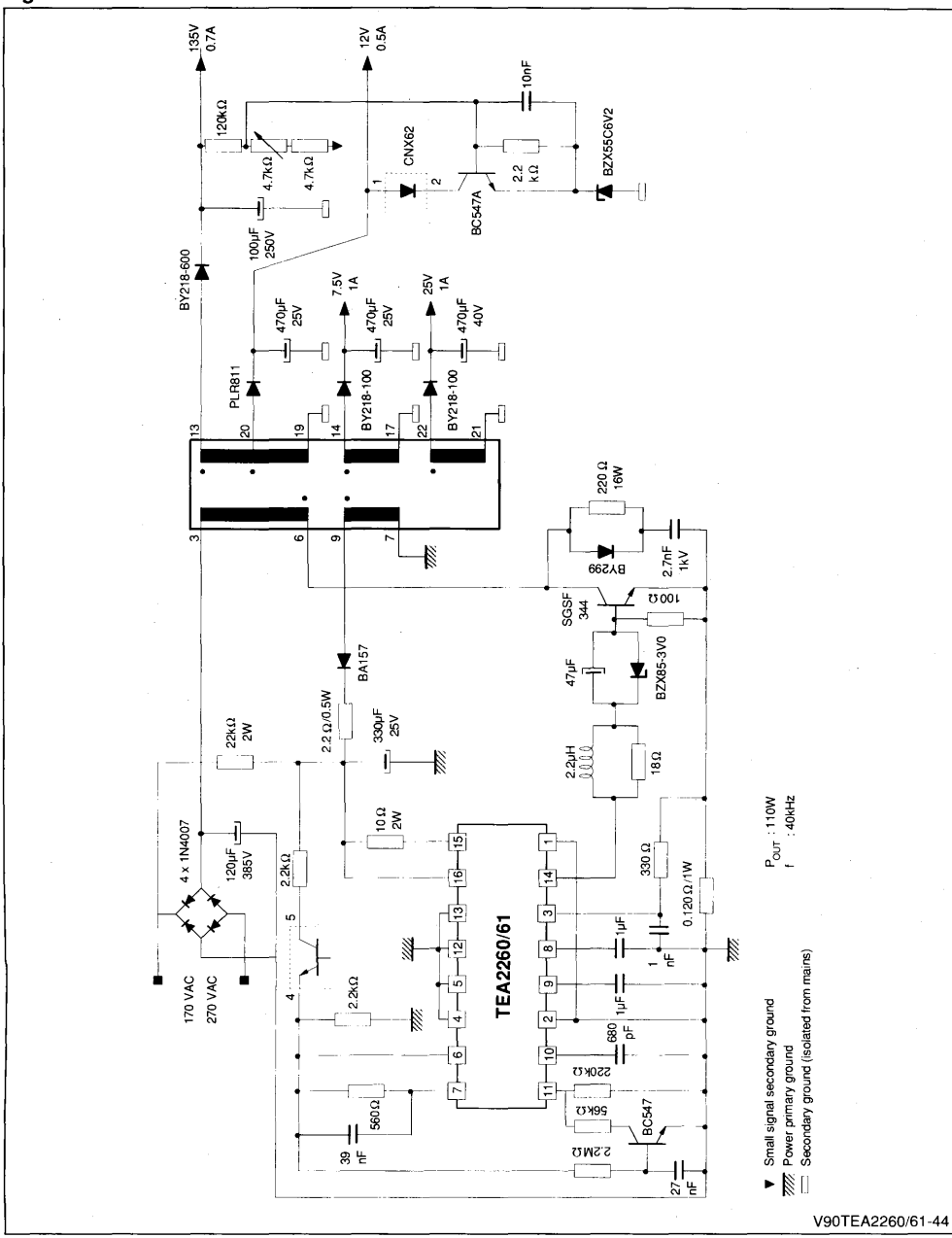


V90TEA2260/61-43

Winding	Pin	Inductance
n_p	3-6	790µH
n_{aux}	7-9	5.4µH
n2	19-13	338µH
n3	19-20	4.8µH
n4	14-17	3.4µH
n5	22-21	13µH

V.4. ELECTRICAL DIAGRAM

Figure 44.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA5101A - RGB HIGH VOLTAGE VIDEO AMPLIFLIER BASIC OPERATION AND APPLICATIONS

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SUMMARY

The aim of this Application Note is to describe the basic operation of the TEA5101A video amplifier and to provide the user with basic hints for the best utilization of the device and the realisation of high performance applications. Application examples are also provided to assist the designer in the maximum exploitation of the circuit.

GENERAL

The control of state-of-the-art color cathode ray tubes requires high performance video amplifiers which must satisfy both tube and video processor characteristics.

When considering tube characteristics (see fig 13-14 on page 14),we note that a 130V cutoff voltage is necessary to ensure a 5mA peak current.However 150V is a more appropriate value if the saturation effect of the amplifier is to be taken into account. As the dispersion range of the three guns is ± 12%, the cutoff voltage should be adjustable from 130V to 170V. The G2 voltage, from 700 to 1500V allows overall adjustment of the cutoff voltage for similar tube types.

A 200V supply voltage of the video amplifier is necessary to achieve a correct blanking operation. In addition, the video amplifier should have an output saturation voltage drop lower than 15V, as a drive voltage of 130V (resp. 115V) is necessary to obtain a beam current of 4 mA for a gun which has a cutoff point of 170V (resp. 130V).

Note : For all the calculations discussed above, the G1 voltage is assumed to be 0V.

The video processor characteristics must also be considered. As it generally delivers an output voltage of 2 to 3V, the video amplifier must provide a closed loop DC gain of approximately 40.

The video amplifier dynamic performances must also meet the requirements of good definition even with RGB input signals (teletext,home computer...), e.g. 1mm resolution on a 54cm CRT width scanned in 52µs. Consequently, a slew rate better than 2000V/µs, i.e. rise and fall times lower than 50ns, is needed. In addition, transition times must be the same for the three channels so as to avoid coloured transitions when displaying white characters. The bandwidth of a video amplifier satisfying all these requirements must be at least 7MHz for high level signals and 10MHz for small signals.

One major feature of a video amplifier is its capability to monitor the beam current of the tube. This function is necessary with modern video processors:

- for automatic adjustment of cutoff and also, where required,video gain in order to improve the long term performances by compensation for aging effects through the life of the CRT. This adjustment can be done either sequentially (gun after gun) or in a parallel mode.
- for limiting the average beam current

A video amplifier must also be flashover protected and provide high crosstalk performances. Crosstalk effects are mainly caused by parasitic capacitors and thus increase with the signal frequency. A crosstalk level of -20dB at 5MHz is generally acceptable.

Table 1 summarizes the main features of a high performance video amplifier.

The SGS-THOMSON Microelectronics TEA5101A is a high performance and large bandwidth 3 channel video amplifier which fulfills all the criteria discussed above. Designed in a 250V DMOS bipolar technology, it operates with a 200V power supply and can deliver 100V peak-to-peak output signals with rise and fall times equal to 50ns.

The 5101A features a large signal bandwidth of 8MHz, which can be extended to 10MHz for small signals (50 Vpp).

Each channel incorporates a PMOS transistor to monitor the beam current. The circuit provides internal protection against electrostatic discharges and high voltage CRT discharges.

The best utilization of the TEA 5101A high performance features such as dynamic characteristics, crosstalk,or flashover protection requires optimized application implementation. This aspect will be discussed in the fourth part of this document.

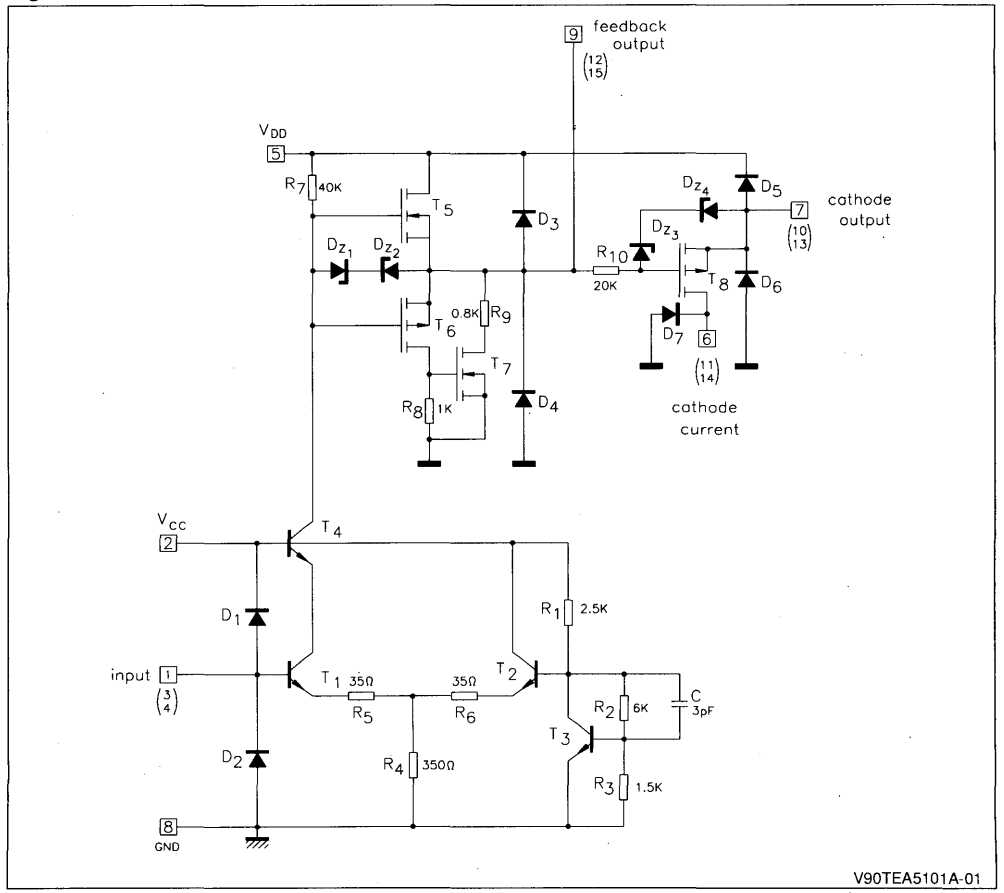
Table 1: Main features of a high performance video amplifier.

• Maximum Supply Voltage	220V
• Output voltage swing "Average"	100V
• Output voltage swing "Peak"	130V
• Low level saturation (refered to VG1)	15V
• Closed loop gain	40
• Transition time	50ns
• Large signal bandwidth	7MHz
• Small signal bandwidth	10MHz
• Beam current monitoring	
• Flash over protection	
• Crosstalk at 5 MHz	-20dB

I - DESCRIPTION

The complete schematic diagram of one channel of the TEA5101A is shown in fig 1.

Figure 1.



I.1 INPUT STAGE

The differential input stage consists of the transistor T_1 and T_2 and the resistors R_4,R_5 and R_6.

This stage is biased by a voltage source T_3,R_1,R_2 and R_3.

$$V_B(T_1) = (1 + \frac{R_2}{R_3}) \times V_B(T_3) \cong 3.8V$$

Each amplifier is biased by a separate voltage source in order to reduce internal crosstalk. The load of the input stage is composed of the transistor T_4 (cascode configuration) and the resistor R_7. The cascode configuration has been chosen so as to reduce the Miller input capacitance. The voltage gain of the input stage is fixed by R_7 and the emitter degeneration resistors R_5,R_6,and the T_1,T_2 internal emitter resistances. The voltage gain is approximately 50dB.

Using a bipolar transistor T_4 and a polysilicon resistor R_7 gives rise to a very low parasitic capacitance at the output of this stage (about 1.5pF). Hence the rise and fall times are about 50ns for a 100V peak-to-peak signal (between 50V and 150V).

I.2 OUTPUT STAGE

The output stage is a quasi-complementary class B push-pull stage. This design ensures a symetrical load of the first stage for both rising and falling signals. The positive output stage is made of the DMOS transistor T_5,and the negative output stage is made of the transistors PMOS T_6 and DMOS T_7. The compound configuration T_6-T_7 is equivalent to a single PMOS. A single PMOS transistor capable of sinking the total current would have been too large.

By virtue of the symetrical drive properties of the output stage the rise and fall times are equal (50ns for 100V DC output voltage).

I.3 BEAM CURRENT MONITORING

This function is performed by the PMOS transistor T_8 in source follower configuration. The voltage on the source (cathode output) follows the gate voltage (feedback output). The beam current is absorbed via T_8 . On the drain of T_8, this current will be monitored by the videoprocessor.

I.4 PROTECTION CIRCUITS

I.4.1. MOS protection

Four zener diodes $DZ_{(1-4)}$ are connected between gate and source of each MOS in order to prevent the voltage from reaching the breakdown voltage.Hence the V_{GS} voltage is internally limited to ± 15V.

I.4.2. Protection against electrostatic discharges

All the input/output pins of the TEA5101A are protected by the diodes D_1-D_7 which limit the overvoltage due to ESD.

I.4.3. Flashover protection

A high voltage and high current diode D_5 is connected between each output and the high voltage power supply. During a flash, most of the current is generally absorbed by the spark gap connected to the CRT socket. The remaining current is absorbed by the high voltage decoupling capacitor through the diode D_5. Hence the cathode voltage is clamped to the supply voltage and the output voltage does not exceed this value.

II - FUNCTIONAL DESCRIPTION

The schematic diagram of one TEA5101A channel with its associated external components is shown in fig.2

II.1 VOLTAGE AMPLIFIER

II.1.1. Bias conditions $V_{in} = V_{ref}$

The bias point is fixed by the feedback resistor R_f,the bias resistor R_p, and by the internal reference voltage when $V_{in} = V_{ref}$.

If V_O is the output voltage (pin 9) :

$$V_O = (1 + \frac{R_f}{R_p}) \times V_{ref} \qquad (1)$$

In this state T_1 and T_2 are conducting. A current flows in R_7 and T_4 soT_5 is on. The T_5 drain current is fed to the amplifier input through the feedback resistor. The current in R_7 is:

$$I(R_7) = \frac{V_{DD} - V_O - V_{GS(T_5)}}{R_7} \cong \frac{V_{DD} - V_O}{R_7}$$

and the current in T_5 and R_f is :

$$I(T_5) = \frac{V_O - V_{ref}}{R_f} \cong \frac{V_O}{R_f}$$

Thus the total current absorbed by each channel of the TEA5101A is :

$$\frac{V_{DD}}{R_7} + V_O \times (\frac{1}{R_f} - \frac{1}{R_7})$$

The cathode (pin 7) output voltage is:

$$V_O + V_{GS(T_8)} = V_O$$

The beam current is absorbed by T_8 and R_m. The voltage developed across R_m by this current is fed to the videoprocessor in order to monitor the beam current.

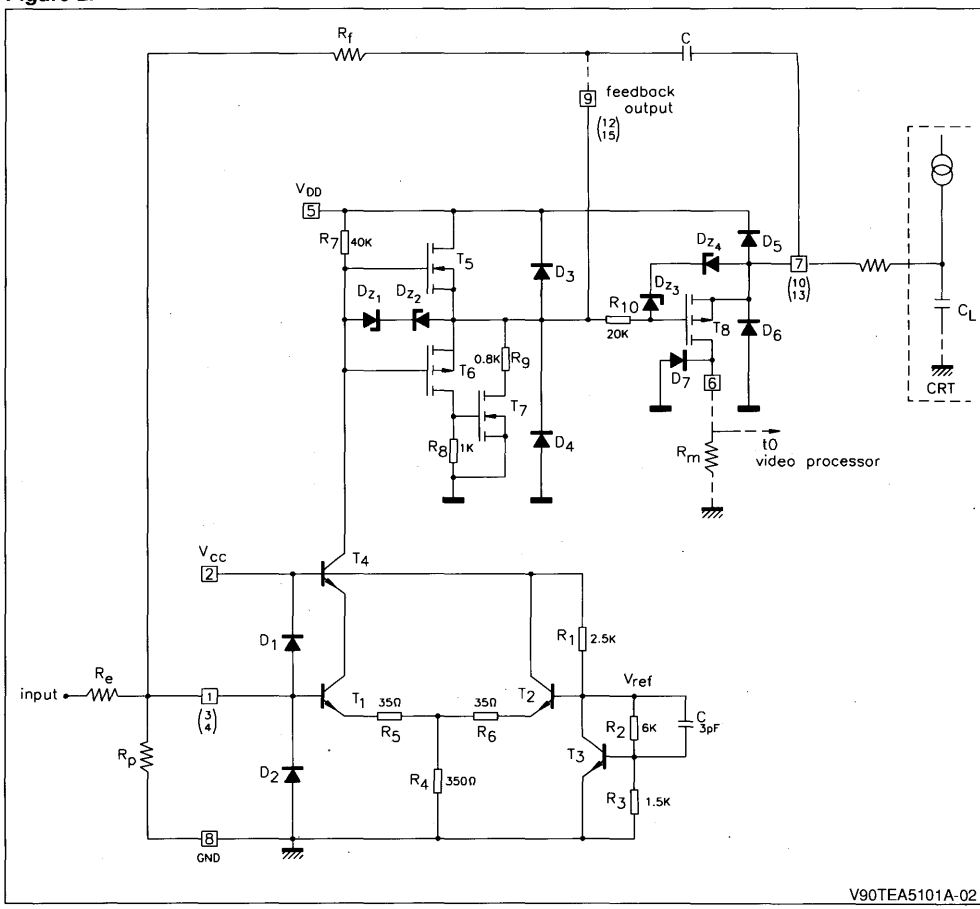
II.1.2. Dynamic operation

The TEA5101A operates as a closed loop amplifier, with its voltage gain fixed by the resistors R_f and R_e.

Since the open loop gain A is not infinite, the resistor R_p and the input impedance R_{in} must be considered.Hence the voltage gain is

$$G = -\frac{R_f}{R_e} \times \frac{1}{1 + \frac{1}{A}(1 + \frac{R_f}{R_p \,//\, R_e \,//\, R_{in}})} \qquad (2)$$

Figure 2.



II.1.2.1. Input voltage $V_{in} < V_{ref}$ (black picture)

In this case the current flowing in R_7 and T_1 decreases whilst the collector voltage of T_4 and the output voltage both increase. In the extreme case, $I(T_1) = I(R_7) = 0$ and $V_O = V_{DD}-V_{GS}(T_5)$

In order to charge the tube capacitor the voltage is fed to the cathode output in two ways:

- through the PMOS (with a VGS difference) for the low frequency part
- through the capacitor C for the high frequency part (output signal leading edge)

To correctly transmit the rising edge, the value of the capacitor C must be high compared to C_L.

With the current values used (C = 1nF,C_L = 10pF), the attenuation is very small (0.99)

II.1.2.2. Input voltage $V_{in} > V_{ref}$ (white picture)

In this case,the current in R_7 and T_1 increases with an accompanying drop of T_4's collector voltage until T_1 and T_4 are saturated. At this point:

$V_O \cong V_C(T_4) \cong V_{CC}$

During a high to low transition (i.e. black-white picture), the beam current is absorbed in two ways:

- through the capacitor C and the compound PMOS T_6-T_7 for the high frequency part (falling edge)
- through the PMOS T_8 and the resistor R_m for the low frequency part.

II.2 BEAM CURRENT MONITORING

II.2.1. Stationary state

The beam current monitoring is performed by the PMOS T_8 and the resistor R_m. When measuring low currents (leakage, quasi cutoff),the R_m value is generally high. When measuring high currents (drive, average or peak beam current),R_m is generally bypassed by a lower impedance.

It should be noted that the current supplied by the three guns flows through this resistor.Hence,with too large a value for the resistor R_m,the cathode voltage of the tubes will become too high for the required operating current values.This is a fundamental difference between the TEA5101A and discrete video amps. In discrete video amps, the current monitoring transistor is a high voltage PNP bipolar which may saturate. In this case the beam current can flow through the transistor base and it is no longer monitored by the video processor. This effect does not occur with the TEA 5101A.

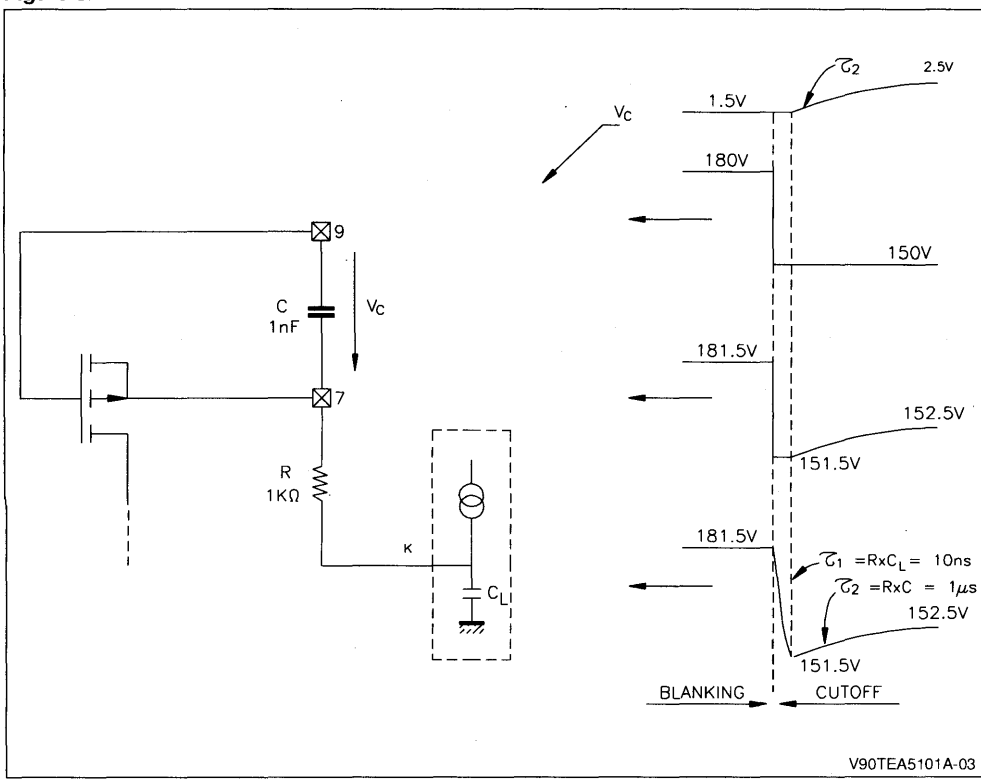
II.2.2. Transient phase : low current measurements

The cut-off adjustment sequence is generally as follows:

In a first step, the cathode is set to a high voltage (180V) in order to blank the CRT and to measure the leakage current. In a second step, the tube is slighly switched on to measure a very low current (quasi cut-off current). This operation is performed by setting the cathode voltage to about 150V and adjusting it until the proper current is obtained. The maximum time available to do this operation is generally about 52µs.

Fig.3 shows the simplified diagram of the TEA5101A output, the voltages during the different steps,and the stationary state the system must reach for correct adjustment.

Figure 3.



During the blanking phase, the tube is switched off, the PMOS is switched off and its V_{GS} voltage is equal to the pinch-off voltage (about 1.5V). The voltages at the different nodes are shown in figure 3 (V(9) = 180V, V(k) = 181.5V). The falling edge of the cutoff pulse is instantaneously transmitted by the capacitor C. When the stationary state is reached, the cathode voltage will be 152.5V if the voltage on pin 9 is 150V, as the VGS voltage of the conducting PMOS is about 2.5V.

We can see that the voltage on C must increase by an amount of $\Delta Vc = 1V$. This charge is furnished by the tube capacitor which is discharged by an amount of $\Delta VC_L = 29V$ with a time constant equal to R x C_L (10 ns). By considering the energy balance, we can calculate the maximum charge ΔV_{max} that C_L can furnished to C

$$\Delta V_{max} = \sqrt{\frac{C_L}{C}} \times \Delta V_{CL} \cong 3V$$

Since this voltage is greater than ΔV_C, the capacitor C can be charged and the stationary state is reached without any contribution being required from the tube current,i.e. the whole tube current can flow through the PMOS and the adjustment can be performed correctly.

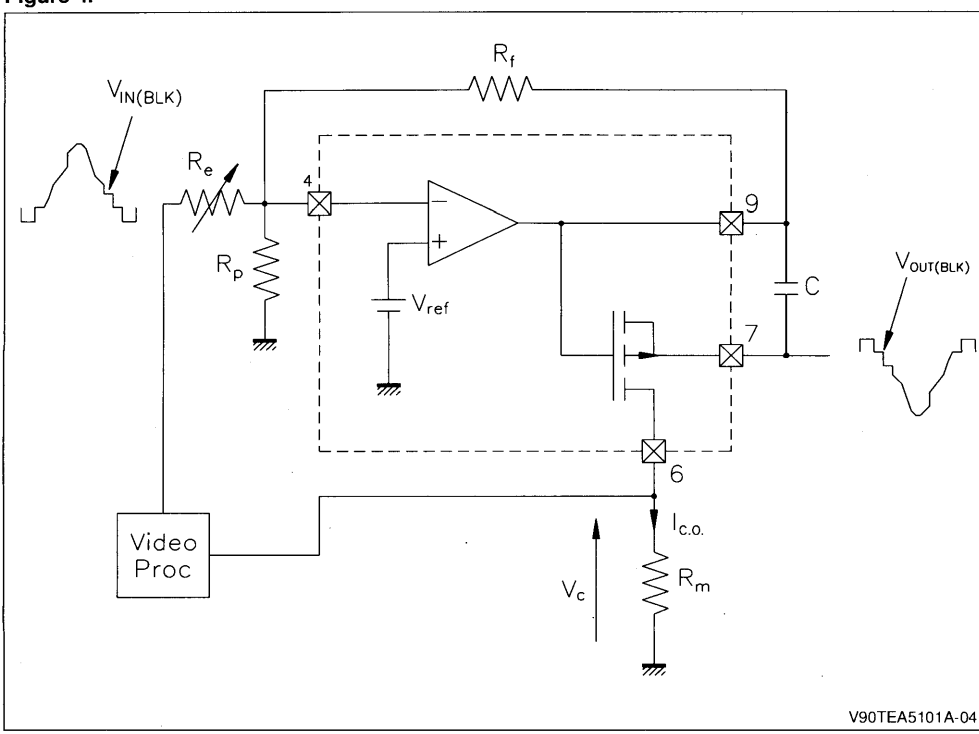
Considering higher voltage and beam current swings, the margin is greater because:

- the voltage swing across the tube capacitor is greater
- the tube current is higher and the picture is not disturbed even if part of the beam current is used to charge the capacitor C.

III - EXTERNAL COMPONENTS CALCULATION

The implementation of the TEA5101A in an application requires the determination of external component values. These components are R_f, R_e, R_p and R_m (see fig.4). The dissipated power in the IC and in the feedback resistor R_f must also be calculated in order to correctly choose the power ratings of the heatsink and resistors.

Figure 4.



III.1 COMPONENTS VALUE CALCULATION

From equations 1 and 2 in section II-1, both the value of the DC output voltage and the voltage gain depend directly on the resistor R_f. Hence R_f must be determined first before calculating the value of R_e and R_p in order to obtain the correct gain and DC output voltage.

III.1.1. Feedback resistor R_f

The value of R_f must be as low as possible in order to obtain the optimum dynamic performance from the TEA5101A (see section IV-1). A typical value of R_f is 39 kΩ.

III.1.2. Input resistor Re

The voltage gain is calculated from the following formula (see section II-1):

$$G = -\frac{R_f}{R_e}\,\frac{1}{1+\frac{1}{A}\left(1+\frac{R_f}{R_p \,//\, R_e \,//\, R_{in}}\right)}$$

Since the open loop gain A is high enough (50dB), we can approximate the calculation:

$$G @ -\frac{R_f}{R_e}$$

where R_e is generally implemented as a variable value for channel gain adjustment.

If the gain adjustment range G_{min}, G_{max} is known:

$$R_{e\,min} = \frac{R_f}{G_{max}} \text{ and } R_{e\,max} = \frac{R_f}{G_{min}}$$

With G_{min} = 15 and G_{max} = 80 :

$R_{e\,min}$ = 470Ω
$R_{e\,max}$ = 2.6kΩ

R_e will be made of a 2.2kΩ potentiometer and 470Ω fixed resistor.

III.1.3. Bias resistor R_p

R_p must be chosen in such a way that the black level output voltage $V_{OUT(BLK)}$ is equal to the cutoff voltage, which is a characteristic of the tube currently used, when the DC black level input voltage $V_{IN(BLK)}$ is the mean value of the adjustment range of the video processor. This is the optimum condition to ensure a correct adjustment during the lifetime of the tube. R_p can be calculated by considering the TEA5101A as an operational amplifier and applying the usual formula :

$$R_p = \frac{V_{ref}}{\frac{V_{out\,(BLK)} - V_{ref}}{R_f} + \frac{V_{in\,(BLK)} - V_{ref}}{R_e}}$$

- If $V_{in(BLK)} = V_{ref}$ $\quad R_p = \frac{V_{ref}}{V_{out\,(BLK)} - V_{ref}} \times R_f$

For a 150V black level :

R_p = 1kΩ with R_f = 39kΩ

- If $V_{in\,(BLK)} \neq V_{ref}$:

R_p = 1.2kΩ with $V_{in\,(BLK)}$ = 2.7V, R_f = 39kΩ, R_e = 1.5kΩ

Or

R_p = 680Ω with $V_{in\,(BLK)}$ = 6.7V, R_f= 39kΩ, R_e = 1.5kΩ

for a 150V black level

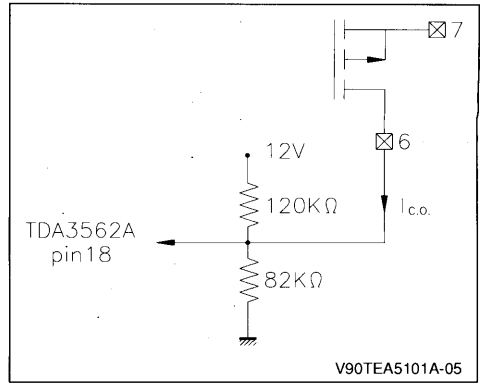
III.1.4. Current measurement resistor R_m

R_m must be determined by taking into account the quasi cutoff current I_{co} and the input voltage V_C of the video processor.

$$R_m = \frac{V_C}{I_{CO}}$$

- With the videoprocessor TEA5031D (V_C = 2V) : R_m = 120kΩ with I_{CO} = 16µA
- With the videoprocessor TDA3562A (V_C = 0.5V) which requires a DC biased input "Black current stabilization" (pin 18), the schematic diagram is the following :

Figure 5.



The DC bias is $12 \times \frac{82}{120 + 82} = 5V$

The quasi cutoff current is

$0.5 (\frac{1}{120} + \frac{1}{82}) \times 1 \times 10^{-3} = 10\mu A$

III.2 DISSIPATED POWER IN EXTERNAL COMPONENTS

The only components dissipating power are the TEA5101A and the feedback resistor. The dissipated power has a constant static component and a dynamic component which increases with frequency. The theoretical calculation is not sufficiently accurate to determine the correct dissipated power. The best way consists of measuring the power in different configurations of the circuit: steady state (no input), sinusoidal input,and in situ (in a TV set with a video input signal). The measurement method will be described first and then the results and calculations will be discussed.

III.2.1. Measurement method

The dissipated power can be determined by measuring the average supply current I_{DD} (principally high voltage supply current V_{DD}) and by subtracting the power dissipated in the external components from the calculated power delivered by this supply voltage.

The power delivered by the high voltage power supply is : $P = V_{DD} \times I_{DD}$

The power dissipated in the external components (principally the feedback resistor R_f) is:

- for the static part: $P_{SR} = \frac{3 \times V^2_{OUT\ (AVG)}}{R_f}$

- for the dynamic part: $P_{DR} = \frac{3 \times V^2_{OUT\ (RMS)}}{R_f}$

When the IC is driven by a sinusoidal signal (capacitive drive),the measurement and calculation are straightforward:
$V_{OUT}(AVG) = V_{OUT}(DC)$

$V_{OUT}(RMS) = \frac{V_{OUT\ (peak\ to\ peak)}}{2 \times \sqrt{2}}$

With V_{OUT} (DC) = 100V and
V_{OUT} (peak to peak) = 100V and $R_f = 39k\Omega$

$P_{SR} = 0.8W$
$P_{DR} = 0.1W$

Measurements are more difficult to carry out when the IC is working in a TV set. $V_{OUT}(AVG)$ can be measured with an oscilloscope (difference of level between AC and DC coupling) and V_{OUT} (RMS) can be measured by connecting an RMS voltmeter to the feedback resistor. In this case we have the following results (see section 2.2.3):

V_{OUT} (AVG) = 130V and P_{SR} = 1.3W

V_{OUT} (RMS) = 32V and P_{DR} = 80mW

In each case, the term P_{DR} can be neglected as a reasonable approximation.Hence, the power dissipated by the IC will be:

$P_i = V_{DD} \times I_{DD} - \frac{3V^2_{OUT\ (AVG)}}{R_f}$

and the power dissipated in R_f will be :

$P_r = \frac{V^2_{OUT\ (AVG)}}{R_f}$

III.2.2. Results

III.2.2.1. Static power

Table 2 shows the measured values of I_{DD} and the calculated power for three values of Vout and for V_{DD} = 200V

Table 2.

V_{OUT} (V)	I_{DD} (mA)	P_i (W)	P_r (W)
50	16	3	0.065
100	15	2.2	0.25
150	14.6	1.2	0.6

We can see that the static power dissipated in the IC decreases with V_{OUT} increasing, but obviously the power dissipated by R_f increases as V_{OUT} increases.

III.2.2.2. Measurement with sinusoidal input

Table 3 summarizes the results obtained from practical measurements as functions of V_{OUT}(DC) and of the frequency (the three channels are driven simultaneously).

Table 3.

V_{OUT} (V)	I_{DD} 1MHz (mA)	I_{DD} 7MHz (mA)	V_{OUT} (PP) 1MHz (V)	V_{OUT} (PP) 7MHz (V)	P_i 1MHz (W)	P_i 7MHz (W)	P_r (W)
50	20.7	44.6	66	50	3.9	8.7	0.065
100	20	59.5	100	80	3	11	0.25
150	18	45	100	67	1.7	8.2	0.6

We can see that when driving the IC with a HF sinusoidal signal, care must be taken to avoid excessive temperature increase.

III.2.2.3. Measurement in a TV set

We have determined the worst cases of dissipation in a TV set. These trials have been carried out on one particular TV set, and may not be representative for all TV sets. In this particular TV set, the worst cases of dissipation occur with noise signal (from HF tuner) and with a multiburst pattern (0.8 to 4.8MHz) in RGB mode.

Table 4 summarizes the results in these two cases when the brightness control is set to min and max value (the contrast control is set to max).

Table 4.

	V_{OUT} (AVG) (V)	I_{DD} (mA)	V_{DD} (V)	P_i (W)	P_r (W)
Bright.max Noise	148	22.2	218	3.15	O.56
Bright.min	188	23.3	224	2.5	0.9
Bright.max Multiburst	131	23.6	213	3.7	0.44
Bright.min	158	22	221	2.9	0.64

III.2.3. Design of heatsink and external components

III.2.3.1. Heatsink

As discussed above, the power dissipated in the IC in a TV set can reach about 4W. In this case, a 12°C/W heatsink seems to be sufficient. Such a heatsink will give $T_j = 115°C$ for $T_{room} = 60°C$.

The resulting margin guarantees correct reliability.

III.2.3.2. Feedback resistors

1 Watt type feedback resistors must be used, as they may need to dissipate 0.9W when the TV set is working and up to 1W when the TV is blanked (V_{OUT} = 200V), for example when the security of the scanning processor is activated.

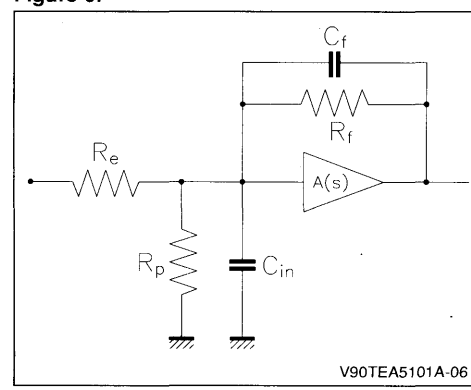
IV - APPLICATION HINTS

IV.1 DYNAMIC PERFORMANCES

Figure 6 shows the simplified schematic diagram of the TEA5101A in AC mode.

C_f is the parasitic capacitor between the input and the output.

Figure 6.



C_{in} is the parasitic capacitor between the input and ground. The voltage gain versus frequency can be deduced from the formula (2) in chapter II section 1.2 :

$$G(s) = -\frac{R_f}{R_e\,(1 + R_f\,C_f\,s)} \times \frac{1}{1 + \frac{1}{A(s)}\left(1 + \frac{R_f}{R_{eq}}\,\frac{1 + R_{eq}\,C_{in}\,s}{1 + R_f\,C_f\,s}\right)}$$

with $R_{eq} = R_p // R_e // R_{in}$ and A(s) open loop gain.

A(s) is a second order function such as $\frac{AO}{1 + bs + as^2}$

with $a = 9 \times 10^{-16}\ s^2$
$b = 60 \times 10^{-9}\ s$
$AO = 400$

Assuming $R_{eq} \times C_{in} = R_f \times C_f$, we find:

$$G(s) = -\frac{R_f}{R_e (1 + R_f C_f s)} \times \frac{1}{1 + \frac{B}{AO}} \times \frac{1}{1 + \frac{B}{AO + B} bs + \frac{B}{AO + B} as^2}$$

with $B = 1 + \frac{R_f}{R_{eq}}$

We see that the closed loop amplifier is equivalent to a combination of a second order circuit and a first order one. The latter comprises the feedback resistor and the parasitic capacitor between input and output. With the current values

$R_f = 39k\Omega$ $C_f = 0.5pF$
$R_e = 2k\Omega$ $C_{in} = 15pF$
$R_{in} = 14k\Omega$
$R_p = 1.2k\Omega$

we have

$R_{eq} \times C_{in} = 10ns$

$R_f \times C_f = 20ns$

$B = 56$

The second order circuit characteristics are :

Natural frequency:

$$F_n = \frac{1}{2 \times \pi \times a} \times \frac{AO + B}{B} = 15MHz$$

damping factor :

$$z = \frac{b}{2 \times a} \times \frac{B}{AO + B} = 0.35$$

The cut off frequency of the first order circuit is :

$$f_C = \frac{1}{2 \times \pi\ R_f \times C_f} = 8MHz$$

The amplifier response is thus the combination of the responses of these two circuits. The contribution of the parasitic capacitor C_f to the frequency response is very important. If the value of C_f is too high, the contribution of the first order circuit will be of overriding importance and the resulting bandwidth of the amplifier will be too small. If the value of C_f is too low, the response curve will have a peak (due to the second order circuit). A "ringing" effect will be present on pulse-type signals and an instability and oscillation can occur at some frequencies.

This capacitor is generally too high. It consists of:
- the self parasitic capacitor of the feedback resistor
- the parasitic capacitor due to the PCB layout.

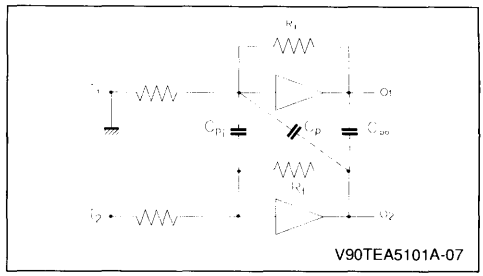
Practically,the best bandwidth performances are achieved by:
- the smallest input-output capacitor and the smallest capacitor between an input and ground
- using a feedback resistor with the smallest possible value but large enough to yield a sufficiently high gain.
- using a feedback resistor with small parasitic capacitance (typ 0.2pF). Some resistors have 0.5 or 0.8 pF parasitic capacitor.

The parasitic capacitors discussed above are usually the ones which need to be taken into account. However any other parasitic capacitor or inductor can modify the frequency response. For instance,a too large capacitor value between the feedback output and ground can create a dominant pole and cause a potential risk of oscillation .

IV.2 CROSSTALK

Figure 7 shows the different parasitic links inducing crosstalk.

Figure 7.



The crosstalk can be caused by:
- parasitic coupling between the inputs (C_{pi})
- parasitic coupling between the outputs (C_{po})
- parasitic coupling between an output and a near input of another channel (C_p).

Parasitic coupling may be capacitive or be caused by HF radiations.

The third type of parasitic coupling is predominant since it involves the addition by feedback at relatively high level(output) signals to relatively low level (input) signals. For example, a 0.1pF C_p parasitic capacitor between an output and the input of another channel will act as a differenciator with the feedback resistor $R_f = 39K\Omega$.

The transfer function of this integrator will be **R_f x C_p x s** (0.2j at 8MHz) and thus the crosstalk will be -14dB at 8MHz. The parasitic coupling between inputs and outputs must be minimized to achieve an acceptable crosstalk (-20dB at 5MHz). This can be done by crossing only the input wires and separating the input and output leads. High voltage components and wires must be laid out as far as possible from small signal wires,even if this results in a larger circuit board.

HF radiations from the feedback resistor must not induced a voltage signal at the input of another channel. This can be achieved by:

- spacing out the feed back resistors
- mounting these resistors in the same direction and strictly aligned one under another.
- mounting these resistors 1cm above the PC board
- using ground connections to insulate the input wires

IV.3 FLASHOVER PROTECTION

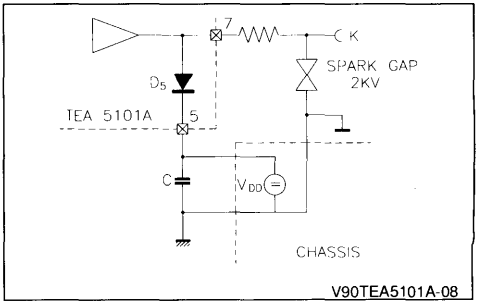
A picture tube has generally several high voltage discharges in its lifetime. This is due to the fact that the vacuum is not perfect coupled with the presence of metallic particles evaporated from the electrodes.Hence, short circuits (very brief fortunately) can occur between two electrodes,one of which is usually the anode (at EHT potential). An overvoltage can be induced on the cathodes or on the supplies even if a flash occurs on an electrode other than a cathode, because of the possibility of flashes in series or overvoltages due to inductive links on the video board or on the chassis. These overvoltages can destroy an IC particularly the video amplifier which is the most vulnerable since it is directly connected to the tube.

The tube manufacturers have made much progress in technology in order to reduce the frequency of flashes and their associated energy (increased quality of vacuum, internal resistance for "soft flash" tubes). Nevertheless, some protection measures are suggested by the tube manufacturers:

- connect spark gaps on each electrode (1 to 3kV or 12kV for focus)
- connect the spark gaps to a separated ground directly connected to the chassis ground by a non inductive link
- connect the cathodes or grids by protective resistors.These resistors must be able to withstand 12kV (20kV for focus)instantaneous voltages without breakdown and without any change of value following successive flashes. These resistors must be of a non-capacitive type. 1/2W (1W for focus) hot molded carbon type resistors are well suited for this application.
- the grid and cathode connections on the PC board must be as short as possible and spaced well away from other connections in order to avoid parasitic inductions.

Furthermore, the TEA5101A has been provided with an additional effective feature to improve the flashover protection.As described in section I-4, a protection device has been included comprising a high voltage high current diode which is connected between each output and the high voltage power supply. The equivalent diagram of this protection is shown in Figure 8.

Figure 8.

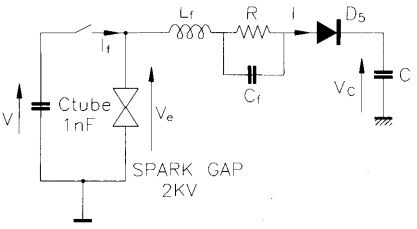


The flash current is diverted to the ground through the diode and the decoupling capacitor C.

Two kinds of flashes can occur:

1) low resistance flashes during which the spark gaps are activated since the cathode voltage exceeds the breakdown value of the spark gap. In this case the equivalent diagram is the following:

Figure 9.



I_f flash current (≅ 1000A)
L_f inductance of the connection (≅ 10µH)

V90TEA5101A-09

Ctube previously charged to 28kV is instantaneously discharged during

$$\Delta t = C_{tube} \times \Delta \frac{V}{I_f} = 30ns$$

Since the voltage across the spark gap falls almost instantaneously to 2000V, the peak current I flowing into the diode is (assuming V_C is held by good decoupling) :

$$I = \frac{V_e \times \Delta t}{L_f} = 6A$$

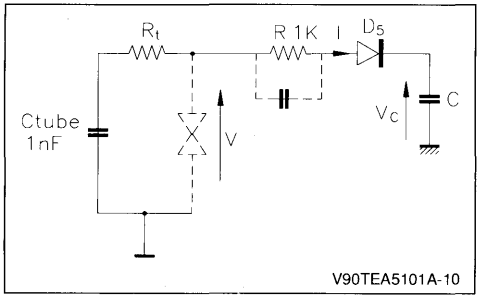
To ensure a variation of V_C less than 10V, C must be

$$C > \frac{I \times \Delta t}{\Delta V_C} \quad eg \quad C > 18nF$$

The decoupling must have good HF characteristics.

2) high resistance flashes in which the spark gaps are not activated. In this case the equivalent diagram is the following:

Figure 10.



V90TEA5101A-10

If $V < 2$ kV, $I < \frac{2000}{R}$, $I < 2A$ and $R_t \cong 12k\Omega$

The time constant of the flash is $R_t \times C_{tube} = 12$ µs, the decay time is approximatevely 30 µs. The value of C must be

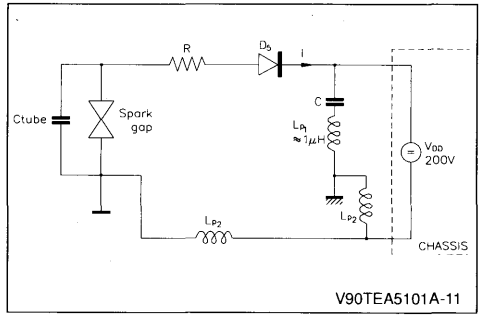
$$C > \frac{\Delta t \times I}{\Delta V_C} \quad eg \quad C > 6\mu F$$

in order to ensure a VC variation less than 10V.

The total decoupling will be made up by a 10µF electrolytic capacitor connected in parallel with a 22nF plastic film capacitor with good HF properties.

It must be placed very close to the TEA5101A to be efficient. Otherwise, the equivalent diagram will be the following (case of low resistance flash).

Figure 11.



V90TEA5101A-11

$$\Delta V_C = \frac{I \times \Delta t}{C} + \frac{L_{P1} \times I}{\Delta t}$$

$\Delta V_C = 210V$ with $L_{p1} = 1$ µH and $L_{p2} = 0$

In this case the V_{DD} voltage can rise to a dangerous value (+210V increase) and the protection is not efficient.

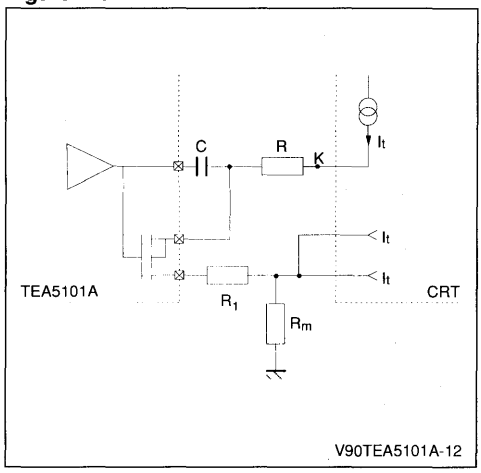
If the connection between the socket ground and the chassis ground is inductive ($L_{p2} \neq 0$), the effect is the same.

However in this case, all the TV IC's,and not only the TEA5101A,will be exposed to destructive overvoltages.

IV.4 OUTPUT SWING

The simplified diagram of this function is shown below (See Chapter II and chapter III):

Figure 12.



The current delivered by a CRT is given by the characteristic curves (fig 13-14).

The minimum value of V_k (due to all the voltage drops in the resistors and in the amplifier) is given by the equation (see fig 12 above):

$V_k = (R + R_{on} + R1 + 3 \times R_m) \times I_t = R_{eq} \times I_t$ (1)

with R_{on} : on state PMOS resistance

To find the maximum available current It_{max}, we can draw the curves of the equation (1) on the tube characteristics. I_{tmax} will be given by the intersection point of the curves. Since the tube characteristics are: I_t vs $V_{cutoff} + V_{G1} - V_k$ the equation (1) must be changed to

$$I_t = \frac{V_{CUTOFF} + V_{G1} - V_k}{R_{eq}} \quad (2)$$

Assuming V_{G1}= 0, we can draw the curves of equation (2) for several values of V_{cutoff} (eg 150V and 200V) and several values of R_{eq} (eg 5k,10k,15k,20k) (see fig 13 and 14). We can see from these curves that R_{eq} must have the following values to allow the tube to source 4mA per gun :

Figure 13.

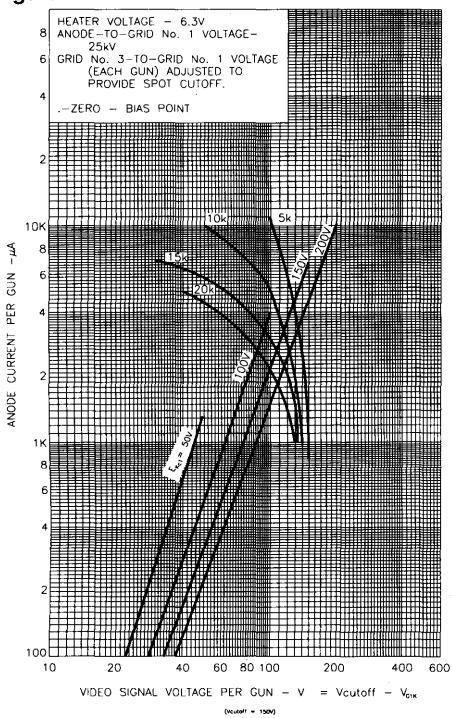
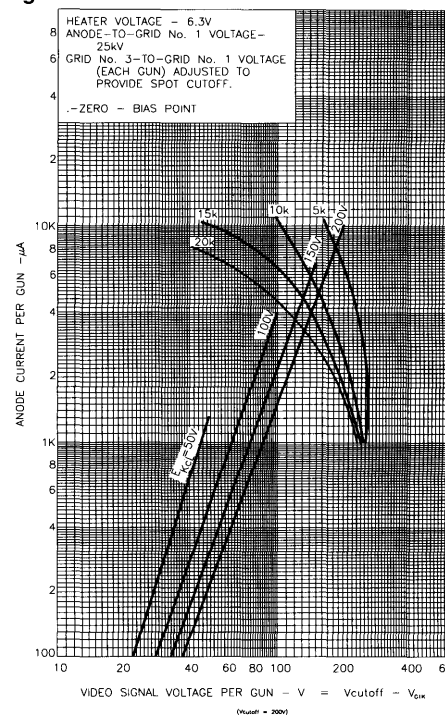


Figure 14.



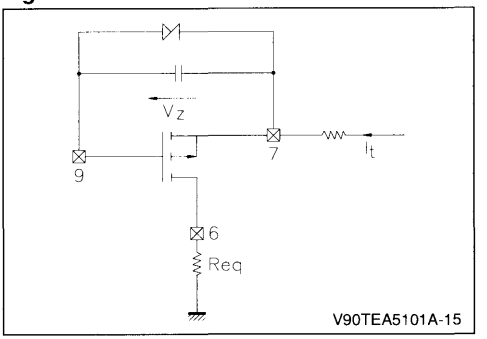
$R_{eq} \leq 5k\Omega$ for a 150V cutoff point
or $R_{eq} \leq 15k\Omega$ for a 200V cutoff point

As R_{on} value is approximatively 1.7kΩ, the measurement resistor must be as low as possible.

Working with higher cutoff point would be an alternative solution. But a 200V cutoff point seems to be too high a value since in this case the supply voltage would be greater than 200V and would affect reliability performances.

Another solution consists of connecting a zener diode as shown in Figure 15.With this device the high current operation of the TEA5101A is similar to that of a discrete amplifier (with PNP) operation.

Figure 15.



For low currents, if the zener voltage is greater than the V_{GS} voltage, the zener diode is biased off and the beam current flows through the measurement resistor. When the cathode voltage (pin 7) drop is limited because of the pin 6 voltage and when the pin 9 voltage continues to decrease,the zener diode is switched on when $V_7 - V_9 = V_Z$. In this case the beam current is absorbed by the voltage amplifier and the tube can provide larger current values.Nevertheless, the pin 7 output voltage will follow the pin 9 voltage with a V_Z difference.

Since the pin 9 voltage is internally limited to 14V, the output voltage will be limited to 22V with a 8V zener diode.

The CRT bias voltages shown on the previous curves are referenced to the G_1 voltage. The TEA5101A is referenced to ground. We can choose to work with a G_1 voltage greater than ground and thus the low level saturation is not taken into account. In this case, the cutoff points must be increased. When choosing V_{G1} = 12V, the cutoff points will be adjusted to 170V (instead of 150V).

Since the power supply is 200V, 30V are available to ensure correct blanking operation. The DC output voltage must be increased by 12V from its previous value.

Note that all the phenomena described in this section concern a static or quasi-static (15kHz) operation (e.g. white picture or rather large white pattern on a black background). When current peaks occur (e.g white characters insertion or straight luminance transition), the peaks will be absorbed by the coupling capacitor and the voltage amplifier,and hence the tube will be able to source a greater current.

IV.5 LOW CURRENT MEASUREMENTS

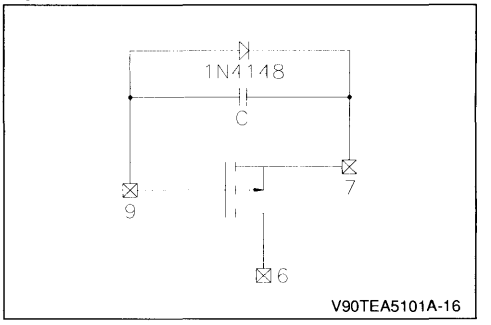
We have seen in section II-2.2 how the beam current monitoring works (see fig.3 page 6). We have seen that the capacitor C must charge again after the blanking phase.

This charge is generally furnished by the tube capacitor independently from the beam current.However,if during the blanking phase, the output voltage is too low (e.g. the PMOS is reverse biased (- 20V) because of a too high leakage current or when measuring with an oscilloscope probe), the ΔVC required to charge C again will be greater than the maximum charge available from the tube capacitor.Hence the beam current will have to charge C in a first step.

Since this current is rather low during the cutoff adjustement phase, a long time will be spent to charge C. The current absorbed by the PMOS and fed to the videoprocessor will not be equal to the beam current and the cutoff adjustement will not be correct.

Hence the reverse voltage across the capacitor C must be limited by a diode connected as follows :

Figure 16.



With this configuration, the voltage across C will be -0.6V max. Since this voltage must be 2.5V in the stationary state (see section II-2.2), the voltage across C must be increased by 3.1V and this charge can be supplied by C_L. We can also slightly decrease the value of C. However if C is too low, the HF behaviour will be impaired.

V - APPLICATION EXAMPLES

V.1 APPLICATION DESCRIPTION

Figures 17 and 18 show two applications, one for a 45AX tube and the videoprocessor TDA3562A (application 1), the other designed for S4 type tube and the videoprocessor TEA5031D (application 2). In these two applications, the nominal gain is 28dB and the output black level is 150V. The quasi cutoff currents are respectively 10µA and 16µA for applications 1 and 2.

These applications are implemented using the same PC board especially designed to allow different options for tube biasing, power supply decoupling and connections. This PC board allows also two different tube sockets (jedec B8274 or B10277) to be connected. Both beam current monitoring modes (sequential and parallel) are possible.

The layout and the electrical diagram of the PC board are shown in Figures 19 and 20.

V.2 PERFORMANCE EVALUATION

As seen in chapter IV, the dynamic performances (bandwidth, crosstalk) of the TEA5101A is very dependent on the PCB layout.Consequently, the evaluation board has been designed to obtain the best results.

To evaluate the performance, the best way is to work outside of the TV set by driving the amplifier by an HF generator (or a network analyser) while simulating the load conditions fixed by the CRT, since AC performances are directly determined by the load.

V.2.1. Measurement conditions

The schematic diagrams of the AC measurements are shown in Figures 21 and 22. The conditions are as follows:

- BIASING : V_{OUTDC} = 100V by choosing $R_{11} = R_{21} = R_{31}$ = 1.5kΩ and V_{DD} = 200V
- AC GAIN = 50 by adjusting P10, P20, P30
- LOADING :
  - by a 8.2pF capacitor and the probe capacitor (2pF), the sum is equivalent to the capacitance of a CRT with the socket and the spark gaps
  - the 1MΩ resistors connected between each output and V_{DD} allow the conduction of the beam current monitoring PMOS transistor in such a way that $VA_{DC} = VB_{DC}$= 100V.
- DRIVING by a 1µF capacitor, the HF generator being loaded by 50Ω.
- the dynamic power dissipated in the IC will increase with frequency. To avoid the temperature increasing, it is necessary to do very quick measurements or to use a low R_{th} (7°C/W) heatsink in forced convection configuration. Such conditions are not present in a TV set since the driving signal will be a video signal instead of a pure HF signal.

V.2.2. Results

V.2.2.1. Bandwidth

The curves Figures 23 and 24 show the frequency responses of one channel with $100V_{pp}$ and $50V_{pp}$ output voltages.

The bandwidths are approximatively 8MHz at $100V_{pp}$ and up to 10MHz at $50V_{pp}$.

V.2.2.2. Crosstalk

The curves Figures 25, 26 and 27 show the crosstalk for this application.The crosstalk is almost the same for the six different combinations of the three channels. The worst value is -24dB at 5MHz.

V.2.2.3. Transition times

The curves Figure 28 show respectively the R, G, B rise and fall times of respectively 49 ns and 48 ns with a $100V_{pp}$ output voltage (between 50 and 150V).

The difference between rise times of the three channels is less than 1ns.

The difference between fall times of the three channels is less than 2ns.

The delay time at rising output is 48ns.

The delay time at falling output is 50ns.

The difference between the delay times is less than 2ns.

The slew rate is about 2000V/µs.

Figure 17 : Application 1 (45AX Tube, TDA3562A) - Electrical Diagram.

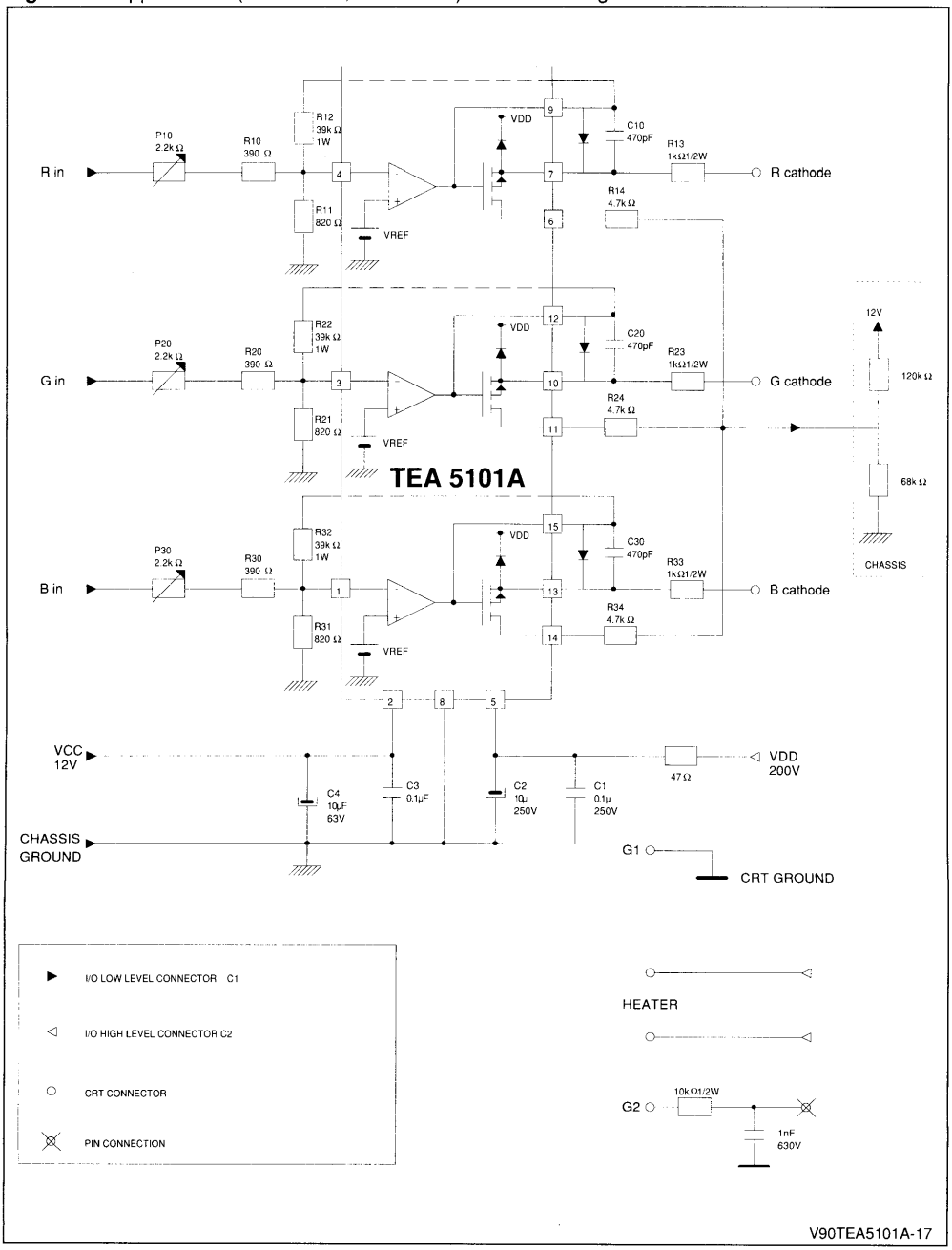


Figure 18 : Application 2 (PIL24 Tube, TEA5031D) - Electrical Diagram.

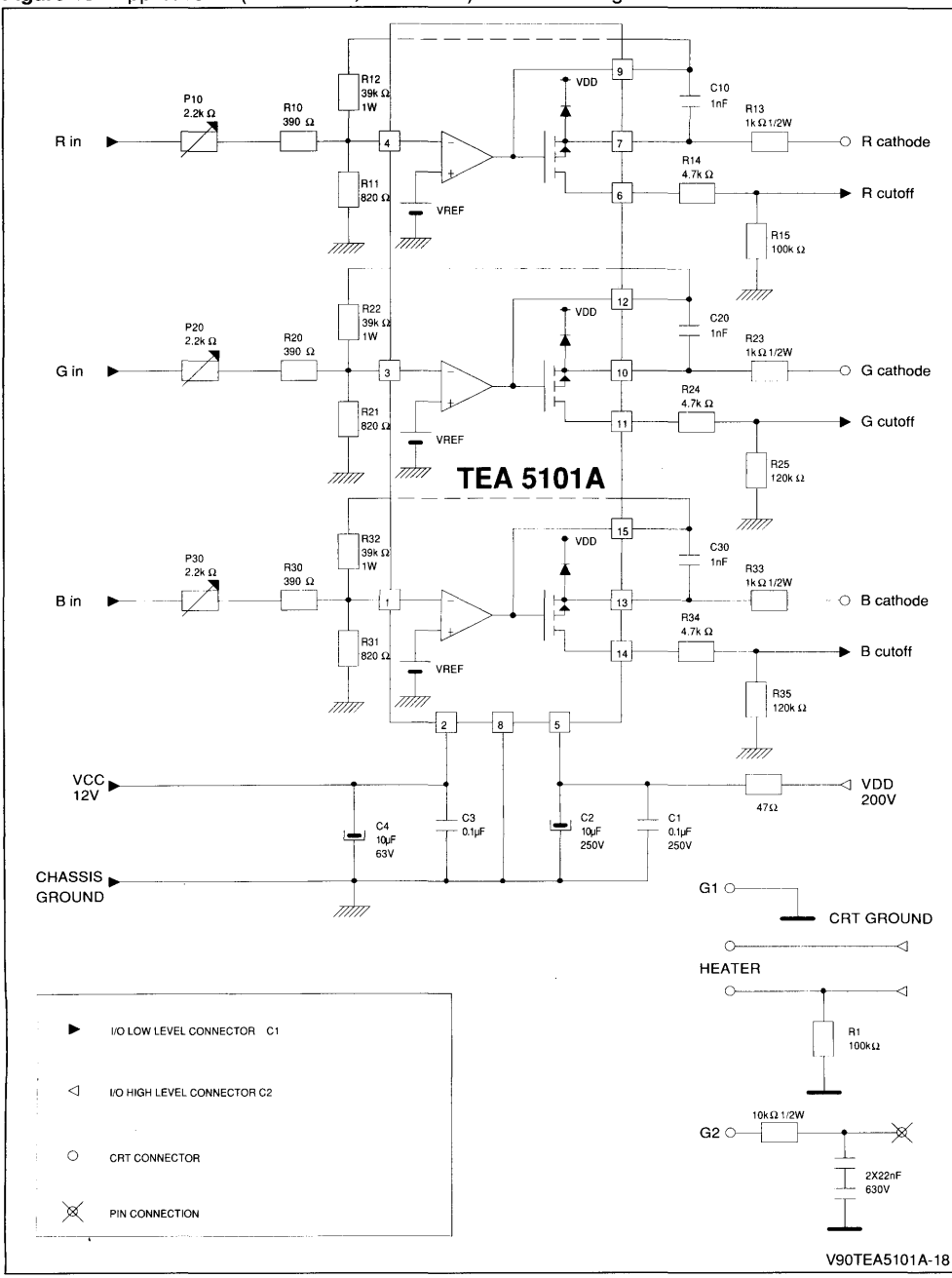
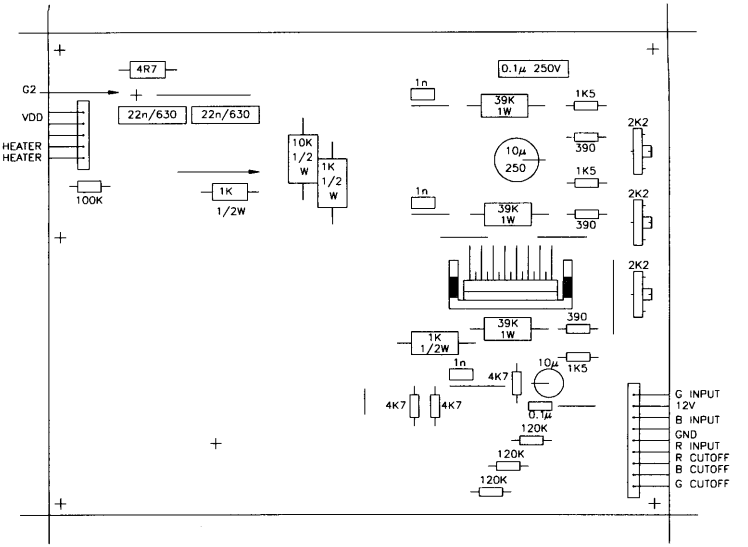
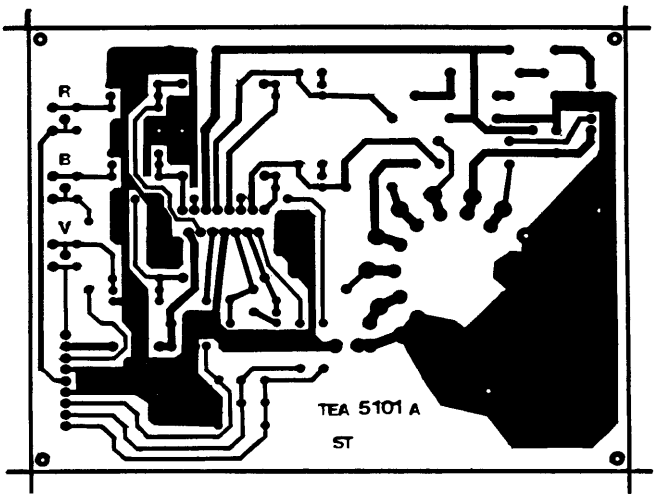


Figure 19 : TEA5101A Evaluation Board Layout and Components View.



COMPONENT SIDE

V90TEA5101-19A



COPPER SIDE

V90TEA5101-19B

Figure 20 : TEA5101A Evaluation Board Electrical Schematic Diagram.

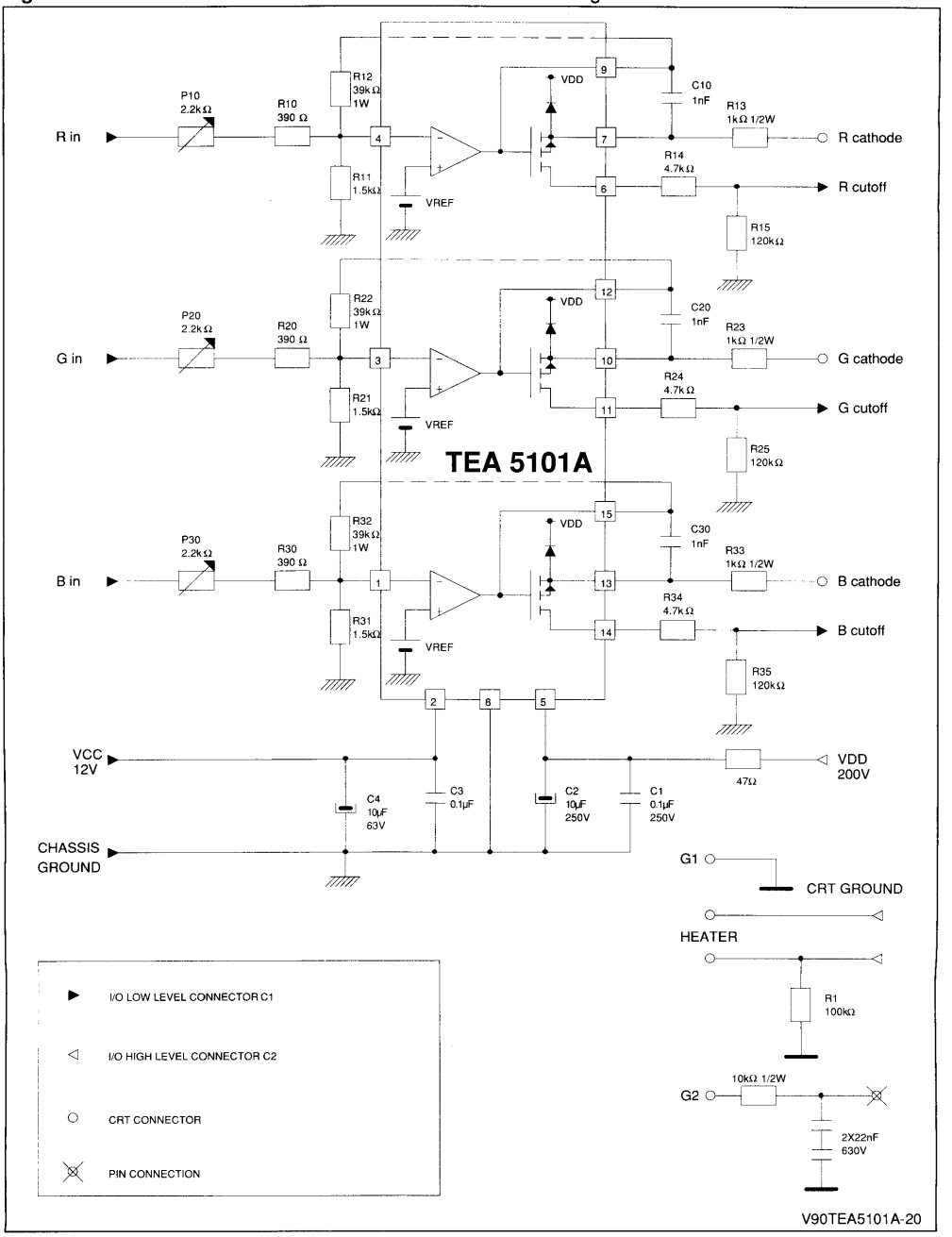


Figure 21 : Bandwith Measurement Configuration.

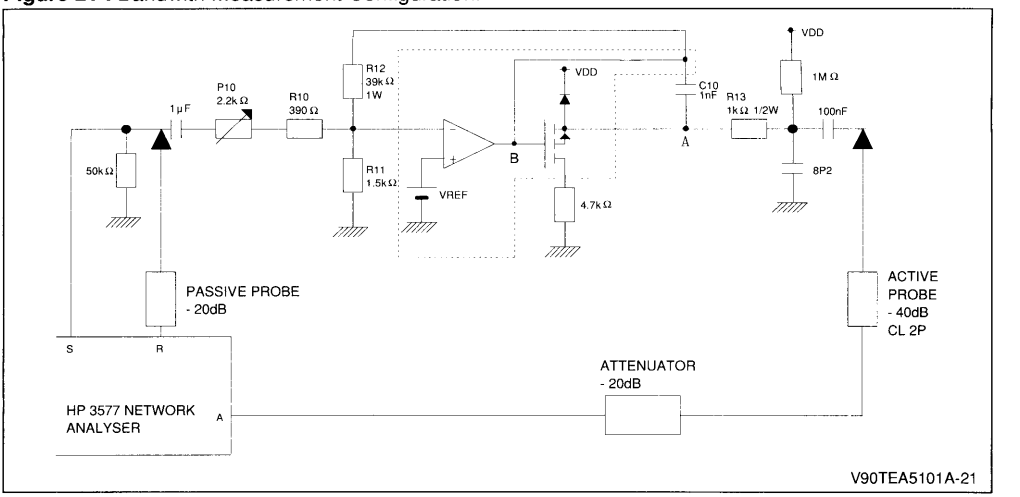


Figure 22 : Crosstalk Measurement Configuration.

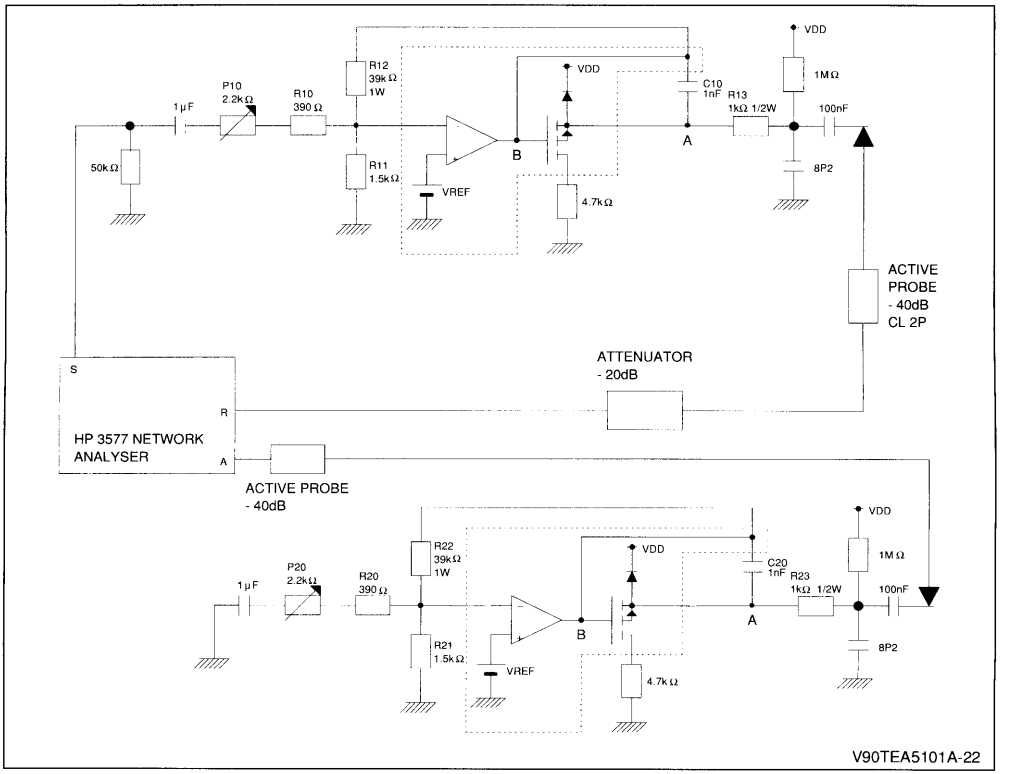
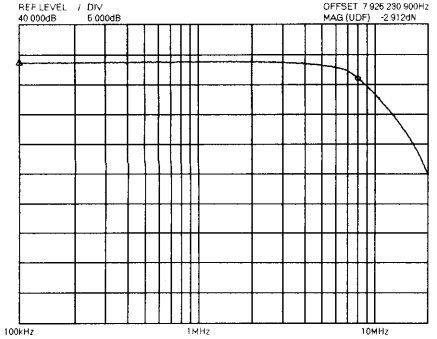
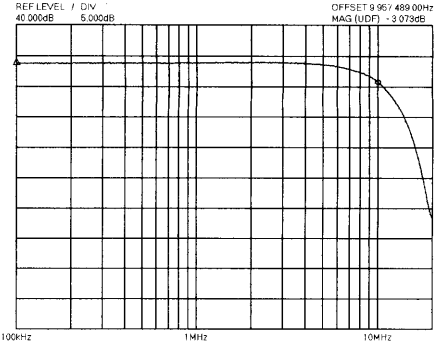


Figure 23 : Frequency Response of R Channel ($100V_{pp}$).



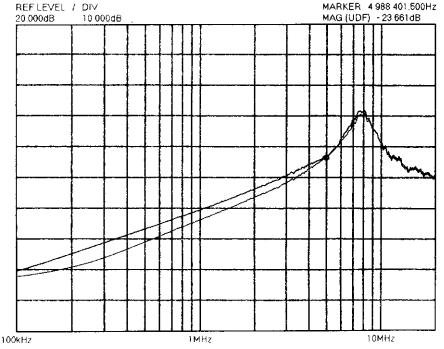
V90TEA5101A-23

Figure 24 : Frequency Response of R Channel ($50V_{pp}$).



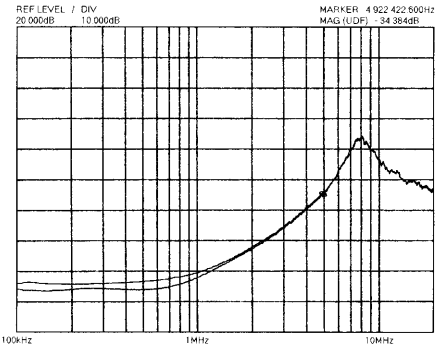
V90TEA5101A-24

Figure 25 : Crosstalk between R Channel and G and B Ones.



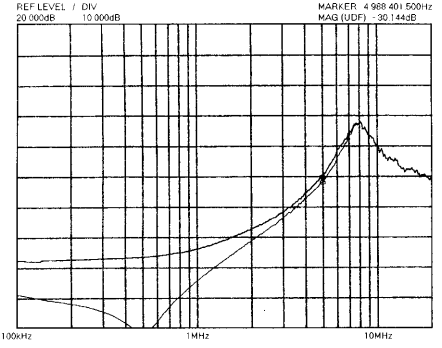
V90TEA5101A-25

Figure 26 : Crosstalk between G Channel and R and B Ones.



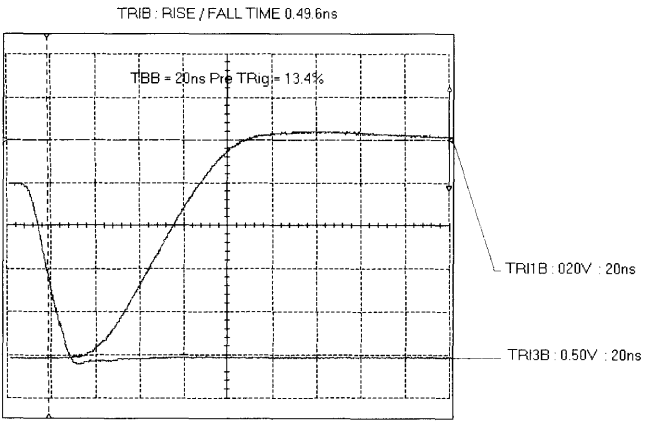
V90TEA5101A-26

Figure 27 : Crosstalk between B Channel and R and G Ones.

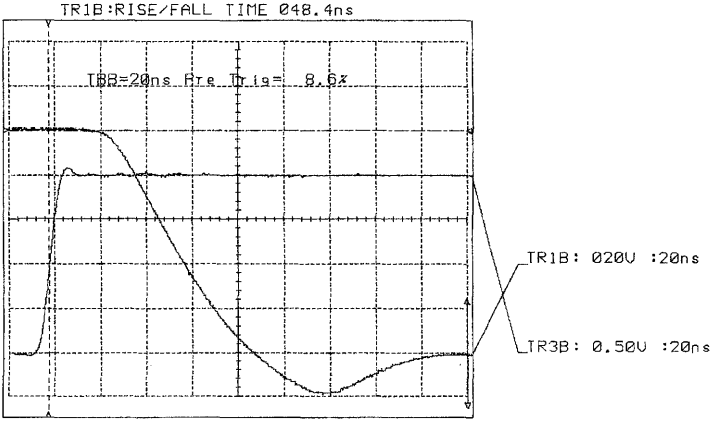


V90TEA5101A-27

Figures 28A and 28B : TEA5101A R Channel Step Response.



V90TEA5101A-28A



V90TEA5101A-28B

AN AUTOMATIC LINE VOLTAGE SWITCHING CIRCUIT

VAJAPEYAM SUKUMAR
THIERRY CASTAGNET

ABSTRACT

The voltages found in line sockets around the world vary widely. Power supply designers have, most often, overcome this problem by the use of a doubler/bridge switch that can double the 120V nominal line and simply rectify the 240V nominal voltage.

A two device solution (comprising an integrated circuit and a customized triac) that will adapt the power supply to various line voltages around the world is described in the following paper. This circuit replaces a manual switch and could also open special markets. Other advantages of this integrated circuit solution are ease of circuit design, lower power dissipation, a smaller component count and additional safety features.

INTRODUCTION - THE DOUBLER/BRIDGE CIRCUIT.

AC line voltages the world over can be divided into two main categories :

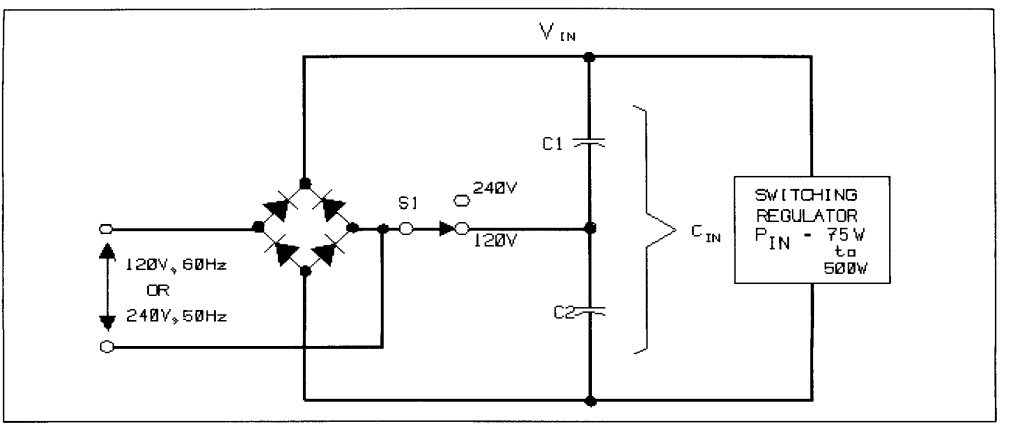
a)120V nominal, 60Hz systems. Electronic equipment is usually designed to run in the 90V - 132V range.

b) 240V nominal, 50Hz systems. Equipment has to be designed to run in the 187V-264V range.

A good reference for the various line voltages around the world is found in [1].

Power supplies built to run off these voltages have to be either wide range input or must use a doubler/bridge circuit. The disadvantage of the wide range input scheme - that all components have to meet worst case current and voltage requirements - makes such a solution popular only at less than 75W power levels. The popular doubler/bridge circuit is shown in Fig. 1. When the AC input voltage is 120V nom. (doubler mode) the switch S1 is closed. During the positive half cycle of the input voltage capacitor C1 is charged. During the negative half cycle of the input voltage, capacitor C2 is charged to the peak line voltage. When the line voltage is 240V nom. (bridge mode), the switch S1 is open and the circuit works like a conventional bridge rectifier.

Figure 1. Schematic Diagram of a Doubler/Bridge Circuit.

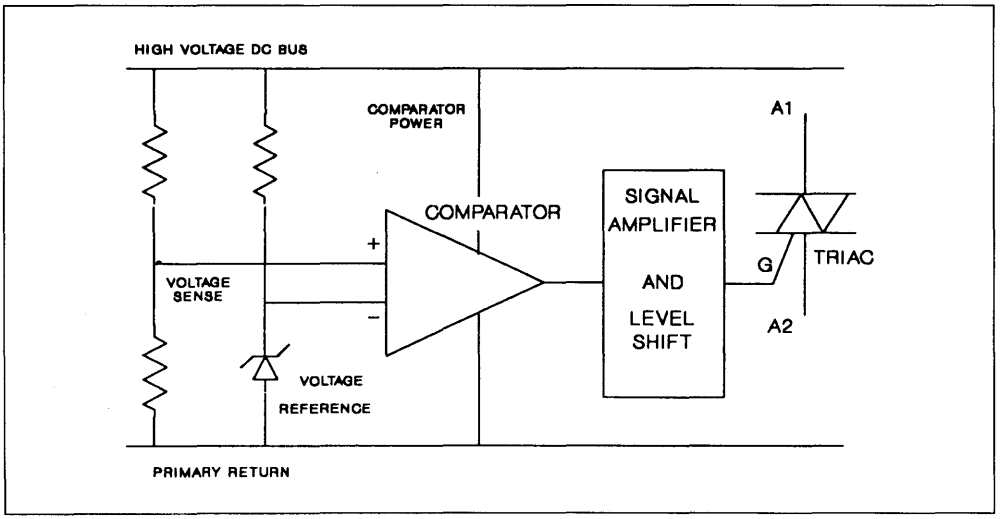


At power levels of over 500W, power factor correction circuits and three phase line input voltage circuits dominate. So, the automatic line voltage switching (AVS) circuit is used mostly in the 75W-500W power range.

The recent push to replace the mechanical switch S1 in Fig.1 with an automatic line voltage switching (AVS) circuit came from computer manufacturers. They found that the small additional cost of the AVS circuit is less than the costs of power supply failures incurred by inadvertently positioning the switch in the wrong position.

While many of the early AVS designs used relays, the triacs, with their superior reliability, small size and low cost are now more popular.

Figure 2. Discrete AVS Circuit Block Diagram



DISCRETE AUTOMATIC VOLTAGE SWITCHING CIRCUIT

Figure 2 shows a diagram of the various blocks comprising a discrete implementation of the AVS circuit. The line voltage selection circuit can be divided into three main functions:

1. Detection of peak line input voltage. Various schemes use resistive or capacitive dividers to measure the voltage across C1 and C2.

2. Comparison with a reference voltage that is generated with the help of a zener diode. A simple comparator can be implemented with two small signal transistors.

3. Drive for the triac. If the circuit is to be in the doubler mode, then the output signal of the comparator is boosted to provide the drive to turn the triac on. This interface circuitry can consist of a high voltage transistor and bias resistors.

DISCRETE VS INTEGRATED CIRCUIT AVS.

An IC based AVS circuit should be designed to overcome the disadvantages of the discrete solution that are listed below.

1. Power Dissipation.

This is critical because the entire supply current necessary for the operation of the AVS circuit comes from the high voltage bus. Every milliampere of current saved in the sensing, comparison and drive circuitry increases the efficiency of the entire system.

$$P_D(AVS)=k^*(V_{AC})^2. \quad (1)$$

About 80% of the power lost in the AVS scheme

is in the gate drive to the triac. This means that a sensitive gate triac is the best candidate for the switch S1 *in Figure 1.*

Discrete AVS solutions usually use between 5W and 12W.

2. Immunity to Input Line Voltage Transients.

Most power supplies today are designed to meet IEEE 587 or similar line transient specifications. We must choose a triac that withstands these transient voltages without any triggering. So we have to make a compromise between low gate drive requirements (I_{GT}) and good static dv/dt immunity. The gate drive circuit of the triac must also be designed to reduce any parasitic voltages at the gate. The gate non- trigger voltage (V_{GD}) of most triacs is about 0.2V.

3. Effect of Line Sags and Surges.

Line voltages are generally considered to vary about +/- 10% from their nominal values. The 120V nominal can be as high as 132V and the 208V nom. can fall to 187V. Between 132Vac and 187Vac, there exists a window, in which we have to design the threshold voltage of the comparator in Fig. 2. Additional ('strife', etc.) test requirements can reduce this window to a smaller 140V to 170V. An analysis of worst case component tolerances is critical in AVS design.

Ultimately, however, there will always be line voltage waveforms that will fool an automatic voltage selection scheme. One can think of situations where, say, a large motor will pull the line voltage down below the threshold voltage during startup. A good AVS system will monitor the line voltage and protect the power supply . In some applications, the bridge mode (240V mode) is considered the fail safe mode and if the unit starts off in the bridge mode, it should not be able to change modes till the power is recycled.

SGS-THOMSON AVS10 SOLUTION.

We at SGS-THOMSON studied the possibility of an integrated circuit solution for this application. The cost constraints ruled out any exotic single chip solutions and forced us to opt for an 8 pin DIP IC for sensing and a TO-220 triac as the power switch. This IC+triac solution, called AVS10, also offers optimal protection against noise.

In order to maximize the design flexibility and reduce turn around time, we chose a semi-custom solution called ANACA. A 12V CMOS ANACA process used offers mixed analog/digital standard cell capability.

OPERATION OF THE AVS10 CIRCUIT

A typical application diagram for the AVS10 in a power supply is shown in Fig. 3.

Figure 3. AVS10 Application Schematic Diagram

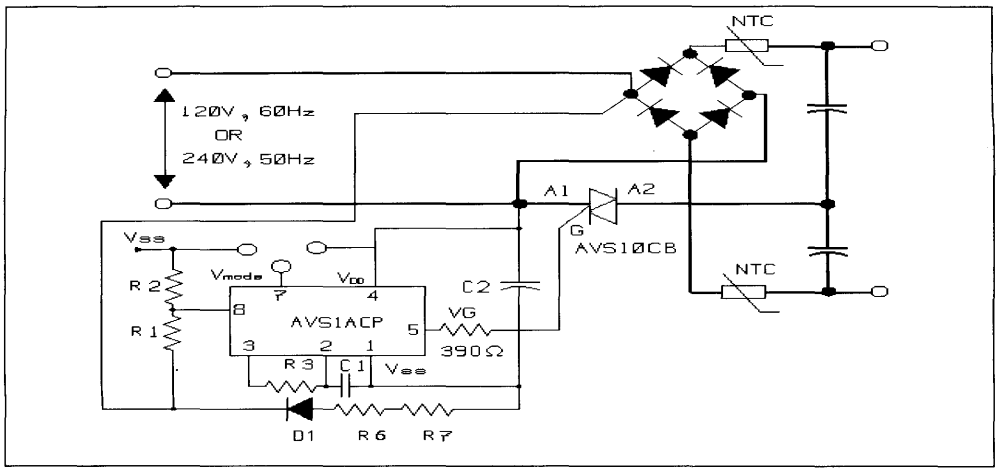
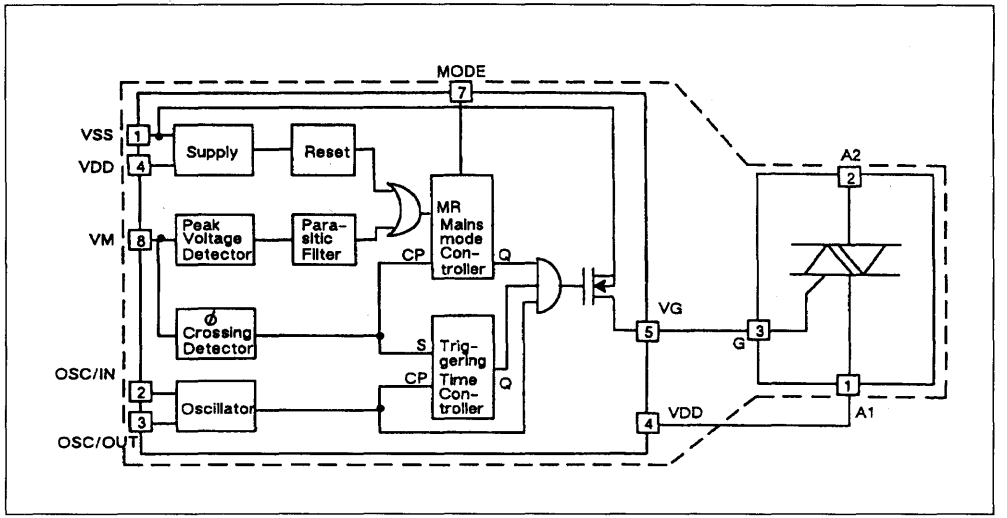


Figure 4. AVS10 Block Diagram



The series circuit of D1, R6, R7 and C2 provide power for the chip. Pin 1, Vss, is a shunt regulator that provides a -9V (nom.) output. R1 and R2 are resistive divider precision resistors that are a measure of the input line. The voltage at Pin 8 varies with the input line. Thus the voltage at Pin 8 is not only a measure of the peak input voltage, but it can also sense line voltage zero crossing. Pins 2 and 3 are inputs to an oscillator. The resistor R3 and C1 set the oscillator frequency. Pin 5 drives the gate of the triac through a 390Ω resistor. Pin 7 offers the user a choice of two different modes of operation. The block diagram of the IC is given in Fig. 4.

1. Decreased Power Dissipation.

Decreased power dissipation is an important advantage of the AVS10. While most discrete AVS schemes need 5W to 12W of power, the AVS10 uses about 2W. This performance is thanks to an innovative gate triggering scheme (Patent Pending). The gate current is made up of a pulse train that has a typical duration of around 23µs (45kHz+/-5%). The duty cycle of the pulses is typically 10%. The values of R2 and C3 in Fig. 3 are chosen to give us the pulse frequency.

2. Immunity To Voltage Transients.

The triac of the AVS10 is a sensitive gate triac that is specified to remain off when subjected to dv/dt of 50V/µs. Circuit layout is critical in preventing false dv/dt turn on of the triac [2]. The IC of the AVS10 circuit has a built in digital filter that suppresses the effect of all spikes of less than 200µs duration.

3. Operating In The Failsafe Mode. $V_{mode} = V_{SS}$.

The mode pin on the AVS10 IC, Pin 7 determines the behavior of the circuit if it is turned on into a line surge/sag situation. If Pin 7 is tied to V_{SS} (Pin 1), the AVS10 circuit is in a failsafe mode. This means that if the device is turned into a bridge mode, it will remain in the bridge mode, even if the voltage were to suddenly dip into the 110V range.

4. Operation In Reactive Mode. $V_{mode} = V_{DD}$.

If Pin 7, the mode pin, is tied to V_{DD}, then the device will switch between bridge and doubler modes if the input voltage changes. If the 110V input changes to 220V, then the AVS10 turns the triac off by the next mains cycle. If the 220V input falls to 110V, the AVS10 circuit has a validation period of 8 mains cycles (when it verifies that the voltage is still at 110V) after which the triac turns on. Thus, safety features are built into the AVS10 circuit. Typical timing diagrams for the two modes are given in Figs. 5 and 6.

Figure 6. Timing diagram - $V_{mode} = V_{SS}$

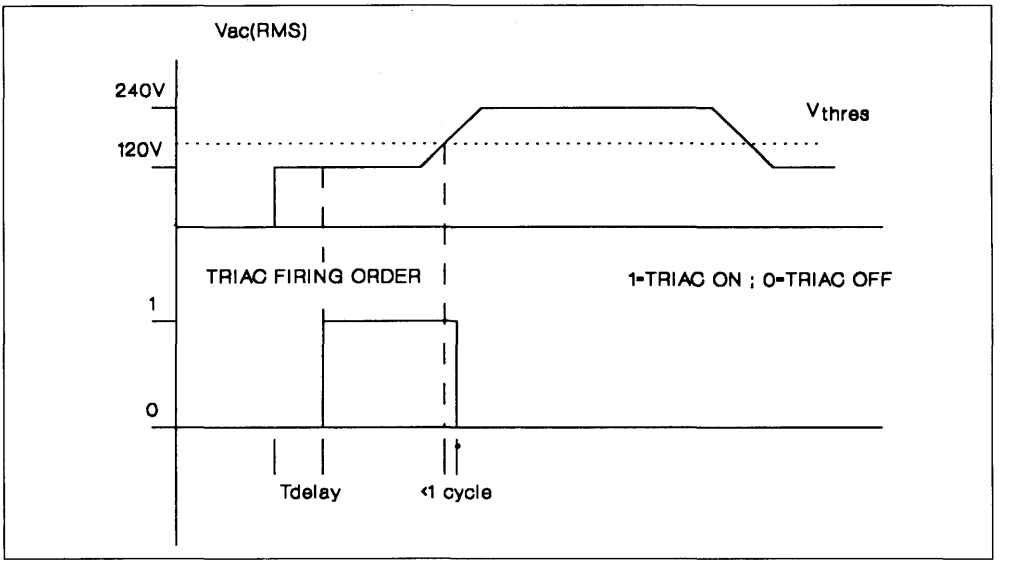
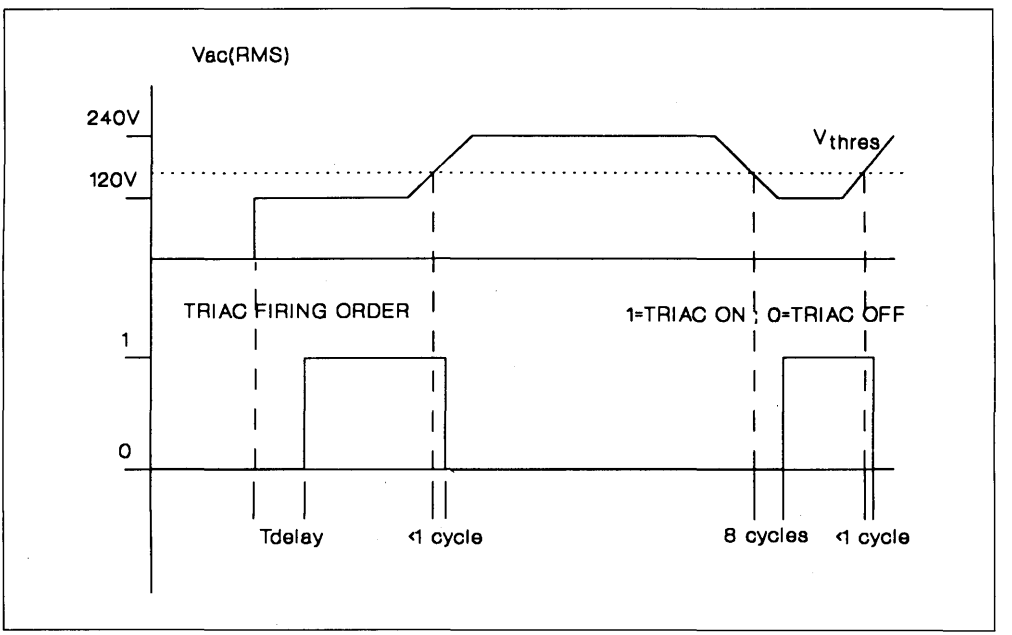


Figure 5. Timing Diagram - $V_{mode} = V_{dd}$



A detailed account of how to set the input voltage threshold is found in [2].

5. Additional Safety Features.

Additional steps are taken to enhance the safety of design include starting up always into the bridge mode. There is a delay of around 250 ms at start up before the AVS10 goes into the doubler mode.

Hysteresis is also built into the comparator to prevent small line voltage variations from causing toggling between bridge and doubler modes. Only a voltage variation of over 10% of the line voltage can cause the AVS10 to change modes.

CONCLUSION

This paper describes an efficient way of implementing an automatic doubler/bridge circuit. The primary use of this circuit is in 75W to 500W SMPS. Other innovative uses are possible. One example would be industrial motor drives which can be designed to accept either 120V line-to-neutral or 208V line-to-line input.

The main advantages of the AVS10 solution are:

1. High Efficiency. Losses are just 2W vs. 5W-10W for discrete schemes.

2. Safety. Uses digital spike suppression, hysteresis, validation of range, a failsafe mode and good control over the triac triggering.

3. Space Optimization., small supply resistor. Good reliability.

4. Ease of Use. Eliminates manual line selection errors.

5. Suitable solution for various power range:
   AVS10 up to 300W
   AVS12 up to 500W.

REFERENCES.

[1] PSMA Handbook of Standardized Terminology for the Power Sources Industry. Appendix C.

[2] SGS-THOMSON technical note 'How To Use The AVS Kit'.

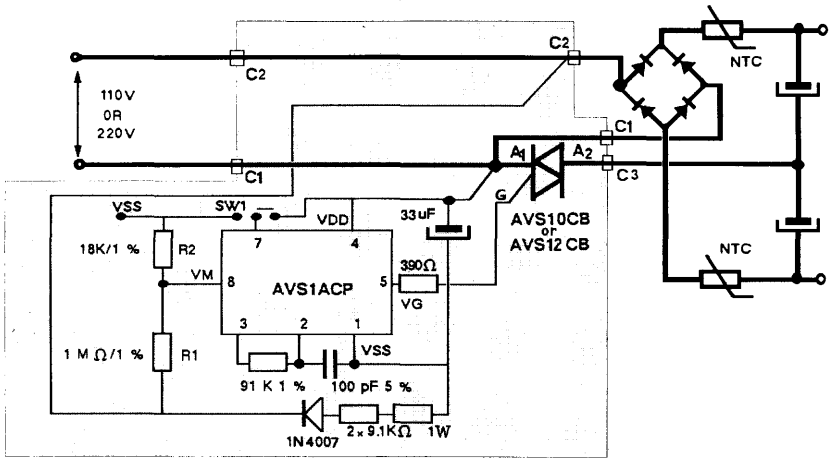
HOW TO USE THE AVS KIT

PRELIMINARY NOTE

I DESCRIPTION OF THE AVS KIT :

The AVS10, or AVS12, is an automatic mains selector to be used in on line SMP supply with Power up to 500W. It is made of two devices.

This switch modifies automatically the structure of the input diodes bridge in order to keep a same DC voltage range.



The AVS is compatible with 50 and 60 Hz mains frequency and operates on two mains voltage ranges :

- On range I (110 V_{RMS}) the AC voltage varies from 88 to 132 V and the triac is ON : the bridge operates as voltage doubling circuit.

- On range II (220 V_{RMS}) the AC voltage varies from 176 V to 276 V and the triac is OFF : the circuit operates as full wave bridge.

II PERFORMANCE OF THE AVS :

The control of the switch is made by the comparison of the mains voltage (VM on pin 8) with internal threshold voltages (VTH and VH on pin 8).

When mains voltage increases from range I to range II the triac conduction is completly stopped before one mains period because VM > VTH.

When mains voltage drops from range II to range I VM becomes lower than VTH - VH. There are two options (V mode on pin 7) :

- V mode = VDD ; the triac triggering is valided 8 mains periods after power on reset.

- V mode = VSS ; the triac control remains locked to range II until circuit reset.

III USE OF THE AVS :

Calculation of the oscillator :

The oscillator frequency is determined by the mains frequency (50 and 60 Hz) and the gate control : its required value must be 45 KHz ± 5%; so the value of components is :

C = 100 pF/5%
R = 91 KOhms/1%

The frequency control is made on pin 3.

Adjustement of the mains mode change :

The measure of the mains voltage is made by a detection of the peak value.
The change of mains range is made by adjustement of resistor bridge and we advice :

800 kOhms < R1 + R2 < 2 mOhms

Calculation of the change from range I to range II (on pin 8) :

$[VTH . (R1 + R2)]/(R2 . \sqrt{2}) + Vreg / \sqrt{2}$ = max.RMS voltage on Range I

Vreg typ = - 9 V and VTH typ = 4.25 V

Calculation of the change from Range II to range I :

$[(VTH - VH) . (R1 + R2)/R2 . \sqrt{2}] + Vreg / \sqrt{2}$ = min . RMS voltage on range II

Vreg typ = - 9 V and VH typ = 0.4 V

Performance of the power on reset :

The power on reset permits the charge of the bulk capacitors of the SMP supply through soft start circuit.
The triac triggering is valided (on range I) after the validation of power on reset (charge of supply capacitor C) and a temporization of 8 mains periods.

T delay = delay time between power on and triac triggering

$Td = 0,89 . Vreg . R . C/[(V_{RMS} . \sqrt{2}/\pi) - R . Iss] + 8/f$

f = mains frequency

R = supply resistor = 18 kOhms

C = supply capacitor = 33 µF

V_{RMS} = mains voltage

Iss = quiescent supply current of AVS

Supply of the controller :

The structure of the supply regulator is a shunt regulator and its current must be lower than Iss max = 30 mA.

In order to have a good behavior of the circuit against mains voltage spikes the pin 4 (VDD) of the integrated circuit has to be connected straightly with the A1 of the triac. In same way the supply diode rectifier and R1 have to be connected to the diode bridge (see typical application diagram).

Triac control :

Between pin 5 and triac gate there is a resistor in order to limit the gate current; its value is given by the controller supply and triac ; the required value is 390 Ohms (5%).

Thermal rating of triac :

The knowlegde of the maximum triac current I_{TM} and the current pulse width tp in worst case conditions allows to calculate the losses, PT dissipated by the triac :

I_{TRM} = RMS triac current
$= I_{TM} \times \sqrt{tp} \times \sqrt{f}$

$PT = 4 . tp . f . I_{TM} . V_{TO}/\pi + rt . tp . f . (I_{TM}^2)$

for AVS10CB :

V_{TO} = threshold voltage of triac = 1.1 V
rt = on state triac resistance = 49 mohms

for AVS12CB:

VTO = 1V
rt = 45 mOhms

The figure 1 of DC general characteristics of triac gives these losses PT versus I_{TRMS} for this application. The figure 2 allows to calculate the external heatsink R_{TH} versus PT and Tamb when Tj = 110C

$Tj - Tc = R_{TH}$ j-c AC . PT
$Tc - Tamb = R_{TH} . PT$

Example on AVS10 :

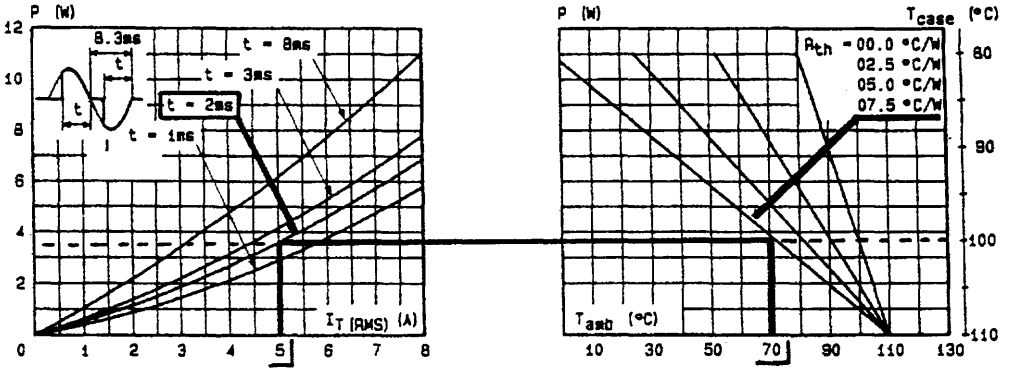


Figure 1 and Figure 2 of AVS10 Datasheet

if tp = 2ms and I_{TRMS} = 5A

- PT = 3.8W

- Tc = 100°C if Tj = 110°C

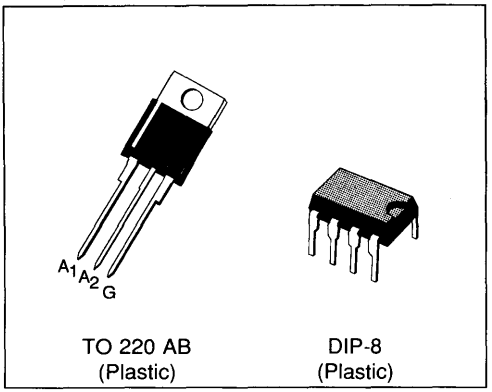
- R_{TH} = 7.5 °C/W if Tj = 110°C and Tamb < 70°C

Annex : AVS demo board

COMPONENT LIST FOR AVS10.

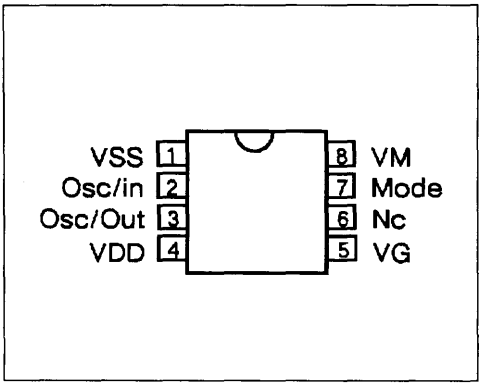
DESIGNATION	QTE	REFERENCE	OBSERVATIONS	MARQUE
PRINTED CIRCUIT	1	4751		
RESISTANCE	1	R1	1 MOhms 1%	
RESISTANCE	1	R2	18 KOhms 1%	
RESISTANCE	1	R3	91 KOhms 1%	
RESISTANCE	2	R4	9.1 KOhms 1W	
RESISTANCE	1	R6	390 Ohms 5%	
DIODE	1	D1	1N4007	
CONDENSATOR	1	C1	100 pF 5%	
CONDENSATOR	1	C2	33µF 16V RADIAL	
TRIAC	1	IC2	AVS10CB / AVS12CB	SGS-THOMSON
INTEGRATED CIRCUIT	1	IC1	AVS1ACP08	SGS-THOMSON
SUPPORT	1		CI 8 PINS	
INVERTER	1	SW1	MINIDIP	
SOCKET	1	SL 3W	3 PINS	WEIDMULLER
PLUG	1	BL3	3 PINS	WEIDMULLER

Products PIN out

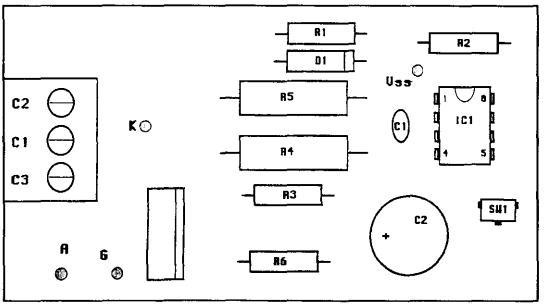


TO 220 AB
(Plastic)

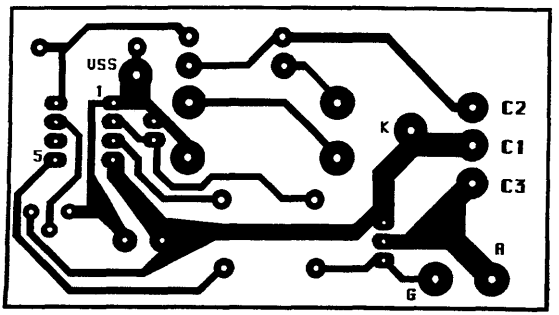
DIP-8
(Plastic)



Components layout



Printed circuit layout (Copper side) : 1/1 scale



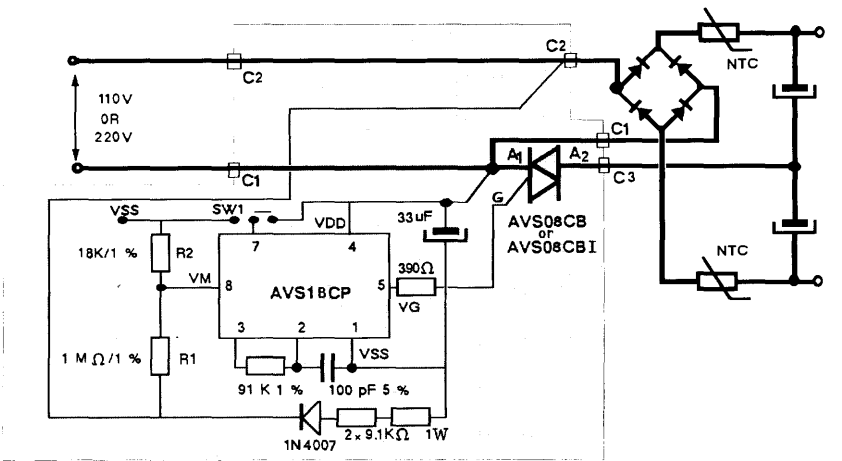
HOW TO USE THE AVS 08

PRELIMINARY NOTE

I DESCRIPTION OF THE AVS 08 :

The AVS08, is an automatic mains selector to be used in on line SMP supply with Power up to 200W. It is made of two devices.

This switch modifies automatically the structure of the input diodes bridge in order to keep a same DC voltage range.



The AVS is compatible with 50 and 60 Hz mains frequency and operates on two mains voltage ranges :

- On range I (110 V_{RMS}) the AC voltage varies from 88 to 132 V and the triac is ON : the bridge operates as voltage doubling circuit.

- On range II (220 V_{RMS}) the AC voltage varies from 176 V to 276 V and the triac is OFF : the circuit operates as full wave bridge.

II PERFORMANCE OF THE AVS :

The control of the switch is made by the comparison of the mains voltage (VM on pin 8) with internal threshold voltages (VTH and VH on pin 8).

When mains voltage increases from range I to range II the triac conduction is completly stopped before one mains period because VM > VTH.

When mains voltage drops from range II to range I VM becomes lower than VTH - VH. There are two options (V mode on pin 7) :

- V mode = VDD ; the triac triggering is valided 8 mains periods after power on reset.

- V mode = VSS ; the triac control remains locked to range II until circuit reset.

III USE OF THE AVS :

Calculation of the oscillator :

The oscillator frequency is determined by the mains frequency (50 and 60 Hz) and the gate control : its required value must be 45 KHz ± 5%; so the value of components is :

C = 100 pF/5%
R = 91 KOhms/1%

The frequency control is made on pin 3.

Adjustement of the mains mode change :

The measure of the mains voltage is made by a detection of the peak value.
The change of mains range is made by adjustement of resistor bridge and we advice :

800 kOhms < R1 + R2 < 2 mOhms

Calculation of the change from range I to range II (on pin 8) :

$[VTH . (R1 + R2)]/(R2 . \sqrt{2}) + Vreg / \sqrt{2}$ = max.RMS voltage on Range I

Vreg typ = - 9 V and VTH typ = 4.25 V

Calculation of the change from Range II to range I :

$[(VTH - VH) . (R1 + R2)/R2 . \sqrt{2}] + Vreg / \sqrt{2}$ = min . RMS voltage on range II

Vreg typ = - 9 V and VH typ = 0.4 V

Performance of the power on reset :

The power on reset permits the charge of the bulk capacitors of the SMP supply through soft start circuit.
The triac triggering is valided (on range I) after the validation of power on reset (charge of supply capacitor C) and a temporization of 8 mains periods.

T delay = delay time between power on and triac triggering

$Td = 0,89 . Vreg . R . C/[(V_{RMS} . \sqrt{2}/\pi) - R . Iss] + 8/f$

f = mains frequency

R = supply resistor = 18 kOhms

C = supply capacitor = 33 µF

V_{RMS} = mains voltage

Iss = quiescent supply current of AVS

Supply of the controller :

The structure of the supply regulator is a shunt regulator and its current must be lower than Iss max = 25 mA.

In order to have a good behavior of the circuit against mains voltage spikes the pin 4 (VDD) of the integrated circuit has to be connected straightly with the A1 of the triac. In same way the supply diode rectifier and R1 have to be connected to the diode bridge (see typical application diagram).

Triac control :

Between pin 5 and triac gate there is a resistor in order to limit the gate current; its value is given by the controller supply and triac ; the required value is 390 Ohms (5%).

Thermal rating of triac :

The knowlegde of the RMS triac current and the current pulse width tp in worst case conditions allows to calculate the losses, PT dissipated by the triac : Figure 1 of DC general characteristics of triac gives these losses PT. The external heatsink R_{TH} can be also calculated with PT and ambient temperature Tamb.

$Tj - Tc = R_{TH}$ j-c AC x PT
$Tc - Tamb = R_{TH} x PT$
$tp = \alpha / 21600$

for example :

if tp = 2ms and I_{TRMS} = 3A

PT = 2W and $\alpha = 43°$

Tc = 92°C if Tj = 100°C

R_{TH} = 21°C/W

if Tj = 100°C and Tamb < 50°C

Example on AVS08 :

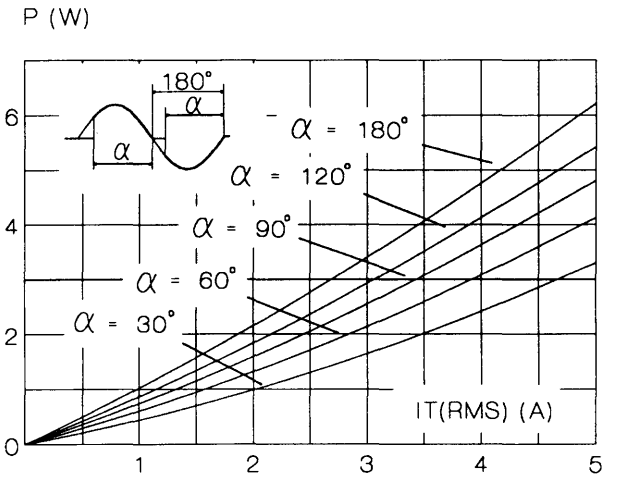


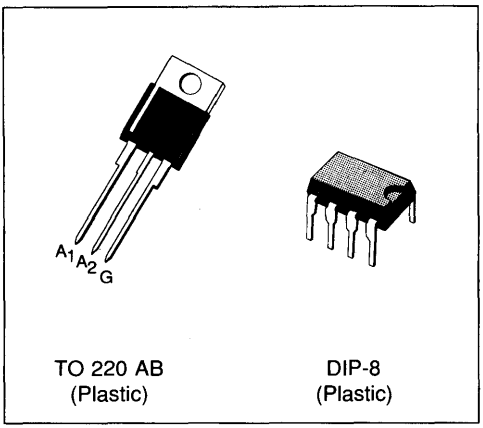
Figure 1 of the AV08 data sheet

Annex : AVS demo board

COMPONENT LIST FOR AVS08.

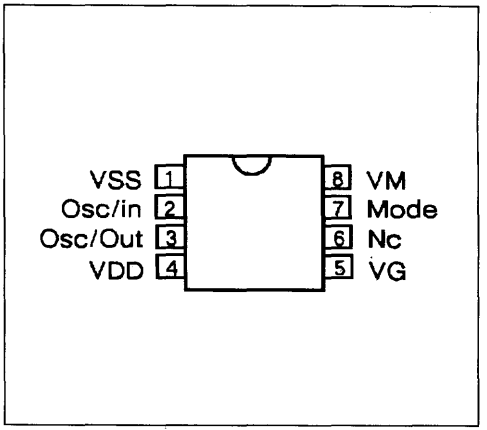
DESIGNATION	QTE	REFERENCE	OBSERVATIONS	MARQUE
PRINTED CIRCUIT	1	4751		
RESISTANCE	1	R1	1 MOhms 1%	
RESISTANCE	1	R2	18 KOhms 1%	
RESISTANCE	1	R3	91 KOhms 1%	
RESISTANCE	2	R4	9.1 KOhms 1W	
RESISTANCE	1	R6	390 Ohms 5%	
DIODE	1	D1	1N4007	
CONDENSATOR	1	C1	100 pF 5%	
CONDENSATOR	1	C2	33µF 16V RADIAL	
TRIAC	1	IC2	AVS08CB	SGS-THOMSON
INTEGRATED CIRCUIT	1	IC1	AVS1BCP08	SGS-THOMSON
SUPPORT	1		CI 8 PINS	
INVERTER	1	SW1	MINIDIP	
SOCKET	1	SL 3W	3 PINS	WEIDMULLER
PLUG	1	BL3	3 PINS	WEIDMULLER

Products PIN out

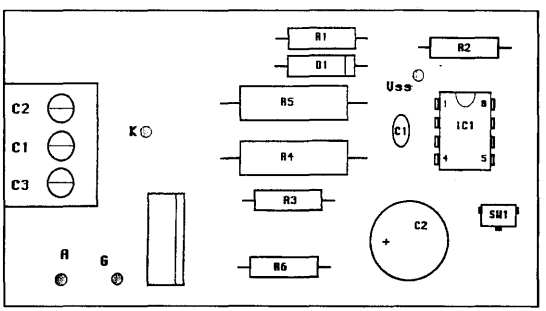


TO 220 AB
(Plastic)

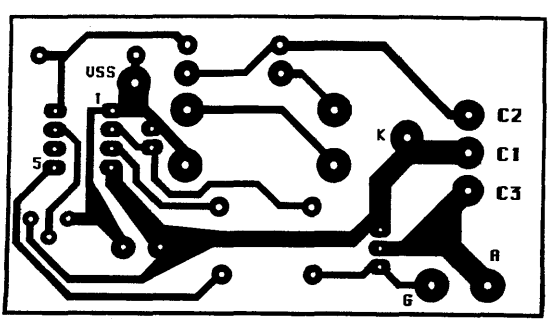
DIP-8
(Plastic)



Components layout



Printed circuit layout (Copper side) : 1/1 scale



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TV EAST/WEST CORRECTION CIRCUITS

SUMMARY **Page**

SUMMARY (continued)

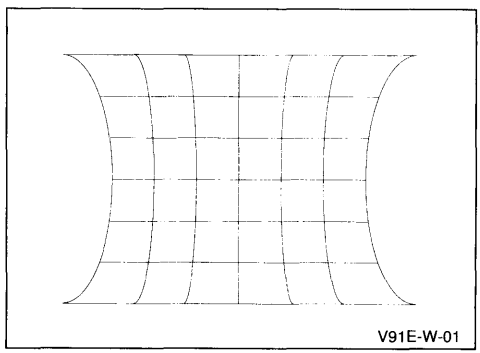
I - TV EAST/WEST CORRECTION GENERAL PRINCIPLES

I.1 - INTRODUCTION

All color picture tubes which are used in the present TV-sets have a magnetic deflection system. Using a homogenous magnetic field, we have generally a pillow-distortion of a rectangular picture on the screen. This is mainly due to the tangens relation between the deflection angle and the beam position on the screen

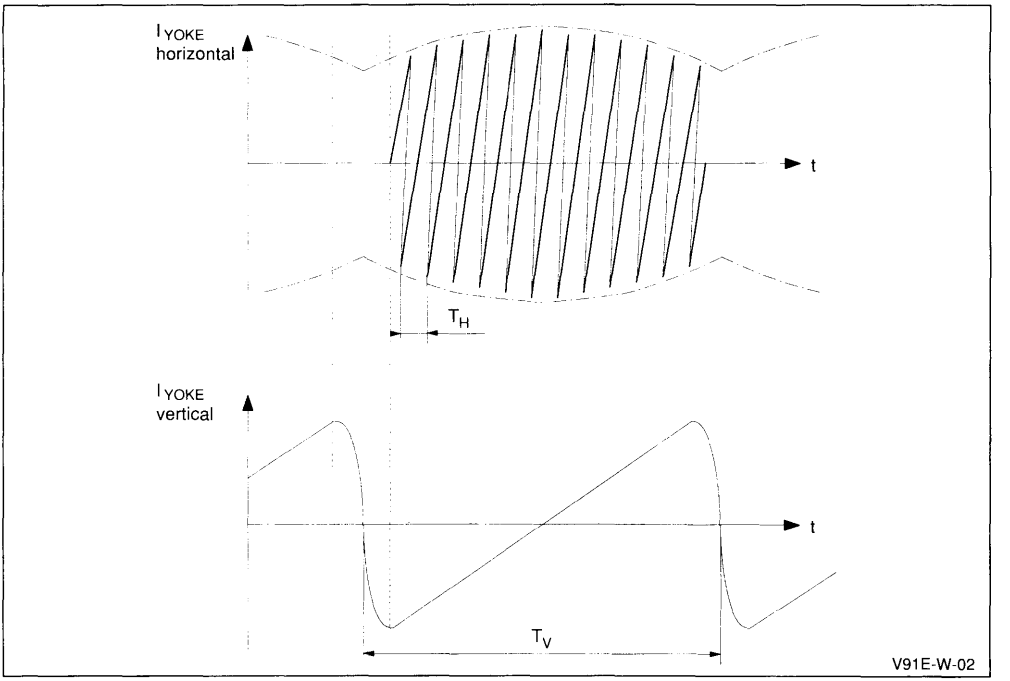
Using a well dimensioned and optimized inhomogenous magnetic deflection field, this distortion can be eliminated completely for picture tubes with a deflection angle of 90°. In the same way the pillow-distortion of 110° deflection tubes can be eliminated in the vertical direction (North-South direction). But until now the distortion in the horizontal direction (East-West direction) can not eliminated with special designed deflection yokes. A distortion remains in Figure 1.

Figure 1 : Test Grid on a 110° Color Tube



In order to compensate this effect, the horizontal deflection current in the yoke must be modulated. This means a large amplitude of the deflection current in the middle of the screen and a small amplitude on the top and the bottom of the screen. The general behaviour of the deflection currents is illustrated in Figure 2.

Figure 2 : Horizontal and Vertical Yoke Current (T_H = 64µs, T_V = 20ms)



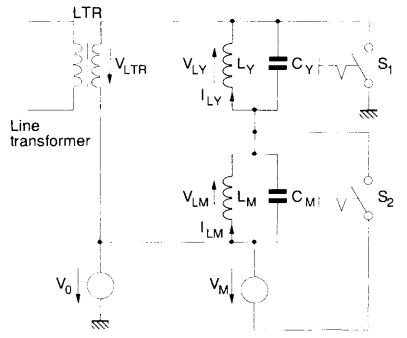
In this picture T_V and T_H are the time periods for the vertical and the horizontal deflection. Note that the envelope of the horizontal yoke current must be a parabola with the same phase as the vertical saw-tooth current. This means an East/West correction can be reached by modulating the horizontal yoke current with a parabola.

There are different possibilities to modulate the yoke current. The most convenient modulator is the so-called **Diode Modulator** described in the next chapter.

I.2 - DIODE MODULATOR PRINCIPLE

Let us consider the basic circuit of the horizontal deflection unit as shown in Figure 3.

Figure 3 : Basic Circuit of the Horizontal Deflection Power Stage including Modulator



L_Y : line yoke
L_M : modulator coil
V_M : modulator voltage
V_0 : supply voltage
S_1 and S_2 : electronic switches

V91E-W-03

For the sake of simplicity, the electronic switches (diodes and transistors) are drawn as simple switches S_1 and S_2. The deflection time T_H of 64µs can be divided in two parts : the scan time T_S at which the electronic switches S_1 and S_2 are closed and the flyback time T_F (S_1 and S_2 opened). The total time period is the

$$T_H = T_F + T_S \quad (1.1)$$

We assume now that the line transformer L_{TR} have a neglectable high inductance and the time behaviour is mainly determined by L_Y, L_M, C_Y, C_M. Small modifications are necessary to consider also the electrical characteristics of L_{TR}, but they should not be discussed here.

During the scan time the inductors L_Y and L_M are directly connected to the voltage sources V_0 and V_M :

$$\left.\begin{aligned} V_{LY} &= V_0 - V_M \\ V_{LM} &= V_M \end{aligned}\right\} \text{ } S_1 \text{ and } S_2 \text{ closed (scan time)} \quad (1.2)\ (1.3)$$

Neglecting any power consumption in possible series resistors, the current in the two inductors increases linear in time :

$$i_{LY} = \frac{t\,(V_0 - V_M)}{L_Y} \quad (1.4)$$

$$i_{LM} = \frac{t\,V_M}{L_M} \quad (1.5)$$

Since the current i_{LY} and i_{LM} must be zero-symmetrical (average value = 0), the peak value of i_{LY} and i_{LM} is obtained after half of the scan time $T_S/2$

$$\hat{i}_{LY} = \frac{T_S\,(V_0 - V_M)}{2\,L_Y} \quad (1.6)$$

$$\hat{i}_{LM} = \frac{T_S\,V_M}{2\,L_M} \quad (1.7)$$

After this time, S_1 and S_2 are opened and the energy in the inductors L_Y and L_M changes to the capacitors C_Y and C_M. We assume now the same resonance frequency for both LC parts

$$L_Y\,C_Y = L_M\,C_M = L\,C \quad (1.8)$$

Under this condition, both capacitors C_Y and C have its peak voltage at the half of the flyback tim $T_F/2$. The energy in the inductors stored at the er of the scan period

$$E_L = \frac{1}{2}\,L\,(i_L)^2 \text{ is then} \quad (1.9)$$

completely transformed into the capacitor

$$E_C = \frac{1}{2}\,C\,(V_C)^2 \quad (1.10)$$

Under this condition, we obtain the general equa tion for the peak voltage in the middle of the flybac period

$$\hat{V}_C = -\,\hat{i}_L\,\sqrt{\frac{L}{C}} + V_{init} \quad (1.11)$$

This voltage is the addition of the initial voltage an the voltage increase due to the energy transfe With (1.6) and (1.11) we get

$$\hat{V}_{LY} = \hat{V}_{CY} = -\,\frac{V_0 - V_M}{\sqrt{L_Y\,C_Y}}\,\frac{T_S}{2} + (V_0 - V_M)$$

$$= (V_0 - V_M)\,(1 - \frac{T_S}{2\sqrt{L\,C}}) \quad (1.12)$$

in the same way (1.7 and 1.11) we obtain

$$\hat{V}_{LM} = \hat{V}_{CM} = V_M\,(1 - \frac{T_S}{2\sqrt{L\,C}}) \quad (1.13)$$

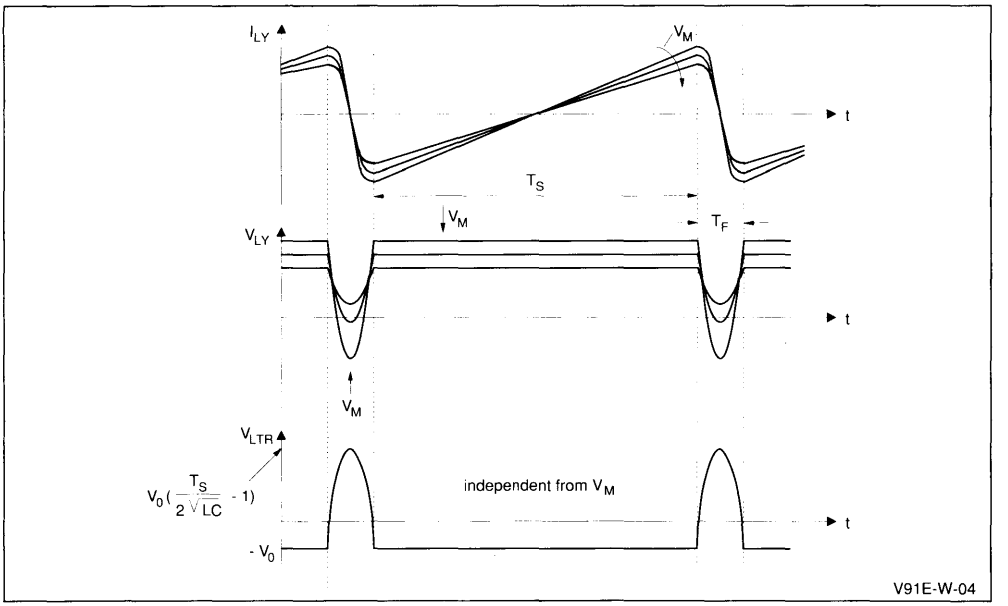
The resulting peak voltage during the flyback tim at the line transformer is then

$$\hat{V}_{LTR} = -\,\hat{V}_{LY} - \hat{V}_{LM} = V_0\,(\frac{T_S}{2\sqrt{L\,C}} - 1) \quad (1.14)$$

Please note that in this circuit, the horizontal flybac voltage $\hat{V}_{LTR}$ (1.14) is independent from the modu lation voltage V_M, though the yoke current I_{LY} ca be changed via the modulator voltage V_M (see 1.6

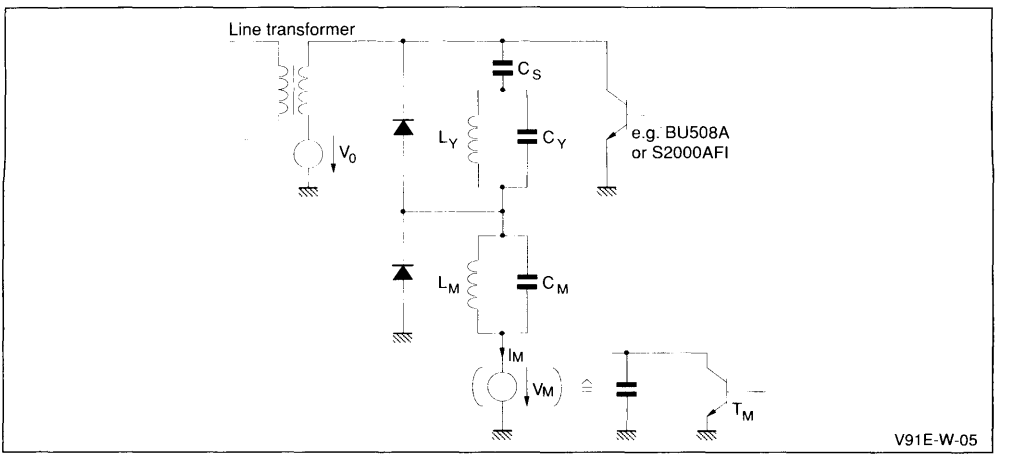
An overview of the currents and voltages is give in Figure 4.

Figure 4 : Currents and Voltages of the Basic Circuit



For a practical application, a large capacitor C_S can be inserted in series to the yoke to get an S-correction of the deflection current I_{LY}. Simultaneously, the voltage V_M can be grouded to have a simpler handling of the modulator driver. The switch S_1 is a standard high voltage power transistor (e.g. BU508A or S2000AFI), the switch S_2 can be replaced by 2 diodes as shown in Figure 5.

Figure 5 : Standard Diode Modulator with Class-A Modulator Driver

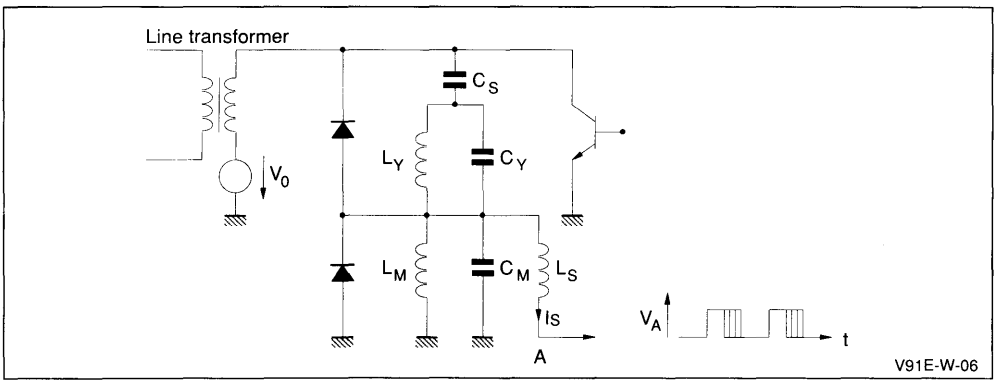


Normally, the current I_M into the modulator voltage source is positive and V_M must only be realized as a variable resistor (e.g. transistor T_M).

Many manufacturers use this simple diode modulator with such active load. A disadvantage of this application is the power consumption in the power transistor T_M (~2W). Under ideal conditions, V_M should have no power consumption (average $i_M = 0$), but in practice the coils and the line transformer are not free from parasitic resistors. Furthermore a reasonably large power is used from the various loads on the line transformer.

An improvement from the power consumption point of view is the use of a switched power stage V_M. For this purpose, an additional inductance L_S (5...20mH) is used and connected as shown in Figure 6.

Figure 6 : Standard Diode Modulator with Class D Modulator Driver (pulse-width modulator)

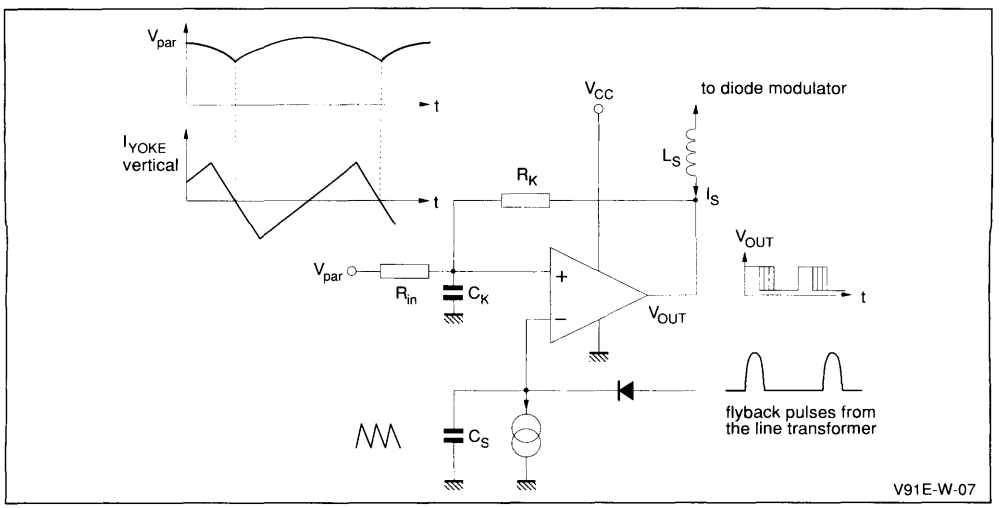


Point A is biased from a pulse-width modulated rectangular wave. The frequency is arbitrary, for a simple pulse-width modulator, The horizontal line frequency is used normally.

I.3 - PULSE-WIDTH MODULATOR PRINCIPLE

The pulse-width modulator for driving the diode modulator contains mainly one power comparator with the external circuitry shown in Figure 7.

Figure 7 : Pulse-Width Modulator

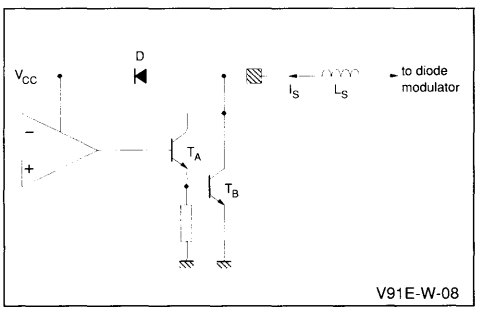


The working frequency is determined by the linear saw-tooth voltage biasing the positive comparator input. It is generated by the flyback pulses of the line transformer. The current sink on the positive input discharges the capacitor C_S during the scan time T_S and yields the negative slope of the saw-tooth voltage.
The negative input is biased from a parabola voltage, its generation is discussed later.

To improve the performance of this pulse-width modulator, a feedback path R_K is provided compensating variations in the power supply V_{CC} of the comparator. The capacitor C_K together with R_{in} and R_K serves as a low-pass filter to suppress the line frequency coming from the comparator output.

If the current I_S in the inductor L_S (see Figures 6 and 7) is only positive, the output stage can have a simple darlington transistor and a diode as seen in Figure 8.

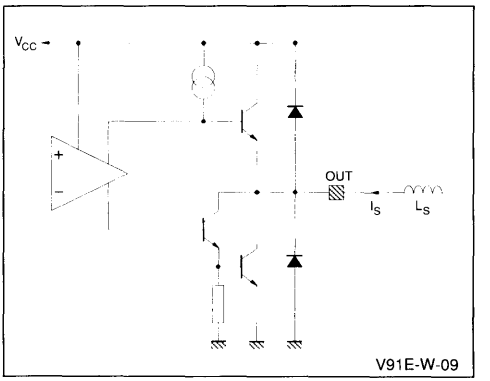
Figure 8 : Comparator Output Stage, only positive modulator current I_S is allowed



If the darlington stage is switched on, the current I_S is flowing through T_A and T_B into ground. Otherwise, the diode D is conducting and I_S flows into the supply voltage.
The power, consumed normally in L_M (see Figure 5) is then redelivered into this supply voltage.

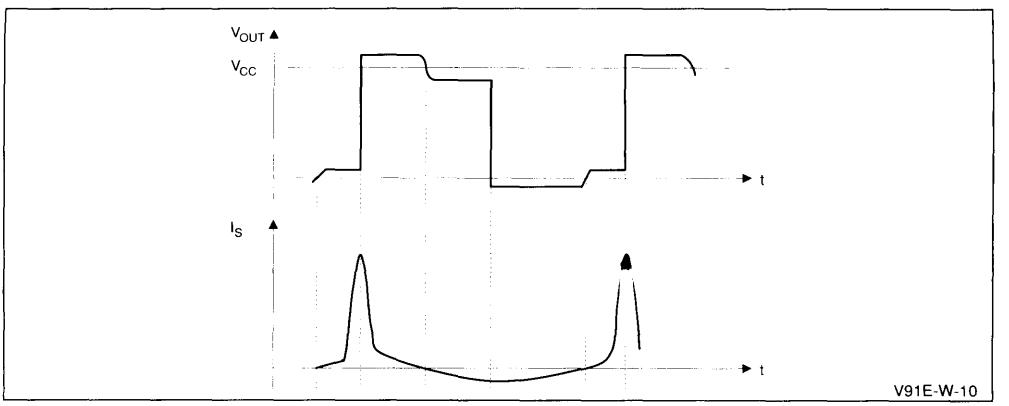
A greater flexibility in the design of the diode modulator can be reached, if the current I_S is allowed to have negative values. For this case, the comparator power stage must be realized as push-pull stage (see Figure 9).

Figure 9 : Comparator Output Push-pull Stage, negative and positive modulator current I_S allowed



Due to the voltage drop across the transistors and diodes, the transition from positive values I_S and negative values I_S yields a voltage step on the output as illustrated in Figure 10.

Figure 10 : Voltage on the comparator output by zero crossing of I_S



In this case the steps in the output voltage produce an additional undesired modulation of the yoke current. Then you can see some irregularities in the vertical lines of the test grid on the screen. With the aid of a reasonable large fedback factor (small R_K, small C_S, large parabola amplitude) this effect becomes neglectable.

I.4 - GENERAL CONSIDERATIONS TO GENERATE THE CORRECTION PARABOLA

The correction parabola which drives the pulse-width modulator (Figure 7) must have the same frequency and phase as the vertical deflection current in the yoke. Therefore, the parabola can be generated directly from the vertical saw-tooth signal which drives the deflection output stage. Principally there are two different kinds for generating the parabola:

a) integrator-network (linear)

b) functional-network (non linear)

Let us consider first the integration method :
The vertical saw-tooth signal can be described with the following simple equation, valid for one period

$$S_{saw\text{-}tooth}(t) = A\frac{t}{T_V} \qquad 0 < t < T_V \qquad (1.15)$$

where A is the amplitude, T_V the time period and t the time.

Integrating this signal we get

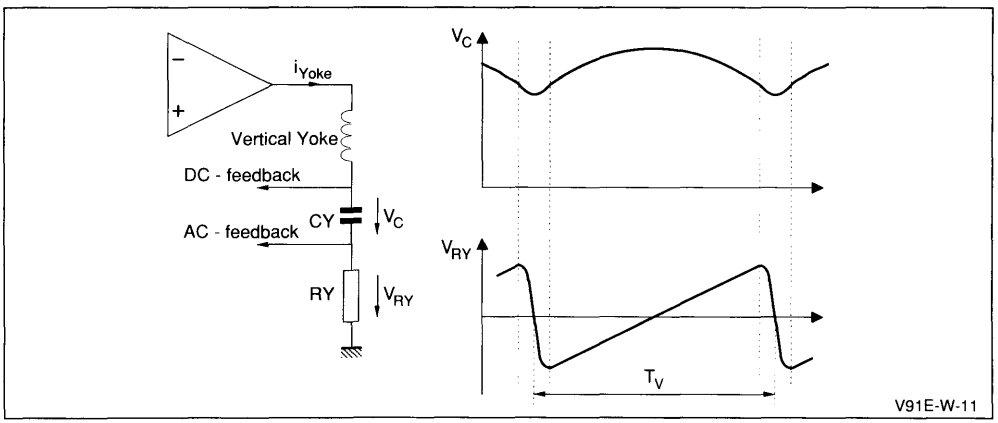
$$\int_0^t S_{saw\text{-}tooth}(t)\,dt = \int_0^t A\frac{t}{T_V}\,dt = \frac{A}{2\,T_V}t^2 \qquad (1.16)$$

Since the relation between the current and the voltage on a capacitor is given by

$$V_C(t) = \int i_C(t)\,dt \qquad (1.17)$$

the parabola can be obtained directly from the coupling capacitor C_Y in the vertical output stage as illustrated in Figure 11.

Figure 11 : Vertical Output Stage and Corresponding Voltages



Due to the aging and the temperature dependence of this (electrolytic) capacitor C_Y, some manufacturers prefer to generate the parabola from the voltage drop across R_Y (V_{RY}) with the aid of a separate integrator.
Due to the small amount of active and passive components, this integration method is the usual method to realize the East/West correction circuit with discrete elements.

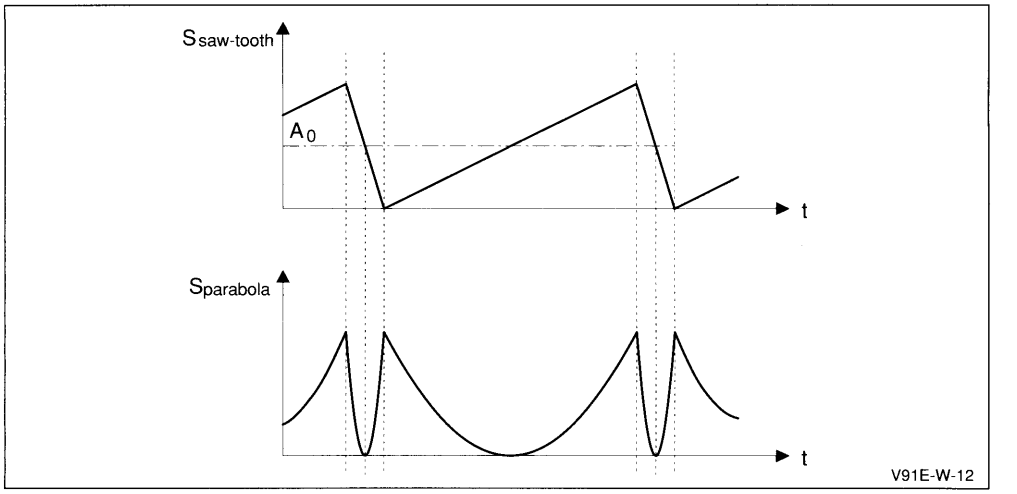
The functional network realization requires a quite larger amount of active components and is therefore especially suited for integrated circuits. The input signal for this kind of parabola generation is also the vertical saw-tooth signal corresponding to (1.15). With the aid of a functional (square) network, the square of this signal can be formed according to the following equation :

$$S_{parabola} = k\,(S_{saw\text{-}tooth} - S_0)^2 = k\,(A\frac{t}{T_V} - A_0)^2 \qquad (1.18)$$

and is illustrated in Figure 12.

Thereby, k is the gain and A_0 is a DC-level which allows to adjust the symmetry of the parabola ("trapezoidal" or "keystone" correction).

Figure 12 : Generation of the Parabola with Functional Network



Comparing the two methods, the following properties are evident :

- the parabola amplitude using the integration method is frequency dependent : assuming a constant amplitude of the saw-tooth signal, the amplitude of the parabola is linear in the time period T_V (see 1.16) . This means different adjustments between 50 and 60Hz TV-sets. The functional (square) method gives a frequency-independent amplitude of the parabola, if a constant saw-tooth signal is provided.
- during the flyback time of the saw-tooth signal, the functional network produces a second (parasitic) parabola as shown in Figure 12

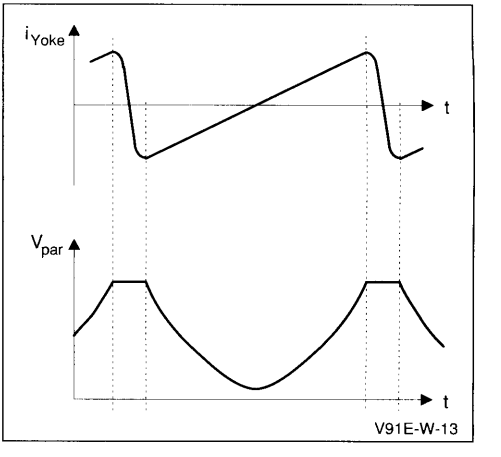
Although this parasitic parabola is present during the vertical flyback time (dark screen) this small parabola (like a spike) produces a damped oscillation of the diode modulator. The result is a damped sinusoidal vertical line on the top of the screen, if a test-grid is on the screen (the vertical lines are similar to a crutch-stick).

The maximum amplitude of this oscillation is present on the left and right top of the screen. Though its amplitude is normally only about 3mm, this effect must be suppressed.

This can be reached by two different methods :

- the linear saw-tooth voltage generating the parabola must have an extremely small flyback time. Then the very small parasitic parabola is integrated in the capacitor C_K of the comparator and has no effect (see Figure 7). The saw-tooth voltage coming from the vertical oscillator fulfills this requirement wherefore the deflection yoke-current has a too large flyback time.
- another possibility is to hold the parabola signal constant during the flyback time as illustrated in Figure 13.
  This behaviour can be reached by providing a parabola output limitation and then overmodulating the functional network during the flyback time.

Figure 13 : Modified parabola : constant during the flyback time



Overcoming the problems of the parasitic parabola, the functional method should be preferred due to the independence of the frequency (50/60Hz compatibility).

The nonlinearity which forms the parabola can be realized in two different ways :

- use of an analog multiplier
- forming a nonlinear network by piece wise linearization.

I.5 - ADJUSTMENTS

I.5.1 - Horizontal size adjustment

Adjustment of horizontal amplitude is made by modifying the mean cyclic ratio (duty factor) of the output pulses. When this mean cyclic ratio is minimum, the picture width is maximum, because the output is more frequently in the low state, and therefore the highest current is drawn from the diode modulator and the deflection current is maximum.

To change the mean cyclic ratio of the pulse train (in addition to the change due to the parabolic shape of the signal) it is necessary to change the continuous level of the sawtooth pulse train (see Figure 14).

The rise of the continous level of the parabola is due to the increase of the cyclic ratio, as we have seen above. The value of pincushion correction is not modified since the parabola peak-to-peak amplitude is kept the same. Only the mean cyclic ratio varies, i.e. also the horizontal scan width.

I.5.2 - Pincushion correction adjustment

Pincushion correction is made by varying the peak-to-peak amplitude of the parabola. The greater this amplitude,the greater the variation of the output signal cyclic ratio is between the ends and the top of the parabola, and therefore the more important is the parabolic modulation of the current drawn from the diode modulator (see Figure 15).

Figure 14 : Horizontal Size Adjustment

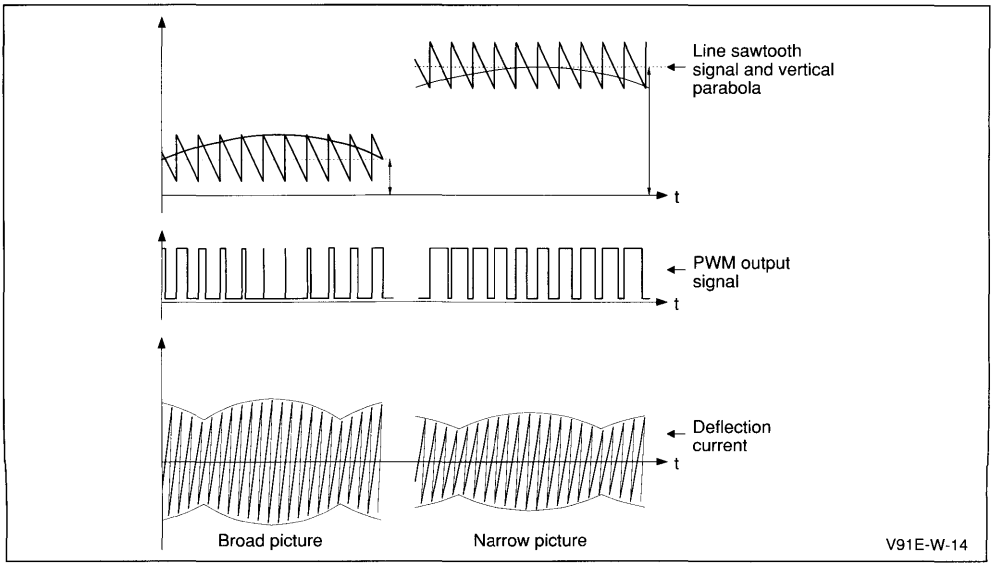
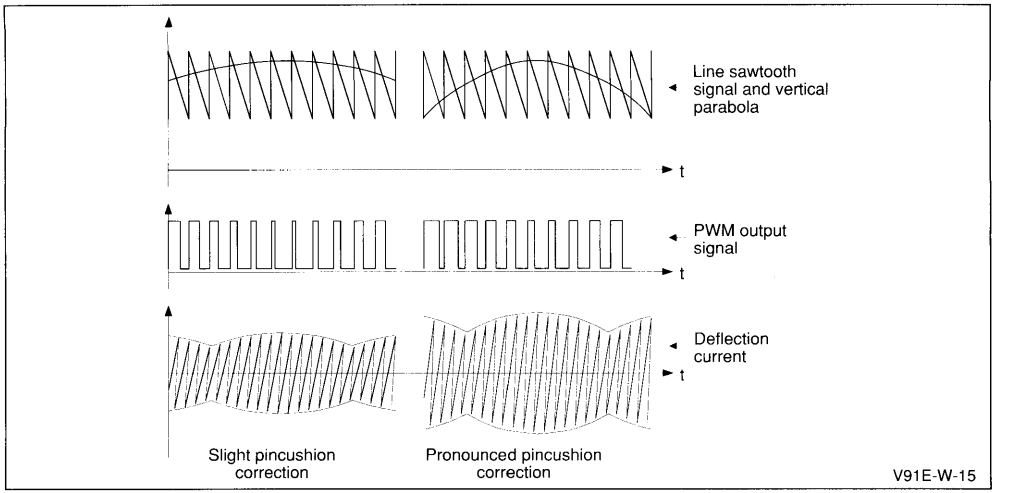


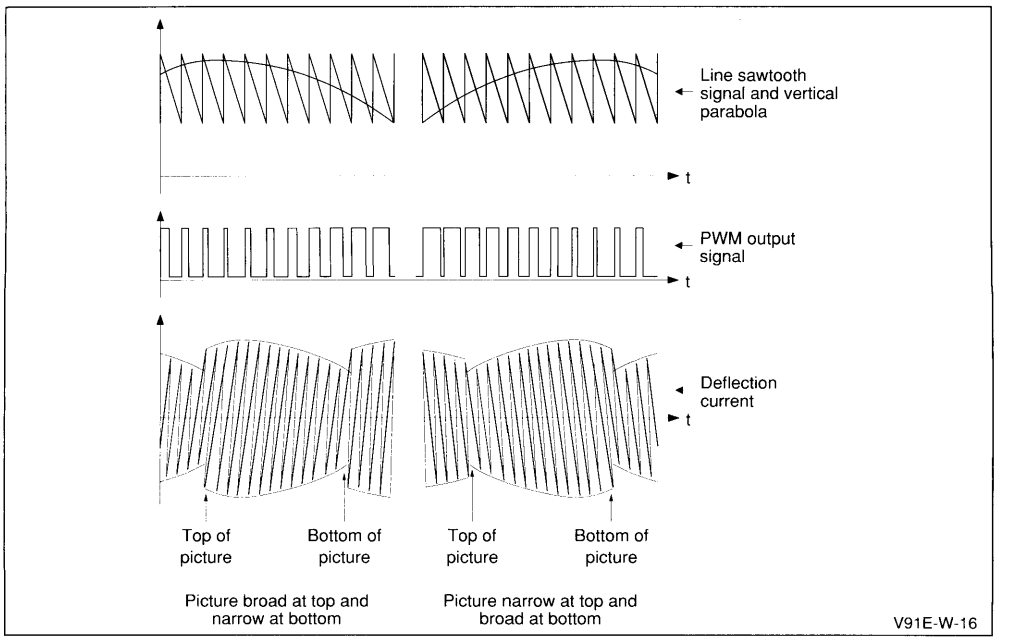
Figure 15 : Pincushion Correction Adjustment



I.5.3 - Trapezium correction adjustment (keystone correction)

Trapezium correction is made by modifying the symmetry of the left and right sides of the parabola (Figure 16).

Figure 16 : Keystone Correction



I.6 - PRODUCTS PRESENTATION

All the East/West correction devices are with class D diode modulator driver. Concerning the frame parabola generation, TDA4950, TDA8145 and TDA8146 use a non-linear network whereas TEA2031A uses an analog multiplier. TDA4950 and TDA8145 generate a parabola with a fixed shape; this shape is different between the two devices and makes the TDA4950 intended for standard CRT and TDA8145 for square tubes. These two devices have a parasitic parabola suppression (during vertical flyback time) by current limitation. TDA8146 has a programmable parabola shape generation by segments which makes it suitable for different CRTs. It has also a parasitic parabola suppression by pulse during vertical flyback.

All the devices can support a keystone correction adjustment (parabola symmetry) and have 50/60Hz capability. Some others adjustments are possible (picture width...).

Finally, another available device the TDA8147 has been designed for use in the East/West pincushion correction by driving a diode modulator but since this device has not the parabola generator and is drived by a PWM, it is very useful in digital TV-sets.

A detailed description about all the devices is done in the next chapters.

II - TEA2031A GENERAL DESCRIPTION

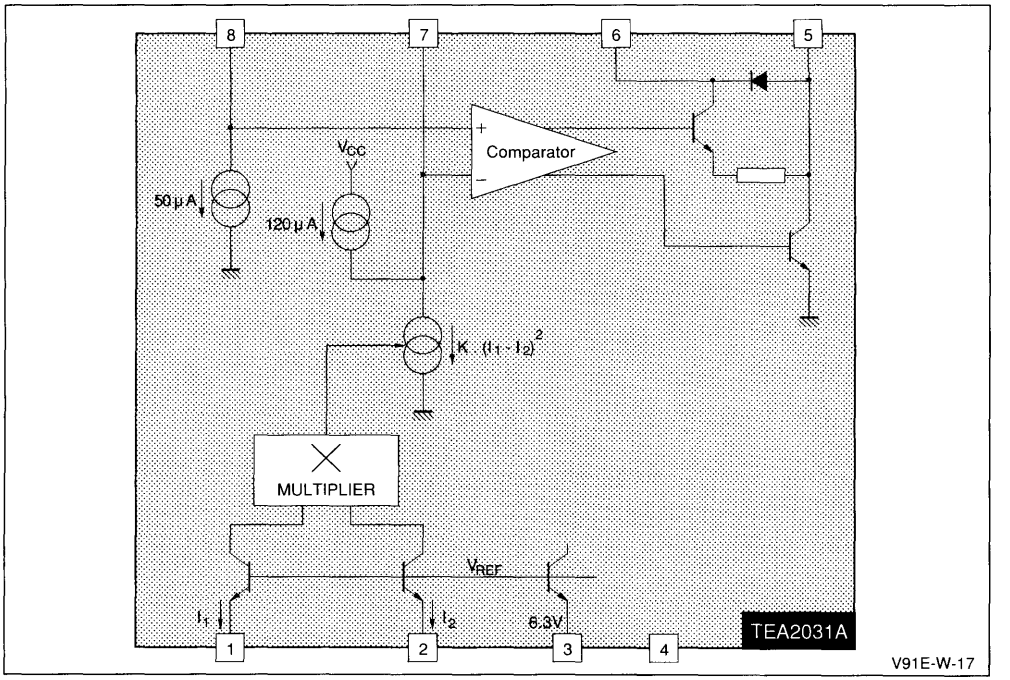
II.1 - INTRODUCTION

The TEA2031A circuit comprises (see Figure 17) : an analog multiplier that uses a frame sawtooth signal applied on Pin 1 so that the current on Pin 7 has a parabolic modulation.
This multiplier operates in current differential mode and uses a reference DC voltage, selected according to the continuous level of the sawtooth voltage, and applied on Pin 2.
The level of this DC voltage also serves to correct trapezium distortion.

- a reference voltage available on Pin 3 that can be used (via a voltage divider) to provide input 2 of the multiplier with a reference voltage.
- a current generator, producing a line frequency sawtooth signal by integrating the line flyback signal and generating current available on Pin 8.
- a comparator controlling the output stage by using the line sawtooth signal applied on its +input (Pin 8) and the parabolic signal generated by the multiplier and applied on its -input (Pin 7).

An output stage that can absorb or deliver current and comprises a diode connected to the DC voltage supply in order to limit the voltage applied on the output terminal during line flyback. This stage enables the diode modulator of the line scan circuit to be driven directly with a maximum current of 0.5A.
This maximum current that the output can absorb is not limited by the size of the transistors but by the maximum power dissipated by the package (Minidip).

Figure 17 : Block Diagram



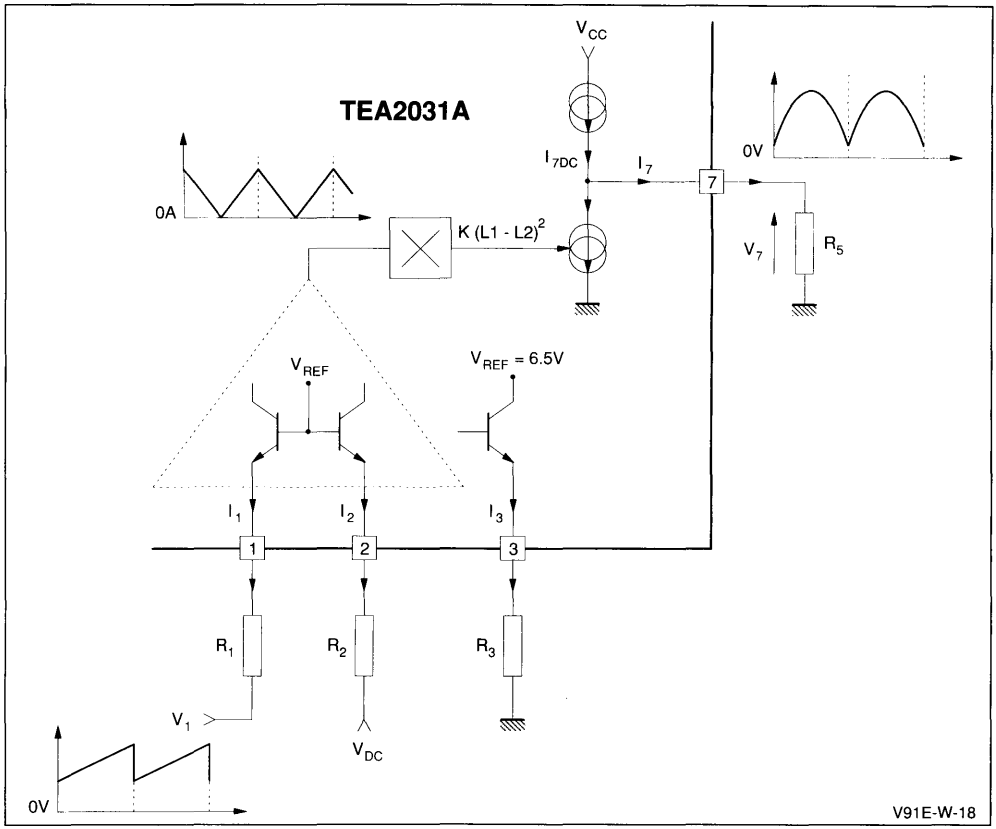
II.2 - PARABOLA GENERATION

Using a fixed continuous current and a vertical sawtooth current, the multiplier generates an output current on Pin 7 with parabolic modulation.

II.2.1 - Multiplier stage operation

The multiplier inputs (Pins 1 and 2) operate in current differential mode (Figure 18).

Figure 18 : Multiplier Stage



The output current is given by :

$$i_7 = i_{7DC} - k\,(i_1 - i_2)^2$$

i_{7DC} and k depend on the current reference on Pin 3.

Remarks : As we can see, the two inputs can be inverted and the slope of the sawtooth has no influence on the parabola shape.

II.2.1.a - Operation without keystone correction

In order to eliminate supply and thermal drift influences, R_1 is taken equal to R_2. In this case, $V_{1DC} = V_{2DC}$ (Figure 19).

II.2.1.b - Operation with keystone correction

In order to correct keystone correction, V_2 voltage becomes adjustable. In this case, the parabola shape presents a dissymmetry (Figure 20).

Figure 19 : Operation without Keystone Correction

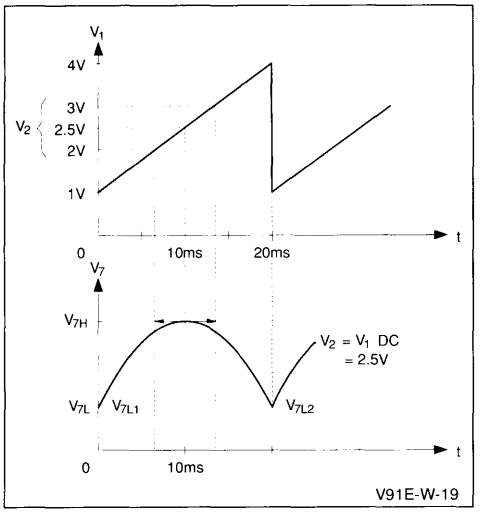
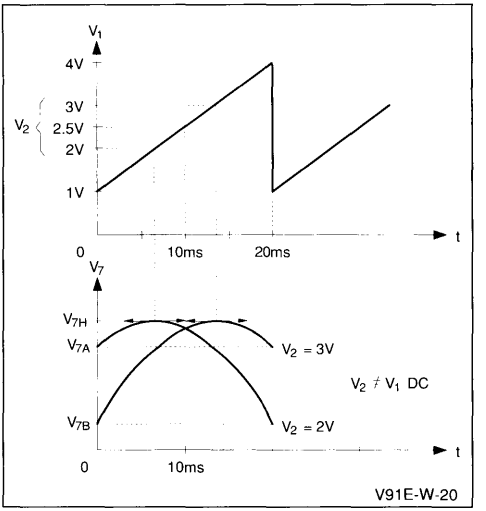


Figure 20 : Operation with Keystone Correction



II.2.1.c - Example of applications

1. Sawtooth coming from the horizontal:vertical processor (e.g. TDA8185, TEA2028B, ...)
   In this case, V_{1DC} = 2.5V (Figure 21).
   For practical reason, the DC voltage comes from internal voltage reference.Impedance value seen between Pin 3 and ground must be 22kΩ for best conditions of operation (to have the good internal current reference).
2. Sawtooth coming from the vertical output stage (Figure 22)
   In this caseV_{1DC} = 0V and $R1 = R2 + \frac{1}{2} RT2$

Figure 21 : Sawtooth coming from H/V Processor

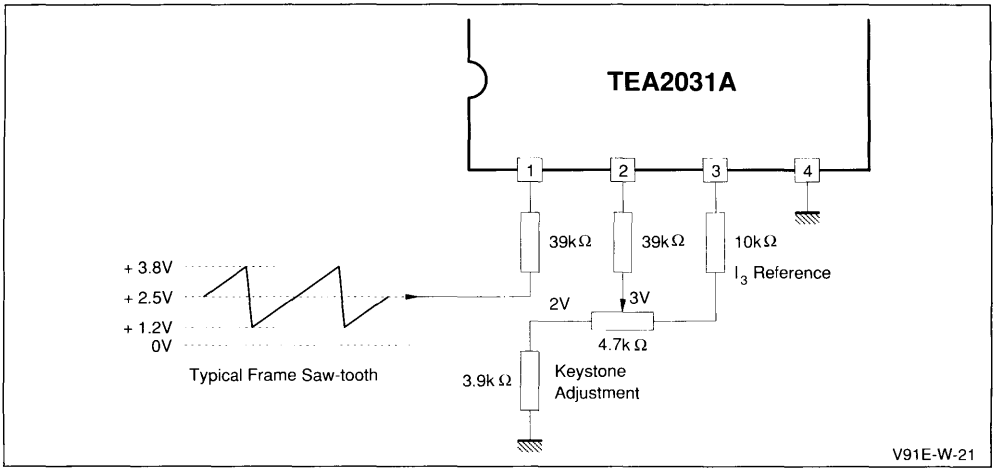
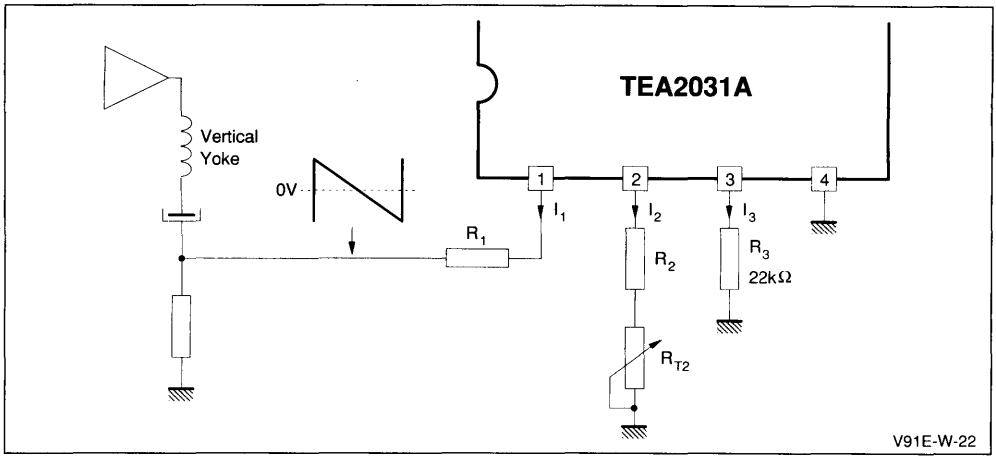


Figure 22 : Sawtooth coming from Vertical Output Stage



II.3 - LINE SAWTOOTH GENERATION

The line sawtooth signal is applied as a reference at the +input terminal of the comparator. It is obtained by integrating the line flyback and the constant current discharge of capacitor C3 in Pin 8 (Figure 23).

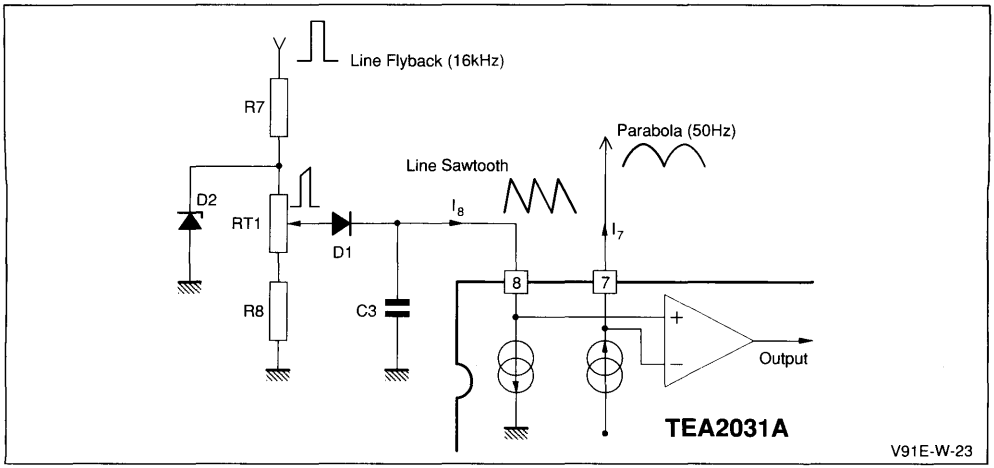
II.3.1 - Role of resistors R7, R8, RT1 and D2

By means of the voltage divider bridge comprising resistors R7, RT1 and R8, a signal that is the image of the line flyback signal applied on R7, is obtained on the slide contact of potentiometer RT1. The peak amplitude of this signal depends on the nominal voltage of the Zener diode D2 and on the adjustment of RT1.

The role of Zener diode D2 is to maintain a constant amplitude of the signal on the slide contact of RT1 whatever the variations in amplitude of the line flyback signal.

This diode D2 can be also replaced by a single diode connected to a regulated 12V or 15V power supply.

Figure 23 : Line Sawtooth Generation



II.3.2 - Role of diode D1 and capacitor C3

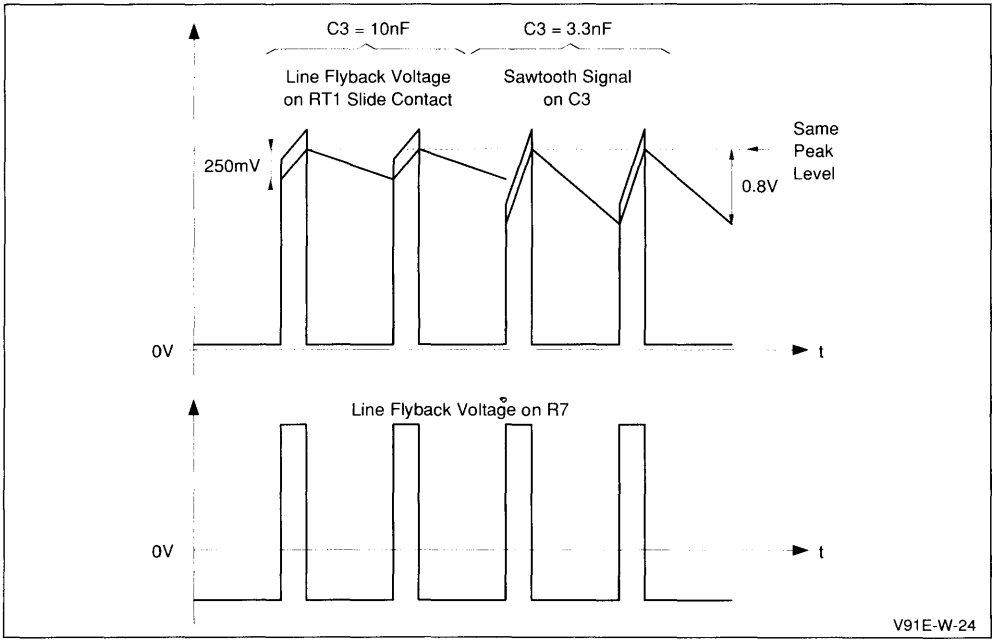
During *line flyback, diode D1 rapidly* charges capacitor C3 at the potential available on the slide contact of RT1.
Then during line scanning, D1 is blocked and C3 is discharged at constant current (about 50µA) through Pin 8.
The peak-to-peak amplitude of the line frequency sawtooth signal obtained in this way depends directly on the value of capacitor C3 since it is defined by the discharge current of the capacitor and the line period (Figure 24).

This amplitude can be calculated using the following equation :

$$V_{8\,(peak\text{-}to\text{-}peak)} = \frac{dt \cdot i_8}{C3}$$

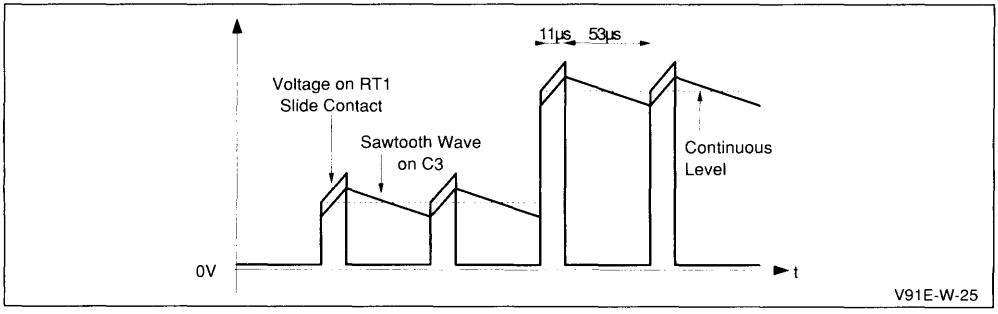
where Dt = duration of line and i_8 = current in Pin 8.

Figure 24 : Peak-to-peak Amplitude of Sawtooth Signal versus Two Different Values of C3 (with RT1 = constant)



The continuous level of this sawtooth signal is set by adjusting potentiometer RT1 (Figure 25).

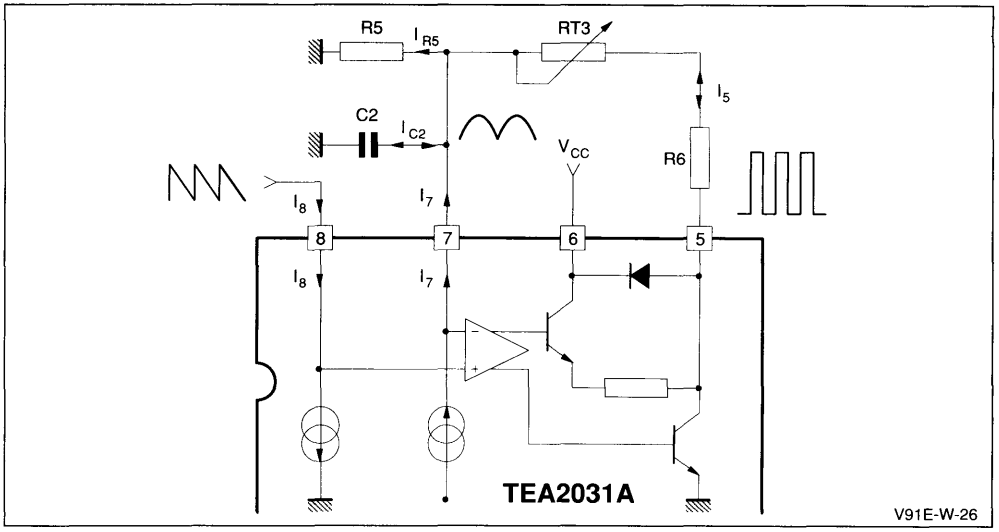
Figure 25 : Continuous Level of Sawtooth Signal for Two Different Adjustments of RT1



II.4 - OUTPUT STAGE

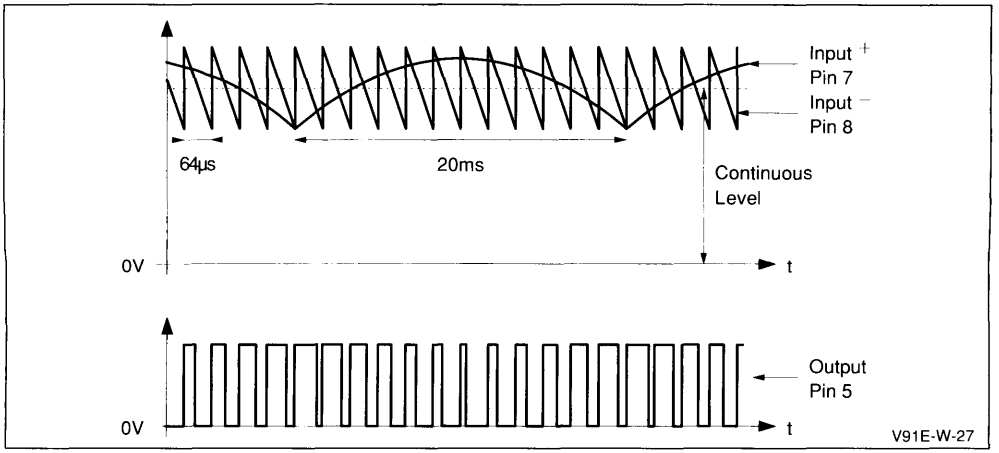
The output stage is controlled by the comparator fed by signals applied on its inputs, i.e. the sawtooth signal at line frequency on +input (Pin 8) and the parabola at vertical frequency on -input (Pin 7) (see Figure 26).

Figure 26 : Output Stage



The comparison between the 50Hz parabola and the sawtooth signal at line frequency (16kHz) produces pulses at line frequency with a duty cycle that is modulated at vertical frequency. This allows, by means of the diode modulator, the modulation of the line scanning current during each field period in order to carry out the pincushion correction (or East/West correction) (see Figure 27).

Figure 27 : PWM Output Signal (with adaptation of time scales)



The role of the filter C2 and RT3 + R6 is to suppress the line frequency of the feedback output signal.

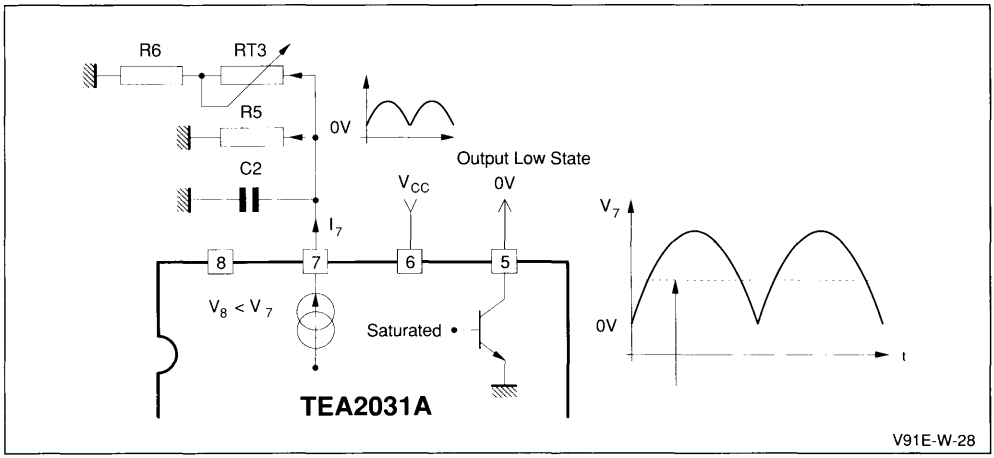
II.4.1 - Operation of the Output Stage

The operation of the output stage can be considered as 3 separate cases according to the 3 possible states of output Pin 5.

II.4.1.a - Output in the low state (Figure 28)

In this case resistances R6 and RT3 are connected to the ground, therefore they are in parallel with R5, according to the following diagram.

Figure 28 : Output in Low State



The continuous level and the peak-to-peak amplitude of the parabola are at their minimum when the RT3 value is minimum.

It is possible to calculate the voltage for a given point of the parabola (Pin 7) using the following equation :

$$V_{7b} = i_7 \cdot \frac{R5 \cdot (R6 + RT3)}{R5 + R6 + RT3}$$

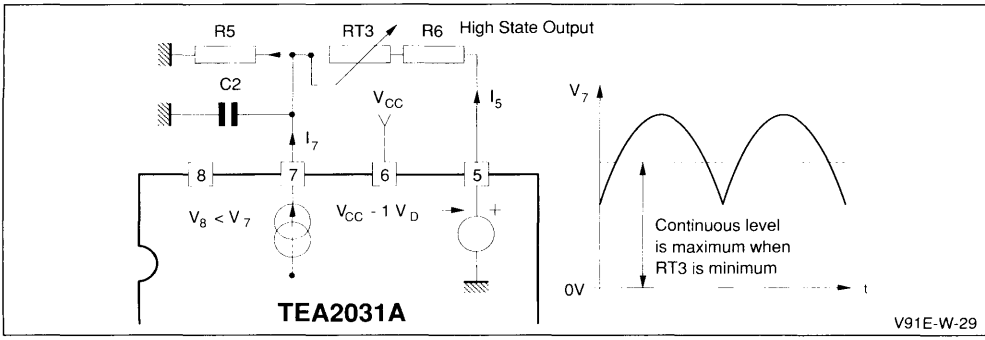
The capacitance of C2 is neglected as this capacitor is equivalent to an open-circuit at vertical frequency.

II.4.1.b - Output in the high state (Figure 29)

In this case, resistances R6, RT3 and R5 form a voltage divider bridge which returns on Pin 7 and capacitor C2 part of the continuous voltage available on the output terminal that is added to the parabola voltage.

The equivalent circuit diagram is the following :

Figure 29 : Output in High State



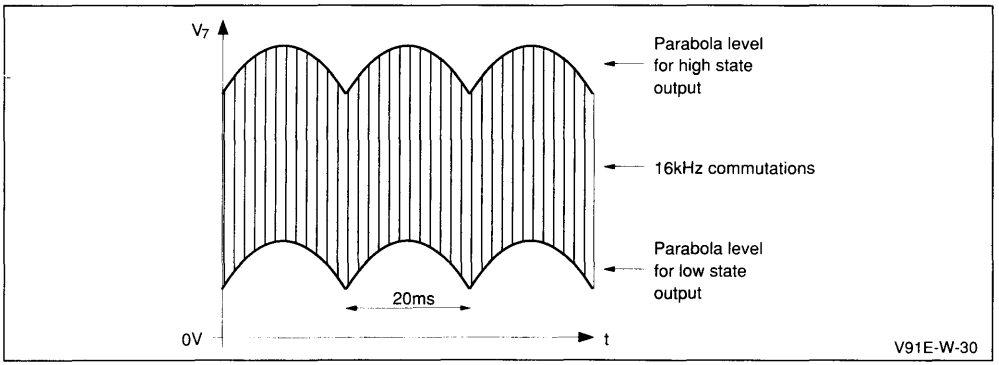
It is possible to calculate the voltage for a given point of the parabola (Pin 7) with the following equation :

$$V_{7h} = i_7 \cdot \frac{R5 \cdot (R6 + RT3)}{R5 + R6 + RT3} + V_5 \cdot \frac{R5}{R5 + R6 + RT3}$$

II.4.1.c - Output with commutation

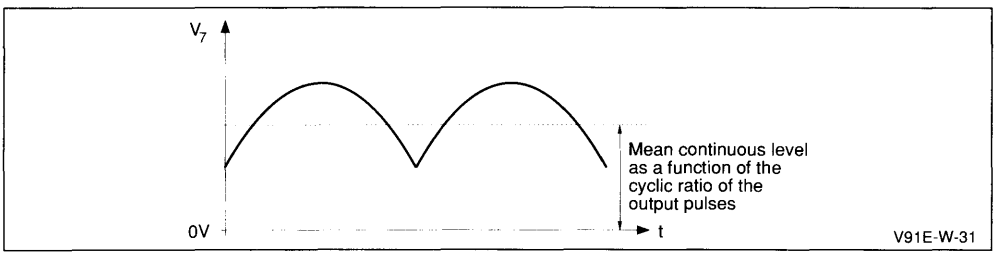
In this case and if capacitor C2 is eliminated, Figure 30 gives the signal obtained on Pin 7. It corresponds exactly to the levels and amplitudes of the parabolas for output in the high state and the low state, linked by 16kHz commutations.

Figure 30 : Output with Commutation (without C2)



In normal circuit configuration, capacitor C2 is connected and constitutes a filter with R6 and RT3. The preceding signal is filtered and is transformed into the signal shown in Figure 31.

Figure 31 : Output with Commutation (with C2)



The 16kHz line frequency component has disappeared in the signal and only the 50Hz parabola remains, but slightly modulated at line frequency by the C2 charge when the output is in the high state, and by the C2 discharge when the output is in the low state; this gives a tiny triangular modulation signal.

So the continuous level of the parabola depends only on the cyclic ratio of the output pulse train. This level can be calculated by means of the following equation : $V_{mean} = M \cdot V_{7h} + (1 - M) \cdot V_{7b}$

where

M : output pulse cyclic ratio

V_{7h} : mean level on Pin 7, output blocked in the high state

V_{7l} : mean level on Pin 7, output blocked in the low state

We see that, when the cyclic ratio increases, the continuous level of the parabola also increases and approaches its maximum level when the output is in the high state. Conversely, when the cyclic ratio decreases, the continuous level of the parabola also decreases since it approaches its minimum continuous level when the output is in the low state.

II.4.1.d - Conclusion

For a given parabolic current i_7, the parabola peak-to-peak amplitude depends only on resistance values R5,R6 and RT3. Therefore by adjusting RT3, it is possible to obtain a more or less pronounced parabola and so adjust the importance of pincushion correction.

The continuous level of the parabola depends principally on the mean cyclic ratio at the output, and much less on the adjustment of RT3.

II.4.2 - Operation in association with the diode modulator

In the majority of cases, the system operates by drawing more or less high current from the modulator through the connecting inductor. The current through terminal Pin 5 of TEA2031A is entering into the circuit. It flows, either to the ground when the output is in the low state, or to V_{CC} through the internal diode when the output is in the high state and the output voltage tends to exceed V_{CC}. The circuit can also produce current.

Figure 32 : Operation with Diode Modulator

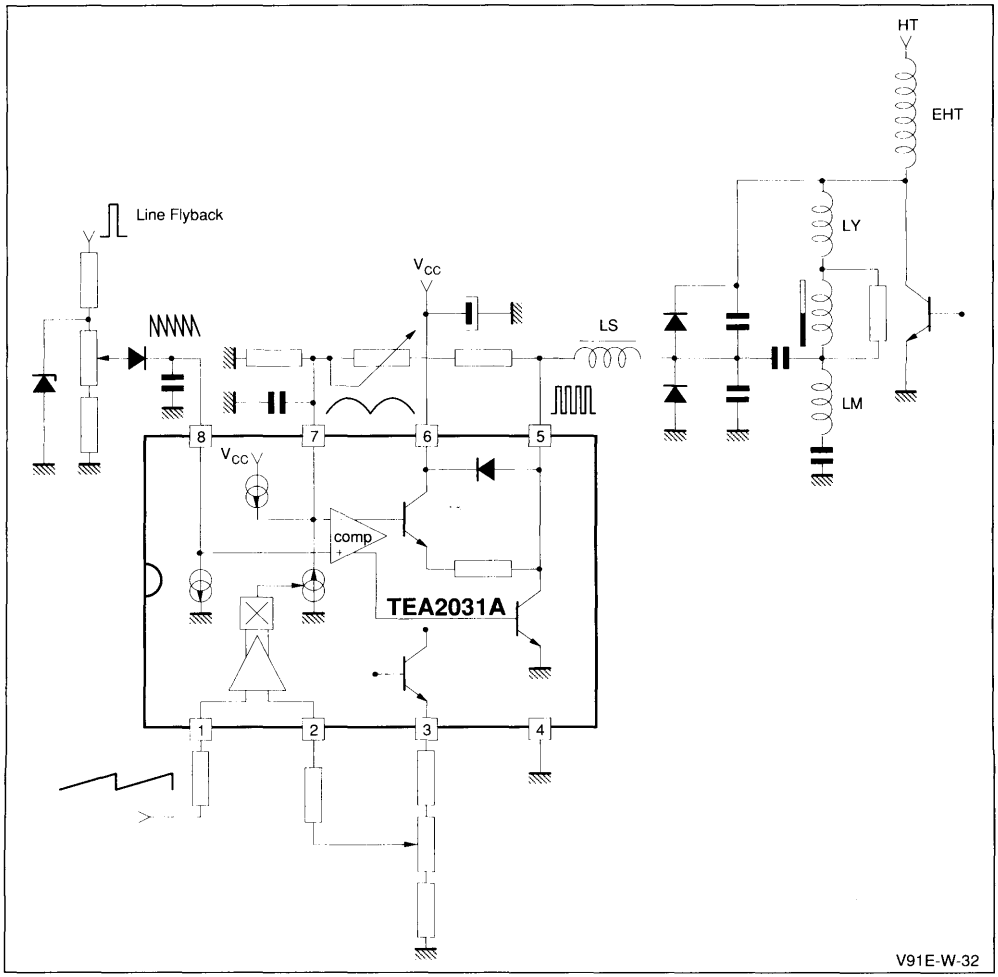
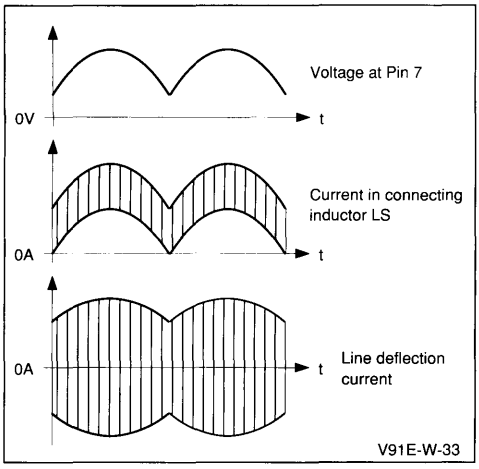


Figure 33 : Output Oscillagrams



II.5 - SELECTION OF THE VALUES OF CAPACITORS C2 AND C3

Correct operation of TEA2031A depends partly on the choice of these values for two reasons :

- for a given amplitude of the parabola, the importance of final pincushion correction at the output of TEA2031A is determined by defining, by means of C3, the amplitude of the line sawtooth wave.
- the absence of oscillation at circuit output is controlled through adjustment of the value of C2 as described below.

II.5.1 - Selection of C3

As seen before (chapter II.3.2), the value of C3 and only this value (in the limits of the available voltage on the slider of RT1) can fix the value for the amplitude of the line sawtooth wave. Now this amplitude must be greater than the parabola amplitude (Pin 7) but not so far in order to have a correction amplitude sufficient but permitting also an horizontal amplitude adjustment :

- if the line sawtooth wave and the parabola have the same amplitude, the pincushion correction is maximum but the horizontal amplitude adjustment range is non-exutent
- if the line sawtooth amplitude is much greater than the parabola's one, we will have a large range for the horizontal amplitude adjustment, but it will be to the detriment of the pincushion correction amplitude.

Once the desired line sawtooth amplitude has been fixed, we can calculate the value of C3 with the following formula

$$C3 = \frac{Dt \cdot i_8}{V_8}$$

where

Dt : line scan duration (around 53µs)

i_8 : Pin 8 current (around 50µA)

V_8 : line sawtooth peak-to-peak amplitude (Pin 8)

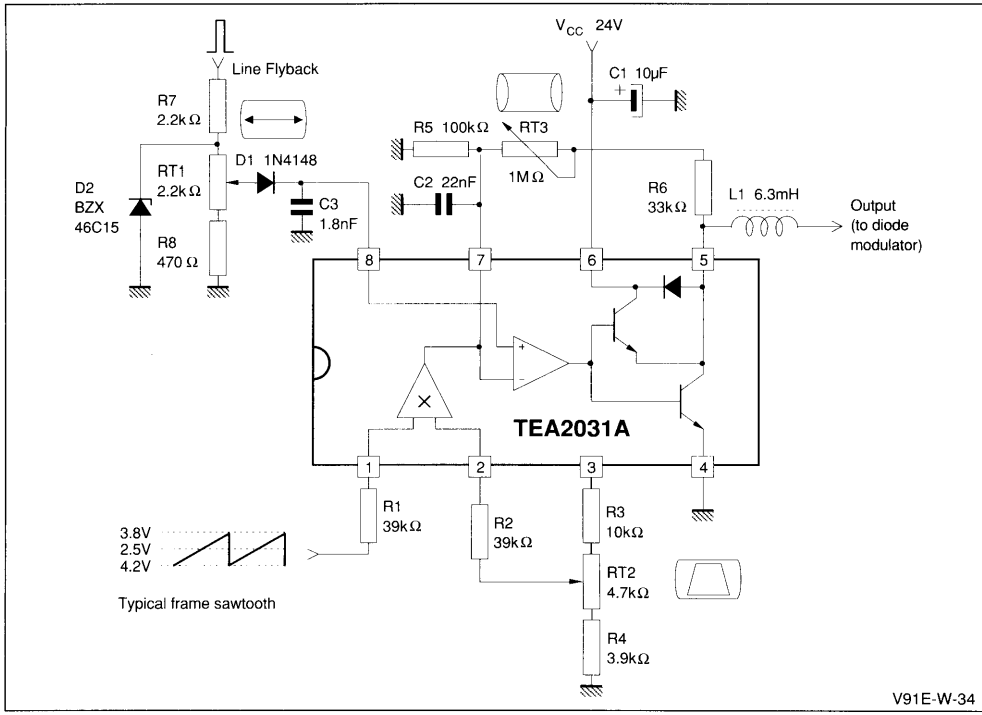
II.5.2 - Selection of C2

The selection of C2 is related to the values of R5, R6 and RT3. The value of C2 must be large enough to avoid any risk of oscillations at output for the entire range of adjustment of potentiometers RT1 and RT3. The value of C2 must be small enough not to influence the shape of the vertical frequency parabola.

II.6 - APPLICATION EXAMPLE

A typical application diagram is given in Figure 34.

Figure 34 : Typical Application



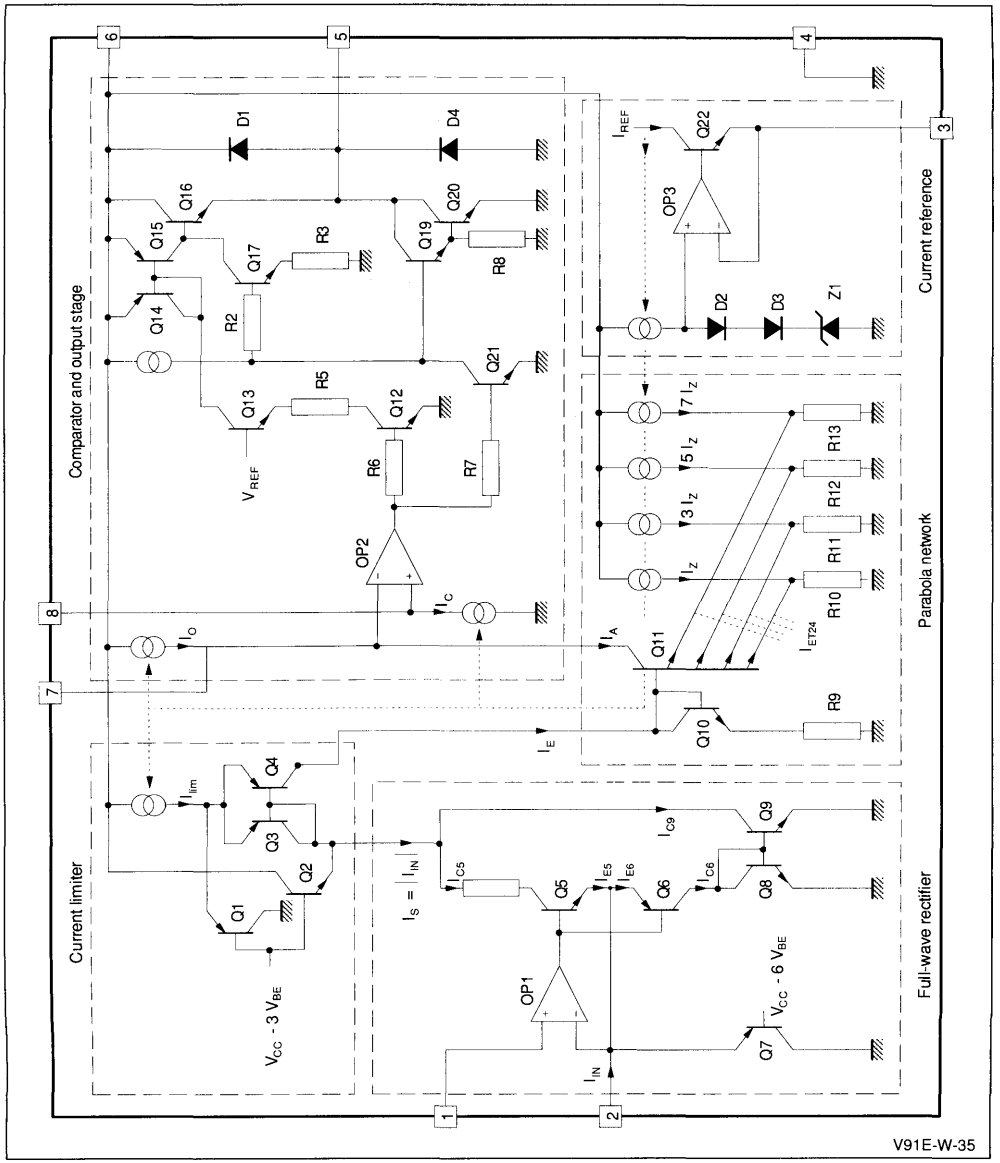
III - TDA4950 - TDA8145 GENERAL DESCRIPTION

III.1 - INTRODUCTION

The TDA4950 and TDA8145 consist mainly of 5 parts as seen in the simplified circuit diagram (Figure 35).

1. Full-wave rectifier for the input current I_{IN}.
2. Current limiter in order to limit the rectified current I_{IN} to the maximum value of 40µA (with this functional block a suppression of the parasitic parabola is possible, see chapter I.4).
3. Parabola network producing the current $I_A = k(I_{IN})^2$ (k = constant).
4. Comparator and output stage working as a pulse-width modulator for driving the diode modulator.
5. Voltage reference and current reference which produces the reference current I_{REF} via external resistor RI between Pin 3 and Ground.

Figure 35 : Simplified Circuit Diagram for TDA4950 - TDA8145



III.2 - DESCRIPTION

Let us consider the blocks in detail :
The input amplifier OP1 drives the transistor Q5 or Q6. They offer two different signal paths, depending on the sign of the input current I_{IN}.

Assuming that I_{IN} is negative, the feedback loop is closed via the transistor Q5 and the output current I_{C5} is given by

$$I_{C5} = I_{E5}\left(\frac{\beta_5}{1+\beta_5}\right) = -I_{IN}\left(\frac{\beta_5}{1+\beta_5}\right)$$

where β_5 is the current gain of the transistor Q5. β_5 can be assumed to be more than 100, so the mismatching between I_{C5} and I_{IN} is less than 1%.

For a positive current I_{IN} the output voltage of OP1 decreases : Q5 is switched off the current I_{IN} is the emitter current I_{E13} of Q6.

Its collector current I_{C6} is given by

$$I_{C6} = I_{IN}\left(\frac{\beta_6}{1+\beta_6}\right)$$

Since the maximum input current is 40µA, the current gain of this PNP transistor is still high enough to give a reasonable small error. This current biases the current mirror Q8 and Q9. A good matching between the current I_{C8} and I_{C9} must be provided. Thus the current I_S is given by

$$I_S = \begin{cases} -I_{IN}\left(\frac{\beta_5}{1+\beta_5}\right) & I_{IN} < 0 \\ +I_{IN}\left(\frac{\beta_6}{1+\beta_6}\right) & I_{IN} > 0 \end{cases}$$

Neglecting the base current of Q6 and Q5, I_S is nearly the absolute value of I_{IN}.

Note that for both signal paths, the OP1 has a feedback factor of 1. This means OP1 must be frequency compensated for unity gain.

The transistors Q3 and Q4 work as a normal current mirror if the current I_S plus I_E is smaller than the current I_{lim} :

$$2\,I_S < I_{lim}$$

In this case the excess current is shunted via the PNP transistor Q1.

If the current I_S becomes higher

$$I_S > I_{lim}/2$$

the transistor Q1 switches off and Q2 picks up the current I_S from the rectifier which exceeds the maximum value of $I_{lim}/2$.

Using the proposed reference resistor RI between Pin 3 and Ground (11kΩ) the current I_E can be described with

$$I_E = \begin{cases} I_{IN} & I_{IN} < 40\mu A \\ 40\mu A & I_{IN} > 40\mu A \end{cases}$$

The parabola network produces an output current I_A which is approximately a parabola : $I_A = k\,I_E^2$

The parabolic behaviour I_A is obtained via piecewise linear approximation. For this purpose the identical resistors R_Z are connected with the four emitters. The four different biasing currents i_Z, $3i_Z$, $5i_Z$, $7i_Z$ yield four different threshold voltages, so the four emitter currents of Q11 are switched stepwise. A schematic illustration of the single emitter currents I_{EQ11} (1...4) of Q11 as a function of the current I_E is given in Figure 36.

Due to the exponential character of the emitter current as a function of the base emitter voltage, the output current I_A is smoothed.

For designing the values of R_Z and i_Z of this parabola network we must take a compromise between the smoothing effect and the temperature dependence. Small values of R_Z and i_Z yield small threshold voltages for the 4 emitters of Q11. This means a good smoothing of the edges, but a worse temperature dependence.

Large values of R_Z and i_Z yield the opposite result. Practical experiences show that a value of 0.5V for the 4th emitter (R13 $7i_Z$) for I_{IN}= 0 gives an acceptable cmpromise.

Due to different values of resistor R_Z, the TDA8145 is adapted to flat square tubes (see Figure 37 for the two different shapes of the parabola).

Figure 36 : Transfer Characteristic of the Parabola Network

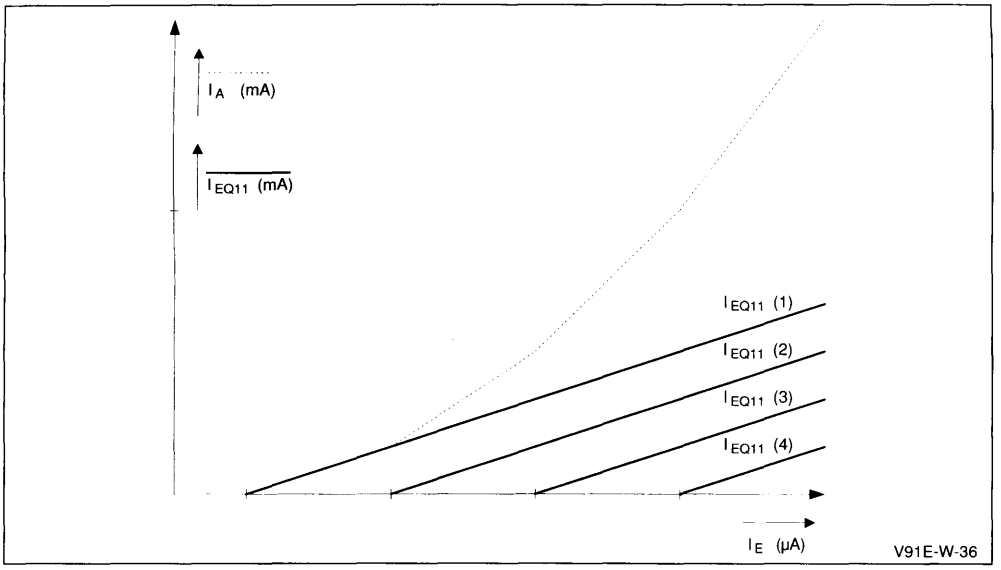
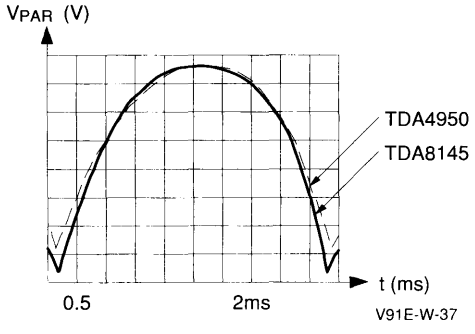


Figure 37 : Parabola Shapes for TDA4950 and TDA8145



The parabolic output current I_A produces a corresponding voltage drop across an external resistor between Pin 7 and Ground (18kΩ). The additional constant current source I_0 shifts the D.C. voltage level to achieve an appropriate operating point of the comparator. Its non-inverting input is connected with a horizontal saw-tooth voltage. For this purpose an external capacitor is connected with Pin 8 and Ground which is discharged with the internal current source I_C. It will be charged with the positive flyback pulses produced in the line transformer during the flyback time.

Due to the linear saw-tooth voltage on Pin 8 this comparator works as a pulse-width modulator.
The output of this comparator controls the output stage. If the output of the comparator OP2 is high, Q21 and Q12 are saturated. Therefore, the Darlington output transistor Q19, Q20 is switched off. The transistor Q13 and the resistor R5 acts as a current source biasing the current mirror Q14, Q15. The transistor Q16 is switched on.

If the output of OP2 becomes low, Q12 and Q21 are switched off. In this case the current in Q14 and Q15 dissappears and Q16 is switched off. Synchronously the darlington stage Q19 and Q20 is saturated.

In order to achieve a fast commutation from Q16 to Q19/Q20 an active discharging of Q16 is provided with the aid of the transistor Q17.
During a normal operation range if the output current i_{OUT} is positive, only the Darlington stage (Q19, Q20) and the diode D1 are necessary to drive the external inductor. With the aid of Q16 and the intrinsic substrate diode D4 the output current i_{OUT} can become negative, too; so that the modulation range of the diode modulator becomes larger.

The Zener diode Z1 serves as the voltage reference. With the aid of the diodes D2 and D3, a good temperature compensation can be achieved.
Using an external resistor of R_I = 11kΩ between Pin 3 and Ground we get an accurate and temperature independent current reference to bias the internal current sources.

III.3 - APPLICATION

A standard application diagram is given in Figure 39.
Pin 2 is biased from a linear saw-tooth voltage, the resistor R_{IN} produces the input saw-tooth current. The non-inverting input (Pin 1) is connected with an adjustable voltage (keystone correction). With the aid of this trimmer, the symmetry of the parabola can be adjusted in order to correct a trapezoidal error in the colour picture tube. A further adjustment trimmer is responsible for the picture width and influences only the DC-level of the comparator input (Pin 8). (Since the discharging current sink on Pin 8 is constant, the amplitude of the horizontal saw-tooth voltage (V_{PP}) remains constant).

The thrid trimmer is in the feedback path and is responsible for the parabola correction factor. With the aid of this trimmer the distortion on the screen can be changed from pillow-distortion up to an over-correction (tun-distorsion).

For some applications the keystone adjustment trimmer is not necessary (small trapezoidal error of the picture tube). In this case, a symmetric parabola should be produced.

This can easily be obtained by AC-coupling the input (Pin 2) as seen in Figure 38.

Figure 38 : AC-coupled Vertical Saw-tooth Voltage, no Keystone (trapezoidal) Correction

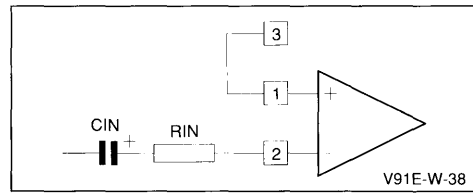
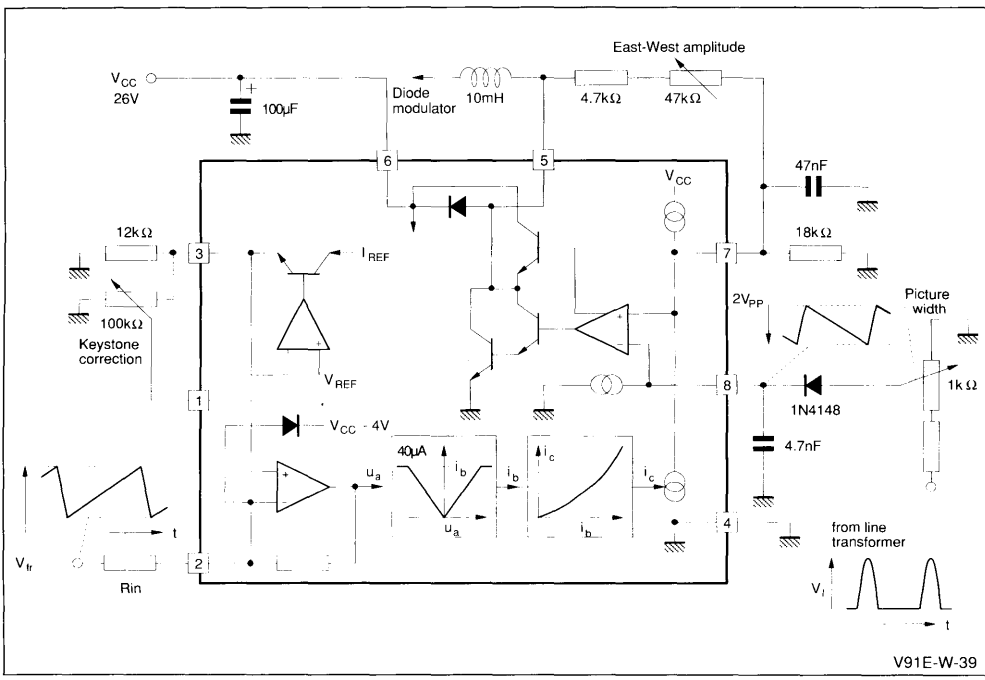


Figure 39 : Standard Application Diagram of TDA4950 and TDA8145



In order to avoid any distorsion, the time constant $C_{IN} \cdot R_{IN}$ should be at least 10 times larger than the time period ($C_{IN} \cdot R_{IN} > 10 \cdot 20ms$). On the other hand a too large time constant yields an undesired bouncing effect in the East/West correction.
The DC voltage on Pin 1 is arbitrary.
For the sake of simplicity, connect Pin 1 with Pin 3. Another possible application with parasitic parabola suppression is given in Figure 40.

The input current into Pin 2 is generated via the voltage drop on R_M. Due to the common mode rejection of the input operational amplifier, the voltage change during the vertical scan time (sawtooth voltage) has nearly no effect. During the flyback time, a positive pulse (> V_{CC}) is present on Pin 1 and Pin 2. With this flyback pulse the current limitation in the parabola generation circuit is activated and limits the parabola amplitude. Since the flyback time is relatively long, this limitation is necessary to suppress the parasitic parabola (see chapter I.4).

IV - TDA8146 GENERAL DESCRIPTION

IV.1 - INTRODUCTION

The TDA8146 was designed for TV and monitor sets with various types of picture tubes, where a programmable parabola is mandatory. The complete block diagram is shown in Figure 41.

The following features confer to this IC an all-purpose suitability :

- programmable parabolic current generator
- parasitic parabola suppression during vertical flyback
- output sink current up to 800mA and source current up to 100mA
- vertical current sense inputs ground compatible

Figure 40 : Application of TDA4950 and TDA8145 with Parasitic Parabola Suppression

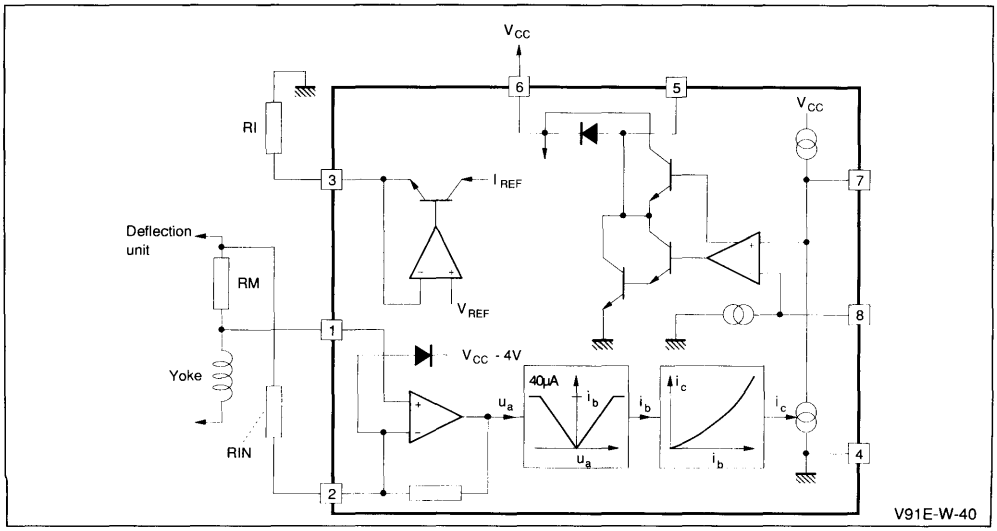
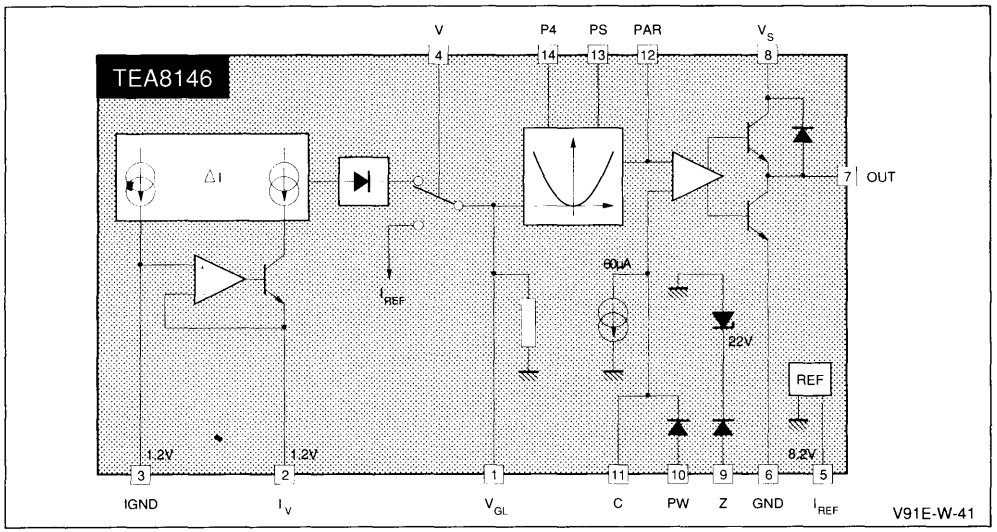


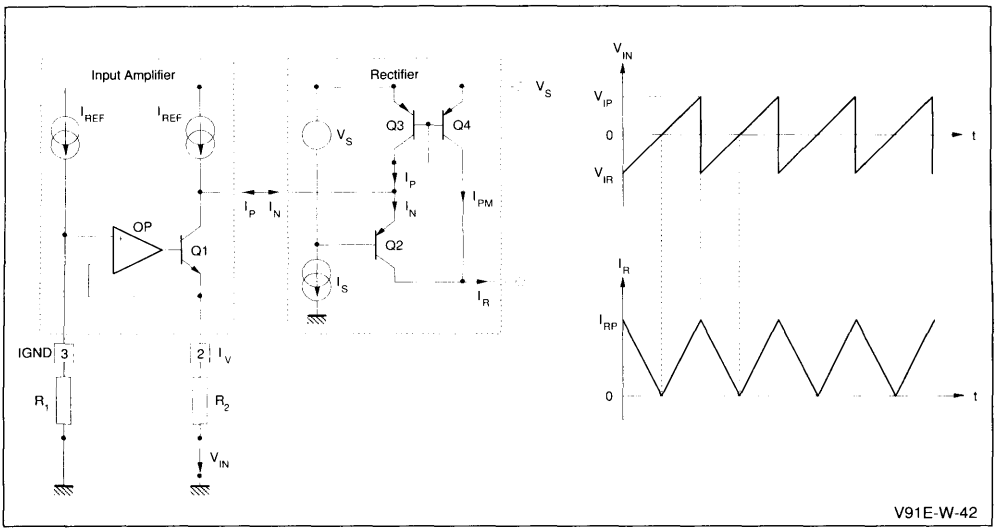
Figure 41 : Block Diagram



IV.2 - INPUT AMPLIFIER AND RECTIFIER

The input circuitry (Figure 42) is designed for a common mode range up to 12V.

Figure 42 : Input and Rectifier Principle Diagram



The voltage drop on R1 gives on I_{GND} (Pin 3) : $V_{R1} = R1 \cdot I_{REF}$

The operational amplifier OP regulates the current through R2, thus :

$I_{R2} = (V_{R1} - V_{IN}) / R2 = (R1 \cdot I_{REF} - V_{IN}) / R2$

For $V_{IN} > 0$, we note the output current of the input amplifier I_N :

$$I_N = I_{REF} - I_{R2} = I_{REF} - (R1 \cdot I_{REF} - V_{IN}) / R2$$

For $V_{IN} < 0$, we note the output current of the input amplifier I_P :

$$I_P = I_{R2} - I_{REF} = (R1 \cdot I_{REF} - V_{IN}) / R2 - I_{REF}$$

The rectifier is formed by Q2, Q3 and Q4. For $V_{IN} > 0$, I_N flows through Q2 to the rectifier output, thus $I_R = I_N$.
For $V_{IN} < 0$, I_P flows through Q3 from V_S into the output of the input amplifier. Q4 reflects the I_P current, thus the rectifier output currrent will be $I_R = I_{PM} = I_P$.

If the sign convention of I_R is considered, we have :

$$I_R = \left| \frac{(R1 \cdot I_{REF} - V_{IN})}{R} - I_{REF} \right| = \left| I_{REF} \left(\frac{R1}{R2} - 1 \right) + \frac{V_{IN}}{R2} \right|$$

In our case, R1 = R2 = 10kΩ and $I_{REF} = 120\mu A$

Thus, $I_R = \left| \frac{V_{IN}}{R2} \right|$

If V_{IN} is a symmetrical saw-tooth with GND as the average value and 1.6 $V_{peak\text{-}to\text{-}peak}$, the rectified peak current will be :

$$I_{RP} = \frac{0.8}{10 \cdot 10^{-3}} = 80\mu A$$

IV.3 - VERTICAL CLAMPING

To avoid the parasitic parabola during the vertical flyback time a vertical clamp circuit was used.

The vertical clamping principle is presented in Figure 43.

The rectified sawtooth current I_R Flows through D2 to the output.

When V goes over V_S, Q1 switches off and Q2 on. I_{REF} flows now through D1 to the output and I_R through Q2 to the ground. $I_{RC} = I_{REF}$ is now the clamped value of the output current.

IV.4 - REFERENCE AND STARTING CIRCUIT

Figure 44 presents the complete voltage and current reference circuitry.

The reference current is $I_{REF} = \frac{8.2V}{100k\Omega} = 82\mu A$

To guarantee the start of the device, it is necessary to choose the value of the resistor R5 in order to have a minimum current of 56μA.

Figure 43 : Vertical Clamping Principle Diagram

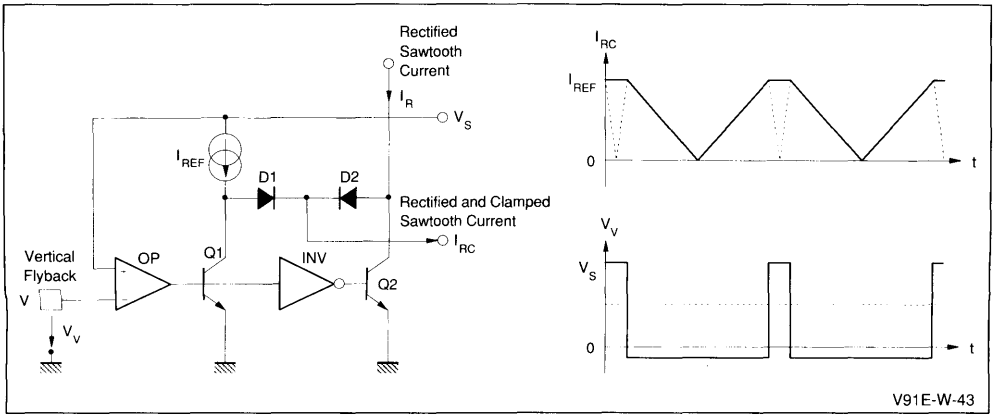
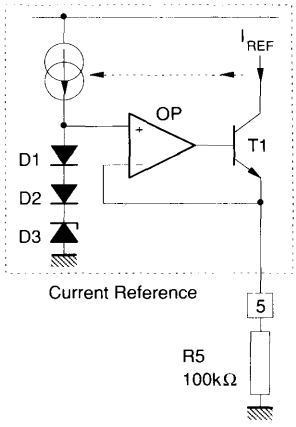


Figure 44 : Reference and Starting Circuit



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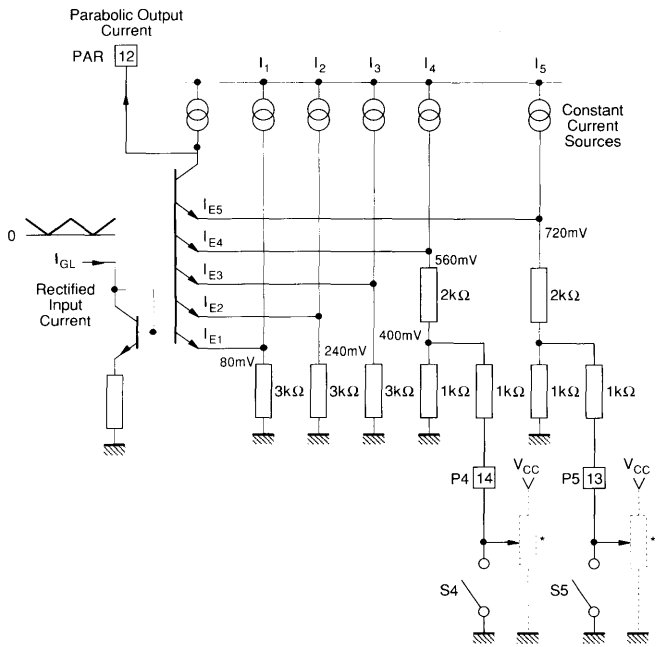
IV.5 - PARABOLA GENERATOR

Figure 45 presents the simplified circuit diagram of the parabola generator.

Figure 45 : Parabola Generation



Note : * It is possible to replace the switches S4 and S5 by this configuration in order to have a continuous shape variations.

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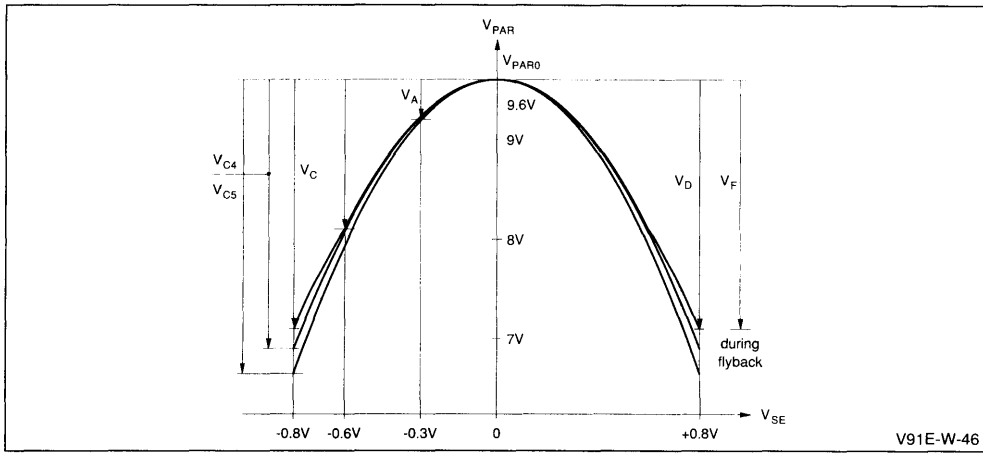
The parabolic behaviour of the parabola output current is obtained via piecewise linear approximation.
Two external pins permit an external adjustment of the parabola shape (these pins can be connected to ground or to resistors).

The parabolic output current on Pin 12 Produces a corresponding voltage drop across an external resistor between Pin 12 and ground.

As it can be seen in Figure 46 the parabola can be corrected in the following limits :

$V_{C5}/V_C = K5 = 1.07$ with Pin 5 to GND
$V_{C4}/V_C = K4 = 1.17$ with Pins 4 and 5 to GND

Figure 46 : Parabola Correction

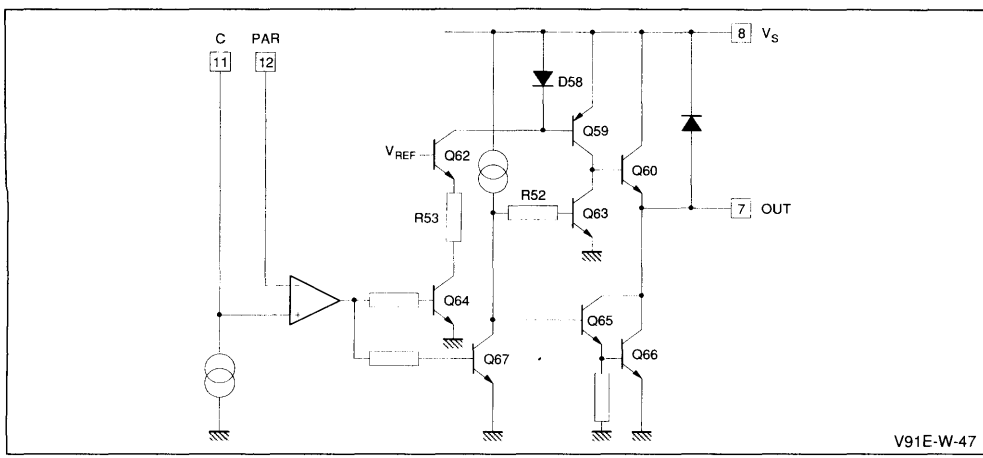


An application specific correction can be thus obtained for various picture tube types.

IV.6 - PULSE-WIDTH MODULATOR AND OUTPUT

The simplified diagram of the pulse-width modulator and output is presented in Figure 47.

Figure 47 : Pulse-width Modulator and Output



The non-inverting input of the comparator (Pin 11) is connected to a horizontal saw-tooth voltage. An external capacitor connected on Pin 11 is charged during the flyback time and then discharged by the internal current source generating the saw-tooth voltage.

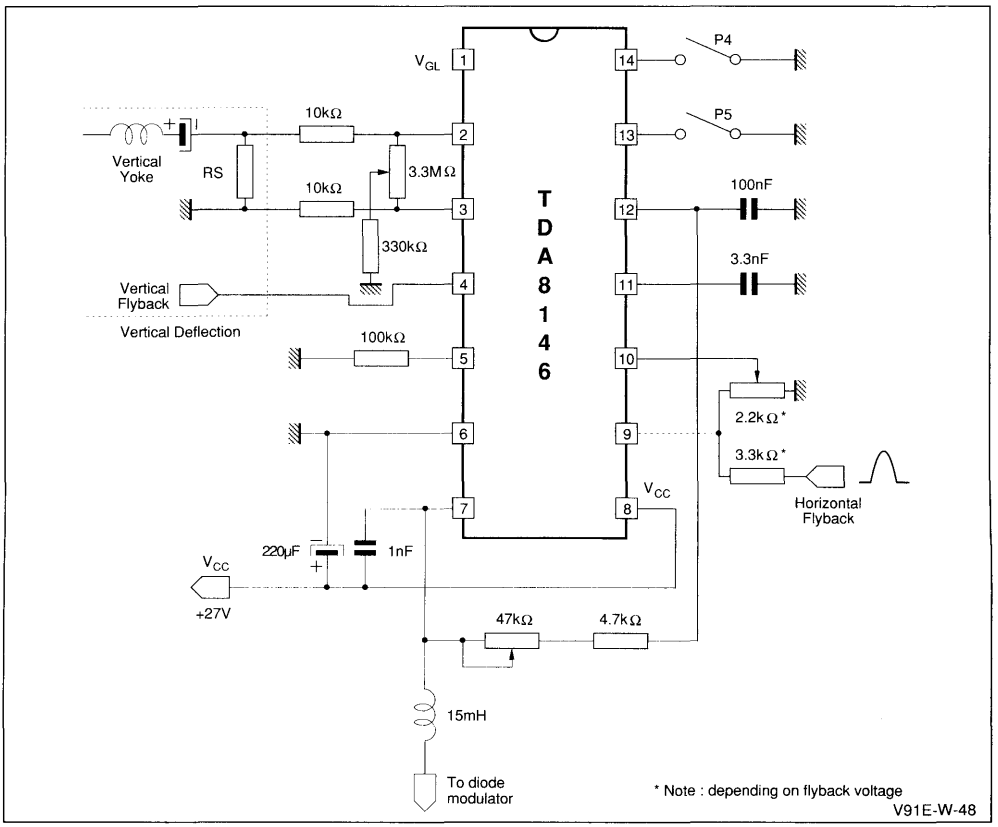
Due to the linear saw-tooth voltage on Pin 11, the comparator works as a pulse-width modulator. The output of this comparator controls the output stage. If the output of the comparator is high, Q67 and Q64 are saturated. The Darlington output configuration Q65/Q66 is switched off. Q62 acts together with R53 as a current source, biasing the current mirror Q58/Q59. The transistor Q60 is switched on.

If the output of the comparator becomes low, Q64 and Q67 are switched off. The current through D58/Q59 disappears and Q60 is switched off. Synchronously the Darlington stage Q65/Q66 is saturated. In order to achieve a fast commutation, an active discharging of the Q60 base charge is provided with the aid of Q63.

IV.7 - APPLICATION

An application diagram is presented in Figure 48. The internal Zener configuration on Pin 9 can be useful in certain application.

Figure 48 : Application Diagram

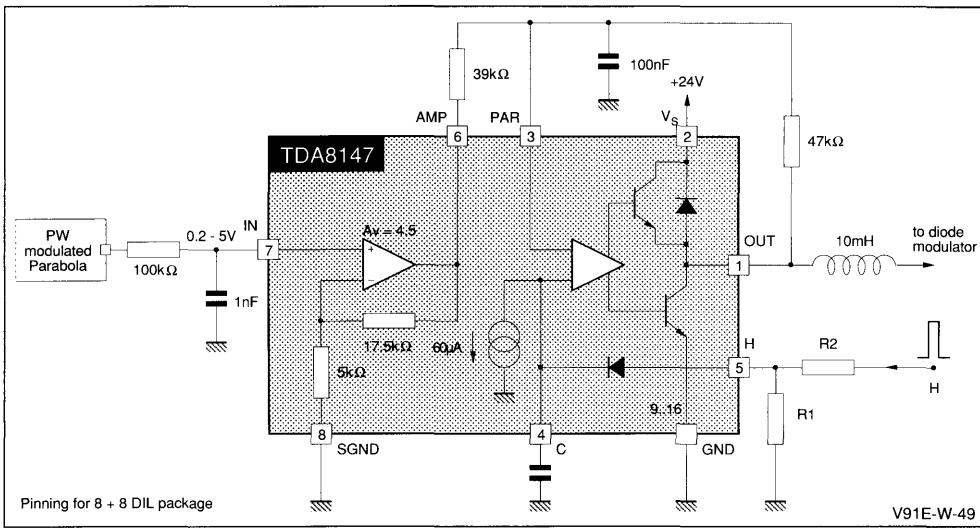


V - TDA8147 GENERAL DESCRIPTION

V.1 - INTRODUCTION

The TDA8147 was designed as an interface IC between the digital circuitry and the diode modulator in digital chassis. The complete block diagram is shown in Figure 49.

Figure 49 : TDA8147 Block Diagram



V.2 - INPUT AMPLIFIER

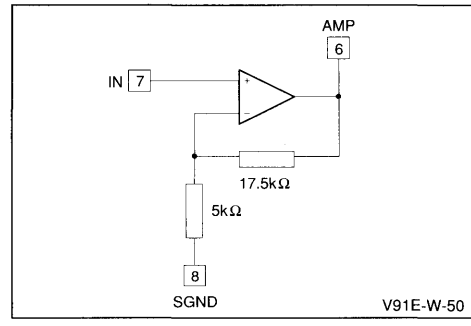
The pulse-width modulator of the TDA8147 is working with input voltages from 1V to 23V. To have the same range for the parabola voltage an input amplifier is necessary. Digital TV sets deliver an analog parabola or a PWM-signal with small amplitude (2V to 3V).

An additional signal ground (SGND Pin) separates the digital ground from the deflection circuit ground.

The internal feedback loop of the amplifier gives a voltage gain

$$A_V = \frac{17.5}{5} + 1 = 4.5 \text{ (see Figure 50)}$$

Figure 50 : Input Amplifier



V.3 - VOLTAGE REFERENCE AND STARTING CIRCUIT

The voltage reference and starting circuit have the same configuration as for the TDA8146 (see paragraph IV.4).

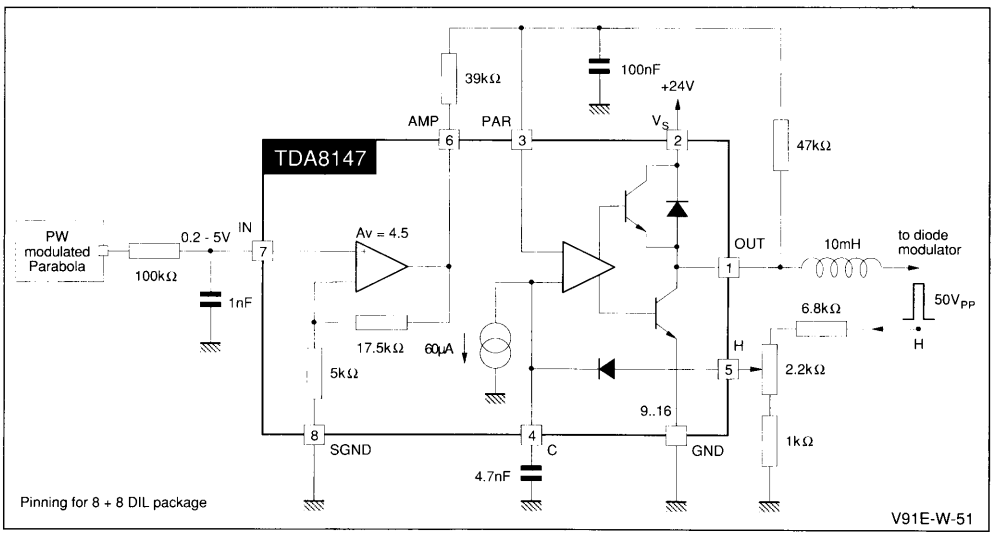
V.4 - PWM MODULATOR AND OUTPUT

The PWM modulator (Figure 51) has the same configuration as for the TDA8146. So see paragraph IV.6 for explanation.

V.5 - APPLICATION

A Standard application diagram is given in Figure 51.
Since all the adjustment of the parabola are made by the digital processor, only the feedback loop of the PWM modulator must be carefully designed. The TDA8147 is well-suited for new TV concepts with 32kHz line frequency.

Figure 51 : Application Diagram



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2018A-TEA2019
FLYBACK SWITCH MODE POWER SUPPLY IMPLEMENTATION

By : J-Y.COUET & T.PIERRE

SUMMARY

SUMMARY *(CONTINUED)*

I - INTRODUCTION

The aim of this application note is to provide the designer with information on how to design and implement a simple and low-cost switching power supply around the TEA2018A SMPS Controller.

This publication has been sub-divided into 3 distinct sections, namely :

- An overview of the current mode regulation
- Detailed description of TEA2018A characteristics
- Application example of a 30W discontinuous mode flyback converter operating directly on 220V_{RMS} mains voltage.

This document also covers a description of **TEA2019** which replaces the **TEA2018A** in applications requiring power transistor turn off synchronization with an external signal.

This function is particularly useful in video applications where the switching transistor turn off is synchronized with the line flyback signal.

SPECIFICATION OF A TYPICAL APPLICATION

- Discontinuous Mode Flyback
- Switching Frequency : up to 40kHz
- Power : the power handling capability is determined by the amount of available base current. Assuming a forced gain of 6 for the power transistor: • $P_{MAX} \approx$ 60W (TEA2018A)
  • $P_{MAX} \approx$ 90W (TEA2019)

II - TABLE OF UNITS AND SYMBOLS

Symbol	Function	Unit
f	Switching Frequency	Hz
f_{OSC}	Oscillator free-running Frequency	Hz
f_{REF}	Reference Frequency (TEA 2019)	Hz
I_{OUT}	Output Current	A
I_P	Primary Current	A
I_S	Secondary Current	A
L_P	Primary Inductance	H
P_{OUT}	Output Power	W
T	Switching Period	s
T_{REF}	Reference Period (TEA2019)	s
t_{ON}	Transistor ON time	s
$t_{ON(L)}$	Conduction time fixed by current regulation	s
t_S	Power transistor storage time	s
V_{AC}	Mains RMS Voltage	V_{RMS}
V_{BE}	Power Transistor base-emitter voltage	V
V_{IN}	Input DC voltage	V
V_{CC}	Positive supply voltage	V
V_{CE}	Power transistor collector-emitter voltage	V
V_{OUT}	Output Voltage	V
ΔI_{CHARGE}	Average current delivered by the PLL of TEA2019	A
η	Power supply efficiency	%

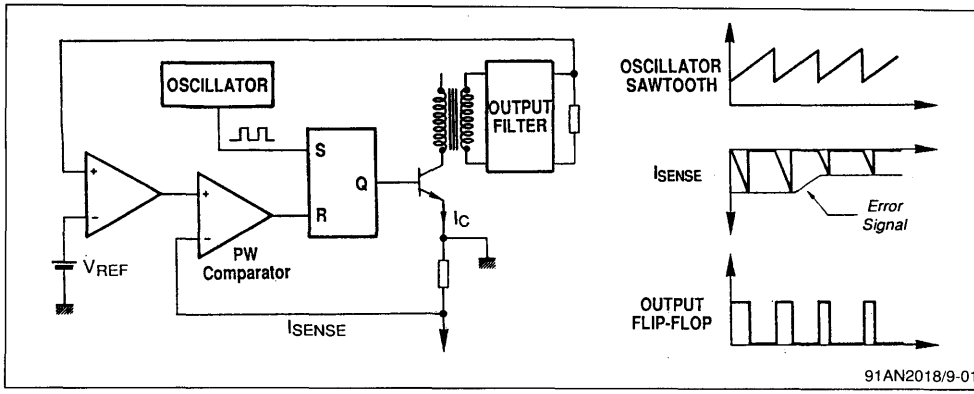
III - CURRENT MODE REGULATION

III.1 - Description

In current mode operation, the regulation is performed by monitoring the peak current through the power switch (switching transistor).

- At every period, the conduction of the power transistor is initialized by a clock signal issued from the oscillator.
- The power transistor is turned-off when its collector current reaches the threshold level fixed by error amplifier.

Figure 1 : Current Mode Control



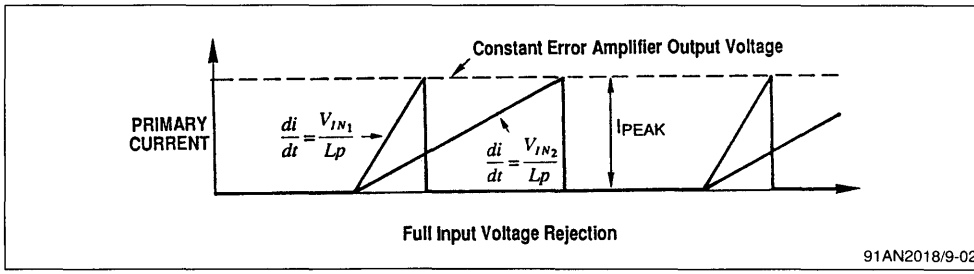
The main advantage of *Current Mode Regulation* in *Discontinuous Mode Flyback Configuration* is that it offers an efficient rejection of all input voltage variations.

The peak current value through the power switch, at constant output power, is independent of the input voltage value.

$$P_{OUT} = \frac{1}{2} \cdot L_P \cdot (I_{PEAK})^2 \cdot f \cdot \eta$$

Variations of the input voltage have no effect on the error amplifier output voltage.

Figure 2

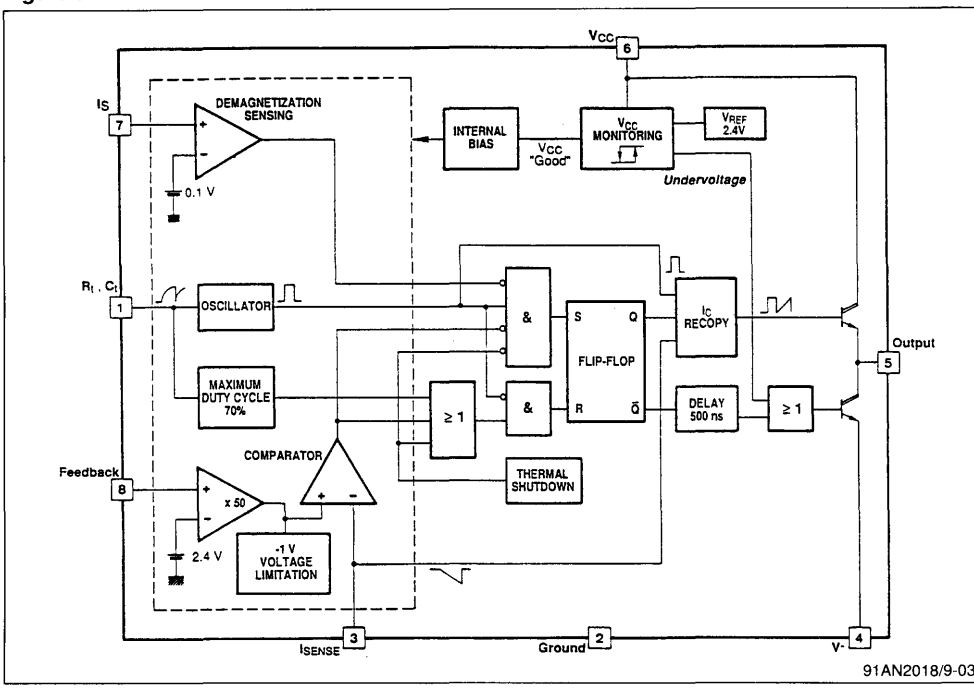


IV - FUNCTIONAL DESCRIPTION OF TEA 2018A

IV.1 - Block diagram

(all values given in the following block diagram are typical values).

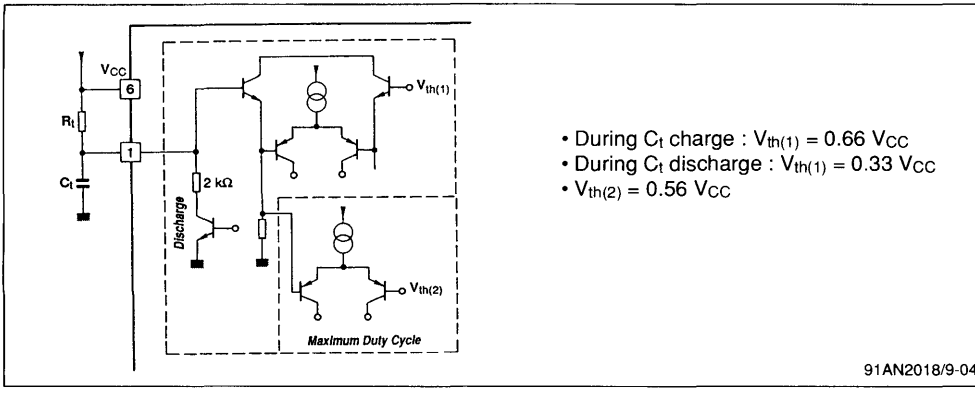
Figure 3



IV.2 - Oscillator and maximum duty cycle

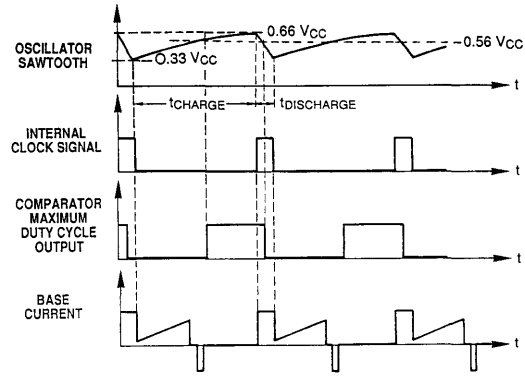
IV.2.1 - Simplified diagram

Figure 4



IV.2.2 - Waveforms

Figure 5



PERIOD : $T \approx t_{CHARGE} + t_{DISCHARGE}$

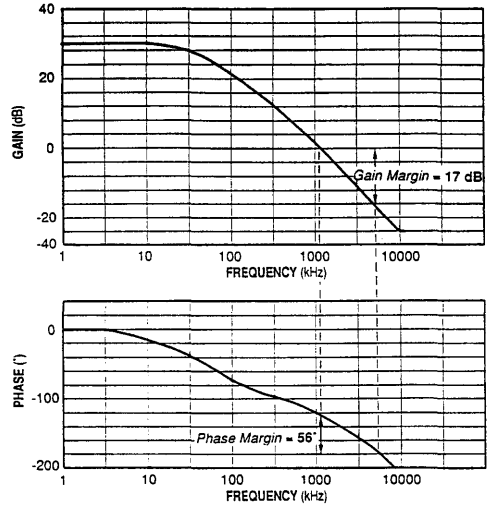
- $t_{CHARGE} \approx 0.66\ R_t\ .\ C_t$
- $t_{DISCHARGE} \approx 0.66\ R_{DISCHARGE}\ .\ C_t$

$\Big\}\ T \approx 0.66\ C_t\ (R_t + 2000)$

IV.3 - Error amplifier

- The error amplifier gain is internally fixed at 30dB typical value.
  Internally implemented compensation networks set the frequency response characteristics.
- Voltage Reference : The value of the reference voltage applied to the inverting terminal is 2.4 V.

Figure 6 : Error Amplifier Frequency Response Characteristics



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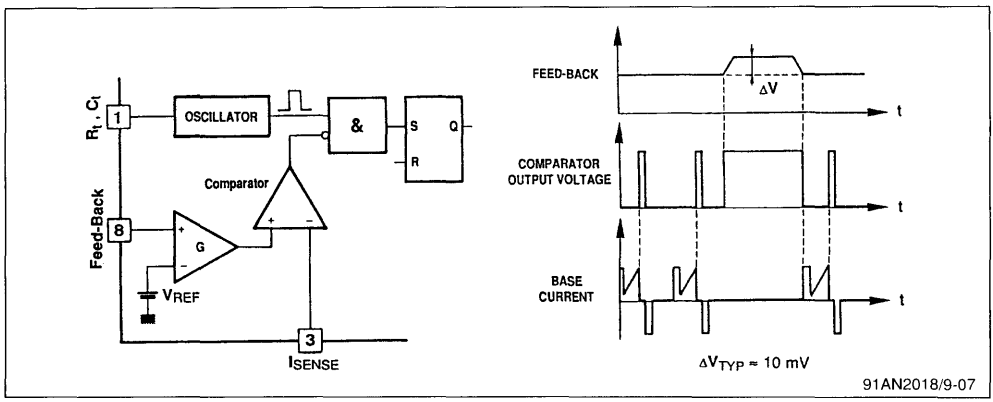
IV.3.1 - Functional behaviour on low-load

When the feed-back voltage exceeds the regulation range, the comparator output remains in high state thereby avoiding the initiation of any new conduction cycle.

Figure 7



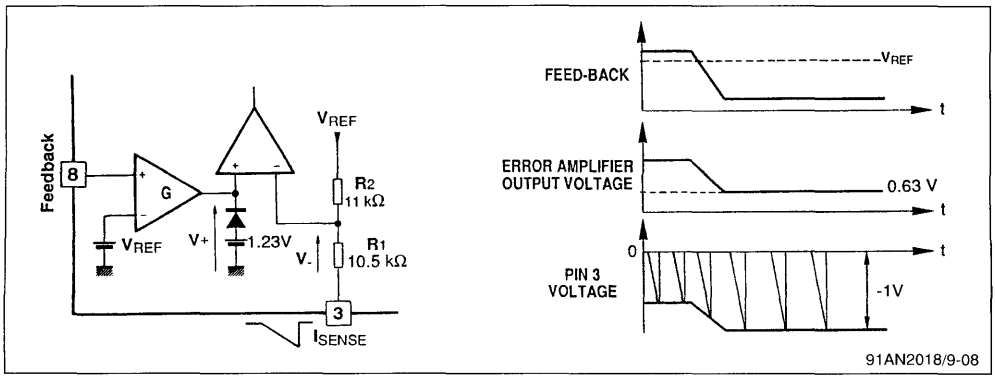
Consequence : On low loads, the conduction frequency becomes lower than the oscillator frequency.

IV.4 - Current measurement & limitation

Peak current through the power switch is set by the error amplifier output voltage.

Clamping the amplifier output voltage at 0.63V will result in limiting the I_{SENSE} pin voltage at 1V level.

Figure 8



In current limitation :

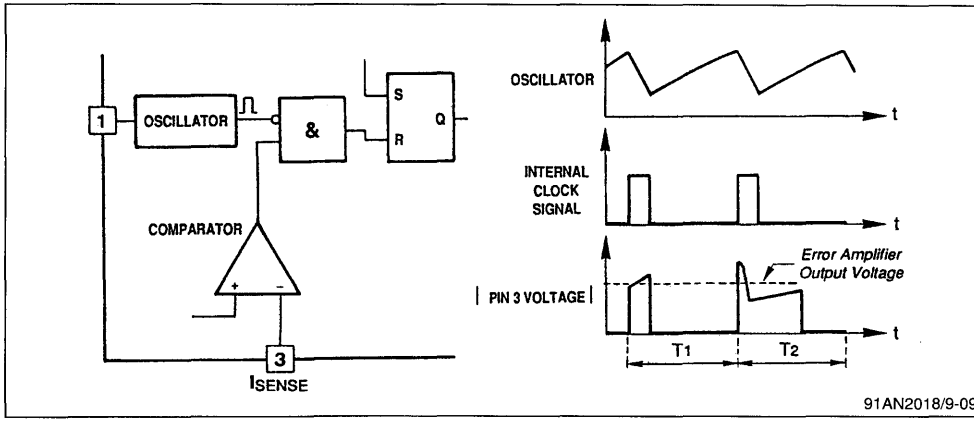
$$\left.\begin{aligned} V^{+} &= 1.23\ V - V_{BE} = 0.63V \\ V^{-} &= V_{(PIN3)} + \left(V_{REF} - V_{(PIN3)} \right) \frac{R1}{R1 + R2} \end{aligned}\right\} \Rightarrow V_{(PIN3)} = -1V$$

IV.4.1 - Disabling the current monitoring function

During oscillator saw-tooth flyback, the output of the PWM comparator is disabled and consequently :

- The minimum conduction time $t_{ON(min)}$ required to discharge the snubber network is fulfilled whatever the status of I_{SENSE} input at the beginning of conduction cycle (T1 period on waveforms of Figure 9).
- All parasitics such as those generated by the recovery of secondary-connected diodes (without RC filter) are eliminated (period T2 on Figure 9).

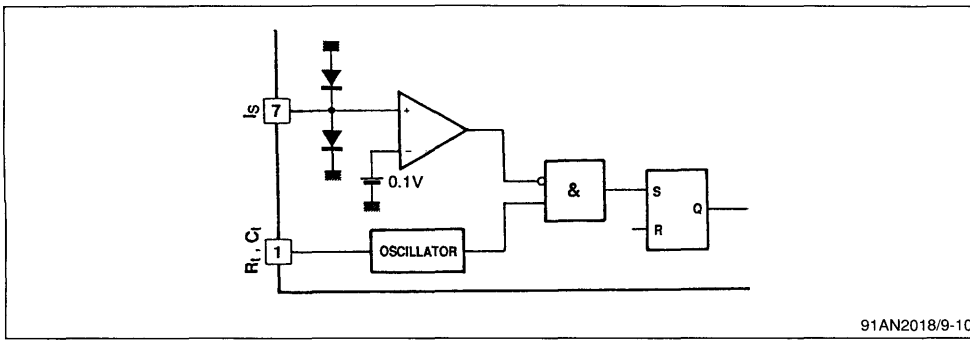
Figure 9



IV.5 - Demagnetization monitoring

No new conduction cycle is allowed as long as the pin 7 voltage remains higher than 0.1V .
When used in *Discontinuous Mode Flyback* configuration, this function will inhibit any new conduction as long as the transformer is not fully demagnetized.
It is obvious that this function offers efficient security in case of overload and short-circuits.

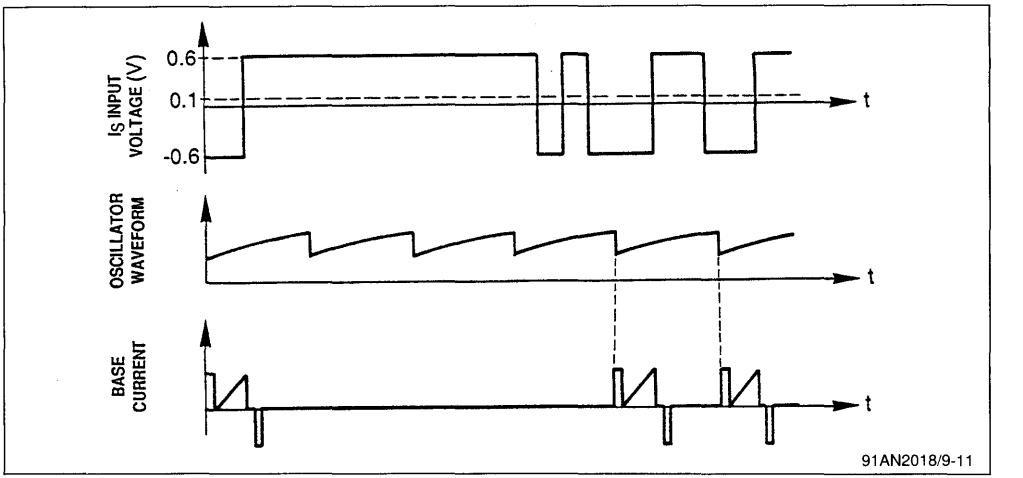
Figure 10 : Demagnetization Sensing



Comments :

- Demagnetization monitoring feature can be used to implement an on-off function.
- This function is disabled by grounding the pin7.

Figure 11 : Waveforms



IV.6 - Thermal protection

When the junction temperature exceeds +150°C, an on-chip protection device will inhibit any new conduction.

IV.7 - TEA2018A behaviour as a function of V_{CC}

Figure 12 : V_{CC} Monitoring Circuit

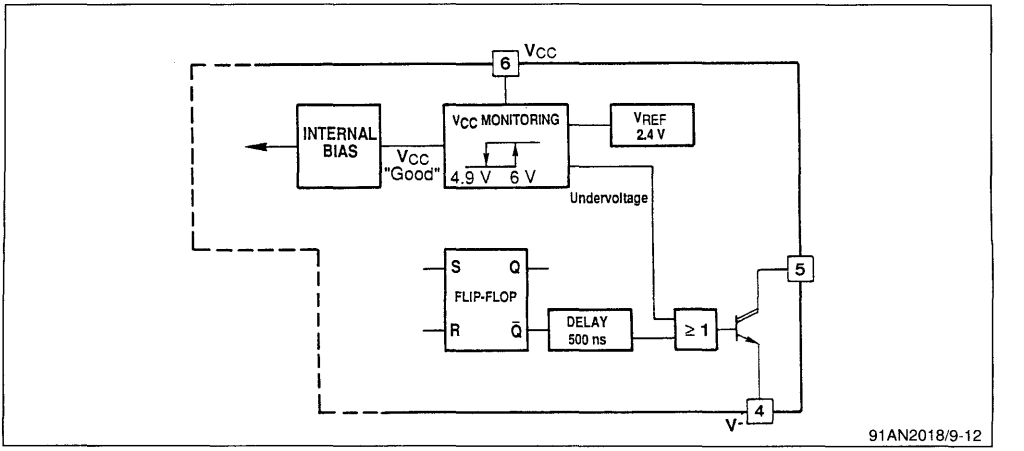
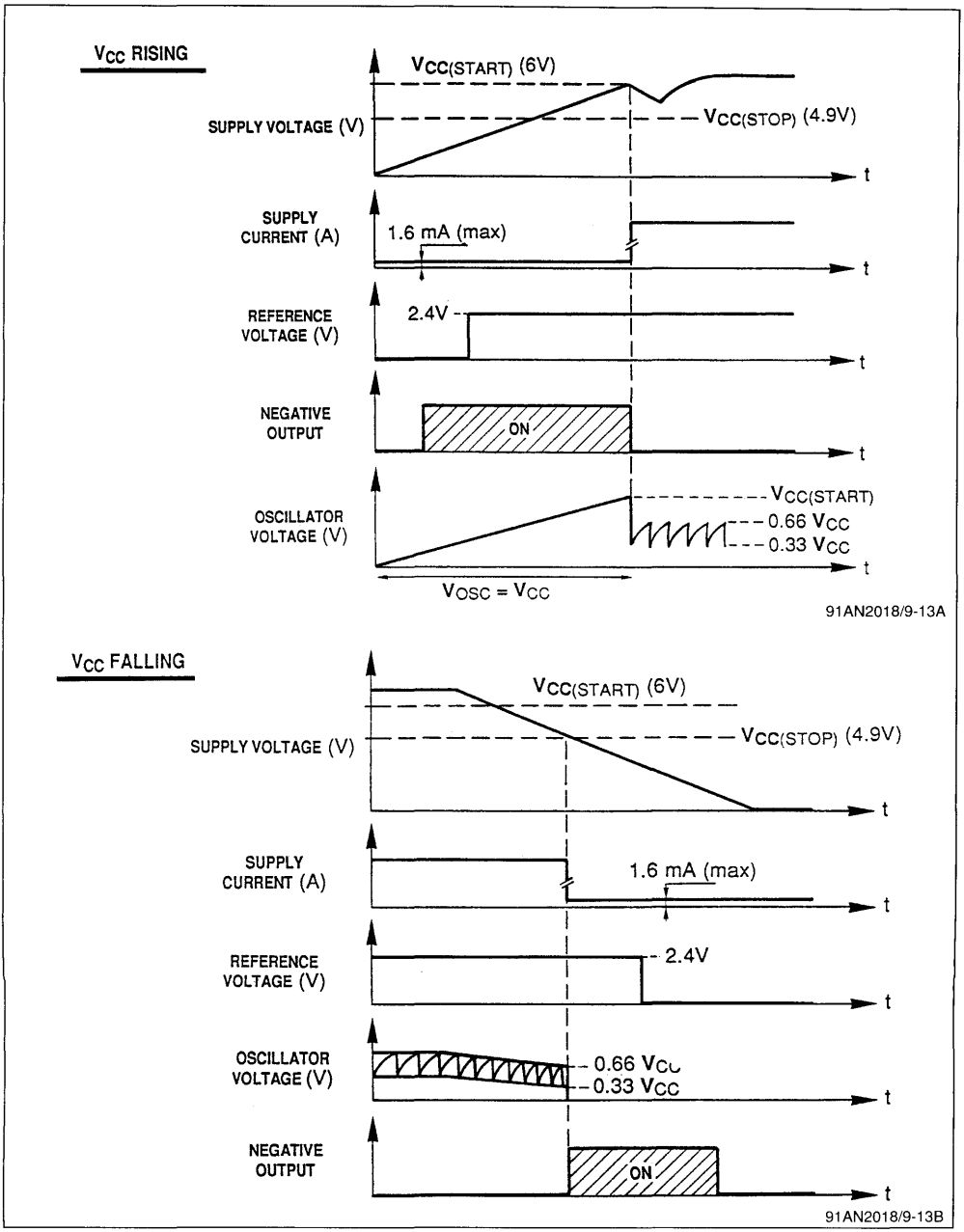


Figure 13 : Waveforms



IV.8 - Output stage (Power transistor base drive)

The TEA2018A has been designed to provide direct drive to bipolar power transistors.

Figure 14 : Simplified Diagram of the Output Stage

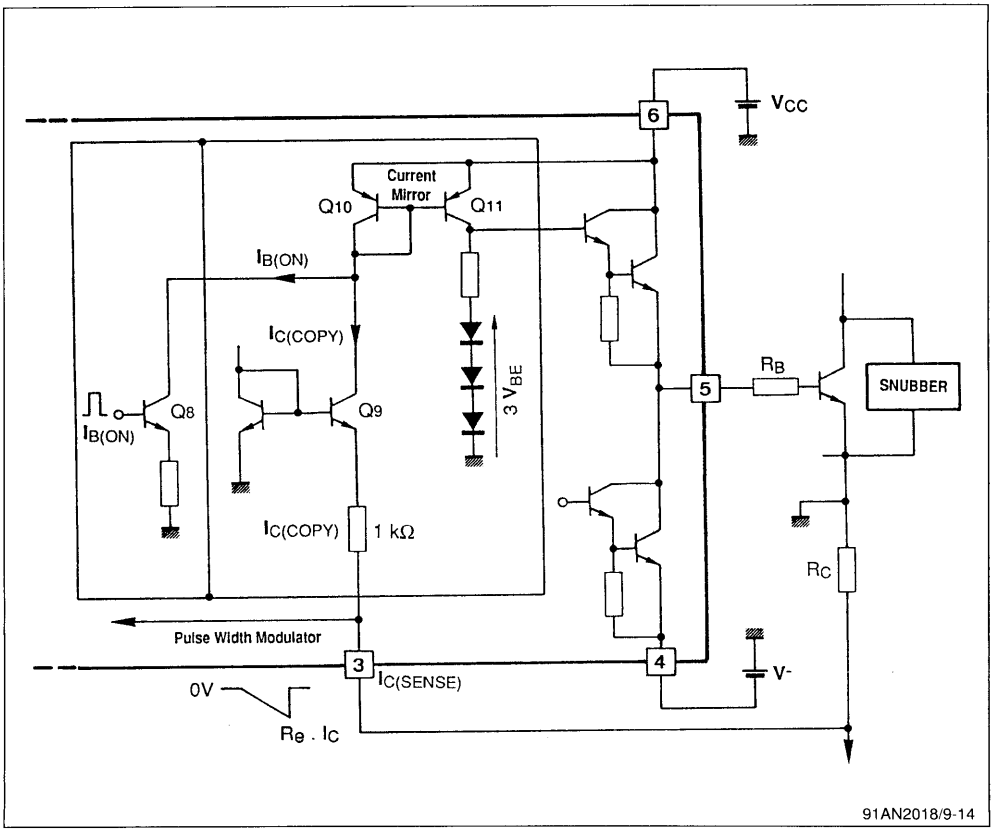
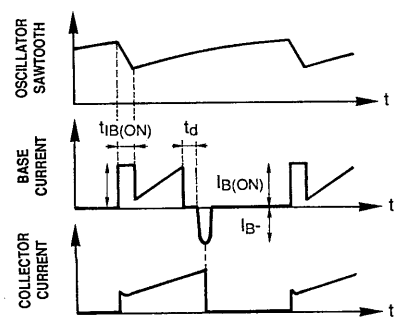


Figure 15 : Waveforms



$t_{IB(ON)} \approx 0.66 \times 2000 \times C_T$

$t_d \approx 500$ ns (typ)

$I_{B(ON)} \approx \frac{1\ V}{R_B}$

$I_{\bar{B}} \approx \frac{|V^-| - V_{NS}}{R_B}$

(V_{NS} : negative stage dropout 0.8 V to 1 V)

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IV.8.1 - Transistor turn-on
A pulse current "$I_{B(ON)}$" provides for rapid transistor turn-on. The duration of this pulse is equal to the oscillator saw-tooth fall time.
The value of this current is : $I_{B(ON)} \approx 1V/R_B$

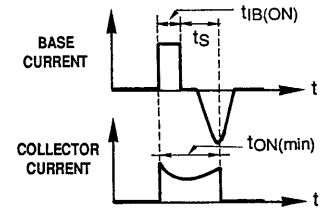
IV.8.2 - Proportional base drive
Once the turn-on current pulse $I_{B(ON)}$ has been issued, the internal current recopy device of TEA2018A will output a voltage V_{OUT} such that :

$$\left.\begin{array}{l} V_{out} = V_{(PIN3)} + V_{BE} \\ V_{OUT} = V_{BE} + R_B \cdot I_B \\ V_{(PIN3)} = R_E \cdot I_C \end{array}\right\} \Rightarrow \text{Forced gain} = \frac{I_C}{I_B} = \frac{R_B}{R_E}$$

IV.8.3 - Transistor turn-off
The power transistor is turned-off by the application of a negative base current. A 500ns typical interval duration between the positive stage turn-off and the negative stage turn-on, will prevent simultaneous conduction of complementary output stages and also abrupt transistor turn-off.

IV.8.4 - Minimum conduction time
In order to allow the discharge of snubber network, each conduction cycle has a minimum duration equal to $t_{ON(min)}$.

Figure 16



- $t_{ON(min)} = t_{IB(ON)} + t_S$
- t_S : Power Transistor storage time

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V - APPLICATION EXAMPLE

V.1 - Customized application design

V.1.1 - Specifications

Output Power	$3.3W \leq P_{OUT} \leq 30W$
Effective Input Voltage	$176\ V_{RMS} \leq V_{AC} \leq 245\ V_{RMS}$
Input Voltage for Start-up and Regulation	$200\ V_{DC} \leq V_{IN} \leq 350\ V_{DC}$
Regulation Input Voltage after Start-up	$130\ V_{DC} \leq V_{IN} \leq 350\ V_{DC}$
Transistor Reflected Voltage	$V_R = 210V$
Switching Frequency	$f = 27kHz$
Expected Efficiency	$\eta = 70\%$
Output Short-circuit Protection	Yes
Open-load Protection	Yes
2 Outputs	(5V, 2A), (12V, 1.5A)

V.1.2 - Calculation of power elements (see also section 7.1)

- $V_{IN(MIN)} = 200V$
- $\frac{t_{ON(L)}}{T} = 0.426$

(where $t_{ON(L)}$ = conduction time fixed in current limitation mode)

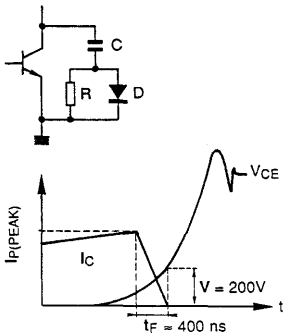
- $I_{P(AV)} = 0.214$
- $I_{P(PEAK)} = 1A$
- $L_p = 3mH$
- $P_{OUT(MIN)} = 2.65W$

- 5V Output : $\frac{ns}{np} \leq 0.029$ $I_{S(PEAK)} = 9.4A \Rightarrow$ Diode : BYW98 - 50
- 12V Output : $\frac{ns}{np} \leq 0.061$ $I_{S(PEAK)} = 7.05A \Rightarrow$ Diode : BYW98 - 50
- Transistor selection

$$\left\{\begin{array}{l} \bullet\ I_{C(MAX)} = 1A \\ \bullet\ V_{C(MAX)} = V_{IN(MAX)} + V_R + V_{SPIKES} \approx 800V \end{array}\right\} \Rightarrow \text{BUV 46A}$$

V.1.3 - Transistor switching aid network

Figure 17



- $C = \frac{I_{(PEAK)} \cdot t_F}{2 \cdot V} \approx 1nF$
- $3RC \approx t_{ON(MIN)}$
  $R \approx 1k\Omega$ [for $t_{ON(MIN)} \approx 3\mu s$]
- Diode : BA159
- Maximum Power dissipated in R :
  $P = \frac{1}{2} C [V_{IN(MAX)}]^2 . f \approx 1.8W$

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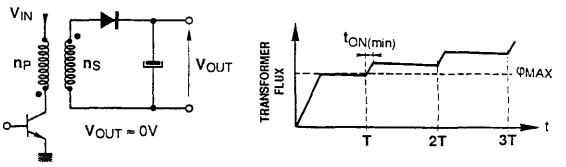
V.1.4 - Demagnetization sensing

a. *Risk of flux runaway without demagnetization sensing*

In the absence of demagnetization sensing, the converter will operate in continuous mode flyback at power supply start-up and also in the case of overloads.

Due to the minimum conduction time imposed by TEA2018A, there will be risk of flux runaway within the transformer and the current through the transistor.

Figure 18



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Flux runaway at start-up or in case of short-circuit : $V_{IN} \cdot t_{ON(MIN)} > V_{LOSS} \cdot \left(\frac{np}{ns}\right) \cdot [T - t_{ON(MIN)}]$

(Where $V_{LOSS} \approx 1.5$ V is the voltage drop accross the rectifier diode and the resistive component of secondary winding).

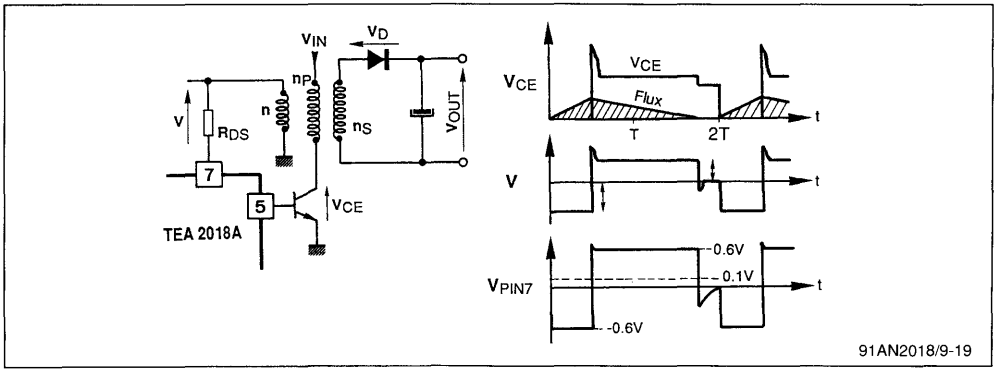
Combining $t_{ON(min)}$ and *demagnetization sensing* functions, will yield highly secure operation ensuring the following functions :

- magnetic flux monitoring
- efficient discharge of snubber networks

b. *Implementing the demagnetization sensing*

The winding used for circuit power supply will also reflect an image of the induced flux. The value of the resistor "R_{DS}" used for this function is not critical and can fall within : $10k\Omega < R_{DS} < 47k\Omega$ range.

Figure 19 : Configuration Arrangement and Short-circuit Waveforms



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No new conduction cycle may be initiated as long as the transformer is not fully demagnetized. On start-up, and in the case of overloads, the demagnetization sensing function will modify the frequency of the conduction cycles accordingly.

c - *Damping network*

Once the transformer has been demagnetized, positive voltage oscillations produced by the discharge of resonant "L_P.C" network may result in unwanted activation of the demagnetization monitoring function.

To prevent this problem, all that required is to damp the voltage oscillations, as shown in Figure 21, through "R_D - D_D" network where diode D_D "shunts" the resistor "R_D".

Figure 20

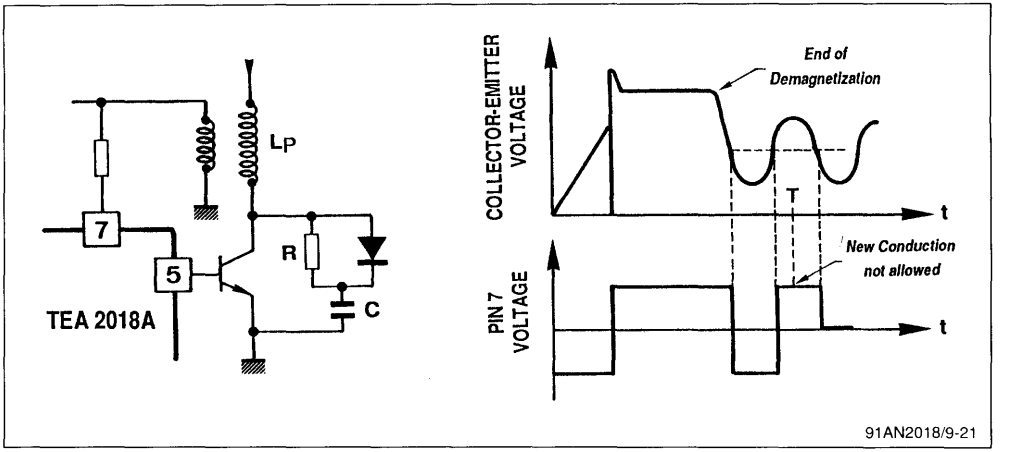
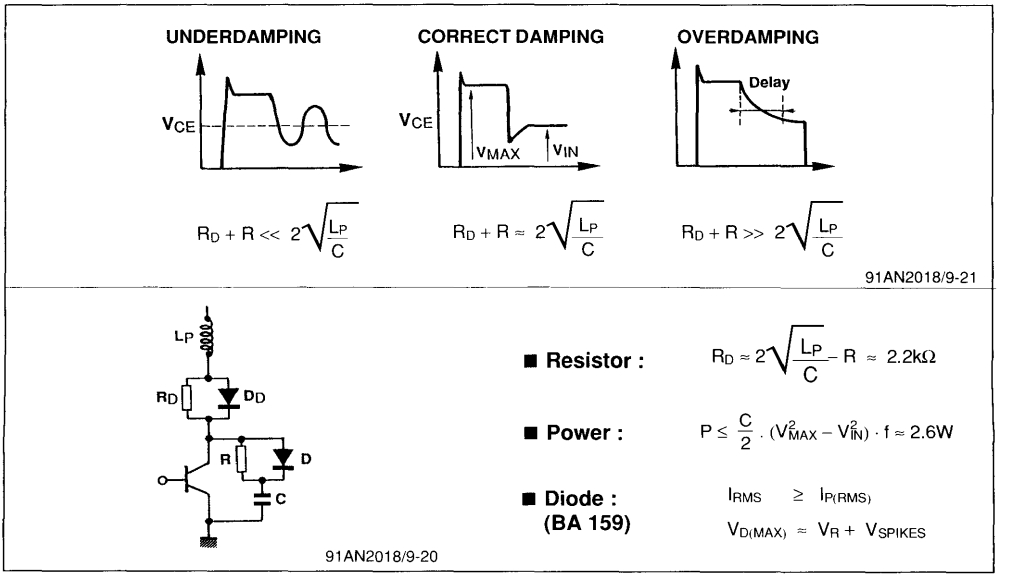


Figure 21

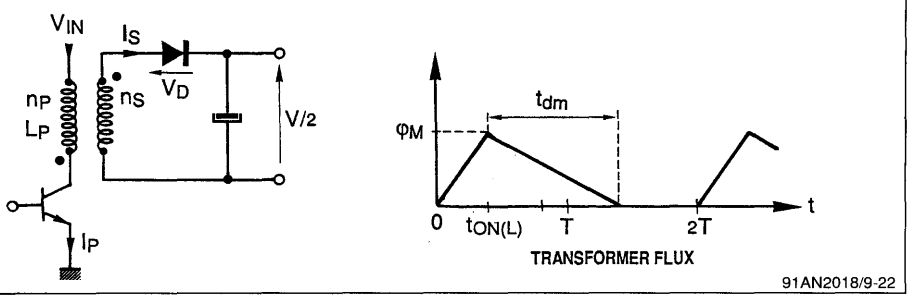


d - *Transformation ratio considerations*

On initial start-up, due to demagnetization monitoring function, the value of conduction frequency will rise in multiples of the normal operating frequency "f" as illustrated below :

Employing a conventionally calculated transformer, the converter will stop operating at "f/2" frequency.

Figure 22



At frequency "f/2" :

$$P_{1/2} = \frac{1}{2} \cdot L(I_p)^2 \cdot \frac{f}{2} = \frac{P_{MAX}}{2}$$

$$V_{1/2} = \frac{V_{out}}{\sqrt{2}}$$

The converter operating frequency will switch from "f/2" to "f" if the following condition is satisfied :

$$t_{on} + t_{DM} < T \qquad (1)$$

(@ f/2 frequency)

$$\varphi_M = L_P \cdot I_P = V_{IN(MIN)} \cdot t_{ON(L)} \qquad (2)$$

(where $t_{ON(L)}$ = conduction time fixed in current limitation mode)

$$\varphi_M = L_S \cdot I_S = \frac{ns}{np}(L_p\, I_p) = \frac{V_{OUT}}{\sqrt{2}} \cdot t_{DM} \qquad (3)$$

Combining (1), (2) and (3) :

$$\frac{ns}{np} \leq \frac{[V_{OUT} + V_D]\,[T - t_{ON(L)}]}{[V_{IN(MIN)} \cdot t_{ON(L)}]\,\sqrt{2}}$$

V.1.5 - Oscillator

The value of capacitor "C_t" is calculated as a function of :

- $t_{ON(min)} : \approx 3\mu s$
- $t_{ON(min)} = t_{IB(ON)} + t_{STORAGE}$ } $C_t = 1.2nF$
- $t_{STORAGE} \approx 1.5\mu s$ } $C_t \geq 470pF$
- $t_{IB(ON)} \approx 0.66\ Ct\ .\ 2000$

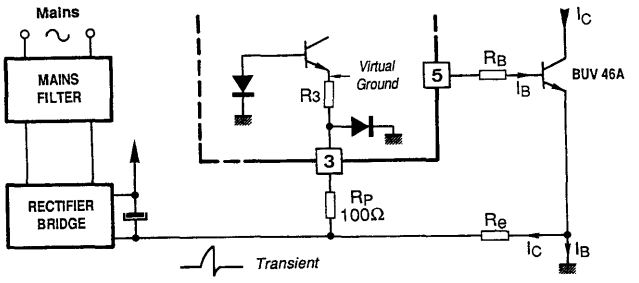
The value of resistor R_t is calculated as a function of period T as follows :

$T = 0.66\ C_t\ (R_t + 2000) = 37\mu s \rightarrow Rt \approx 47k\Omega$

V.1.6 - Power transistor base drive

The "R_e" resistor is calculated as a function of "current limitation" and the resistor "R_B" as a function of "forced gain". Resistor "R_P" can be connected to pin 3 "I_{SENSE}" to protect the device against mains-generated transitional overvoltages.

Figure 23



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Current limitation

$$V_{(PIN3)} \approx 0.88V \text{ (current limitation threshold value)}$$

$$V_{(PIN3)} \approx \frac{R3}{R_P + R3} \cdot R_E \cdot I_C \Rightarrow R_E = 1\Omega \begin{cases} \bullet\ R_p = 100\Omega \\ \bullet\ R3 = 1\Omega \\ \bullet\ I_{C(MAX)} \approx 1A \end{cases}$$

Gain calculation

$$I_{C(MAX)} = 1A \Rightarrow \text{Transistor : BUV46A} \Rightarrow \text{Forced Gain} \approx \frac{I_C}{I_B} = 9$$

$$V_{(PIN3)} = R_B \cdot I_B \,, V_{(PIN3)} = \frac{R3}{R_P + R3} \cdot R_C \cdot I_C \Rightarrow R_B = 8.2\Omega$$

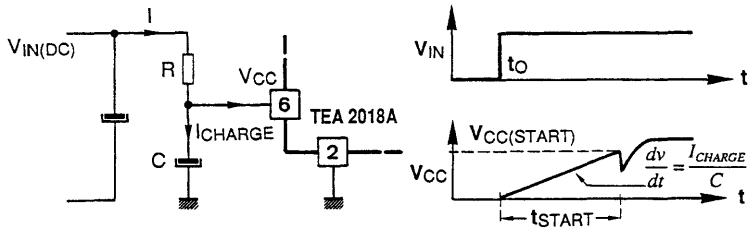
V.1.7 - Self-supply

Power supply start-up

A high value resistor inserted between the "high voltage source" and "V_{CC}" capacitor will charge up this capacitor upon the initial supply start-up.

The TEA2018A starts operating at $V_{CC} \approx 6V$ (typ). On-chip implemented hysteresis of 1.1V (typ) will trigger the self-supply function.

Figure 24



The value of R is calculated to yield maximum start-up time.

- $C = 220\mu F$
- $V_{CC(START)MAX} = 6.6V$
- $I_{CC(MAX)} = 1.6mA$
- $t_{START} = 3s$

- $I_{CHARGE} = \dfrac{V_{CC(START)MAX} \cdot C}{t_{START}}$
- $R = \dfrac{V_{AC(MIN)} \cdot \sqrt{2}}{I_{CC(MAX)} + I_{CHARGE}}$
- $R = 120\ k\Omega$

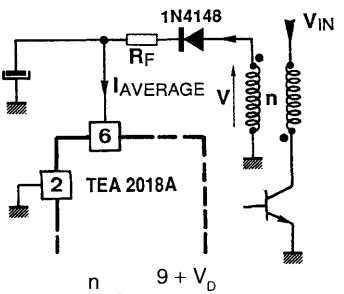
a - *Positive self-supply : V_{CC}*

The V_{CC} supply is provided by a flyback-type winding. The number of turns "n" is selected to yield a voltage "V" of approximately 10V.

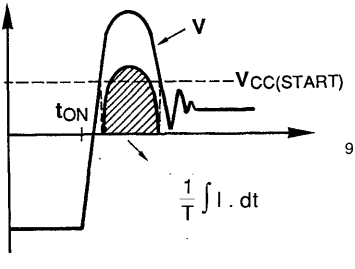
Within the self-supply arrangement, the resistor "$R_F = 15\Omega$" in combination with the capacitor of V_{CC}, form a filter network which attenuates mains-generated voltage spikes.

Note that in the absence of this filter, the energy generated by voltage spikes can often satisfy the power supply requirements of the TEA2018A in case of any short-circuit on low-voltage windings.

Figure 25



$$\frac{n}{n_s} \approx \frac{9 + V_D}{V_{OUT} + V_D}$$



is sufficiently high to meet the power supply requirements without R_F

b. *Negative Self-supply : V*

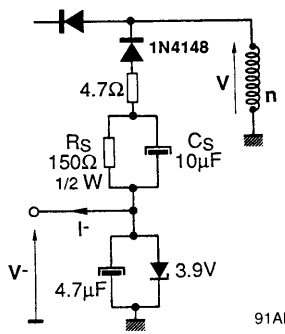
A negative supply voltage "V-" is required for efficient transistor turn-off.

This voltage is generated by an auxiliary winding connected in forward arrangement.

The "zener diode" will clamp this negative voltage and make it independent from the input voltage (V_{IN} > 200V).

The "C_S" capacitor will accelerate V- settling process upon the initial power supply start-up. Resistor "R_S" is used to limit the current upon the negative power supply setup.

Figure 26



- $I_{\overline{AV}} \approx I_{\overline{B}} \times \frac{t_s}{T} \approx 15$ mA

- $R_{S(MAX)} \approx \dfrac{\left(V_{IN} \cdot \frac{n}{n_p}\right) - (1V - |V^-|)}{I_{(\overline{AV})}}$

$\approx 230\Omega$ (@ V_{IN} = 200V)

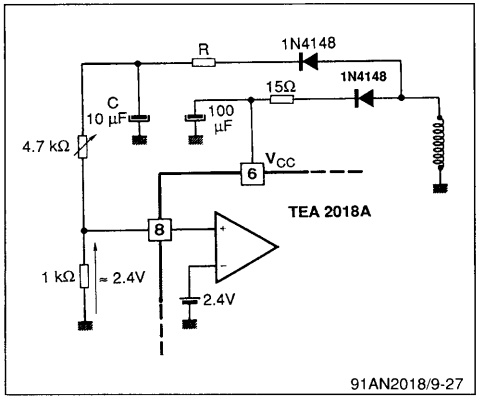
Prefered value : $R_S = 150\Omega$

V.1.8 - Regulation

As illustrated in Figure 28, the self-supply winding is also used for voltage regulation.

To avoid the power drawn by TEA2018A to influence the regulation, the supply for regulation is generated by a source independent from "V_{CC}".

Figure 27



The RC filter attenuates the parasitics due to voltage spikes generated by switching. However, the cut-off frequency of this filter must be sufficiently high so as to avoid excessive slow-down of the regulation loop response.

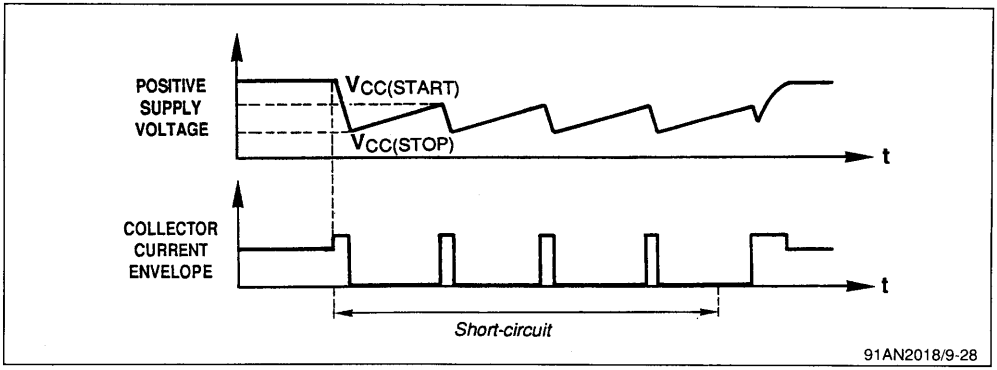
V.1.9 - Operation under overload & short-circuit conditions

In case of any overload, the secondary voltage will fall, circuit power supply will drop below $V_{CC(STOP)}$, consequently TEA2018A stops operating and its power consumption will fall under the current supplied by the start-up resistor.

The capacitor of "V_{CC}" begins charging up and a new conduction cycle will be initiated as soon as "V_{CC}" reaches "$V_{CC(START)}$" level.

The system will function in relaxation mode as long as the overload persists.

Figure 28

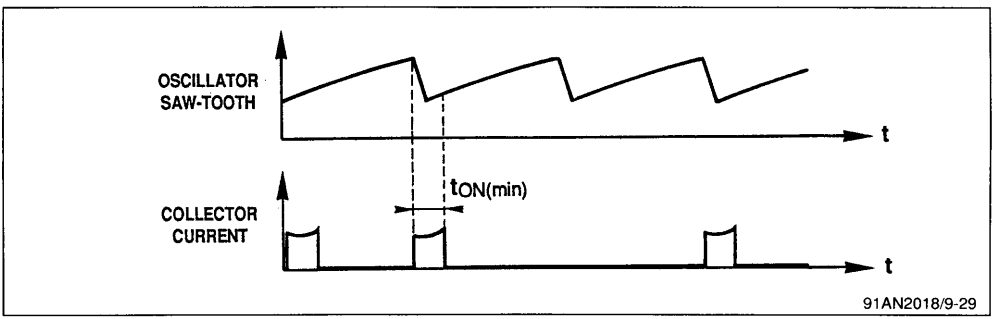


V.1.10 - Operation on Low-loads
When the output power falls below :

$$P_{OUT(MIN)} = \frac{(V_{IN} \cdot t_{(ON(MIN))})^2}{2 \cdot L_P} \cdot f \cdot \eta$$

the regulation becomes incompatible with the operating frequency "f", conduction cycles occur in a random fashion and at a frequency lower than "f".

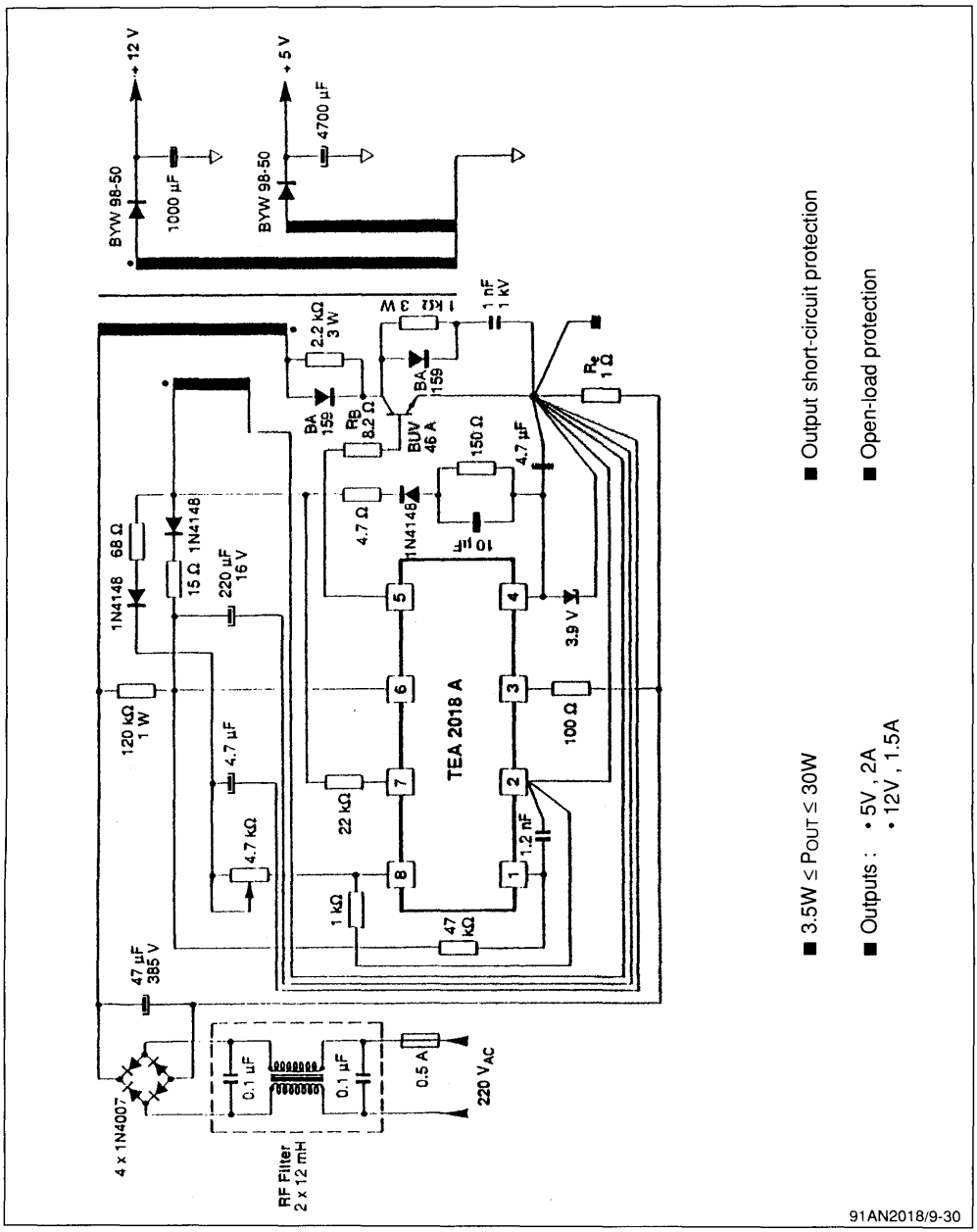
Figure 29



Note : This event has no impact on the power supply reliability.

V.1.11 - Complete Application Diagram

Figure 30



VI - FUNCTIONAL DESCRIPTION OF TEA2019

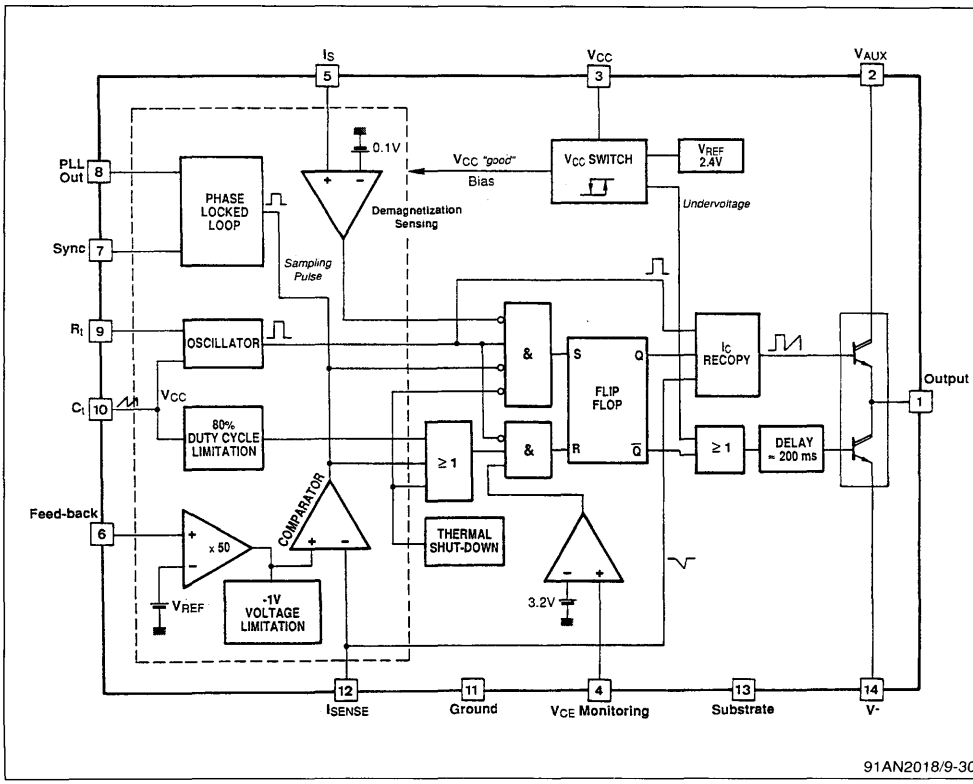
VI.1 - Introduction

The TEA2019 has an internal architecture similar to TEA2018A and offers the following additional features :

- a true positive current source providing linear charge-up of the timing capacitor "Ct"
- an internal PLL which allows synchronization of the power transistor turn-off with an external clock signal
- power transistor desaturation monitoring
- possibility to dissipate externally the power required for transistor base drive

VI.2 - Block Diagram

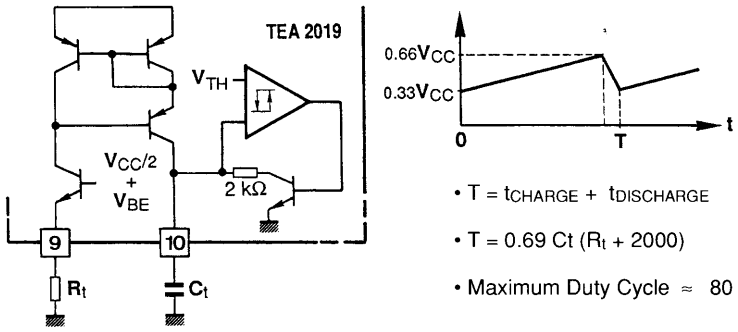
Figure 31



VI.3 - Differences between TEA2018A & TEA2019

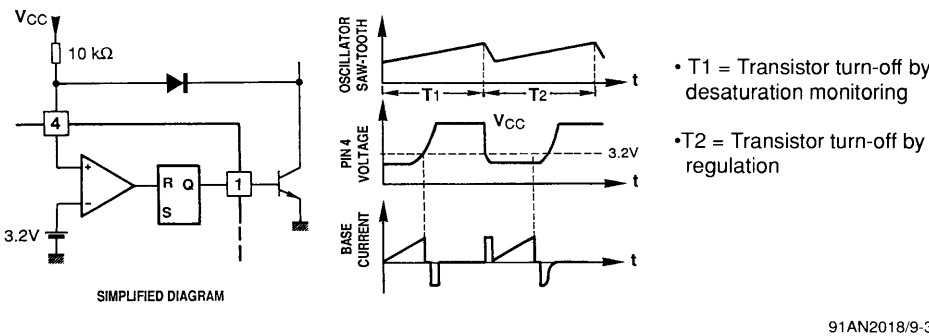
VI.3.1 - Oscillator
The oscillator saw-tooth waveform is linear. The capacitor "C_t" charging current is constant and is determined by the value of resistor "R_t".

Figure 32



VI.3.2 - V_{CE} Monitoring
If during the power transistor conduction period the pin 4 voltage exceeds 3.2V, the transistor would be turned-off until the next conduction cycle. To disable this function, pin 4 must be grounded.

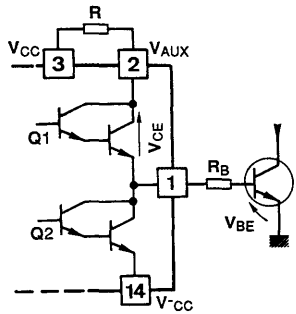
Figure 33



VI.3.3 - Output stage

An external resistor connected between V_{CC} and V_{AUX} will dissipate a portion of the power required by the base drive. The value of this resistor is calculated to be as large as possible but appropriately dimentioned to avoid the saturation of the output stage Q1.

Figure 34



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$$R = \frac{V_{CC} - V_{BE} - V_{CE(MIN)}}{I_{B(MAX)}} - R_B \quad \text{(where } V_{CE(MIN)} \approx 1.5 \text{ V)}$$

- Power dissipated in Q_1 (Flyback) :

$$P = \frac{t_{ON}}{T}\left[(V_{CC} - V_{BE}) \cdot \frac{I_{B(MAX)}}{2} - (R_B + R) \cdot \frac{I^2_{B(MAX)}}{3} \right]$$

- Power improvement compared to TEA2018A :

$$\frac{\Delta P}{P} = \frac{2 \cdot R \cdot I_{B(MAX)}}{3 (V_{CC} - V_{BE}) - 2 \cdot R_B \cdot I_{B(MAX)}} \approx \frac{2 (V_{CC} - 3.5\ V)}{V_{CC} - 5V}$$

$$\left\{ \text{at : } V_{CC} = +9\ V \Rightarrow \frac{\Delta P}{P} = 0.5 \quad \text{i.e.} \quad 50\% \right\}$$

VI.3.4 - PLL

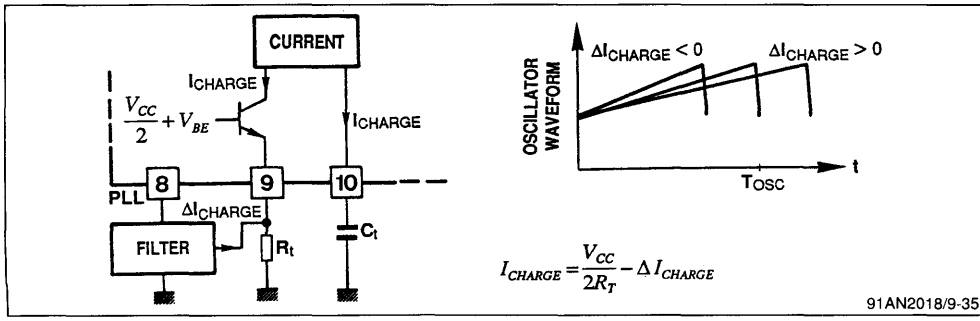
In a discontinuous mode flyback configuration, the power transistor turn-off produces significant amount of noise. It is therefore interesting to synchronize this event with an external signal.

Since the transistor turn-off instant in current mode operation is generally unknown, consequently, only phase and frequency locking of the oscillator will enable to synchronize the transistor turn-off time without disturbing the voltage regulation loop.

a. - *Operating principles*

Oscillator phase and frequency can be accurately controlled by adjusting the charge current of "C_t" capacitor. The PLL behaves as a current generator, the direction and the magnitude of which are function of the phase difference between transistor turn-off and the synchronization signal.

Figure 35



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b - *Internal structure*

The major building block of the PLL is an analog multiplier whose two inputs are the synchronization signal and power transistor turn-off monitoring signal. Multiplier output signal has a complex spectrum; a low-pass filter is employed to extract the DC and low-frequency components.

Figure 36

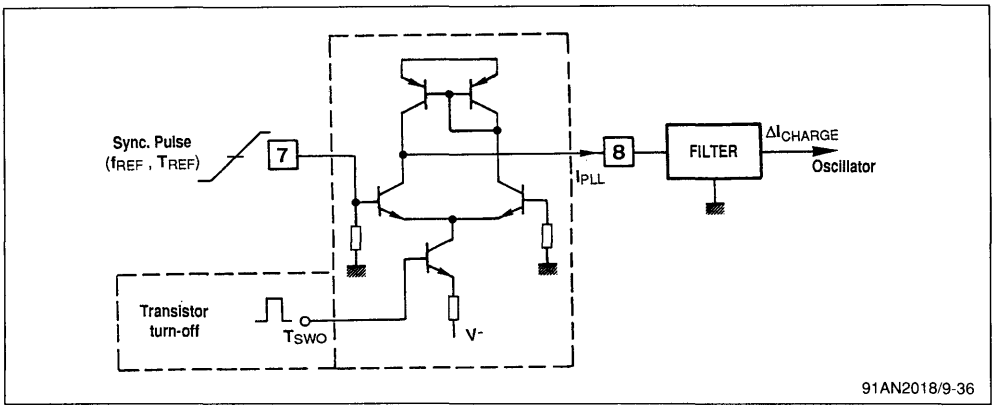
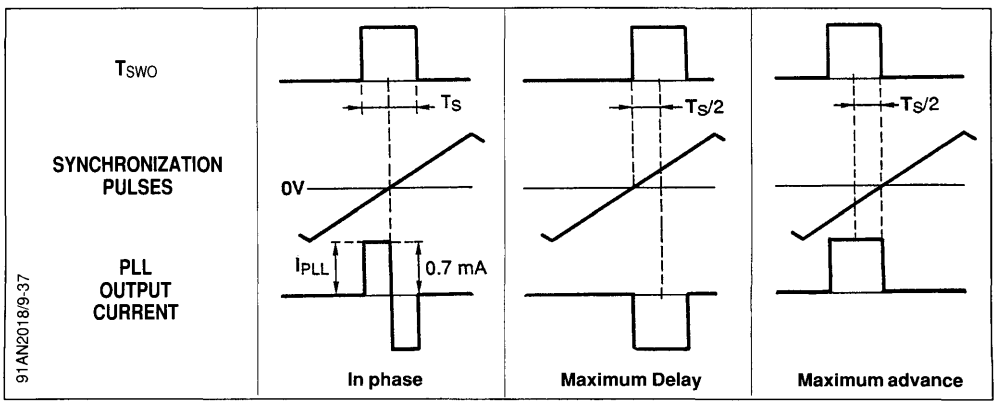


Figure 37 : Synchronization configuration waveforms

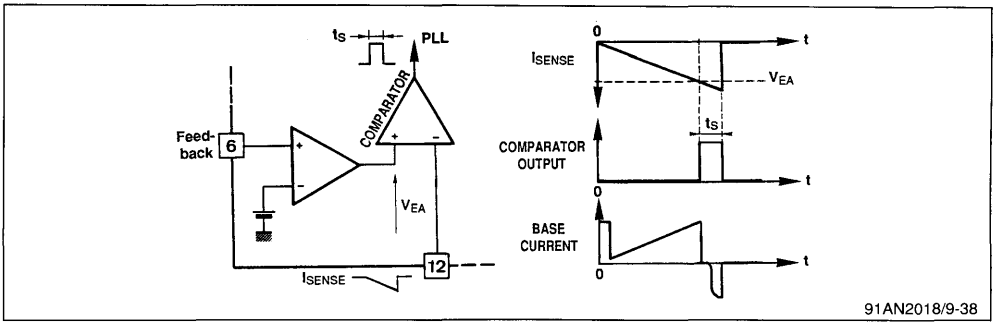


The PLL will source or sink the maximal current when the shift interval between synchronization signal and the transistor turn-off equals $t_s/2$.

c - *PLL input signal*

c1 - Transistor turn-off Signal : T_{SWO}
Due to transistor storage time, the PWM comparator will generate a pulse which will be used as T_{SWO} signal.

Figure 38

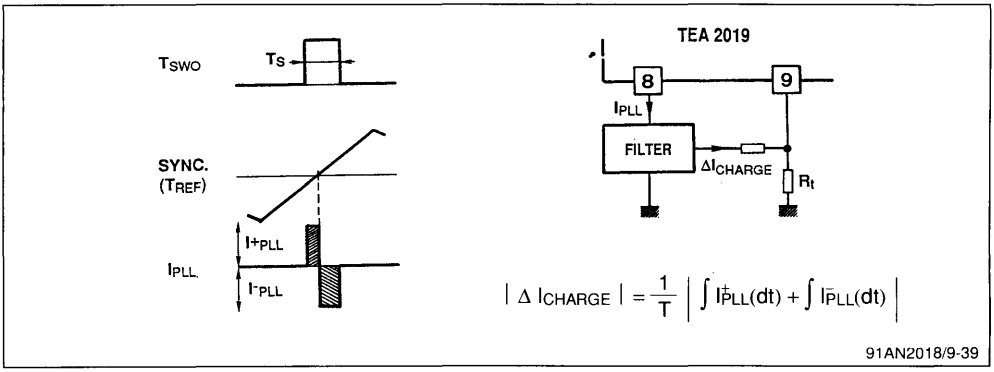


c2 - Synchronization Signal
The characteristics of synchronization signal are outlined in section 6.3.5.

d. - *Characteristics of the PLL*

d1 - Synchronization
When synchronization occurs, the average current delivered by PLL is equal to ΔI_{CHARGE} required for frequency compensation.

Figure 39

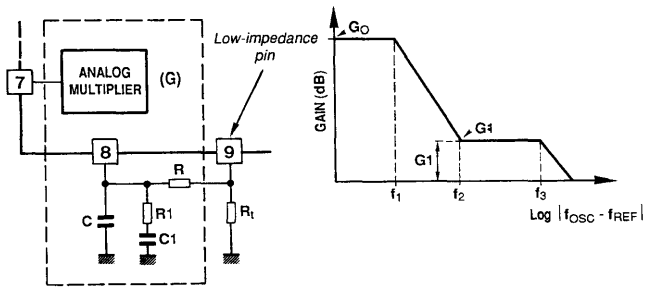


d2. - Capture Range : $| f_O - f_{REF} |_{MAX}$

The signal delivered by PLL prior to synchronization has $| f_O - f_{REF} |$ component. G_{dB} is the overall gain of multiplier and filter stages. Phase locking is possible if the frequency difference $| f_O - f_{REF} |$ satisfies the following relationship :

$$G_{dB}\ | f_O - f_{REF} | \geq 0\ db$$

Figure 40



91AN2018/9-40

$$f_1 = \frac{1}{2\pi (R + R1)\, C1} \qquad f_2 = \frac{1}{2\pi R1C1} \qquad f_3 = \frac{R + R1}{2\pi . C . R . R1}$$

e - *Output filter calculation*

For stability reasons, the output filter is calculated at gain G1 ≈ 0 dB.

- "f2" frequency determines the capture range.
- "f3" frequency is equal to the free-running frequency "f_O".
- The "G_O" gain is rather complex to evaluate. By approximation, it is proportional to the switching transistor storage time "t_S".
  At $t_S = 2\mu s$, the gain $G_O \approx 24dB$

f - *Numerical application*

The following calculations yield the optimum value of capture range :

- $f_O = 15.6kHz$ (switching frequency)
- $f_2 = 2.2kHz$ (this is the selected capture range ± 8µs with respect to 64µs period)

G1 = 0dB , $V_{CC} = 8V$, $t_S = 2\mu s$, $C_t = 1.5nF$,

$R_t = 56kW$, $G_O = 24dB$

R = R_t yields excellent noise immunity.

$$G_0 - G_1 = -20 \log \frac{R1}{R + R1} \Rightarrow R1 \approx 3.9k\Omega$$

$$f_2 = \frac{1}{2\pi R1C1} \Rightarrow C_1 \approx 22nF$$

$$f_3 = \frac{R + R1}{2\pi . C . R . R1} \Rightarrow C \approx 3.3nF$$

g - *Holding range*

Once the capture occurs, the free-running frequency "f_{OSC}" can rise within the holding range without causing loss of synchronization.

When synchronization is achieved, the filter no longer introduces any attenuation and thus the holding range becomes larger than the capture range.The holding range is given by :

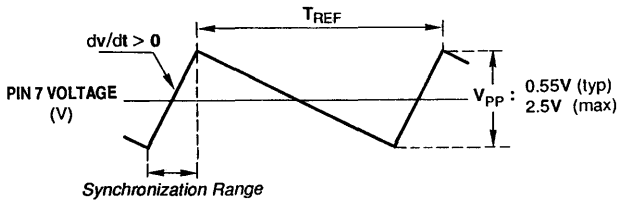
$$\Delta T = T_{REF} . \frac{1}{1 + \frac{0.33 . V_{CC} . C_T}{I_{PLL} . t_S}}$$

Where :

- T_{REF} : the period of synchronization signal
- I_{PLL} : the maximum current the PLL can source or sink (0.7mA typ)

VI.3.5 - Synchronization signal and the input filter
The synchronization signal applied to PLL input (pin7) must respect the following conditions :

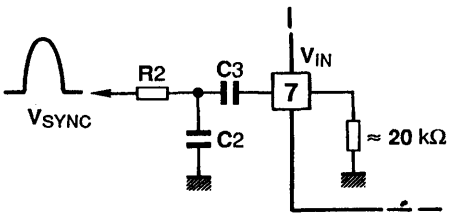
Figure 41

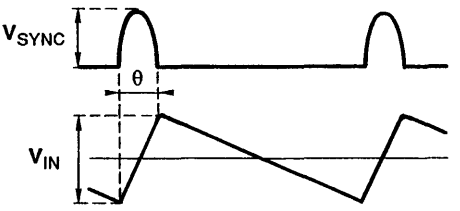


91AN2018/9-41

The TEA2019 has been particularly designed for video applications where the synchronization signal is obtained from the flyback signal generated during the line flyback.
Figure below illustrates the configuration arrangement used in such applications.

Figure 42





- In typical application : C3 = 47nF, C2 = 33nF
- R2 is calculated as a function of :

$$R2 \approx \frac{\theta}{C2 \log\left(\frac{V_{SYNC}}{V_{SYNC} - V_{IN}}\right)}$$

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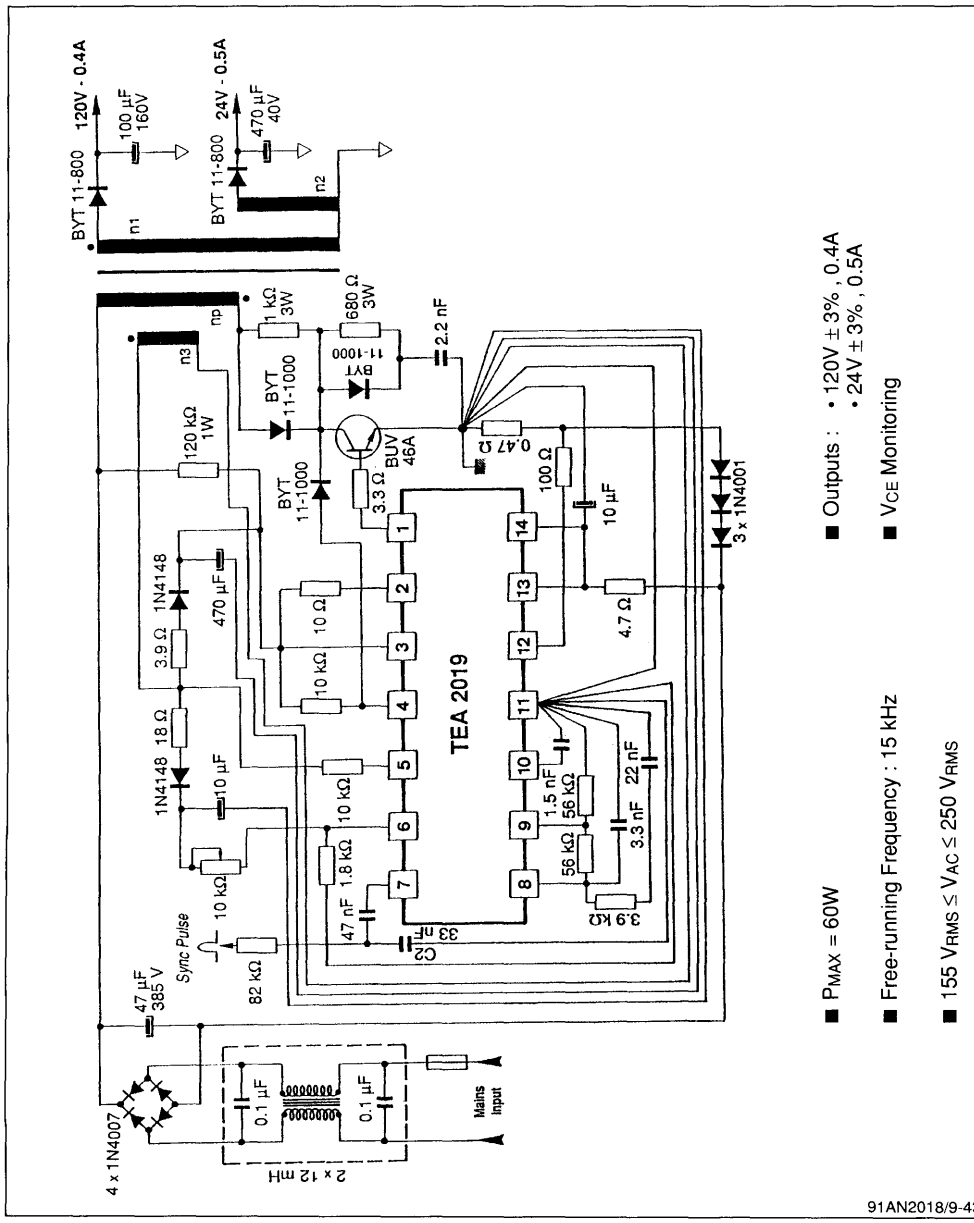
VI.4 - Applications

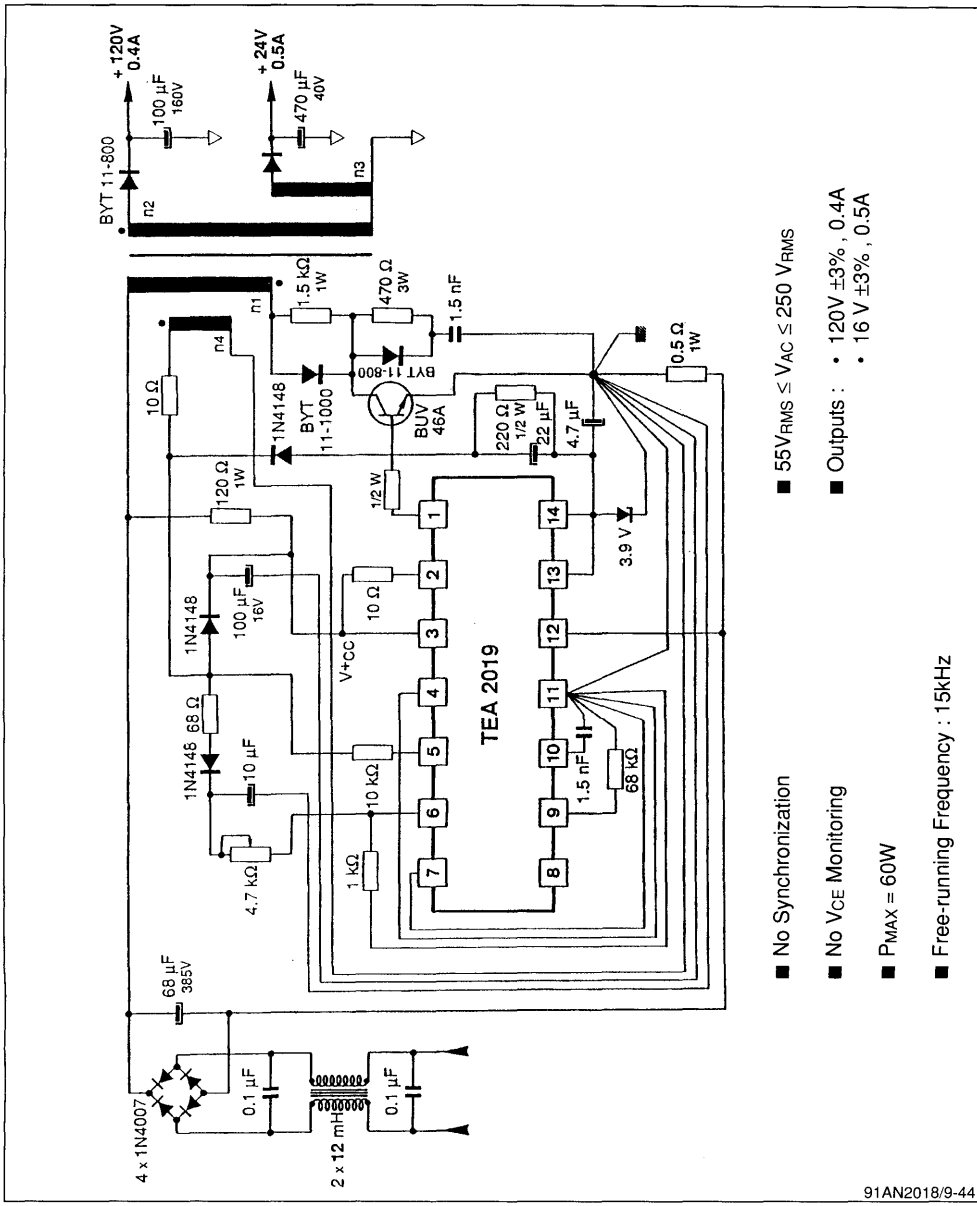
VI.4.1 - Typical application with synchronization

Figure 43



VI.4.2 - TEA2019 Configuration for power boosting

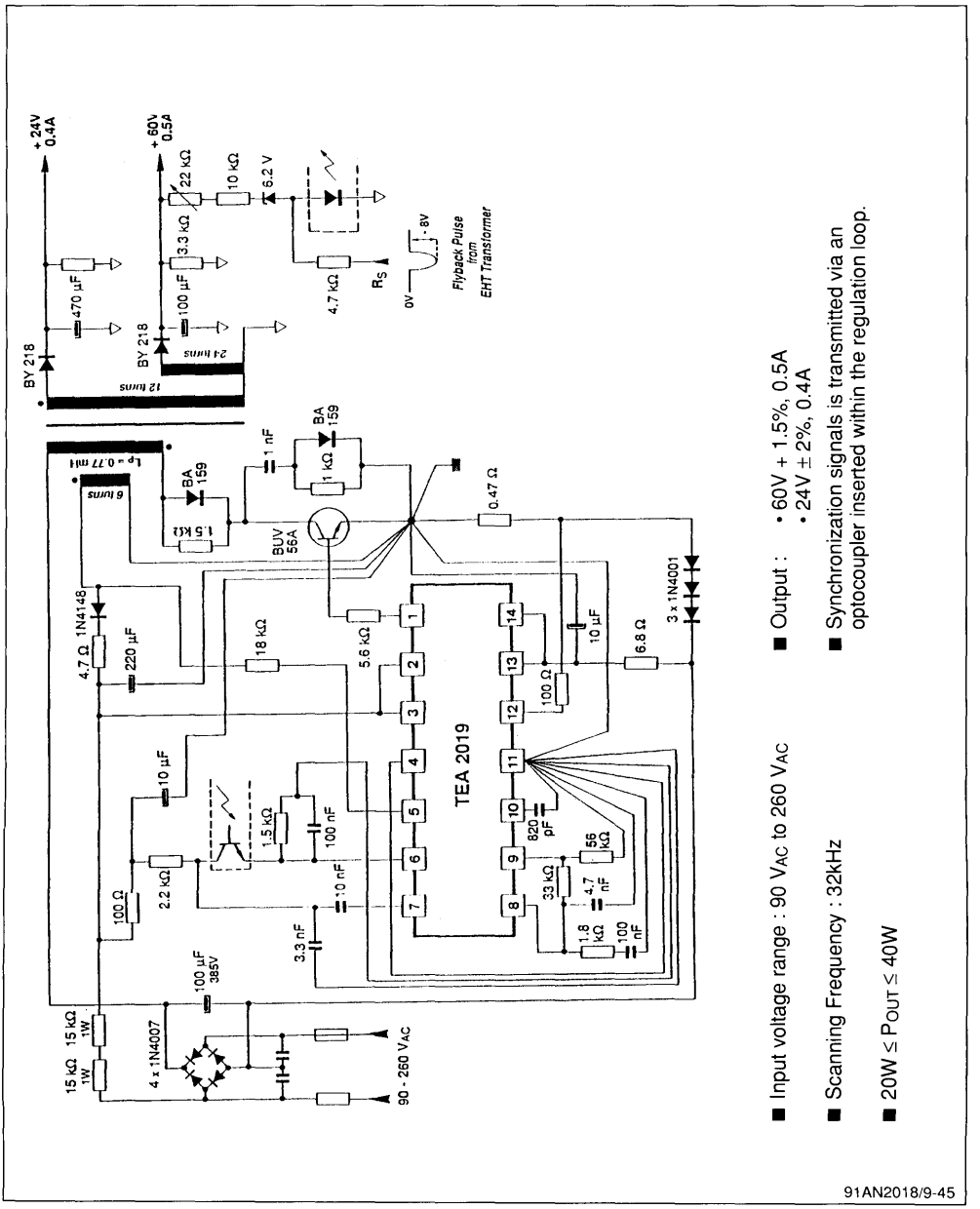
Figure 44



Comment : V- voltage is generated by the auxiliary winding.

VI.4.3 - Monitor application

Figure 45



VI.5 - Synchronization signal transmission

This signal is often generated from the secondary of the power supply, and therefore requires galvanic isolation.
Two solutions outlined below are both appropriate :

Figure 46 : Transmission through EHT transformer winding

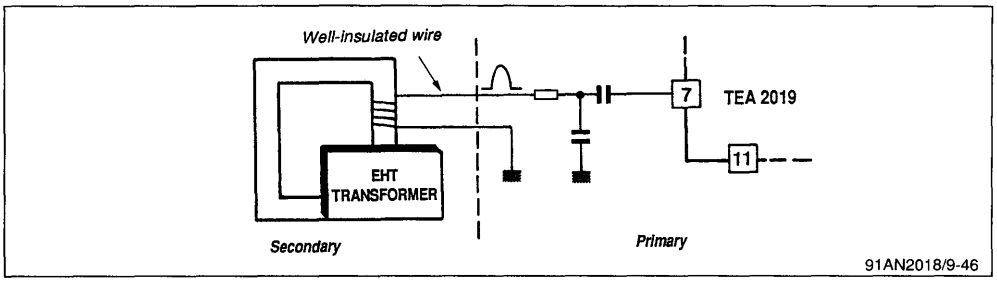
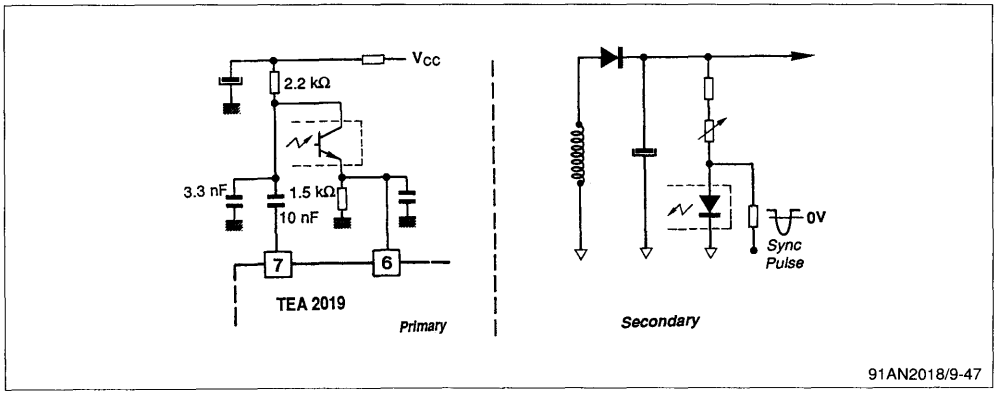


Figure 47 : Transmission via the Optocoupler of Regulation Loop

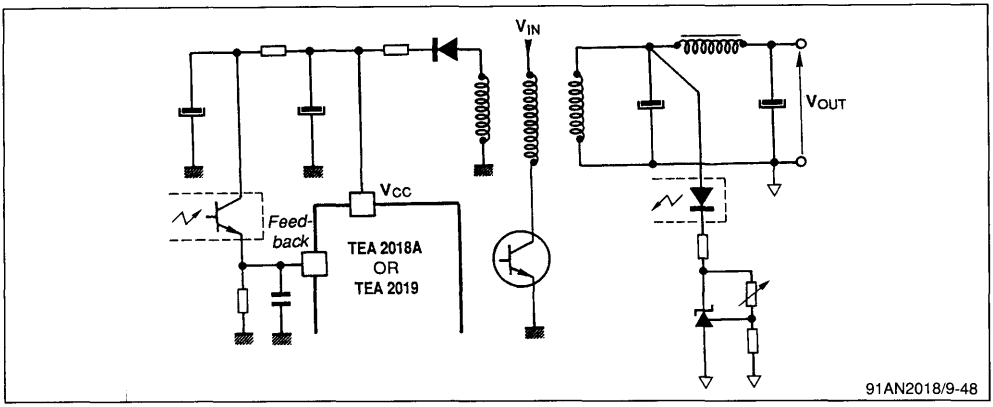


In this configuration, the optocoupler is used for the transmission of both, feed-back voltage and the synchronization signal.

VI.6 - APPLICATION VARIANTS

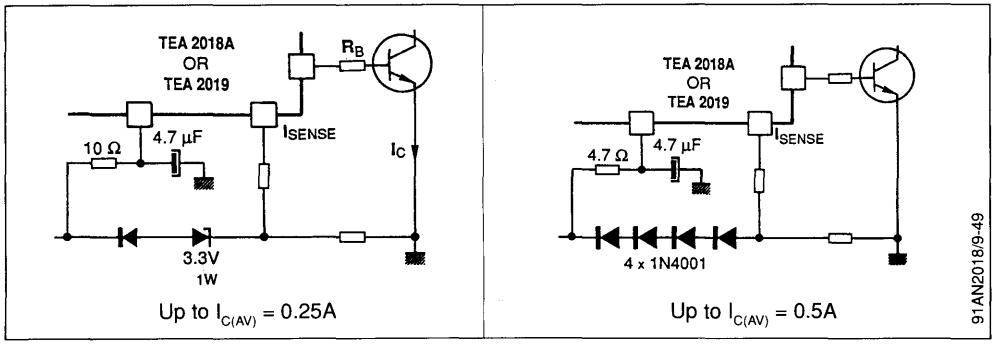
VI.6.1 - Regulation by optocoupler

Figure 48



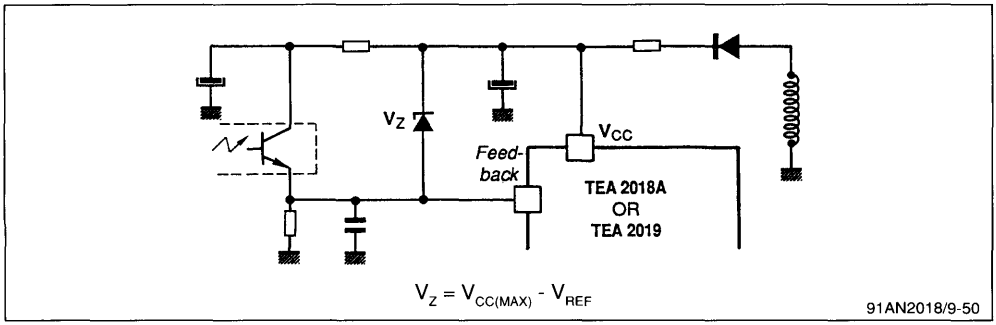
VI.6.2 - V⁻ Generator

Figure 49



VI.6.3 - Overvoltage protection

Figure 50



VI.6.4 - Application without demagnetization sensing

If the condition given below is satisfied, the demagnetization sensing function can be omitted without any risk of flux runaway in case of short-circuits or at start-up.

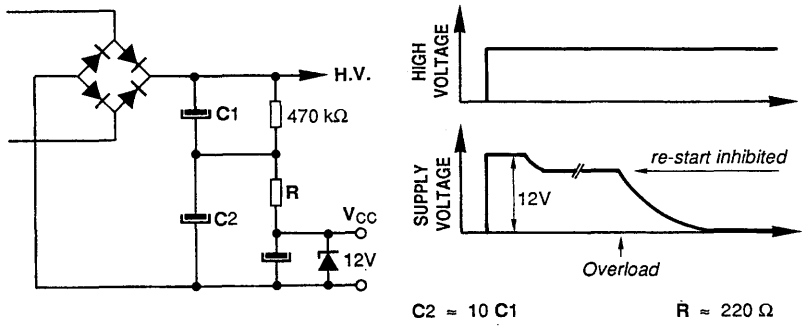
$$(V_{OUT} + V_{LOSS}) \leq V_{LOSS} \frac{V_{IN(MIN)}}{V_{IN(MAX)}} \cdot \frac{T - t_{ON(MIN)}}{t_{ON(MIN)}} \cdot \frac{T - t_{ON(L)}}{t_{ON(MAX)}}$$

Consequently, the damping network is no longer required and the "demagnetization sensing input" can be grounded.

VI.6.5 - Full shut-down at overload

In case of overload, the arrangement depicted below will completely shut-down the power supply. To re-start the system, capacitor "C1" must be discharged.

Figure 51



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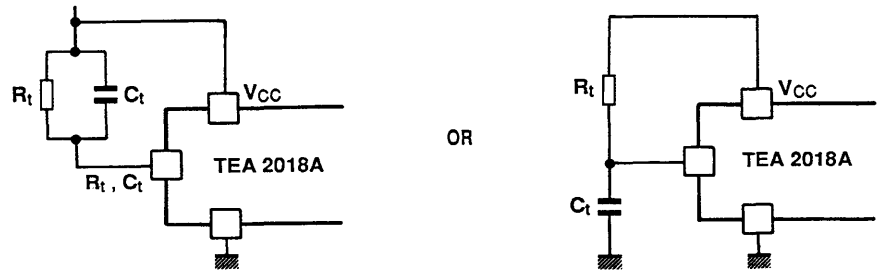
VI.6.6 - Oscillator (TEA2018A only)

Figure 52



Both configurations are functionally equivalent

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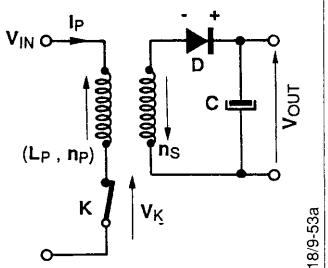
VII - FIXED FREQUENCY DISCONTINUOUS MODE FLYBACK

VII.1 - Fundamentals

An operating phase includes 3 phases :

- $0 \le t \le t_{ON}$: energy is stored within the primary inductance
- $t_{ON} \le t \le t_{dm}$: energy transfer toward the secondary winding
- $t_{dm} \le t \le T$: dead time, the transformer is fully demagnetized.

Figure 53

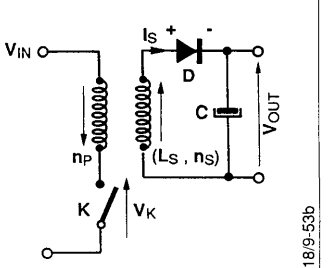


91AN2018/9-53a

$0 < t < t_{ON}$

- K : closed
- $V_K = 0$
- $\frac{dI_p}{dt} = \frac{V_{IN}}{L_p}$
- $V_D = V_{OUT} + \frac{ns}{np} V_{IN}$
- Energy stored during t_{ON}

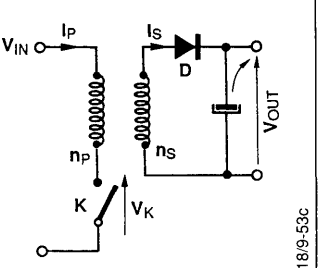
$$W_{LP} = \frac{(V_{IN}\, t_{on})^2}{2L_p}$$



91AN2018/9-53b

$t_{ON} < t < t_{dm}$

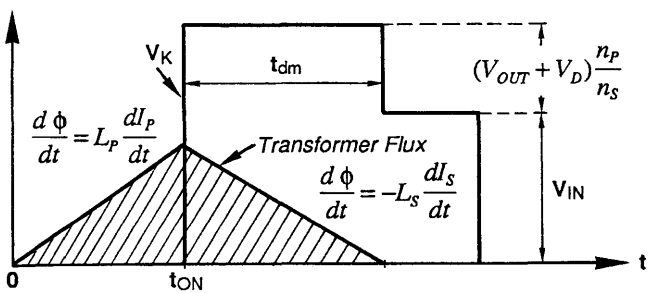
- K : open
- D : conducts
- $V_K = V_{IN} + (V_{out} + V_D)\frac{np}{ns}$
- $\frac{dI_s}{dt} = -\frac{(V_{OUT} + V_D)}{L_s}$
- $t_{dm} - t_{ON} = \frac{ns}{np} \cdot \frac{V_{IN} \cdot t_{ON}}{V_{OUT} + V_D}$



91AN2018/9-53c

$t_{dm} < t < T$

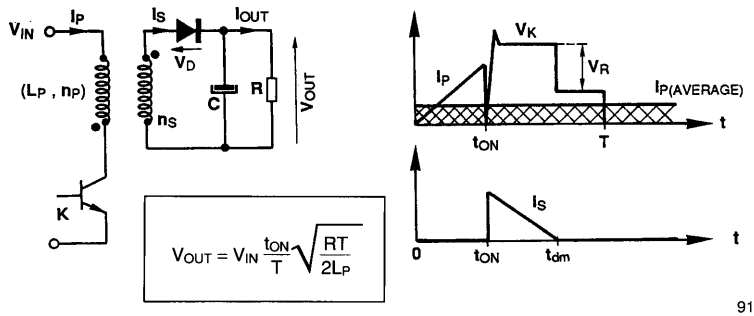
- $I_P = 0$, $I_S = 0$
- K : open
- D: blocked
- $V_K = V_{IN}$



91AN2018/9-53d

VII.2 - Transformer calculation and power semiconductors selection

Figure 54



91AN2018/9-53d

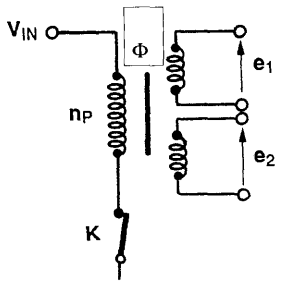
• Maximum operation duty cycle :	
(1) $\frac{t_{ON(L)}}{T} = \frac{V_R}{V_R + V_{IN(MIN)}}$	(2) $\frac{t_{ON(L)}}{T} = \frac{V_R}{V_R + \sqrt{2} \cdot V_{IN(MIN)}}$
• Maximum average primary current :	$I_{P(AV)MAX} = \frac{P_{OUT(MAX)}}{\eta} \cdot \frac{1}{V_{IN(MIN)}}$
• Maximum peak primary current :	$I_{P(PEAK)} = 2\, I_{P(AV)MAX} \cdot \frac{T}{t_{ON(L)}}$
• Primary inductance :	$L_P = V_{IN(MIN)} \cdot \frac{t_{ON(L)}}{I_{P(PEAK)}}$
• Maximum transformation ratio :	
(1) $\left(\frac{ns}{np}\right)_{(MAX)} = \frac{[V_{OUT} + V_D][T - t_{ON(L)}]}{V_{IN(MIN)} \cdot t_{ON(L)}}$	(2) $\left(\frac{ns}{np}\right)_{(MAX)} = \frac{[V_{OUT} + V_D][T - t_{ON(L)}]}{V_{IN(MIN)} \cdot t_{ON(L)} \cdot \sqrt{2}}$
• Peak rectifier current :	$I_{S(PEAK)} = 2\, I_{OUT} \frac{T}{(t_{dm} - t_{ON})}$
• Minimum power transfer at frequency "f" :	$P_{OUT(MIN)} = \eta \cdot \frac{[V_{IN(MAX)} \cdot t_{ON(MIN)}]^2}{2 \cdot L_P} \cdot f$

Where :
- (1) : without demagnetization monitoring
- (2) : with demagnetization monitoring
- $t_{ON(L)}$: Conduction time before current limitation

VII.3 - Multi-output flyback

All transformer windings undergo the same flux change of dϕ/dt. Regulation of any output causes regulation of all other windings.

Figure 55



$$\bullet \frac{e_1}{n_1} = \frac{d\Phi}{dt}$$

$$\bullet \frac{e_2}{n_2} = \frac{d\Phi}{dt}$$

$$\Rightarrow \boxed{\frac{e_1}{e_2} = \frac{n_1}{n_2}}$$

91AN2018/9-55

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2028-2029

By : J-M.MERVAL / B. D'HALLUIN

SUMMARY

Page

TEA2028

SUMMARY *(continued)*

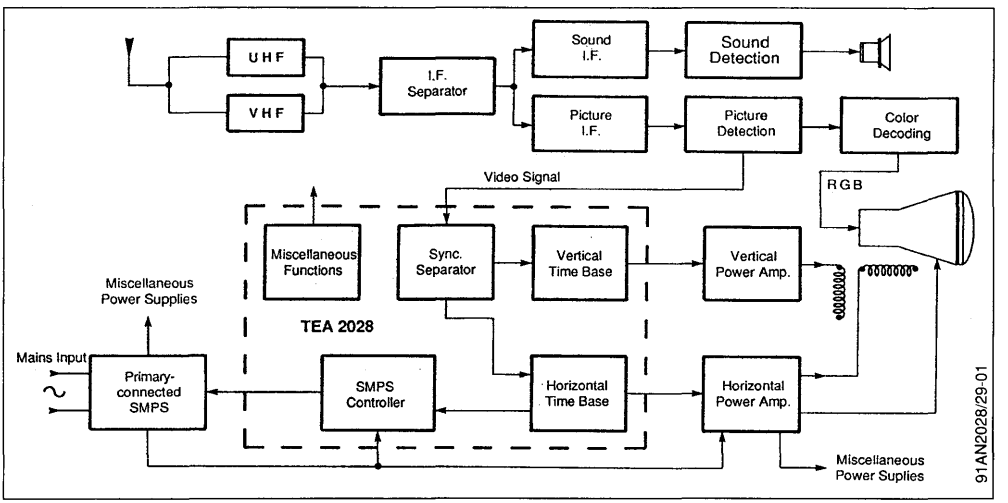
SUMMARY *(continued)*

I - GENERAL DESCRIPTION

As depicted in figure below, the TEA2028 combines 3 major functions of a TV set as follows :

- Horizontal (line) and vertical (frame) time base generation for spot deviation. The video signal is used for the synchronization of both time bases.
- On-chip switching power supply controller synchronized on line frequency.

Figure 1



This integrated circuit has been implemented in bipolar I^2L technology, and various functions are digitally processed. In fact, resorting to logic functions has the advantage of working with pure and accurate signals while full benefit is drawn from high integration of logic gates (approx. 110 gates per mm^2).

The main objective is to drive all functions using an accurate time base generated by a master 500 kHz oscillator.

Also, horizontal and vertical time bases, are obtained by binary division of reference frequency. This has the advantage of eliminating the 2 adjustments which were necessary in former devices.

One section of this integrated circuit is designed to drive a switching power supply of recent implementation called "master-slave". Switching takes place on the primary side (i.e., directly on mains) of a transformer. The device ensures **SMPS Control**, **Start-up** and **Protection** functions. Control signals go through a small pulse transformer thereby providing full isolation from mains supply.

This new approach fully eliminates the bulky mains transformers used in the past. In addition, it offers optimized power consumption and reduction of TV cost-price.

II - MAIN FUNCTIONS

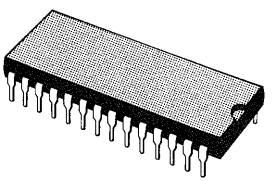
- Detection and extraction of line and frame synchronization pulses from the composite video signal.
- Horizontal scanning control and synchronization by two phase-locked loop devices.
- Video identification.
- 50 or 60Hz standard recognition for vertical scanning.
- Generation of a self-synchronized frame sawtooth for 50/60Hz standards.
- Line time constant switching for VCR operation through an input labeled "VCR" (Video Cassette Recorder).
- Control and regulation of a primary-connected switching power supply by on-chip controller device combining :
  - an error amplifier
  - a pulse width modulator synchronized on line frequency
  - a start-up and protection system

- Overall TV set protection input
- Frame blanking and super sandcastle output signals
- Frame blanking safety input for CRT protection in case of vertical stage failure.

III - PIN CONNECTION (TEA2028B)

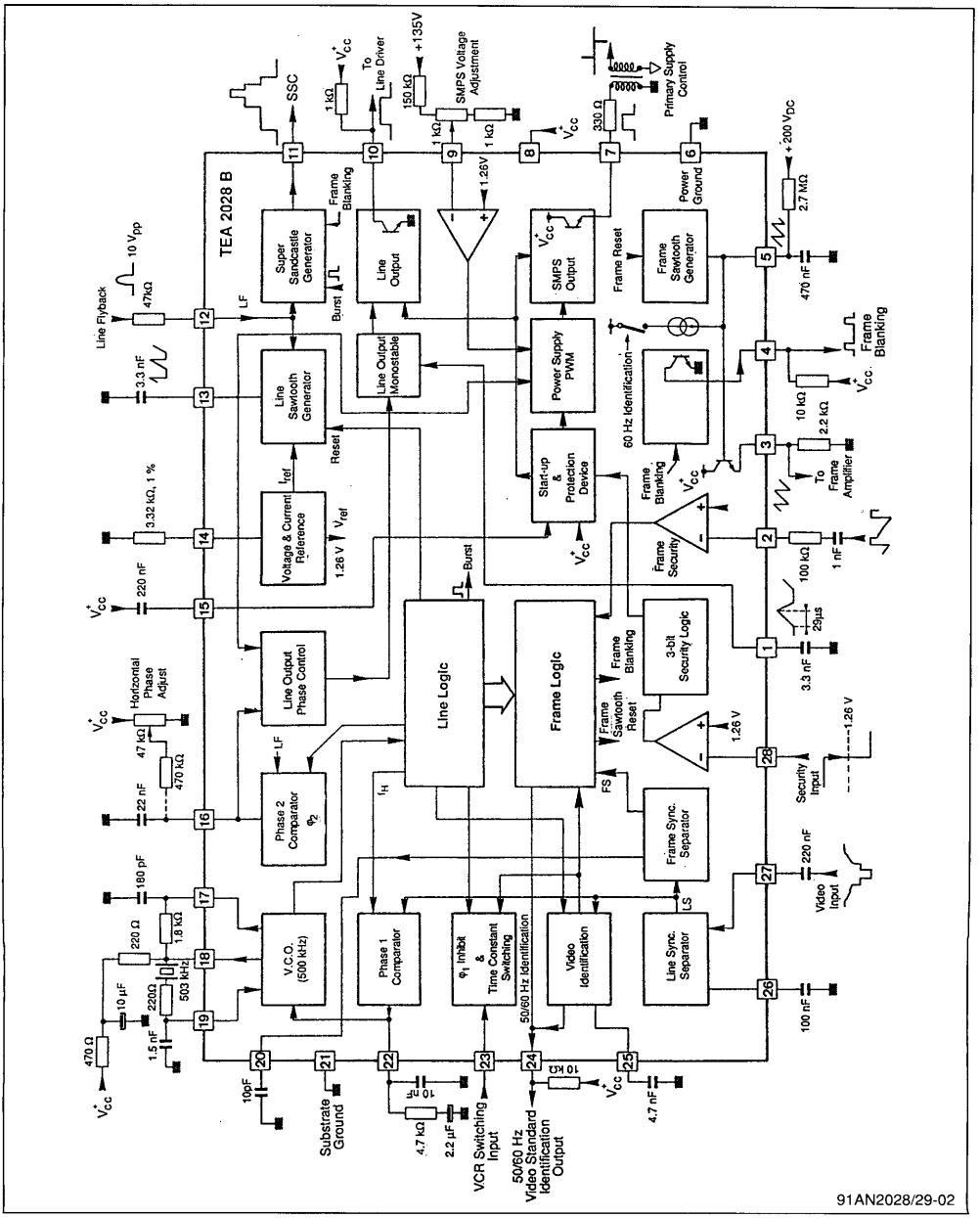
Pin Number	Description
1	Horizontal output monostable capacitor
2	Frame blanking safety input
3	Frame saw-tooth output
4	Frame blanking output
5	Frame ramp generator
6	Power ground
7	SMPS control output
8	Supply voltage (V_{CC})
9	SMPS regulation input
10	Horizontal output
11	Super-sandcastle output
12	Horizontal flyback input
13	Horizontal saw-tooth generator
14	Current reference
15	SMPS soft-start and safety time constant capacitor
16	$\phi 2$ phase comparator capacitor (and horizontal phase adjustment)
17	V_{CO} phase shift network
18	V_{CO} output
19	V_{CO} input
20	Frame sync time constant adjustment capacitor
21	Substrate Ground
22	$\phi 1$ phase comparator capacitor
23	VCR switching input
24	Video and 50/60Hz identification output (Mute)
25	Video identification capacitor
26	Horizontal sync detection capacitor (50% of peak to peak sync level)
27	Video input
28	Safety input

Package : DIP28



IV. INTERNAL BLOCK DIAGRAM

Figure 2



V. FUNCTIONAL DESCRIPTION

Majority of the on-chip analog functions were computer simulated and results such as temperature variation, technological characteristic dispersion and stability, have led to the enhancement and implementation of actually employed structures. A parallel in-depth study of the device implemented in form of integrated sub-sections is provided to analyze the overall performance in a TV set.

V.1 - Internal voltage and current references

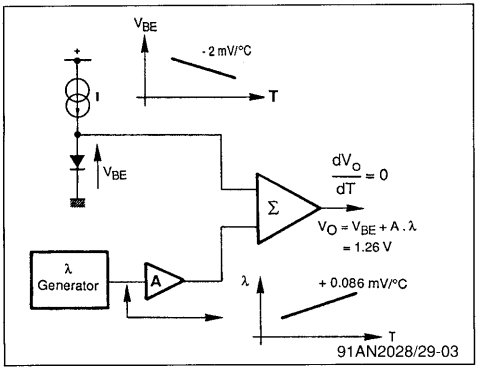
V.1.1 - 1.26V Voltage reference

For optimum operation of the device, an accurate and temperature-stable voltage generator independent from V_{CC} variations is used (Band-gap type generator).

The generated 1.26 V is particularly used as reference setting on input comparators.

V.1.1.1 - Generator block diagram

Figure 3



$$\text{with } \lambda = \frac{K \cdot T}{q} = 25.7\text{mV at } +25^{\circ}\text{C}$$

$$\frac{d\lambda}{dT} = \frac{K}{q} = +0.086\text{mV}/^{\circ}\text{C}$$

$$\frac{dV_{BE}}{dT} = \frac{V_{BE(25^{\circ})} - 1.26}{T} = -2\text{mV}/^{\circ}\text{C}$$

If $A\lambda = 1.26 - V_{BE}$

Then : $V_O = 1.26\text{V}$ (temperature-independent)

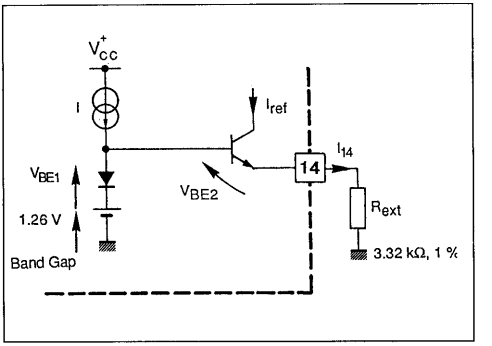
In practice, maximum drift due to temperature can be +0.23 mV/°C

i.e., ± 1.5 % for a ΔT of 80°C.

V.1.2 - Current reference

This is implemented using the 1.26V generator in combination with an external resistor.

Figure 4



$$I_{REF} \approx I_{14} = \frac{V_{14}}{R_{EXT}} = \frac{1.26 + V_{BE1} - V_{BE2}}{R_{EXT}}$$

Let's $I_{14} = I$ and $V_{BE1} = V_{BE2}$

then : $I_{REF} = \frac{1.26}{R_{EXT}} = 380\mu\text{A}$

91AN2028/29-04

Thus, it follows that I_{REF} is accurate and independent of both V_{CC} and temperature.

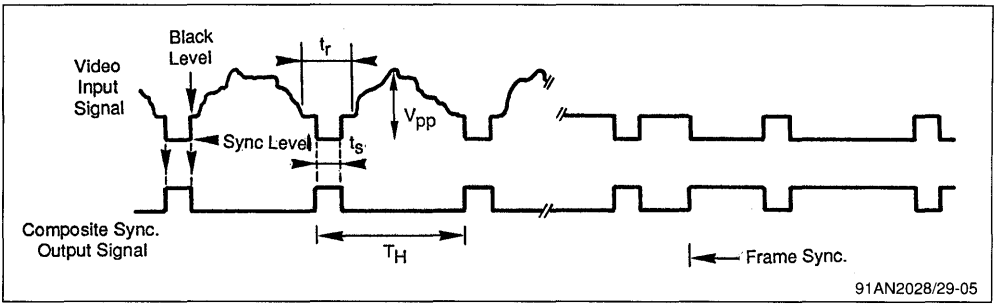
A set of current generators proportional to I_{REF} current are used in various circuit blocks.

V.2 - Line sync. extraction

Horizontal and vertical time bases should be synchronized with corresponding sync. pulses transmitted inside the infra-black portion of video signal. The duty of this stage is to extract these sync pulses. The output signal, called composite sync, contains the vertical sync which is transmitted by simple inversion of line sync. pulses.

The vertical sync pulse is then extracted from this composite signal.

Figure 5



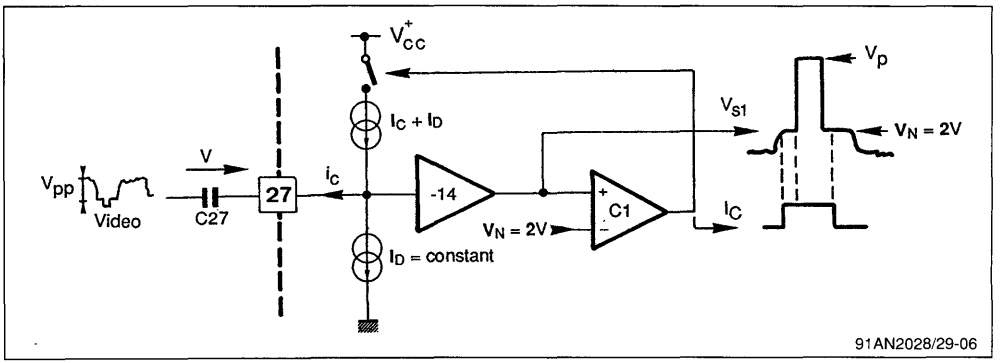
The main advantage of this arrangement is its ability to operate at video input signal levels falling within 0.2V to 3V peak-to-peak range and at any average value.

The operating principle is to lock the black level of the input signal (pin 27) onto internaly fixed voltage (V_N) and then memorize the average voltage of the sync pulse by using an integrating capacitor connected to pin 26.

Finally, the composite sync signal is delivered by a comparator the inputs of which are driven by $V_{50\%}$ and video signals.

V.2.1 - Black level locking

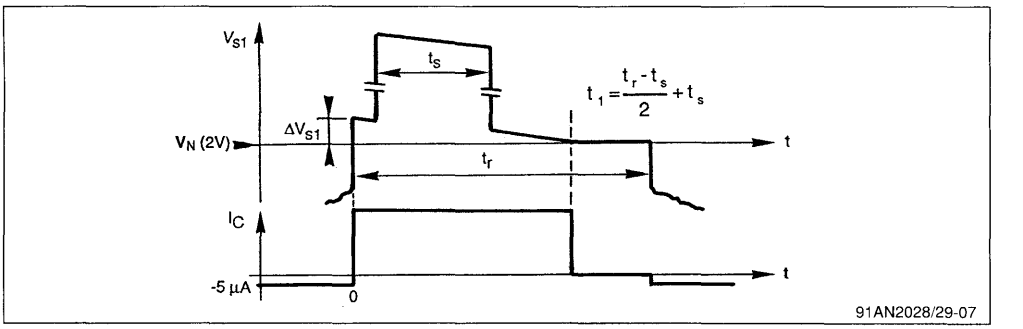
Figure 6



The video signal is applied to pin 27 through the coupling capacitor "C27". Since the sync pulse amplitude is generally equal to 1/3 of V_{PP} (i.e. 66mV to 1V) and in order to obtain a good precision of the black level, the sync pulse should be amplified by a coefficient of - 14 before being applied to the comparator "C1". This comparator will charge the "C27" capacitor as long as $V_{S1} > V_N$. V_{S1} will stabilize at V_N during the line flyback interval "T_r" if the average charge of "C27" capacitor is nil for one T_H period.

I_C/I_D is calculated such that the locking occurs at the middle of the back porch.

Figure 7



The ΔV_{S1} produced by I_D during the line trace which is :

$$14 \times \frac{I_D \cdot t_A}{C_{27}}$$

must be equal to ΔV_{S1} during the time interval "t1", i.e. :

$$14 \times \frac{I_C \cdot t_1}{C_{27}}$$

It follows that :

$$\frac{I_C}{I_D} = \frac{t_A}{t_1} = \frac{T_H - t_R}{t_s + \frac{t_R - t_s}{2}}$$

substituting $T_H = 64\ \mu s$, $t_r = 12\ \mu s$, $t_S = 4.7\ \mu s$ (which are standard and constant values) into above *equation* : $\frac{I_C}{I_D} = 6.23$

V.2.1.1 - Application

At $I_C = 5\mu A \Rightarrow I_D = 31\ \mu A$

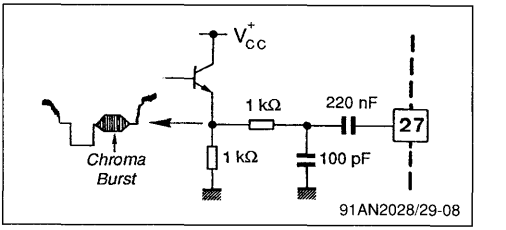
- With C27 = 220nF, ΔV_S will be

$$14 \times \frac{5 \times 52}{220} = 16\ mV$$

which yields 0.8 % maximum error in black level with respect to V_N = 2V at the beginning of retrace time

- Due to transposition on amplifier stage, the black level voltage on pin 27 is equal to 2V.
- In practice, at low amplitude video signals, it is recommended to insert a low-pass filter before the "C27" capacitor so as to attenuate the chrominance sub-carrier and the noise components. The aim is to reduce the phase variations of the detected sync pulse and thus enhance the horizontal scanning stability.

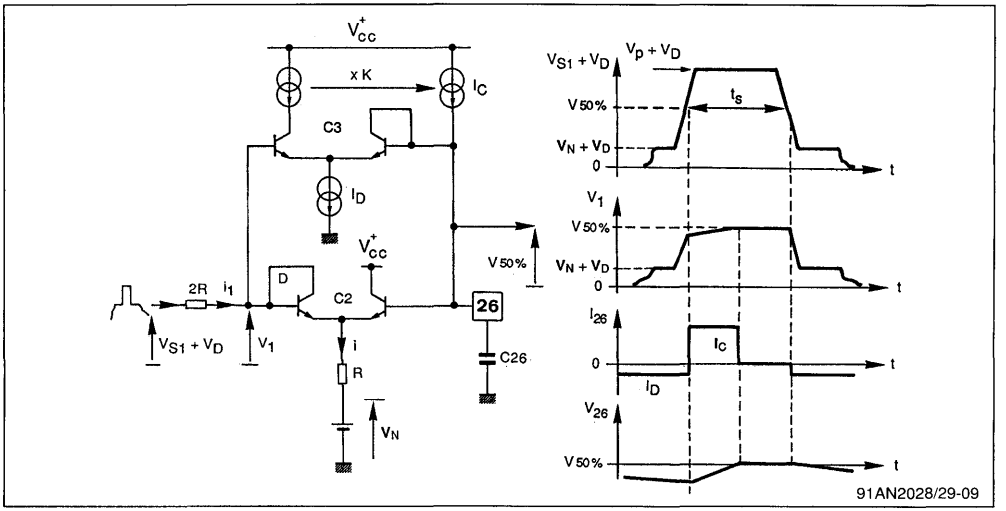
Figure 8



V.2.2 - Memorizing the sync pulse 50% value

The objective is to memorize the voltage corresponding to 50 % of the line sync pulse V_{S1} by using an external capacitor connected to pin 26.

Figure 9



The overall arrangement comprises two comparators.

- Comparator C2 : delivers an output voltage "V1" by comparing $V_{S1} + V_D$, V_{26} and the voltage drop across two resistors.
- Comparator C3 : which delivers a constant output current thereby maintaining on capacitor "C26", the voltage $V_{50\%}$ corresponding to 50% of peak to peak sync pulse.

During the line scanning, diode "D" is reverse biased : $V_{S1} + V_D = V_1 < V_{26}$ and C3 will deliver a current I_D which will discharge the capacitor.

During sync pulse interval, $V_{S1} + V_D = V_P + V_D$, diode "D" begins conducting and thus :
$V_1 = (V_P + V_D) - (2\ R\ i_1)$. Since the capacitor has been slightly discharged $\Rightarrow V_1 > V_{26}$, comparator C3 begins charging the capacitor until C2 is brought to equilibrium. At this time,

$$I_1 = \frac{i}{2} \text{ where } i = \frac{V_{26} - V_D - V_N}{R}$$

$$\text{thus } V_1 = V_P + V_D - 2R\frac{i}{2} = V_P + V_N + 2V_D - V_{26}$$

$$\text{and } V_1 = V_{26} \Leftrightarrow V_{26} = \frac{V_P + V_N}{2} + V_D = V_{50\%}$$

A high value C26 capacitor will thus memorize the voltage level corresponding to 50% of the line sync. pulse.

V.2.2.1 - $\frac{I_C}{I_D}$ Ratio calculation

During the line scanning period (T_H - T_S), the capacitor C26 will loose a charge equivalent to : $I_D (T_H - T_S)$.
This energy must be recovered before the end of sync pulse such that : $I_C \cdot t_S > I_D (T_H - T_S)$

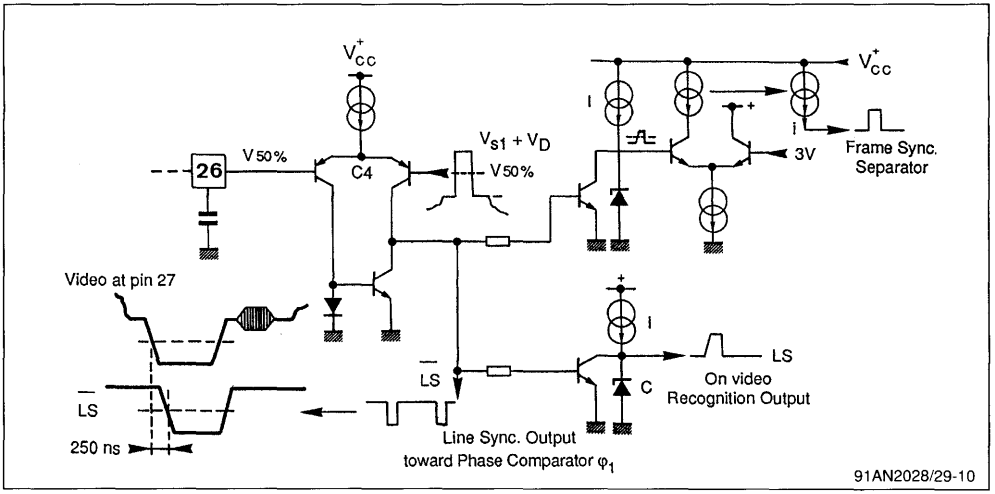
$$\text{therefore } \frac{I_C}{I_D} > \frac{T_H - t_S}{t_S} \qquad \frac{I_C}{I_D} > 12.6$$

In practice, for C26 = 100nF, I_D = 25µA and I_C = 800µA

V.2.3 - Sync pulse detection

This function is fulfilled by comparing the inverted video signal ($V_{S1} + V_D$) whose black level is constant at 2V, with the sync 50% voltage level on pin 26.

Figure 10



Comparator C4 will deliver the line sync pulse (LS) which will be used for 3 functions :

- Horizontal scanning frequency locking : output to $\phi 1$ phase comparator.
- Frame sync extraction for vertical scanning synchronization.
- Detecting the presence of a video signal at circuit input.

The LS signal in two latter functions is filtered for noise by using combination of current generator I and a zener diode equivalent to a capacitor.

Using this extraction technique at a very noisy video signal yields remarkable display stability.

The device also provides for scanning synchronization at aerial signal attenuation of approximately 75dB, i.e. 15 to 20dB better than other sync processors.

V.3 - First phase locked-loop stage "$\phi 1$"

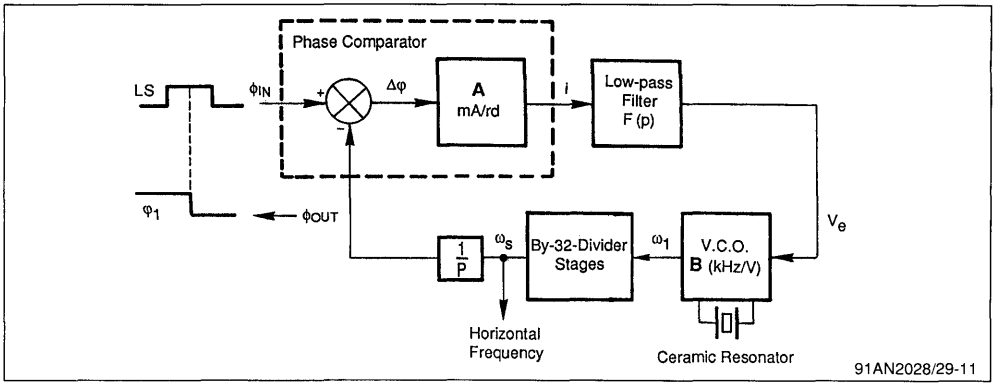
This stage is commonly called the first Phase Locked-Loop "$\phi 1$".

Its duty is to lock the frequency and the phase of the horizontal time base with respect to the line sync signal.

In the absence of transmission (i.e. lack of line sync), the horizontal scanning frequency is obtained by dividing the output frequency of a VCO device. This VCO oscillates at approximately 500kHz and uses a low frequency drift ceramic resonator. This method eliminates the need of horizontal frequency adjustment.

V.3.1 - Phase locked-loop "ϕ1" block diagram

Figure 11



V.3.2 - Functional duty of individual blocks

V.3.2.1 - Phase comparator

The duty of this comparator is to issue an output current proportional to the phase difference between ϕ_{IN} and ϕ_{OUT}.

V.3.2.2 - Low-pass filter

This filter suppresses the parasitic component containing the sum of phases, smoothens the phase difference component and determines the timing characteristics of the loop.

V.3.2.3 - VCO centered on 500kHz

This is a voltage-controlled oscillator which generates an output frequency proportional to the voltage applied to its input.

This voltage is delivered by low-pass filter.

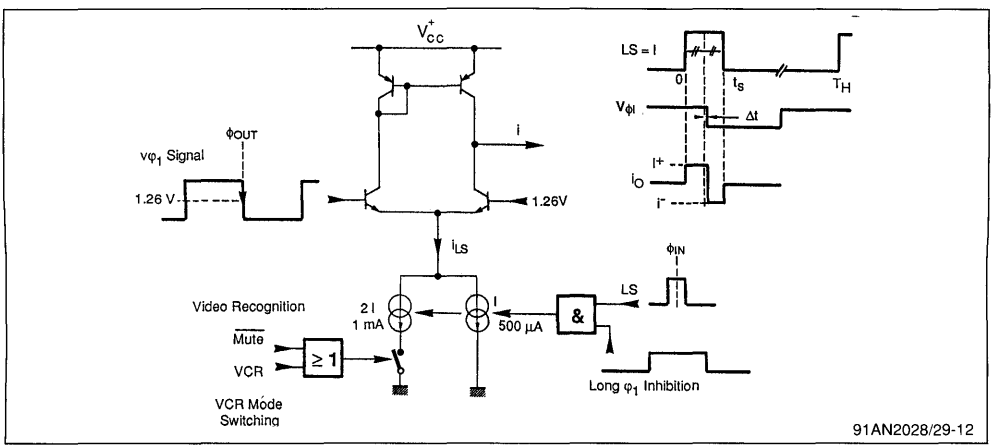
V.3.2.4 - Divider stage

It is used to divide the VCO frequency (500kHz) by 32 so that it can be compared with the line sync signal frequency of 15625Hz.

V.3.3 - Functional description of building blocks

V.3.3.1 - Phase comparator "ϕ1"

Figure 12

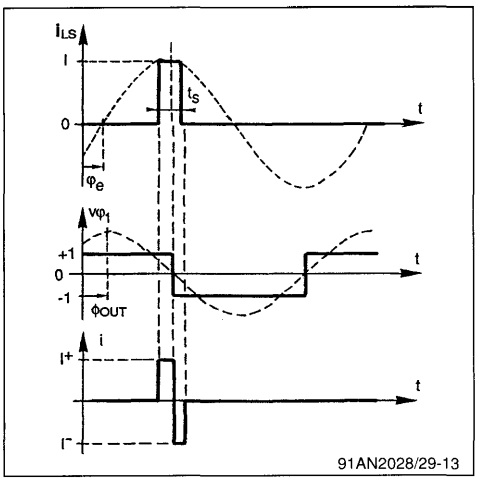


The comparator is functionally equivalent to a signal multiplier.

Let's assume that :
$i_{LS} = I \sin(\omega_H t + \phi_{IN})$
and $V_{\phi 1} = k \cos(\omega_H t + \phi_{OUT})$
then :

$$i = \frac{i_{LS} \cdot k}{2}\left[\sin\Phi_{IN} - \Phi_{out}) + \sin(2\omega_H t + \Phi_{IN} + \Phi_{out})\right]$$

Figure 13



- the low-pass filter will suppress the $2f_H$ frequency component
- ϕ_{IN} - ϕ_{OUT} difference being low :
  $\sin(\phi_{IN} - \phi_{OUT}) \approx \phi_{IN} - \phi_{OUT}$
- the output current will be therefore proportional to the phase difference between the signals compared.

In other words, the average current over one period is :

$$i_{AV} \times T_H = I\left(\frac{t_S}{2} + \Delta t\right) - I\left(\frac{t_S}{2} - \Delta t\right) = 2I\,\Delta t$$

$$i_{AV} = 2I\frac{\Delta t}{T_H} \text{ and } \Delta t = \Delta\Phi\frac{T_H}{2\pi}$$

The comparator conversion gain is thus :

$$A = \frac{i}{\Delta\Phi} = \frac{I}{\pi} \text{ (inA/rd)}$$

Later in our discussion we shall consider the two possible values of the current I.

For the time being, let's define these values as follows :

- I = 500µA for "long time constant" or normal operation
- I = 1.5mA for "short time constant" VCR mode or synchronization search (Mute).

The values of A are therefore :

- A_{LONG} = 0.16 mA/rd
- A_{SHORT} = 0.47 mA/rd

Use of comparator inhibition signal is quite useful under noisy transmission conditions. It eliminates risk of incorrect comparison during the line scanning phase which would be due to the noise present on LS signal. Horizontal phase and image stability are thus highly enhanced.

Characteristics of this inhibition signal will be discussed at the end of this chapter.

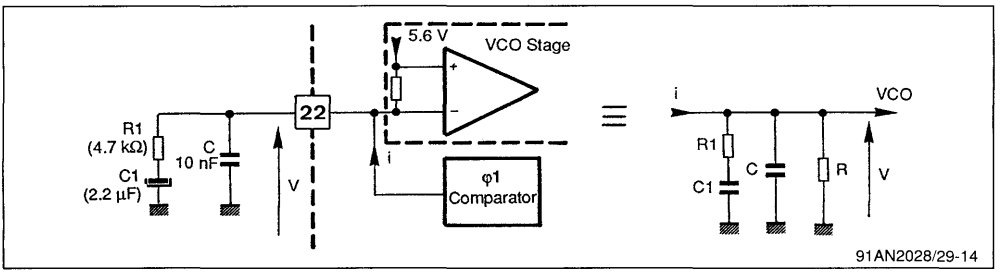
V.3.3.2 - Low-pass filter

- Its main function is to reject the $2f_H$ (31kHz) frequency component delivered by the phase comparator.
- It also defines the characteristics of the loop in transient mode.

The filter is built around two sub-sections which determine the stability and the response time of the loop in the following modes of transmission :

- Normal or VCR modes. See section V.3.6 "Dynamic study of φ1".

Figure 14



R is the dynamic input resistance of the VCO.
The filter transfer function may be defined as follows :

$$f(p) = \frac{V}{i} = Z(p)$$

$$Z(p) = R\frac{1 + R1C1p}{1 + p(RC + R1C1 + RC1) + RR1CC1p^2}$$

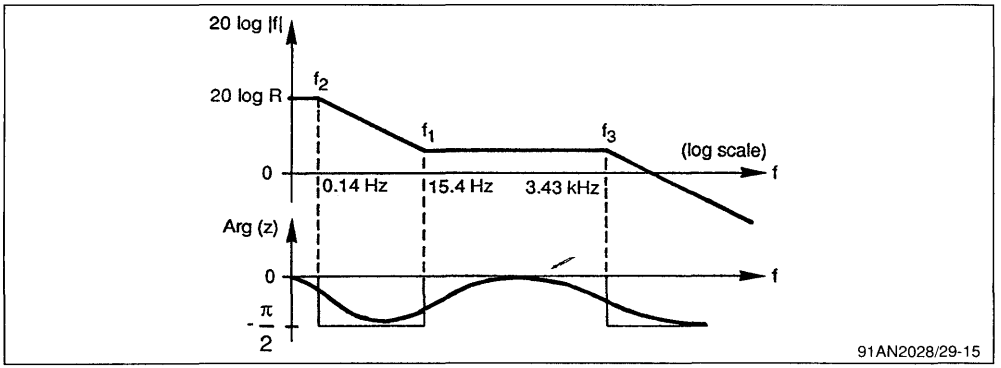
The second order terms of the denominator can be converted to first order products as a function of frequency as follow :

$$f(jf) = R\frac{1 + j\frac{f}{f1}}{(1 + j\frac{f}{f2})(1 + j\frac{f}{f3})}$$

with R1 = 4.7kΩ, R = 500kΩ, C1 = 2.2µF, C = 10nF we obtain :

- $f1 = \frac{1}{2\pi R1C1} = 15.4Hz$
- $f2 = \frac{1}{2\pi(RC1 + RC + R1C1)} = 0.14Hz$
- f3 = 3.43kHz

Figure 15



V.3.3.3 - VCO (Voltage Controlled Oscillator)

Its function is to generate a frequency proportional to a control voltage issued externally, by the low-pass filter in our case.

The period of the output signal is used as timing reference for various functions such as, horizontal and vertical time bases. The frequency range must be short and accurate :

- It must be short since the power dissipated within the horizontal scanning block is inversely proportional to the line frequency.
- The accuracy is required if the adjustment is to be omitted.

The basic arrangement is to employ a ceramic resonator (or ceramic filter) which has quite stable characteristics as a function of frequency.
A filter whose resonating frequency is a multiple of line frequency (15625Hz) is to be selected. An example is 32 x 15625 = 500kHz.

a. 503 kHz Ceramic Filter

Figure 16

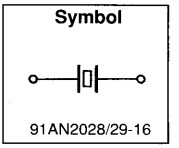
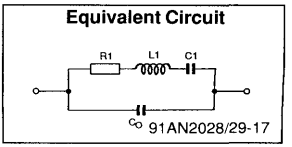


Figure 17



Where :

R1 = 7Ω, L1 = 1.26 mH, C1 = 78 pF, CO = 507 pF

- Series resonance frequency :

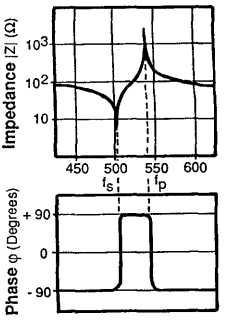
$$f_S = \frac{1}{2\pi\sqrt{L1C1}} = 503kHz$$

- Parallel resonance frequency :

$$f_P = f_S \cdot \sqrt{1 + \frac{C1}{C_0}} = 540kHz$$

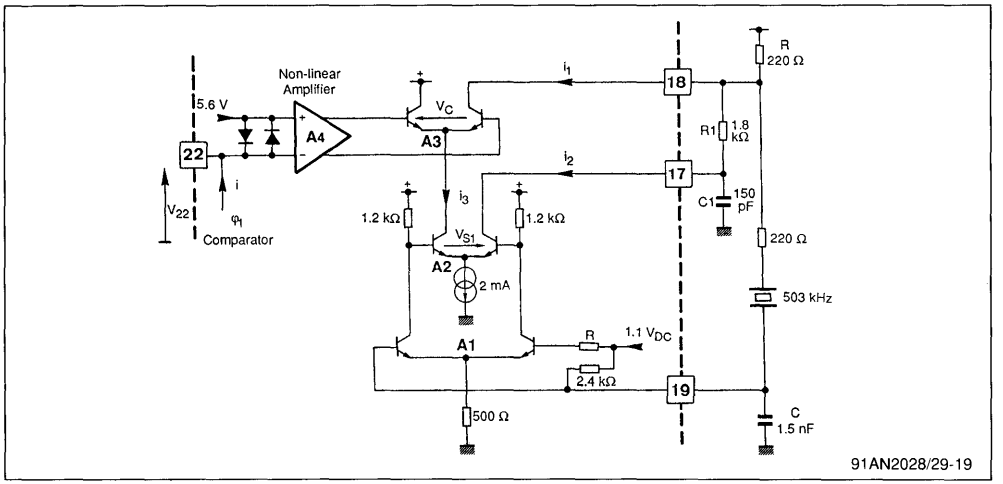
- Tolerance within the resonance area :
  503kHz ± 0.3 %
- Temperature stability :
  ±0.3 % of f_O at $\Delta T = 100\ ^{\circ}C$

Figure 18



b - Simplified Block Diagram of VCO

Figure 19



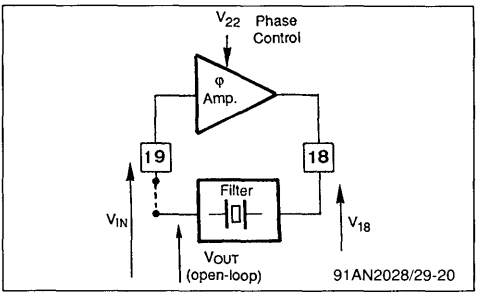
The overall arrangement is equivalent to a variable-phase amplifier configured in closed loop with the external passive filter.

The system will oscillate if the open-loop gain is 0dB and if VOUT leads VIN.

In closed-loop oscillating mode, the phase variation of V_{18}/V_{IN} imposed by V_{22} will result in same V_{OUT}/V_{18} variation but of opposite sign.

This phase change will finally correspond to a change in frequency.

Figure 20

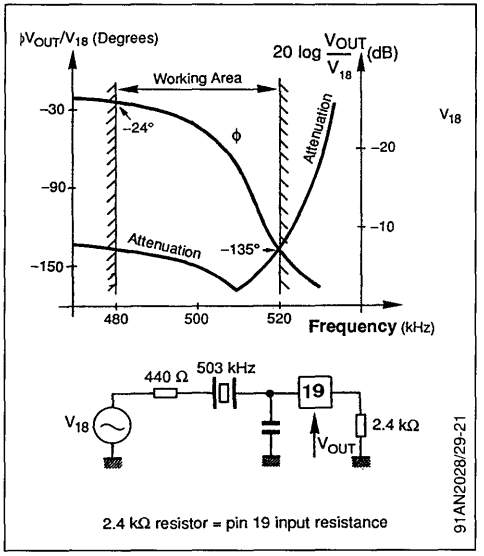


c. - Characteristics of the External Filter

The ceramic resonator behaves as a capacitor at $f < f_S$ (f_S : series resonance frequency) and as an inductor at frequencies falling between its two resonance frequencies.

Combined with a "R.C" network to generate a 90° phase lag, the overall arrangement will exhibit the following characteristics :

Figure 21



Thus, a variable (24° to + 135°) phase lead with a gain higher than 10 dB, must be implemented on-chip so as to enable the system to enter into oscillation.

The frequency dead points correspond to the maximum internal phase variations. This phase shift is controlled by voltage V_{22} whose value of 5.6V ± 0.7 is determined by two diodes.

From the above Figure, the non-linearity of phase-frequency characteristics is clearly apparent. If linear voltage-frequency response is required for a symmetrical gain of φ1 loop, it would then be necessary to implement a non-linearity, on the phase control amplifier A4, but in the opposite direction.

d. - Study of the Internal Amplifier

Let's study the gain and phase response of $\frac{V_{18}}{V_{IN}}$

as a function of V_{22}.

$V_{22} = \frac{V_C}{K}$ where K is a non-linear coefficient

To start with, the "V_C" voltage of comparator "A3" is taken as reference parameter.

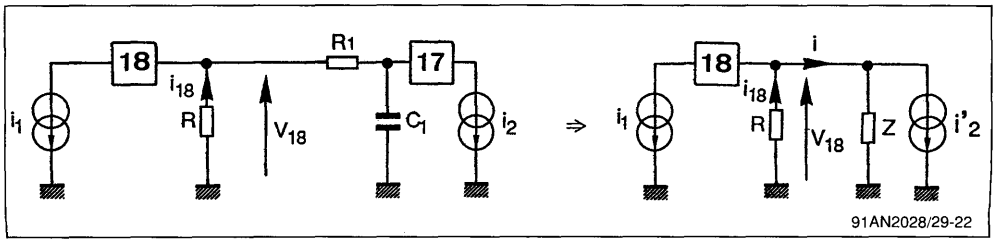
The dynamic representation of the output stage can be depicted as below (figure 22).

with : $I_2' = \frac{i_2}{1 + j\omega R_1 C_1}$ (at f = 500kHz)

$R_1C_1\omega = 1 \Rightarrow i_2' = \frac{i_2}{1+j}$

and $Z = R_1 + \frac{1}{j\omega C} << R \Leftrightarrow i \approx i_2'$

Figure 22



R1C1 network produces -45° phase lag of "i" with respect to "i2", around 500kHz.

$V_{18} \approx -R \cdot (i1 + I'_2)$

i1 AND i2 calculation as a function of "V_{in}" on pin 19

- A1 Amplifier : $\frac{V_{S1}}{V_{In}} = \frac{R_C}{dr_1} = \frac{1200}{57} = 21$

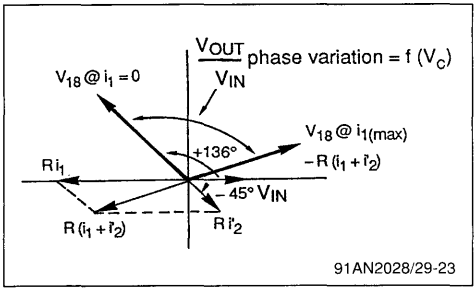
dr : dynamic resistance = $\frac{\lambda}{I}$

- A2 Amplifier : $\frac{i_2}{V_{S2}} = \frac{1}{2dr_2} = \frac{1}{54}$

$\Leftrightarrow \frac{i_2}{V_{IN}} = \frac{V_{S1}}{V_{IN}} \times \frac{i_2}{V_{S1}} = 0.395 \rightarrow i_2 = 0.39\ V_{IN}$

- i_2 is in phase with V_{IN} therefore : $i_3 = -i_2 = -0.39\ V_{IN}$

Figure 23 : Vector representation of V_{18}/V_{IN}



- A3 Amplifier :

$$i_1 = i_3 - \left(\frac{V_C}{4\lambda} + \frac{1}{2}\right) = -0.39\ V_{IN}\left(\frac{-V_C}{4\lambda} + \frac{1}{2}\right)$$

"V_{IN}" always leads the "i_1" by 180, only the amplitude of i1 is a function of V_C (See figure 23).

- $\frac{V_{OUT}}{V_{IN}} = -R\,\frac{i_1(1 + jR_1C_1\omega) + i_2}{1 + j(R_1 + R)C_1\omega}$
- $i1 = -0.39\ V_{IN}\left(\frac{i}{2} - \frac{V_C}{4\lambda}\right)$ and $i2 = 0.39\ V_{IN}$

The following figure 24 illustrates the characteristics of V_{18}/V_{IN} phase versus V_C.

- Phase variation determined by V_C falls between $+24^o$ and $+135^o$ range
- The gain is higher than 10 dB. The pin 18 output signal of 30 to 40 dB has a rectangular component (See figure 24).

e. - Characteristics of the non-linear Amplifier "A4"

This is a differential amplifier whose equivalent feed-back resistors of emitters vary as a function of its input voltage.

Figure 25 : $V_C = F(V_{22})$

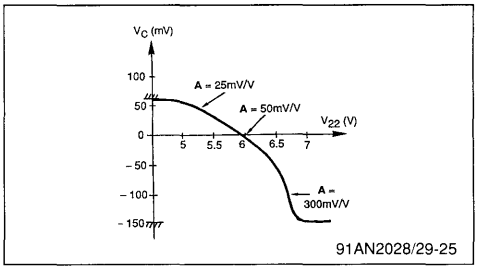
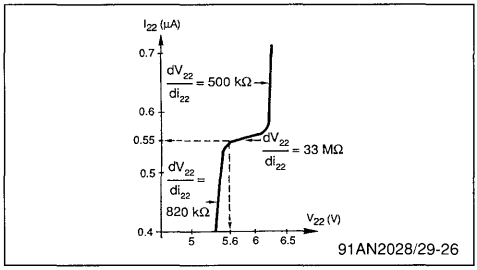


Figure 26 : $I_{22} = F(V_{22})$



The maximum output voltage swing is set by two "clamp" diodes connected to "V_{22}" input.

f. - Voltage-frequency transfer characteristics of VCO

The transfer characteristic is linear and centered at 5.6V at 500kHz operating frequency.

- T transfer $= \frac{\Delta f}{\Delta V} = 22.4$kHz/V and once it goes through five divide-by-two stages :

$T = \frac{22.4}{32} = 0.7$kHz/V

Figure 24

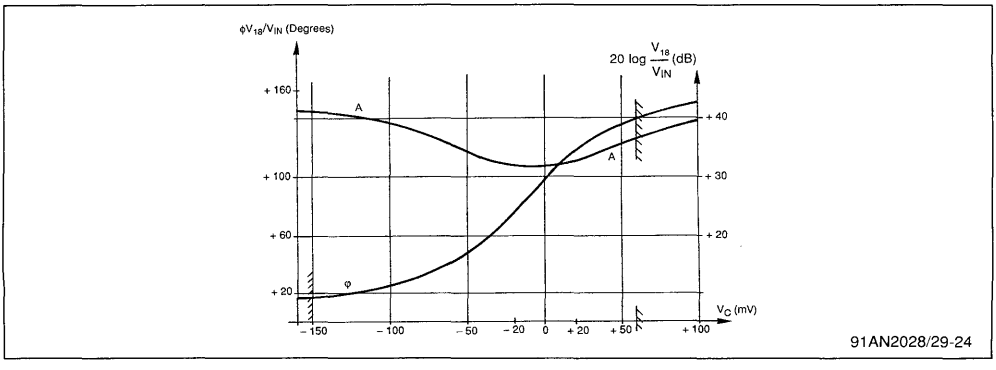
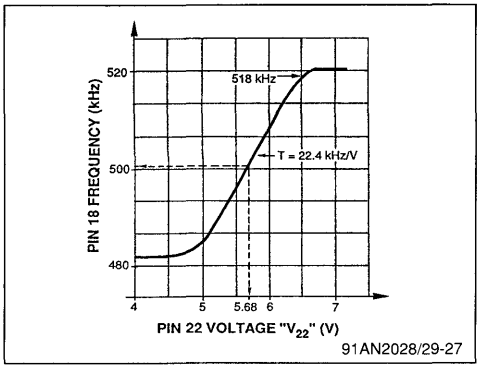


Figure 27



V. 3.4. - "ϕ1" time constant switching

When switching between stations or receiving signal via a VCR, the loop locking interval must be as short as possible so as to avoid unwanted visible effect on the picture. In fact, since the synchronization between the VCR motor drive and the playback head is rather imperfect, it will produce frequency and phase fluctuations in the output composite video signal. Under these conditions, phase locking interval must be "short" (VCR Mode).

In the case of broadcast transmission, this loop must also filter all phase variations produced by noisy sync signal. In this case, its locking time constant must be "long" (normal mode).

In other "jungle" circuits, this time constant switching is carried out by capacitor switching within the filter loop. In our case, this function is achieved by changing the current amplitude of the phase comparator.

This amplitude changing modifies the open-loop system gain and therefore the damping coefficient and the locking time constant.

The device will be in short time constant mode under the following two conditions :

- VCR Mode or SCART Connector Mode :
  This mode is enabled by a low state on pin 23. V23 < 2.1 V.
- Transmitter search and tunning.
  In order to accelerate the capture, a "Video Identification" stage will detect the presence or the absence of a video signal on input pin 27, and deliver accordingly a signal called "Mute".

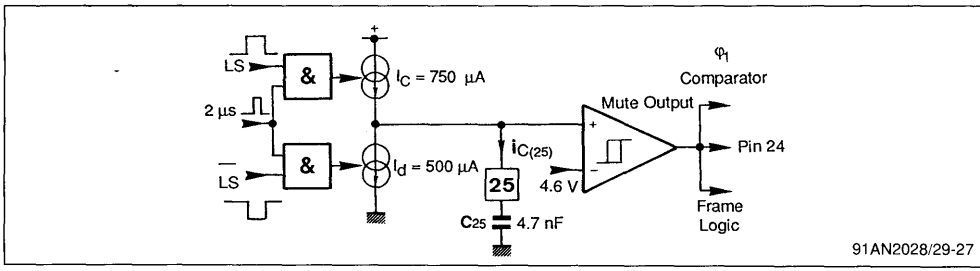
V.3.5 - Video identification stage

This stage will detect the coincidence between the line sync pulse (if present) and a 2µs pulse issued from the logic block. This 2µs pulse at line frequency is positionned at the center of line sync pulse when the first loop "φ1" is locked.

This sampled detection is stored by an external capacitor connected to pin 25. The video recognition status is also available on pin 24 so as to enable Sound Muting during station search process and the inhibition of Automatic Frequency Tuning.

V.3.5.1 - Block diagram

Figure 28



The video recognition signal is delivered by a hysteresis comparator.

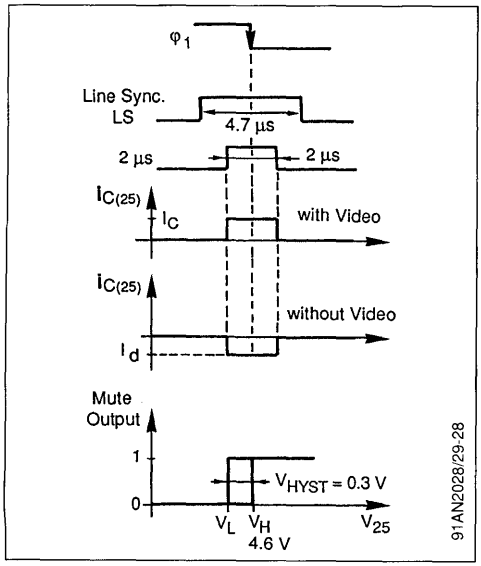
The recognition time "Tr" is adjustable by an external capacitor, as soon as φ1 is locked :

- $I_{C25(AV)} = I_C \times \frac{2\ \mu s}{64\ \mu s}$

and :

- $T_R = C_{25} \times \frac{V_H}{I_{C25(AV)}} = 1.96 \times 10^5 \times C_{25}$
- with C_{25} = 4.7 nF ⇒ Tr = 1 ms (which is clearly quite fast)

Figure 29



V.3.6 - Characteristics of loop φ1

V.3.6.1 - Locking accuracy

Let's study the phase error "φ_{OUT} - φ_{IN}" under steady state conditions :

The open-loop gain is :

- $T(p) = \frac{AB\ f(p)}{f}$

Where :

- A = 0.16 mA/rd (long time constant)
- A = 0.47 mA/rd (short time constant)
- B = 0.7 kHz/V or B = 4.4 10^3 rd/s

- $f(p) = R \times \frac{1 + \tau_1 p}{(1 + \tau_2 p)(1 + \tau_3 p)}$

Where :

- R = Dynamic input resistance of VCO.

If a phase step of $\Delta\varphi$ is applied to the input, the following would be obtained as a function of (p) :

$$\Phi_{IN}(p) = \frac{\Delta\Phi}{p}$$

Using the last value theorem : lim f(t) = lim p . f(p)

Let's calculate $\lim_{p \to 0} (\varphi_{IN} - \varphi_{OUT})$

- The closed-loop gain is :

- $H(p) = \frac{T(p)}{1 + T(p)} = \frac{ABf(p)}{p + ABf(p)} = \frac{\Phi_{OUT}(p)}{\Phi_{IN}(p)}$

that is : $\lim_{p \to 0} p(\Phi_{IN} - \Phi_{OUT}) = \lim_{p \to 0} \frac{p\Delta\Phi}{p + AB\ f(0)} \to 0$

It is therefore deduced that the system can follow all input phase variations without producing any static error.

In practice, there will be a slight error due to the input bias current "I_B" of VCO, which is 0.55µA at f_O = 500kHz. This DC current is delivered by a phase comparator which will generate a phase error of :

- long time constant :

$$\Delta\Phi_{LONG} = \frac{I_B}{A_{LONG}} = 0.55 \times \frac{10^{-3}}{0.16} = 3.4 \times 10^{-3} rd$$

or 35ns in Δt

- short time constant :

$$\Delta\Phi_{SHORT} = \frac{I_B}{A_{SHORT}} \equiv 12ns$$

These two errors cause a horizontal picture displacement. On a large screen of 54cm wide, this will be : 64 - 12 = 52µs, which for both modes corresponds to a shift of :

$$\Delta_{LINE} = \frac{\Delta\Phi_{LONG} - \Delta\Phi_{SHORT}}{52} \times 520 = 0.24 \text{ mm}$$

It is obvious that such displacement can be fully neglected.

Response to a Frequency Step

- The input phase is : $\Phi_{IN}(t) = \Delta\omega t$

  which as a function of (p) is : $\Phi_{IN}(p) = \frac{\Delta\omega}{p^2}$

- The accuracy is :

$$\lim_{p->0} (\Phi_{IN} - \Phi_{OUT}) = \lim_{p->0} \frac{\Delta\omega}{p + ABf(o)} = \frac{\Delta\omega}{ABR}$$

where R = 500kΩ at f(o)

In this case, the phase error depends on both, the magnitude of the frequency step and the static gain ABR.

In general, $\frac{\Delta f}{\Delta f}$ which is the open-loop static gain, is taken into consideration.

$$\frac{\Delta\omega}{\Delta\Phi} = ABR = \frac{2\pi\Delta f}{\Delta t \times 2\pi} = A \cdot 2\pi \cdot B' \cdot R$$

$$\Rightarrow \frac{\Delta f}{\Delta t} = AB'R \times \frac{2\pi}{T_H} \text{ (B' in kHz/V)}$$

- In normal mode : A_{LONG} = 0.16 mA/rd

  $\Rightarrow \frac{\Delta f}{\Delta t} = 5.5 kHz/\mu s$ R = 500kΩ

- In VCR mode : A_{SHORT} = 0.47 mA/rd

  $\Rightarrow \frac{\Delta f}{\Delta t} = 16.5 kHz/\mu s$

Note : The capture range is specified within ± 500 Hz with respect to 15625 Hz.

Numerical Example

Let's suppose that in VCR mode there is a frequency variation of ± 100Hz, this will yield a phase variation of 0.1/16.5, i.e. ± 6ns which, on a 54 cm wide screen, will produce a horizontal shift of Δ_{LINE} = ± 0.06 mm !

It is obvious that an excellent image stability is thus obtained.

V.3.6.2 - Dynamic study

The loop response in transient mode is quite important. It determines the overall system stability and the phase recovery time, which are imposed by the external filter "f(p)".

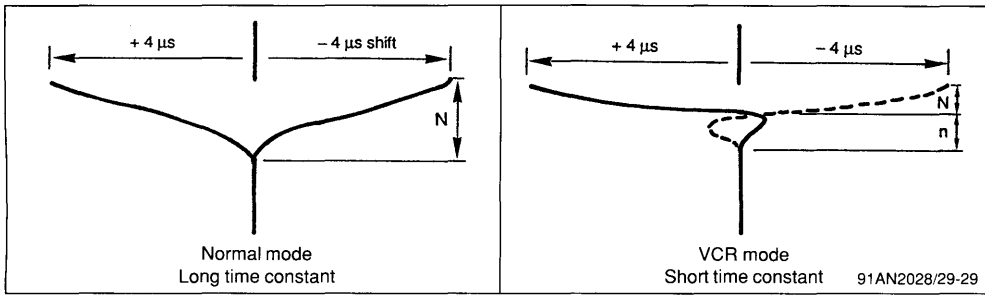
The close-loop transfer function is equivalent to a second order system. These time constants are in practice displayed on screen by a bar delivered by a special pattern generator representing the phase errors.

The following optimized results were obtained from filter f(p) connected to pin 22.

Filter component values are :

R1 = 4.7kΩ, C1 = 2.2µF, C = 10nF

Figure 30 : On Screen Display of Time Constants



Where :

N : number of lines required for phase correction

n : number of lines required for the horizontal oscillator to fully stabilize

a. Long time constant

- At Δt of 4µs ⇒ N=18 lines, i.e. τ_{LONG} = 1.15ms. System oscillations are perfectly damped. Image stability with a noisy video signal is very satisfactory.

b. Short time constant

- At Δt = 4µs ⇒ N = 5 lines, i.e. τ_{SHORT} = 0.32ms
- n = 5 lines

One should notice fast phase recovery, naturally followed by bounced oscillations due to the characteristics of a second order device.

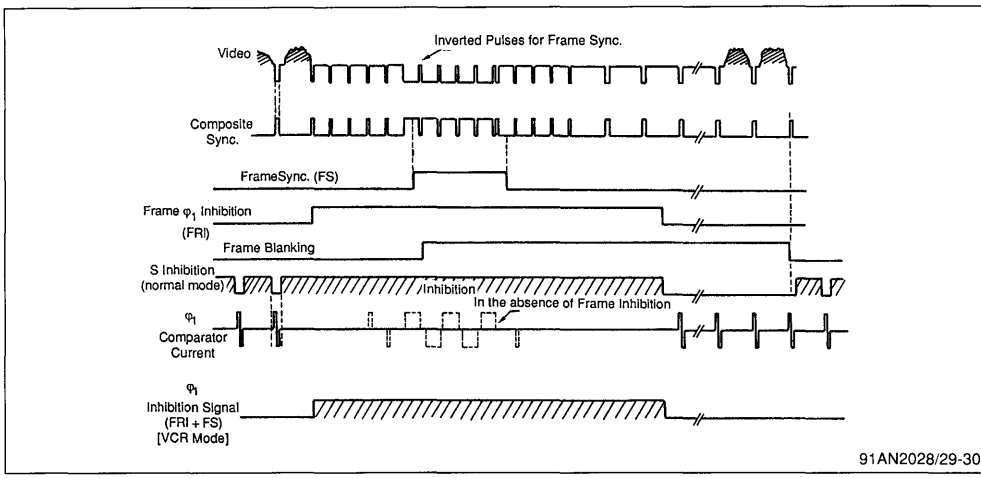
As given in application diagram section 6, an other alternative would be to use the following component values :R1 = 3.9kΩ, C1 = 4.7µF, C = 15nF

V.3.7 - Phase comparator inhibition

The phase comparator is disabled under two conditions :

- During frame sync pulse (see figure 30)

Figure 31



Inverting the line sync pulse contained within the video signal will provide the frame sync pulses required for the synchronization of vertical scanning.

Since the current supply to comparator ϕ1 is controlled by the line sync pulse, the comparator must be inhibited at the time of line sync inversions so as to avoid occurence of phase errors at the beginning of each frame.

This inhibition is activated during FRI (Frame Retrace Inhibition) issued by frame logic circuitry. If ϕ1 is locked before the vertical scanning synchronization occurs, (e.g. when switching between channels), and since FRI phase is not yet correctly positioned, the φ1 must be further inhibited by FS signal which is the extracted frame sync pulse.

- During line scanning (see figures 31 and 32)

This inhibition will eliminate the occurrence of all possible phase errors due to a noisy sync signal or parasitics during the line scanning phase. It yields excellent display stability at noisy video signals.

Figure 32

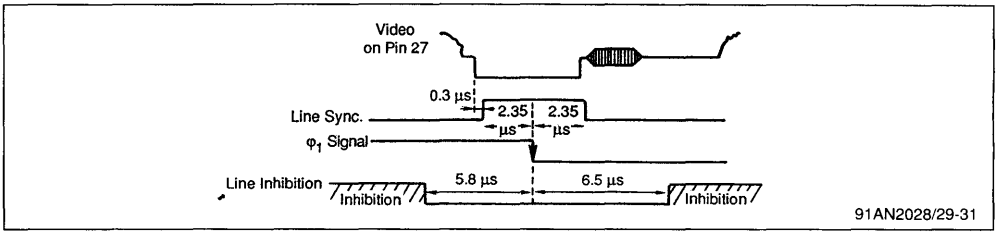
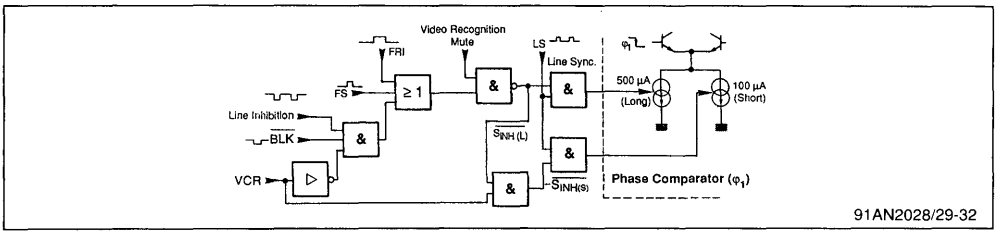


Figure 33 : ϕ_1 Inhibition logic block diagram



- ϕ1 Inhibition in long time constant mode (VCR = 0)
  - $S_{INH(LONG)}$ = Mute . (FRI + FS + $\overline{BLK}$. $LINE_{INH}$) and
  - $S_{INH(SHORT)}$ = 1
    Inhibition is activated during, frame sync, FRI and each time line trace interval - except at frame beginning between lines 8 and 21.
- ϕ1 Inhibition in short time constant mode (VCR = 1)
  - $S_{INH(SHORT)}$ = Mute . (FRI + FS) = $S_{INH(LONG)}$
    In VCR mode, inhibition is disabled during line trace since phase or frequency variations are not taken into account instantenously.

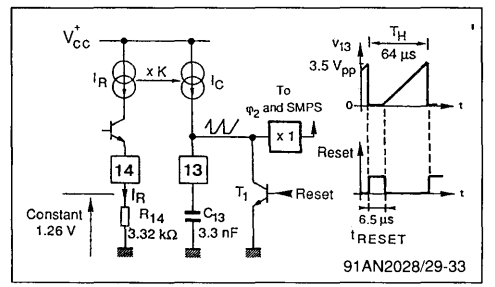
V.4 - Line saw-tooth generator

Before going through a detailed study of the second phase locked loop "ϕ2", let's have an overview of the line saw-tooth generator which has been mainly implemented for ϕ2 phase variations and also the phase modulation of the switching power supply.

It uses the combination of an external capacitor connected to pin 13 and an internally implemented constant current generator to generate a saw-tooth voltage at line frequency.

Its frequency is determined by the reset frequency of the capacitor "C_{13}". This reset signal is issued by

Figure 34



the line logic circuitry at a period multiple of VCO period (×32).

- $I_C = K \cdot I_R = K \cdot \frac{1.26}{R_{14}} = 200\mu A$
- $V_{13PP} = \frac{I_C(T_H - t_{reset})}{C_{13}} = \frac{K \times 1.26(T_H - t_{reset})}{R_{14} \cdot C_{13}} = 3.48V$
- $V_{CE(SAT)T1} \approx 20$ mV $\Rightarrow V_{13(MAX)} = 3.5V$
- In sync mode :
  - $T_H = 64\mu s$, $t_{RESET} = 6.5\mu s$
  - $K = 0.527 \pm 2$ %

V.5 - Second phase locked loop "$\phi 2$"

This stage controls the horizontal deflection of the electron beam i.e., the horizontal picture scanning. The frequency of operation, in the absence of video signal, is a multiple of the VCO frequency, i.e. 15625Hz - 500Hz.

When video signal is present, the scanning frequency is synchronized with the video signal through the first phase locked-loop "$\phi 1$".

The output rectangular waveform signal drives the line switching transistor. This transistor, when turned-off, generates what is commonly called the "line flyback".

In order to obtain a horizontally centered picture, the line flyback (LF) must coincide with the blanking time on tube cathodes.

The turn-off delay is due to transistor base storage time. This time varies in different TV sets as the transistors employed may have different operating characteristics which are functions of temperature variations, power rating and base drive.

Therefore, it follows that in order to obtain stable image centering, the line flyback must be phase-locked with respect to the video signal.

The second phase-locked loop also offers the possibility of horizontal phase-shift adjustment.

Figure 35

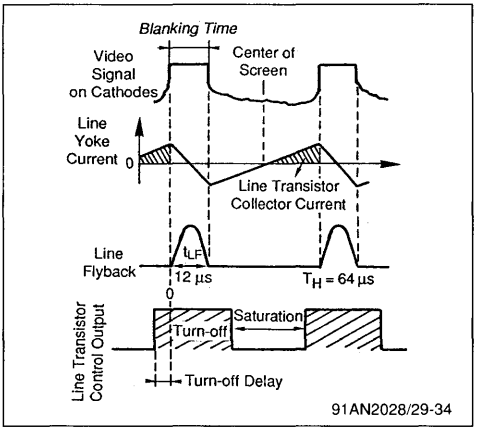
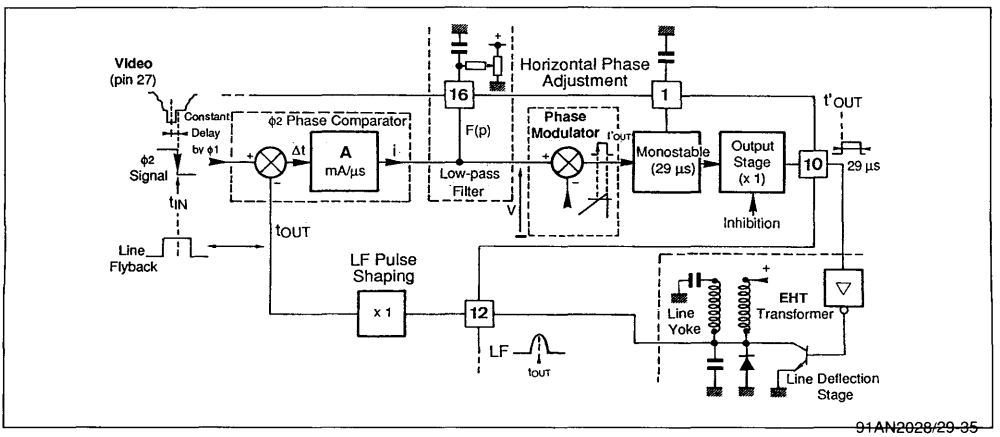


Figure 36 : Second Phase Locked Loop " ϕ_2" Block Diagram



V.5.1 - Duty of different building blocks

V.5.1.1 - "$\phi 2$" Phase comparator

This block generates a current proportional to the phase difference between the phase reference "$\phi 2$" and the middle of the line flyback to be phase-locked.

V.5.1.2 - Low-pass filter

- Rejects the parasitic component "sum of phases"
- Smoothens the "phase difference" component
- Allow "phase adjustment" by generating an error within the loop

V.5.1.3 - Phase modulator

Uses the line saw-tooth voltage to convert the voltage delivered by the low-pass filter into a phase corresponding to the line transistor turn-off control signal.

V.5.1.4 - Flip-flop

Generates the turn-off control signal for a constant time (fixed by the external capacitor), the phase of which is set by the modulator.

V.5.*1.5 - Output stage*

- Delivers the control signal for line transistor driver
- Disables the output during start-up and protection phases

V.5.1.6 - Line deflection stage

- Generates the saw-tooth current for line yoke
- Generates the high voltage required by picture tube and other supply voltages

The line flyback information is provided by the EHT transformer

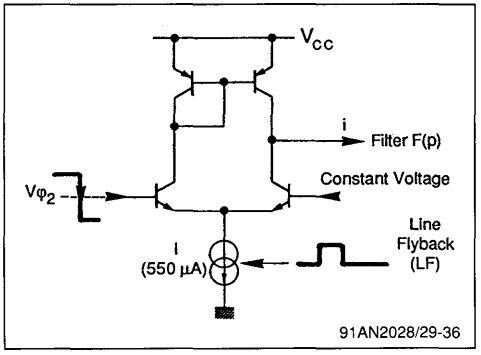
V.5.2 - Operation of building blocks

To provide an easier understanding of the subject, the "$\phi 2$" loop study will be covered as a function of various time intervals and not as a function of phase.

V.5.2.1 - Phase comparator "$\phi 2$"

The operation is identical to that of "$\phi 1$" loop.

Figure 37



The $V_{\phi 2}$ signal issued by logic block is phased with respect to the middle of line sync pulse on pin 27 and delayed by a 2.6 µs interval so as to be at the middle of blanking time on video cathodes.

The output current component "$2f_H$" is rejected by the low-pass filter.

- The average current is $i = 2I\frac{\Delta t}{T_H}$

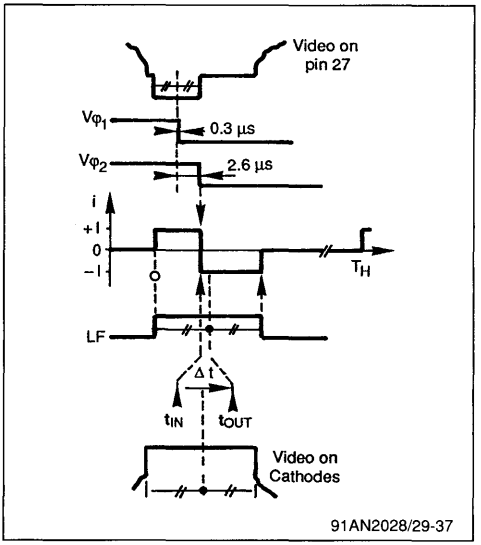
  Where : $\Delta t = t_{IN} - t_{OUT}$
- The conversion gain is therefore :

$$A = \frac{i}{\Delta t} = \frac{2I}{T_H} = 17\mu A/\mu s$$

At : I = 550 µA and T_H = 64 µs

"A" will remain constant since "I" is a multiple of "I_{REF}" current on pin 14.

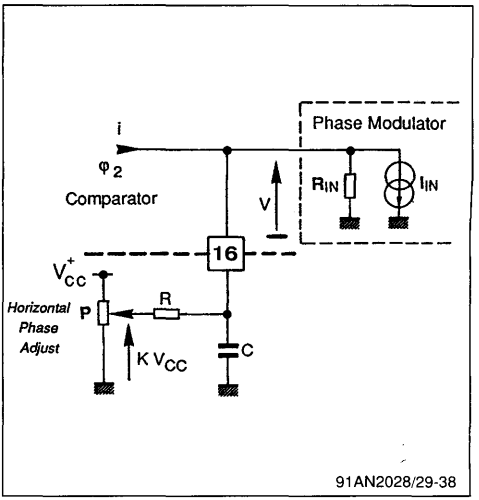
Figure 38



V.5.2.2 - Low-pass filter f(p)

The horizontal phase-shift adjustment is taken into account :

Figure 39



- Filter V = f(i) transfer characteristic is given as :

$$V = Zi + \frac{Z}{R} \cdot K \cdot V_{CC} - Z \cdot I_{IN}$$

Where :

- $Z = R_{IN} // R // \frac{1}{C \cdot p}$
- R_{IN}, I_{IN} : modulator input characteristics

In Dynamic Mode

- $V = Zi \Rightarrow f(p) = \frac{V}{i} = Z(p) = \frac{R'}{1 + \tau p}$

Where :

- R' = R_{IN} // R (R >> Potentiometer P)
- τ = R' . C : Filter time constant

The network behaves as a first order low-pass filter whose cut-off frequency at -3 dB is :

$$f_{-3dB} = \frac{1}{2\pi R'C}$$

Filter component values

- R = 470kΩ and C = 22nF
  - In practice, (K ∈ [0,1]) V_{CC} = 12 V
- R_{IN} = 25MΩ , I_{IN} = 0.65µA (base input current)

F_{-3db} = 15.7 Hz with adjustment and 0.3Hz without adjustment

V.5.2.3 - Phase modulator

This is built around a comparator which converts the filter voltage to a rectangular waveform such that its rising edge phase, variable as a function of filter voltage "V", will trigger the line transistor turn-off control circuitry.

The conversion gain is determined by the slope of the line saw-tooth applied to comparator.

Figure 40

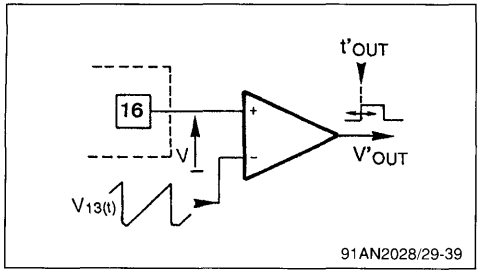
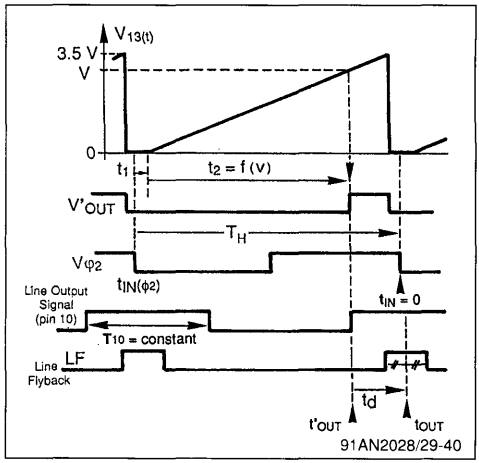


Figure 41



- Transfer characteristic is given by :

$$\frac{\Delta t'_{OUT}}{\Delta V} = \frac{\Delta t_{13}}{\Delta V_{13}} = B = 16.4\mu s/V$$

therefore t_2 = B.V

Let's consider the delay interval between "t_{OUT}" and the reference time "t_{IN}"

where t_{OUT} is the middle of line flyback :

- $t_{OUT} - t_{IN} = t_2 + t_d + t_1 - t_H$

Where :

- t1 = 4.3µs

(Reset for V_{13} and $V_{\phi 2}$ are signals coming from line logic block and are synchronized on line sync.)

- t_d = 2 to 15µs

(Delay between leading edge of output signal - pin 10 - and the middle of line flyback)

- t_H = 64µs
- $t_{OUT} - t_{IN}$ = B.V + t_d - 59.7µs

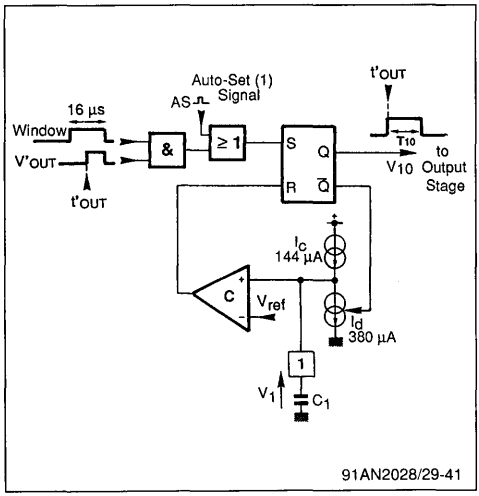
V.5.2.4 - Line flip-flop (TEA2028 only for TEA2029 refer to Section VII.6)

It generates a constant duration rectangular signal used to turn-off the line transistor. It is triggered by the rising-edge of the phase comparator output voltage and reset after capacitor on pin 1 is charged.

a. Block diagram

"V'OUT" will set the flip-flop thereby allowing the capacitor "C1" to be charged by current "IC" delivered through current generator. The voltage across capacitor begins rising until it reaches "VREF". At this time, comparator "C" is triggered, the output of which will in turn reset the flip-flop. The capacitor "C" is consequently discharged by current ID - IC.

Figure 42



b. T10 Calculation

$$T_{10} = \frac{C1 \cdot \Delta V_1}{I_C} = \frac{C1 \cdot V_{REF}}{I_C}$$

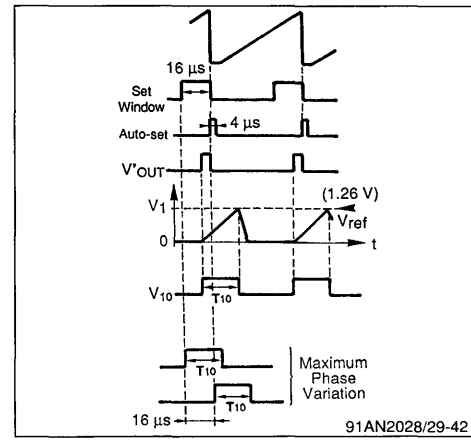
"IC" is a fraction of "IREF" on pin 14

$$I_C = \frac{I_{REF}}{\alpha} = \frac{V_{REF}}{\alpha \cdot R14} = 144\mu A$$

$$\Rightarrow T10 = \alpha \cdot R14 \cdot C1 = 2.64 \times R14 \times C1$$

- R14 = 3.32kΩ ⇒T10 = 29µs
- C1 = 3.3nF
  - T10 is independent from temperature and VCC
  - α has a maximum dispersion of ± 3% from device to device

Figure 43



c. 16µs Window

This window is generated by the line logic circuitry and sets the maximum phase variations of the output signal "V10".

Also, for protection purposes, should "V16" voltage equal "0", the output signal will be always present and have a maximum phase shift of 16µs with respect to the falling-edge of the line saw-tooth.

d. Auto-set to "1"

To provide protection, this function will trigger the flip-flop if the modulator is disabled, i.e. $V_{16} > V_{13(MAX)}$.

e. Maximum "T10" value as a function of "C1"

$T_{10(MIN)}$: 16µs(window) + 4µs(auto set) = 20µs

$$\Rightarrow C_{1(MIN)} = 2.3 \text{ nF}$$

$$T_{10(MAX)} : \text{for } \frac{C_1 \cdot V_{REF}}{I_d - I_C} + \frac{C_1 \cdot V_{REF}}{I_C} \leq 64\mu s$$

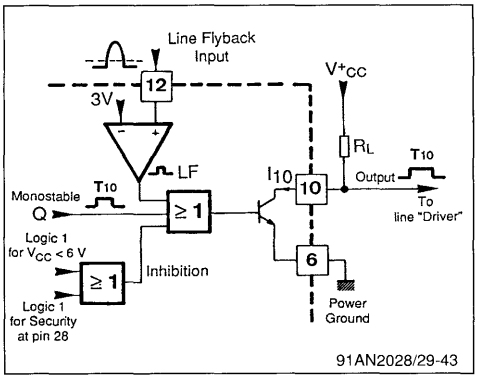
$$\Rightarrow T_{10(MAX)} = 40\mu s \Rightarrow C_{1(MAX)} = 4.6 \text{ nF}$$

For normal operation, C1 value has to be chosen between 2.3nF and 4.6nF.

If pin 1 is grounded, output signal (pin 10) is inhibited and goes high.

V.5.2.5 - Line output stage & inhibitions

Figure 44



- Open-collector output : $V_{10(SAT)}$ < 1.5V at $I_{10(MAX)}$ = 20mA

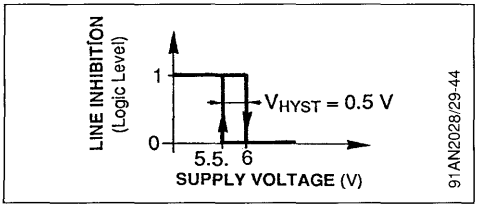
The line output (pin 10) will go high if either the following three inhibitions is activated :

a. Inhibition at start-up

This is generated by a hysteresis comparator which is driven by "KV_{CC}" and the "1.26V" reference voltage.

This inhibition is mandatory since the device will operate only at $V_{CC} \geq 5$ V.

Figure 45



b. Inhibition during line flyback

The output signal pin 10 is high during line transistor turn-off. The leading edge of output signal pin 10 turns off the line transistor after a delay interval (storage time).

The line transistor turn-off generates an overvoltage on the collector corresponding to the line flyback pulse. During this interval, in order to avoid transistor destruction, the pin 10 output must absolutely remain high.

This is done internally with the line flyback pulse (pin 12), which forces pin 10 output to high level during the line flyback time.

c. Safety inhibition

The device has a security input terminal "pin 28". If a signal lower than V_{REF} (1.26V) is applied to this pin, line and power supply outputs are all inhibited.

This function is particularly useful for TV chassis protection. Refer to section V.7.5 for further details.

V.5.2.6 - Line deflection stage

This chapter will cover a general description of the "horizontal deflection stage" employed almost commonly in all recent TV sets.

Deflection of electron beam is proportional to the intensity of magnetic field induced by the line yoke. This yoke is equivalent to an inductor. The deflection is therefore proportional to the current through inductor.

In order to obtain a linear deflection from left to right as a function of time, a saw-tooth current must be generated within the yoke. The approach is to apply a switched DC voltage to the line yoke.

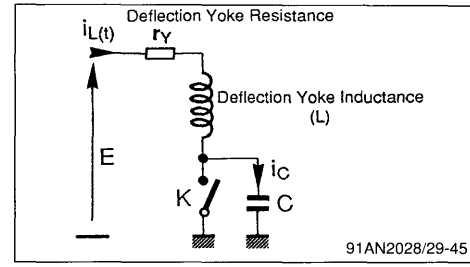
- When K is closed :

$$i_{L(t)} = \frac{E}{r_y}(1 - e^{-\frac{ryt}{L}})$$

- $\frac{L}{r_y}$ is always higher than half of trace time :

$$\frac{t_{trace}}{2} = \frac{T_H - t_{LF}}{2} = \frac{64 - 12}{2} = 26\mu s$$

Figure 46



- "i_L" variations as a function of time :

$$\frac{di_L}{dt} = \frac{E}{L} e^{-\frac{rt}{L}} \approx \frac{E}{L} \left(\text{for } t << \frac{L}{r_y} \right)$$

The current will therefore be linear as a function of time $i_L(t) = \frac{E}{L} \cdot t$ from "t_1" to "t_2" which is the second portion of the line trace interval.

- Current at the end of trace : $I_M = \frac{E}{L} \cdot \frac{t_{TRACE}}{2}$

- Energy stored within inductor : $W = \frac{1}{2} \cdot L \cdot I_M^2$

If the switch is opened at $t = t_2$, the "L.C" combination will enter into oscillation, the energy stored within inductor is transfered to the capacitor, which will return it to the inductor and so on.

The circuit period is classically given by :
$T = 2\pi \cdot \sqrt{LC}$

If "K" is closed at time "t_3", the inductor will once again have a voltage "E" across its terminals. The current falls linearly until "t_4". This phase corresponds to the first half of line trace interval.

The overvoltage across C is :

$$V_p = E \frac{t_{trace}}{2\sqrt{LC}} + E$$

during $t_{LF} \approx \pi\sqrt{LC}$

That is : $V_P = E \frac{t_{TRACE} \cdot \pi}{2t_{LF}} + E$

In practice, E is higher than 100V.

- $t_{TRACE} = 52\mu s$
- $t_{LF} = 12\mu s$

$\Rightarrow V_P \geq 780V$

Note that this overvoltage is almost 8 times higher than the source voltage "E". This overvoltage is applied to the primary winding of a "step-up transformer" (EHT Transformer) in order to generate the high voltage required by picture tube anode.

In practice, the power switch "K" is built by a combination of "High Voltage Switching Transistor" and "Fast Recovery Diode".

Figure 47

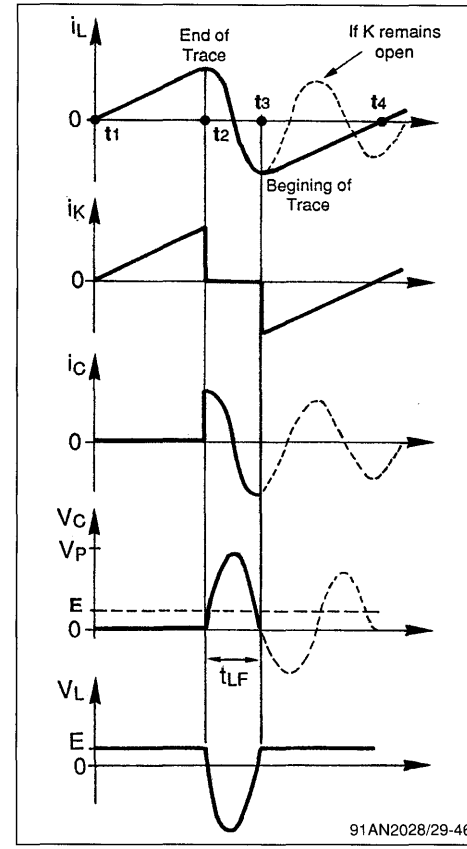
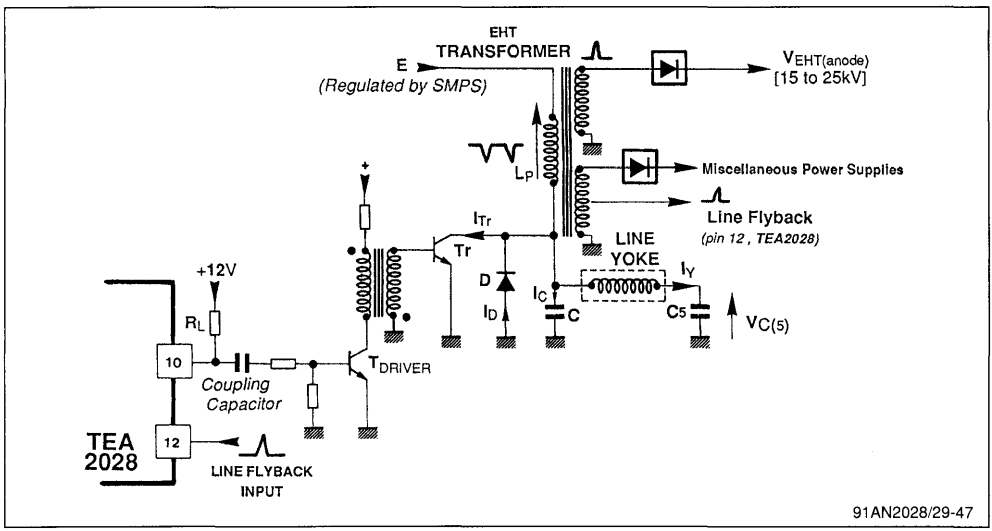


Figure 48 : Simplified diagram of the horizontal deflection stage



If considered in average value, it is seen that the voltage across capacitor "CS" is almost equal to the source voltage "E". The saw-tooth current through this capacitor will produce a parabolic ripple around "E", which will thus modify the equivalent source of the line yoke and induce a modified current of "S" shape within the yoke. This "S" current is used to produce a linear picture as a function of the picture tube geometry.

The basic arrangement can be reconstructed by assuming that the equivalent inductor "L" is the transformer "L_P" and line yoke inductors put in parallel (since $VC_{S(AV)} = E$).

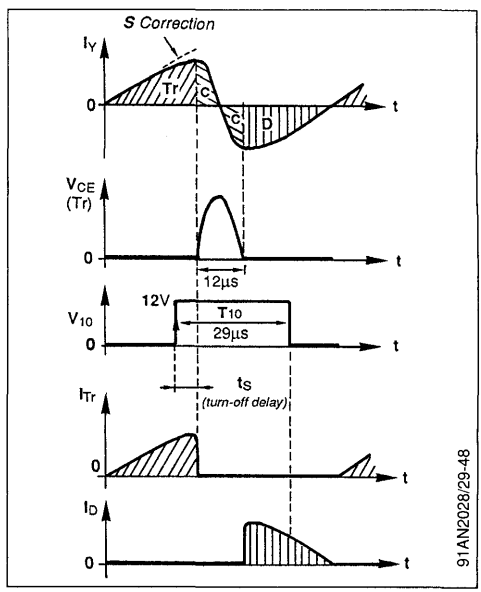
The output pin 10 of TEA2028 is applied to a matching stage called "line driver" the output of which drives the power transistor "T_r". The matching stage is necessary for optimized base drive.

At middle of trace, the transistor enters into saturation and its current rises linearly. V10 will then issue a control signal to turn the transistor off. The transistor will be in fact turned-off after a delay interval "t_S" (storage time) varying from 2 to 8 µs depending on application. The system will then enter into oscillation during its half-period thereby generating the line flyback. At the end of flyback time, the line yoke current is negative while the voltage across capacitor "C" has fallen to zero. The energy transfer automatically takes place by the recovery diode during the first portion of trace time.

Also, it is clear that the line scanning phase with respect to video signal is determined by the rising-edge of pin 10 output signal.

High level duration (T10) of pin 10 output signal

Figure 49



must be higher than the delay interval "$t_{S(MAX)}$" + the flyback time (i.e. 8 + 12 = 20µs) and must turn-off before the end of diode conduction :

$$T10 < t_{S(MIN)} + t_{LF} + \frac{t_{TRACE}}{2} \Rightarrow < 40\mu s$$

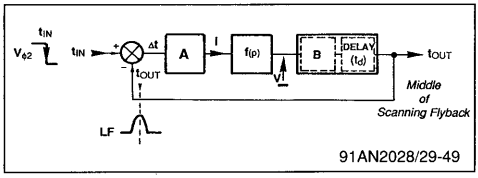
In practice, one will select the pin 1 capacitor C1 = 3.3nF to yield T10 = 29µs.

V.5.3 - Characteristics of loop "ϕ_2"

The function to calculate is a time with respect to the origin time set by "$V_{\phi 2}$". In fact, it is an easy task to inter-relate the horizontal displacement (in mm) to a time interval specified in µs.

For a large screen width of 540 mm, the horizontal scanning time :64 - 12 = 52µs, which corresponds to : ≈ 10mm/µs.

Figure 50



- $i = A \cdot (t_{IN} - t_{OUT})$ (1)
- $V = Z \cdot i + \frac{Z}{R} \cdot K \cdot V_{CC} - Z \cdot I_{IN}$ (2)
- $t_{OUT} - t_{IN} = B \cdot V + t_d - 59.7\mu s$ (3)
- $Z = \frac{R'}{1 + \tau p}$
- $R' = R_{IN} // R$
- $A = 17\mu A/\mu s$
- $\tau = R'C$
- $B = 16.4\mu s/V$

The open-loop dynamic gain is :

- $T = ABf(p) = ABZ = \frac{ABR'}{1 + \tau p}$ (4)

The system exhibits the characteristics inherent to a first order circuit and is therefore stable.

combining equations (1), (2), (3) and (4), the t_{OUT} delay is found as follows :

$$t_{OUT} = t_{IN} - \underbrace{\frac{BZI_{IN}}{1+T}}_{\text{Error term due to the input current } "I_{IN}"} + \underbrace{\frac{t_D - 59.7\mu s}{1+T}}_{\text{Error term due to delay}} + \underbrace{\frac{B\frac{Z}{R} \cdot KV_{CC}}{1+T}}_{\text{Error term due to phase shift adjustment (if applicable)}}$$

(Dynamic gain = 1)

It is therefore clear that the second phase-locked loop does not cause any dynamic delay.

This can be explained by the fact that the phase modulator responds instanenously to all variations of "ϕ_2".

V.5.3.1 - Study of the Static Error

t_{IN} = 0 (phase of $V_{\phi 2}$) is taken as timing reference.

The equivalent impedance of F(p) filter is :

- R' = 460kΩ (R // R_{IN}) : if an adjustment is applied to pin 16, or
- Modulator input resistance RIN = 25MΩ : without adjustment

a. Phase shift error in case of no adjustment

Equation (5) becomes :

$$T_{OUT} = \frac{BR_{IN}I_{IN}}{1 + T_1} + \frac{t_D - 59.7\mu s}{1 + T_1}$$

with : T1 = ABR_{IN}

Where :

- R_{IN} = 25MΩ
- I_{IN} = 0.65mA
- t_d = 10µs
- T1 = 6.8 x 10^3 = 76dB

} t_{OUT} = - 46ns which corresponds to a picture shift of 0.46 mm !

The error is quite negligible and thanks to rather high open-loop gain, the display accuracy with respect to the phase set by "ϕ_2", is very satisfactory.

b. Study of shift adjustment

With R, P network connected to pin 16, the t_{out} becomes :

$$t_{OUT} = \frac{-BR'I_{IN}}{1+T_2} + \frac{t_D - 59.7\mu s}{1+T_2} + \frac{B\frac{R'}{R} \cdot KV_{CC}}{1+T_2}$$

With : T2 = ABR' (where R' = R // R_{IN})

and K ∈ [0;1]

Substituting the following values into above equation :

- R = 470kΩ
- R' = 470kΩ // 25MΩ = 461kΩ
- A = 17×10^{-6} A/µs
- B = 16µs/V
- td = 10µs
- T_2 = 125
- V_{CC} = 12V

t_{OUT} = - 38ns - 390ns + 1.5µs×K

therefore t_{out} = 1.5×K - 0.43 (in µs)

If K varies between 0 and 1

⇒ t_{out} [- 0.43ms to 1.07µs]

which corresponds to a picture displacement of :

Δ_{LINE} [- 4mm to + 11mm].

Shift variations as a function of V_{CC} (with adjustment)

$$\frac{dt_{out}}{dV_{CC}} = \frac{B\frac{R'}{R} \cdot K}{1 + T_2} \approx \frac{B\frac{R'}{R} \cdot K}{T_2} \approx \frac{K}{AR}$$

$$= K \times 0.12\mu s/V \begin{cases} \frac{dL}{dV_{CC}} = 0.34mm/V \\ \text{at } K_{NOMINAL} = 0.28 \end{cases}$$

Therefore, a constant V_{CC} must be applied to the potentiometer.

V.6 - Vertical deflection driver stage

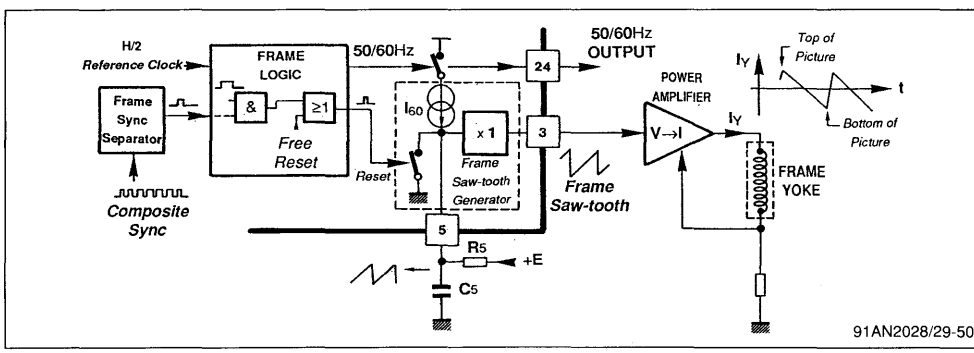
This stage must constantly drive the vertical spot deflection. Such deflection will horizontally scan the screen from top to bottom thus generating the displayed image. Similar to horizontal deflection, the vertical deflection is obtained by magnetic field variations of a coil mounted on the picture tube.

A saw-tooth current at frame frequency will go through this coil commonly called "frame yoke". Frame period is the time required for the entire screen to be scanned vertically.

C.C.I.R. and N.T.S.C. TV standards require respectively 50Hz and 60Hz Frame Scanning Frequencies. Also, a full screen display is obtained by two successive vertical scannings such that the second scanning is delayed by a half line period with respect to the first.

This method increases the number of images per second (50 half images/s or 50 frames/s in 50 Hz standard). This scanning mode called "Interlaced Scanning" eliminates the fliker which would have been otherwise produced by scanning 25 entire images per second.

Figure 51 : Block Diagram of the Vertical Deflection Stage



The circuit will generate a saw-tooth voltage which is linear as a function of time and called "frame saw-tooth". A power amplifier will deliver to the "frame yoke" a current proportional to this saw-tooth voltage. It is thus clear that this saw-tooth voltage reflects the function of the vertical spot deflection; which must itself be synchronized with the video signal. Synchronization signals are obtained from an extraction stage which will extract the useful signal during line pulse inversion of the composite sync signal.

Synchronization occurs at the end of scanning, in other words, when the saw-tooth voltage at pin 5 is reset. This function is accomplished by the "frame logic circuitry" of full digital implementation.

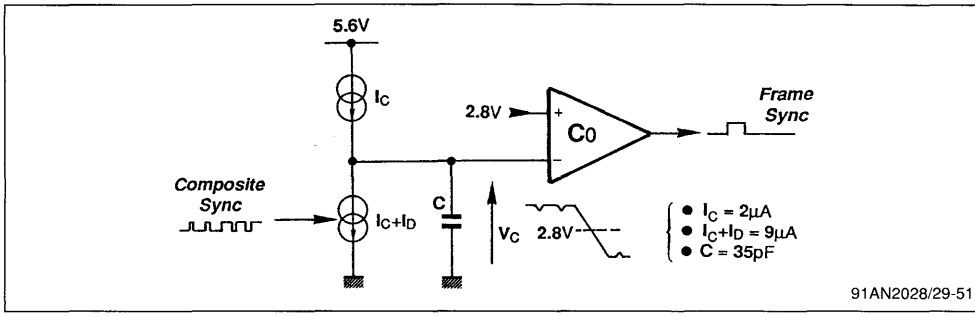
This processing method offers various advantages :

- **Accurate free-running scanning frequency** eliminates the frequency adjustment required by previous devices.
- **Digital synchronization** locked onto half line frequency thereby yielding perfect interlaced display and excellent stability with noisy video signal.
- **Automatic 50/60 Hz standard recognition** and switching the corresponding display amplitude.
- **Optimized synchronization in VCR mode.**
- **Generation of various accurate time intervals**, such as narrow "sync windows" thus reducing considerably the vertical image instability in case of for instance, mains interference, superimposed on frame sync pulse.
- **Generation of vertical blanking** signal for spot flyback and to **protect the picture tube in case of scanning failure.**

V.6.1 - Frame sync extraction

The main duty of this stage is to extract the frame sync pulses contained in composite sync signal.

Figure 52 : Sync extractor block diagram



Two current generators are used to charge and discharge the integrated capacitor "C". The discharge generator ($I_C + I_D$) is driven by the composite sync signal.

The ΔV_C across capacitor is : $-\frac{I_D \cdot t_{SYNC}}{C}$

During frame trace, the capacitor is discharged at each line sync pulse thereby generating a ΔV of -0.94V with respect to 5.6V and then recovers the charge by current "I_C". The comparator output remains low.

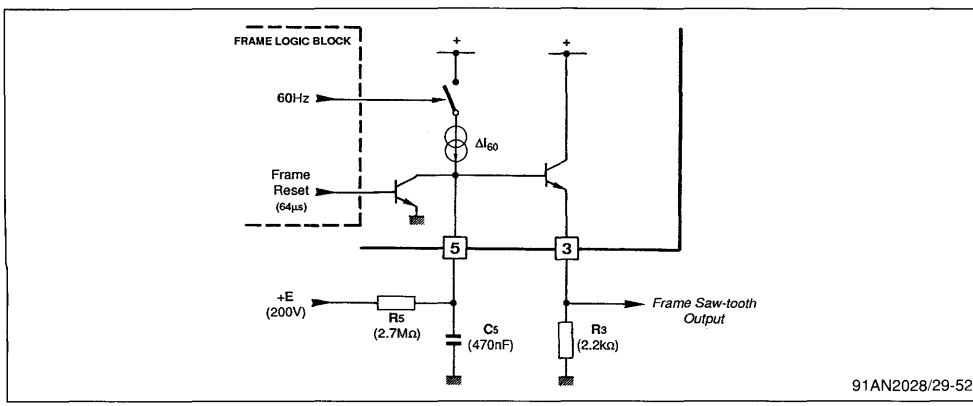
The discharge time is 27µs at the first line sync inversion applied to comparator input. The voltage "V_C" then falls from 5.6V to 0.2V and triggers the comparator "C_0" which will deliver a frame sync pulse when "V_C" crosses the 2.8V level.

The overall arrangement behaves as an integrator and will therefore suppress any noise susceptible to be present on input signal.

An external capacitor pin 20 can be added to the integrated capacitor C to increase the frame sync time constant.

V.6.2 - Frame saw-tooth generator

Figure 53

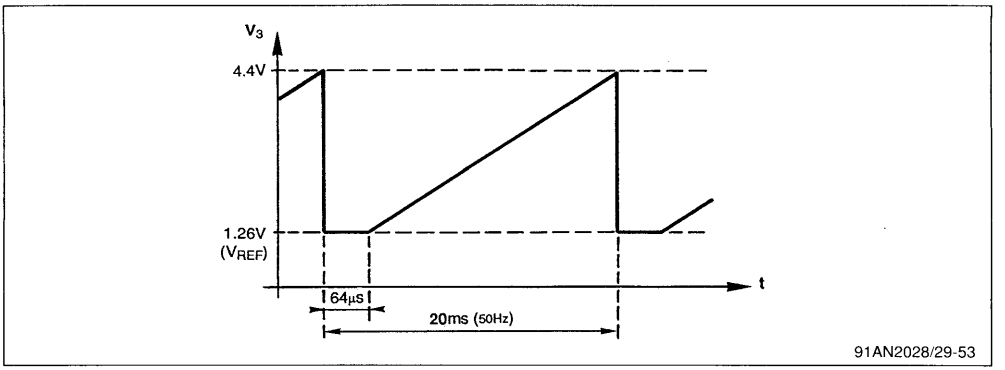


The frame saw-tooth is generated by an external RC network on pin 5.

The time constant "R5 x C5" is much higher than the frame period. Therefore, the generated saw-tooth is quite linear.

The network is discharged by an internal transistor, controlled by the frame logic block.

Figure 54



V.6.2.1 - *60Hz STANDARD SWITCHING*

The NTSC standard requires a vertical picture scanning frequency of 60Hz, i.e. a saw-tooth period of 16.66ms.

In order to obtain an identical deflection amplitude whatever the standard (50 or 60Hz), the saw-tooth amplitude for both periods must be the same.

60Hz standard recognition is performed automatically by the frame logic block, which will issue a signal to drive a current generator "ΔI_{60}". This current will be summed with the external charge current and will increase the saw-tooth slope, so as to yield same saw-tooth amplitude to that set in 50Hz standard. This current is centered around 14µA and is a fraction of I_{REF} applied to pin 14.

Employing the recommended component values for network connected to pin 5, this current will result in identical amplitude in both standards.

$$\Delta V_5 = \frac{I_{60} \times T_{60}}{C_5} = \frac{I_{50} \times T_{50}}{C_5} \Rightarrow I_{60} = I_{50} \times \frac{60}{50} = 1.2 \times I_{50}$$

$$I_{50} = \frac{E}{R_5} = \frac{200V}{2.7M\Omega} = 74\mu A \Rightarrow I_{60} = 88\mu A$$

therefore $\Delta I_{60} = 14\mu A$

V.6.3 - Functions of frame logic block

This section is fully implemented by I^2L logic gates. It is clocked by an accurate "H/2" clock running at half line period (32µs). The required periods and time intervals are obtained by counting the clock pulses.

For the sake of clarity, timing signals so obtained are labeled by the line number corresponding to video signal.

The time corresponding to "x" scanned lines with respect to the beginning of frame saw-tooth (RESET) is therefore :

$t_x = 64\mu s\ (x - 1) + 32\mu s$

Figure 55

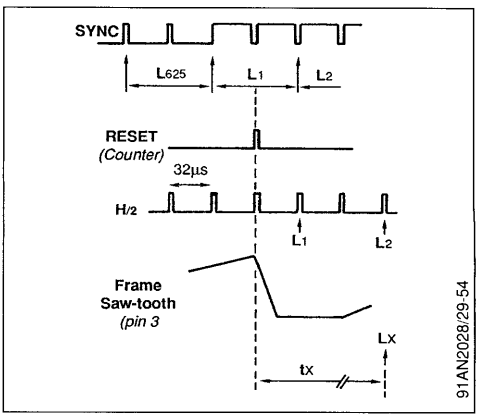
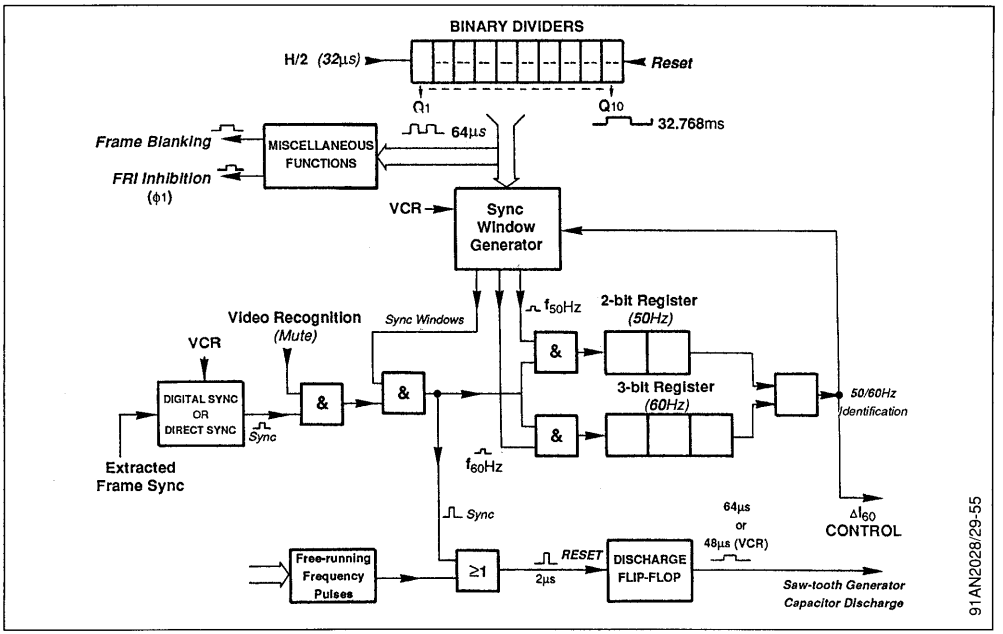


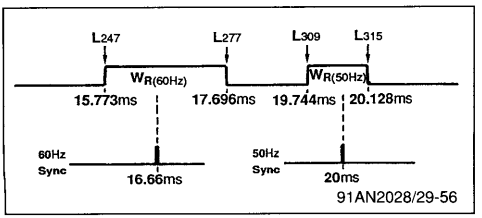
Figure 56 : Block Diagram



V.6.3.1 - 50/60 Hz Standard recognition

This function is performed by two shift registers which are loaded by sync pulses (if present) and if these pulses fall within the time interval specific to each standard. These intervals are called "Register Windows" and labeled "$W_R(50)$" and $W_R(60)$.

Figure 57



a. 50 Hz Standard Recognition

This identification is considered valid if two sucessive sync pulses applied to 50 Hz shift register fall within the 50Hz window "$W_R(50)$". At the time of synchronization capture, the first pulse will reset the counters. The second pulse, if present, will then trigger the 50Hz identification 20ms later [$I_D(50) = 1$].

The identification is not valid if two sucessive 50Hz pulses are not detected. Identification signal is also used to reduce the vertical synchronization window in 50Hz standard thereby offering excellent noise immunity against noise susceptible to be present in sync signal and hence good display stability.

b. - 60 Hz Standard Recognition

This identification is validated after three sucessive sync pulses at 16.6µs period have been detected. Three pulses are necessary to ascertain the identification prior to switching the saw-tooth amplitude. The identification signal [$I_D(60) = 1$] is also used to reduce the synchronization window and, in case of one or two missing pulses close to 60Hz, to set the free-running frequency.

V.6.3.2. - Vertical synchronization window - Free-running period

In the absence of sync pulse various free-running periods are specified. Since vertical scanning must be always active, these free-running periods must be higher than those of 50 and 60Hz standards so as to ensure synchronization.

An other window, allowing synchronization only at the end of scanning, is also necessary. Upon syn-

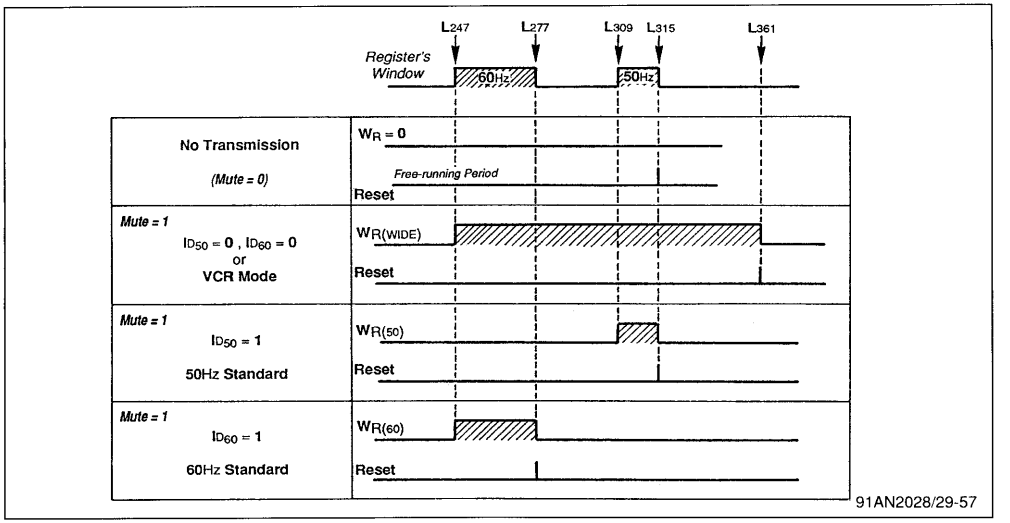
chronization, this window will allow vertical flyback only at the bottom of screen. This window should be narrow for good noise immunity but also wide enough to yield, upon synchronization, a capture time unperceptible on screen.

In our case, as long as no standard identification takes place the window will remain wide, and once one of the standards has been identified, the window will be considerably reduced.

In VCR mode, this window will be always wide since frame frequencies delivered in high-speed search, slow review and picture pause modes are very much variable and must be taken into consideration.

In the absence of transmission (Mute = 0), synchronization is disabled (so as to avoid incorrect synchronization due to noise) and the free-running frequency is around 50Hz. This will eliminate the occurrence of picture overlay at the end of trace at a lower free-running frequency.

Figure 58 : Definition of Synchronization Windows and Free-running Periods



Maximum capture time

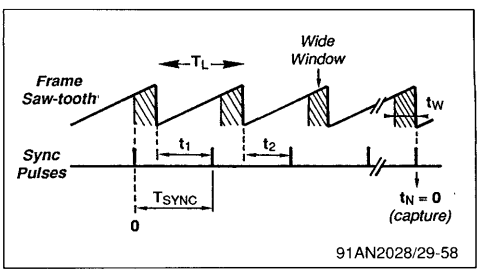
The worst case capture time occurs when the first sync pulse just precedes the sync window.

Let's find the number of periods necessary for the capture to occur, i.e. tn = 0.

$$\Rightarrow n = \frac{T_L - T_W}{T_L - T_{SYNC}}, \; T_L = 23ms, \; T_W = 7.3ms$$

- 50Hz : the number of periods is 6
  $\Rightarrow T_{CAPTURE(MAX)} = 120ms$
- 60Hz : the number of periods is 3
  $\Rightarrow T_{CAPTURE(MAX)} = 50ms$

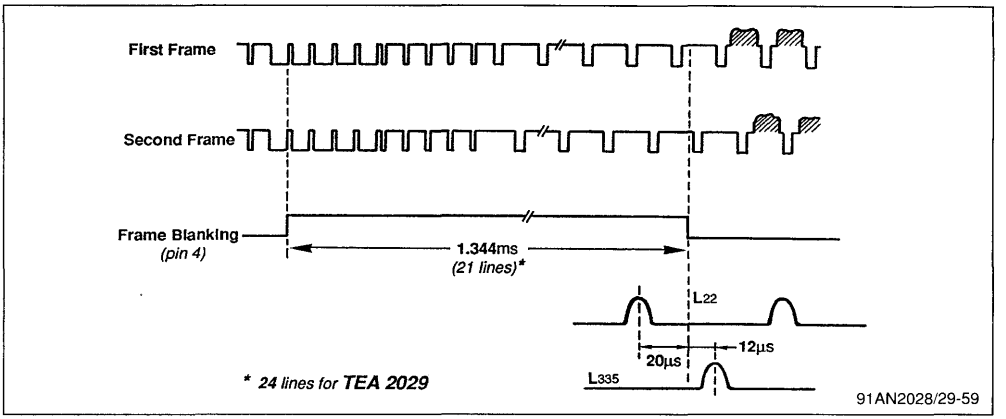
Figure 59



V.6.3.3 - *Frame blanking signal*

This signal is necessay to blank the display during each frame flyback. It is triggered at the beginning of frame saw-tooth flyback. The duration of this signal is 1.344 ms (or 21 lines).

Figure 60



This "frame blanking" signal is available through pin 4 (TEA2028 only) which is an open-collector output.

It is also present within the normalized super sandcastle signal on pin 11 (TEA2028 and TEA2029).

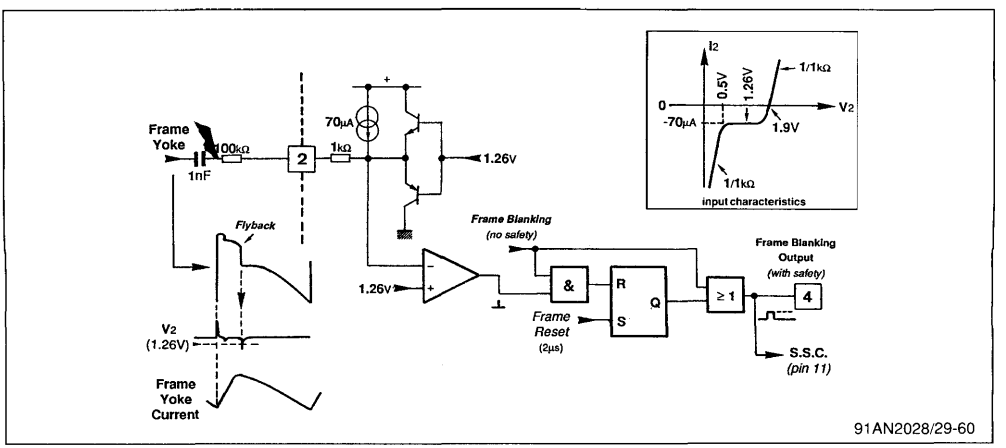
V.6.3.4. - Frame blanking safety (TEA2028 only, for TEA2029 refer to section VII.5)

Its duty is to protect the phosphor coating of picture tube in case of any problem with vertical deflection function such as scanning failure.

A signal to monitor correct scanning is provided by the frame yoke and applied to pin 2.

In case of any failure, all frame blanking outputs are disabled and go high thereby blanking the entire screen.

Figure 61 : Block diagram



During trace phase, the voltage across frame yoke has a parabolical shape due to the coupling capacitor in series with yoke. During frame flyback, the current through frame yoke must be rapidly in-

verted. Conventionally, a two-fold higher supply voltage is applied across the yoke. This will produce an overvoltage called "flyback".

The safety monitoring status is detected on the falling-edge of flyback, i.e. at the beginning of scanning. A differentiator network is used to transmit only fast voltage variations.

The required pulse is then compared to 1.26 V level. Frame blanking goes high in the absence of negative pulse (zero deflection current) or if the pulse does not fall within the first 21 lines (exagerated over-scanning).

V.7 -Switching power supply driver stage

Switching takes place on the primary side (mains side) of a transformer by using TEA2164 SMPS Controller manufactured by SGS-THOMSON Microelectrics.

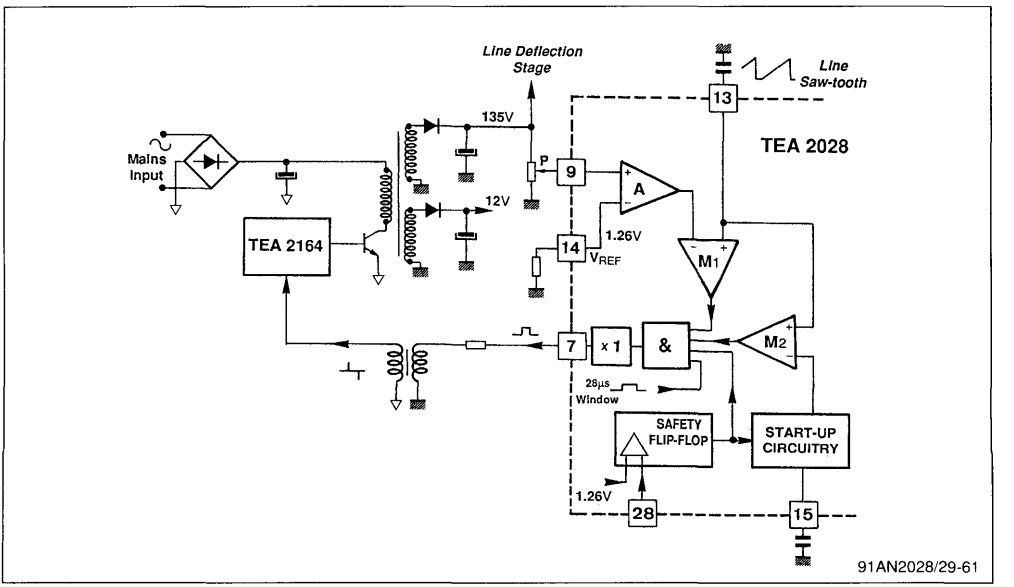
Required voltage values are obtained by rectifying different voltage outputs delivered through secondary windings. The horizontal deflection stage is powered by one of these outputs delivering around hundred volts.

This voltage source must be regulated since any voltage fluctuation will yield variations of the horizontal display amplitude.

The TEA2028 monitors this voltage and transmits the regulation signal to the primary controller circuitry via a small pulse transformer. The characteristics of this regulation signal are directly related to the conduction period of switching transistor.

V.7.1 - Power supply block diagram

Figure 62



V.7.2 - General operating principles

A fraction of the 135V output voltage to be regulated is compared to the 1.26V reference voltage. Resulting error signal is amplified and then applied to phase modulator "M_1", which will deliver a square waveform at line frequency whose duty cycle depends on the value of input voltage "V_9".

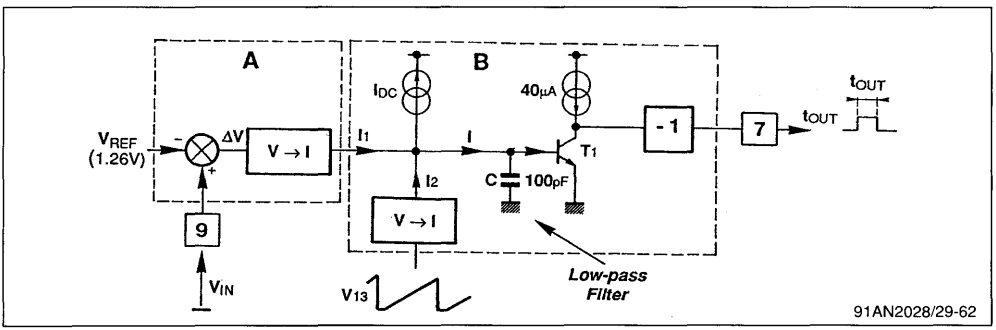
A second phase modulator "M_2" will determine the conduction period as a function of voltage on pin 15. This function is mandatory for system start-up.

A 28µs window is used to limit the conduction period of the primary-connected transistor.

Supply output (pin 7) and line output (pin 10) will be disabled if any information indicating abnormal operation is applied to safety input (pin 28). Consequently, all power stages are disabled and the TV set is thus protected.

V.7.3 - Electrical characteristics of the internal regulation loop

Figure 63



The phase modulator implemented by a simple transistor "T1" will compare in current mode, the image of amplified input (i_1) with saw-tooth current (i_2) at line frequency. With "i_2" rising, as soon as the sum of "$i_1 + i_2 - I_{DC}$" goes positive, the transistor enters into saturation thus determining the output conduction period.

A low-pass filter implemented by combination of a 100pF capacitor and the input impedance of transistor "T_1", attenuates all frequency variations higher than the line frequency.

- Input Amplification :

$$A = \frac{di_1}{dV_{IN}} = 3.3\mu A/mV$$

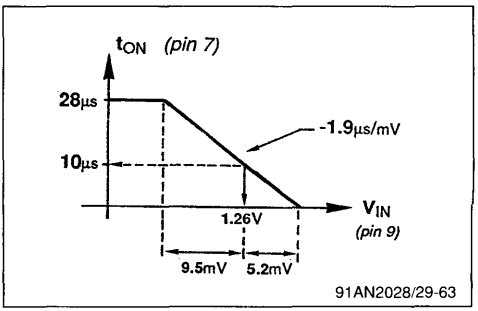
- Modulator conversion gain :

$$B = \frac{dt_{OUT}}{di_1} = -0.558\mu s/\mu A$$

- Overall gain of the internal loop :

$$\frac{dt_{OUT}}{dV_{IN}} = -1.9\mu s/mV \times \frac{1}{1 + j\frac{f}{f_0}} \quad (f_0 = 15kHz)$$

Figure 64 : Conduction period (pin 7) versus Input voltage (pin 9)



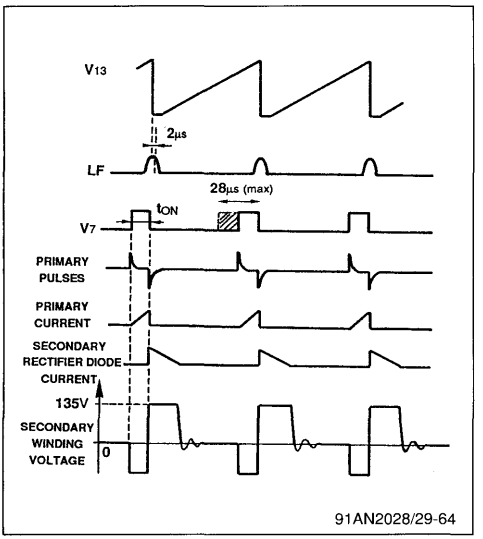
SMPS WAVEFORMS

For discontinous mode "flyback" configuration

The primary-connected transistor is turned-off during the line flyback.

All interference signals due to switching and susceptible to affect the video signal will not therefore be visible on screen.

Figure 65



Regulation Characteristics

The following characteristics have been measured on a large screen and yield excellent results :

- 135V voltage regulation as a function of mains voltage : better than 0.5% for mains voltage variations of $170V_{RMS}$ to $270V_{RMS}$ (P = 60W at 135V)
- 135 V voltage regulation as a function of load : better than 0.5% for a delivered power of 35W to 120W.

This type of power supply offers the following advantages :

- Overall efficiency enhancement : better than 80%
- Reduction of interferences by synchronization on horizontal frequency
- Full protection of the primary-connected transistor in case of short-circuit or open-load on secondary terminals
- Can provide 1W to 7W, for TV standby mode operation (refer to TEA2164 application note).

V.7.4 - Power supply soft-start

When the TV set is initially turned on, control pulses are not yet available and consequently the controller block on primary side will impose a low-power transfer to the secondary winding. This power is produced by an intermittent switching mode called "Burst Mode".

As soon as the V_{CC} supply to TEA2028 exceeds 6V level, line and SMPS outputs are enabled. Since the filtering capactitors on secondary side cannot charge up instantaneously, the voltage to be regulated would not yet be at its nominal value. Without conduction period limitation upon start-up, the device will set a maximum cycle of 28µs which will result in a high current flow through the primary winding and thus through the switching transistor which will in turn activate the protection function implemented on primary side.

Consequently, the primary controller block will be inhibited and the set will not turn-on.

A start-up system has been implemented within TEA2028 to overcome this problem.

This soft start system, will upon initial start-up, use the image of the falling voltage on pin 15 to increase progressively the conduction cycle. The phase modulator "M2" compares this voltage with line saw-tooth voltage and delivers the corresponding limitation cycle.

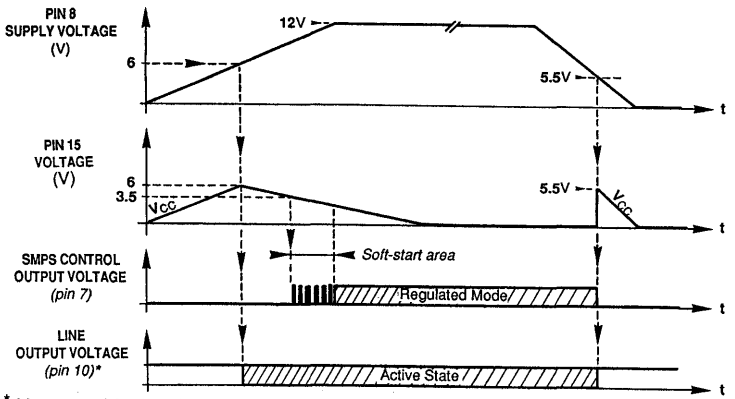
During supply voltage rising cycle [V_{CC} (pin 8) < 6V], the capacitor pin 15 will charge up rapidly while the voltage across it follows V_{CC}.

At $V_{CC} \geq 6V$, the capacitor is discharged via an internal current generator and the voltage across it decays linearly.

At $V_{15} \leq 3.5V$ (line saw-tooth peak-to-peak voltage), phase comparator "M2" delivers a low conduction period which will gradually increase.

The conduction period (pin 7) will rise until the secondary voltage reaches the value set by potentiometer "P". When this occurs, the loop is activated.

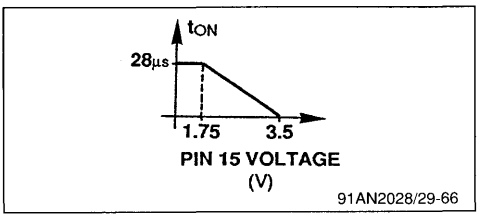
Figure 66



The pin 15 discharge current value is 100µA for a duration of 2µs line frequency.

Therefore $I_{D(AV)} = 100 \times \frac{2}{64} = 3.1\mu A$

Figure 67



Conduction period limitation voltage (pin 15)
$T_{ON(LIM)} = 56\mu s - 16 \times V_{15}$ (in µs)

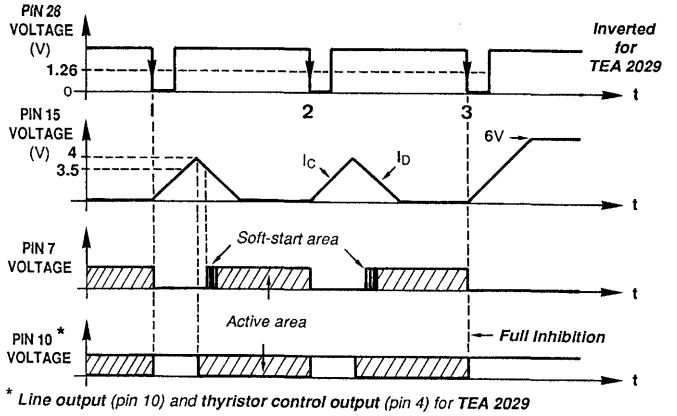
V.7.5 - Protection features

As soon as a safety signal ($V \leq 1.26$ V) is applied to pin 28, line and supply outputs (pins 10 and 7) are both disabled. Capacitor "C15" begins charging up until the voltage across it reaches 4 V ($K \times V_{CC}$). Outputs are again enabled and conduction period gradually increases as it occurs upon initial start-up.

The device will be definitively inhibited if the cycle of events is repeated 3 times.

For the device to restart, the internal 3-bit register should be reset which requires the V_{CC} to fall below 4 V.

Figure 68



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Pin 15 charging current : $I_{C(AV)} = - I_{D(AV)} = - 3.1\mu A$

V.7.6 - TV Power supply in standby mode

V.7.6.1 - Regulation by primary controller circuit

This mode of regulation called "Burst Mode" is performed only by the primary controller circuit and is activated in the case of missing control pulses or in the absence of power supply to TEA2028.

In this mode, power available through secondary winding is limited. Refer to TEA2164 Application Note for further details.

Higher powers can be obtained by using the regulation feature offered by TEA2028. In this case, the horizontal output (pin 10) must be disabled.

V.7.6.2 - Regulation by TEA2028

In this case, all that is required is to disable the line scanning function thus reducing the overall power by 90%.

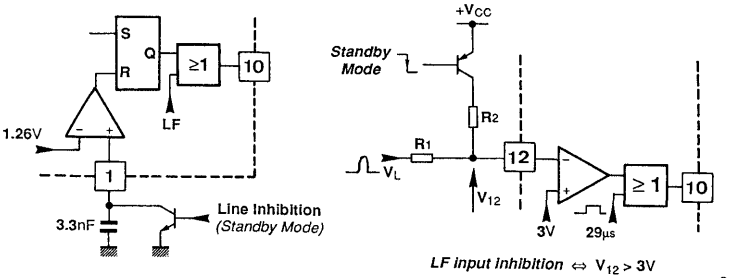
The device power supply regulation loop remains active, for minimum conduction period to be 1.5 ms the power delivered through secondary must be higher than 3 W.

Line Output Inhibition

Two alternatives are possible :

- Grounding flip-flop pin 1
- Apply a voltage higher than 3 V to pin 12.

Figure 69



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V.8 - Miscellaneous functions

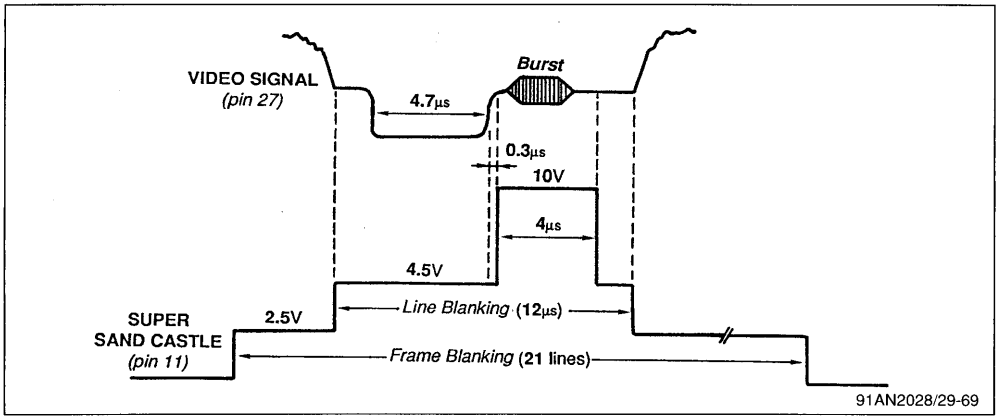
V.8.1 - Super sandcastle signal generator

This signal used in video stage, is available on pin 11.

It has 3 levels at specified time intervals :

- 2.5 V level
  Used for vertical blanking at each frame flyback. Its duration is 21 lines and is generated by the frame logic.
  This level will be maintained if vertical scanning failure is detected on pin 2.
- 4.5V level
  Used for horizontal blanking, its duration is determined by comparing the line flyback signal on pin 12 to an internal voltage of 0.25V.
- 10 V level
  This signal is used by color decoding stage. Its duration of 4µs is determined by line logic circuitry. With respect to the video signal on pin 27, this level is positioned such that it is used to sample the burst frequency transmitted just after the sync pulse.

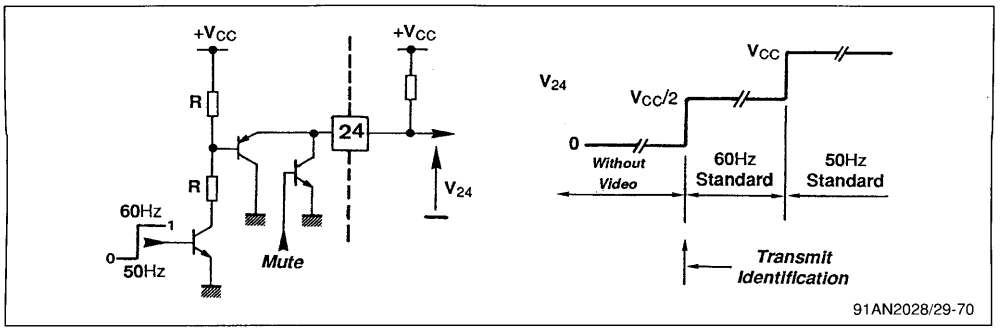
Figure 70



V.8.2 - Video and 50/60Hz standard recognition output

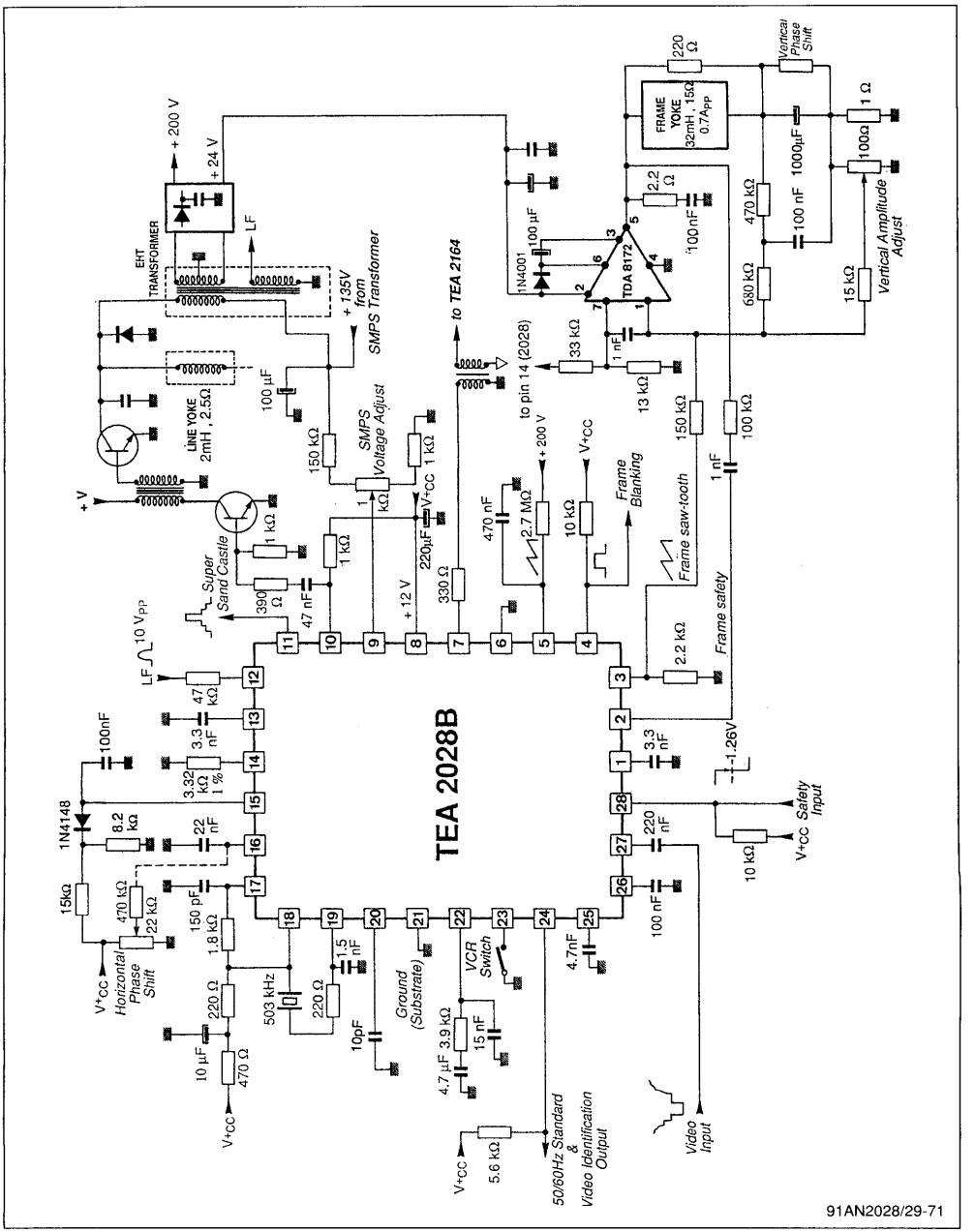
A 3-level signal is available at pin 24 for video identification (Mute) and for 50 and 60Hz standards recognition.

Figure 71



VI - TEA2028 APPLICATION DIAGRAM

Figure 72



VII - TEA2029 : DIFFERENCES WITH TEA2028

VII.1 - General

The TEA2029 has quite the same functions compared to TEA2028.

The main difference is that the TEA2029 incorporates a frame phase modulator intended to work with a switched mode vertical stage using a thyristor.

The TEA2029 can also be used with a linear vertical power amplifier such as the TDA 8170.

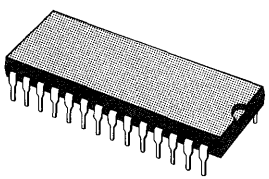
VII.2 - Pin by pin differences

Pin number	TEA2029C	TEA2028B
1	Differential inputs of the frame error amplifier (including frame blanking safety in case of vertical stage failure).	Capacitor for horizontal output duration adjustment (29µs typ. with c1 = 3.3nF)
2		Vertical blanking safety input
4	Frame output for thyristor control	Vertical blanking output (21 lines duration)
10	Horizontal output (26µs typ. duration)	Horizontal output (duration is adjustable)
11	Supersandcastle output (with a frame blanking duration of 24 lines)	Supersandcastle output (with a frame blanking duration of 21 lines)
12	Negative horizontal flyback input (115 V_{PP} through a 47 kΩ resistor)	positive horizontal flyback input ($10V_{pp}$ through a 47kΩ resistor)
20	Positive AGC key pulse output (low level when no video)	Capacitor for frame sync. time constant adjustment
28	Safety input (inhibition of SMPS, Horizontal and Frame outputs when $V_{28} > 1.26V$)	Safety input (inhibition of SMPS, Horizontal outputs when $V_{28} < 1.26V$)

VII.3 - TEA2029C Pin connections

Pin number	Description
1	Frame error amplifier non-inverting input
2	Frame error amplifier inverting input
3	Frame saw-tooth output
4	Frame output (for thyristor control)
5	Frame ramp generator
6	Power Ground
7	SMPS control output
8	VCC Supply voltage
9	SMPS regulation input
10	Horizontal output
11	Supersandcastle output
12	Horizontal flyback input
13	Horizontal saw-tooth generator
14	Current reference
15	SMPS soft-start and safety time constant
16	Φ2 phase comparator capacitor (and horizontal phase adjustment)
17	VCO phase shift network
18	VCO output
19	VCO input
20	AGC key pulse output
21	Substrate Ground
22	Φ1 phase comparator capacitor
23	VCR switching input
24	Video and 50/60Hz identification output (Mute)
25	Video identification capacitor
26	Horizontal sync detection capacitor (50% of peak to peak sync level)
27	Video input
28	Safety input

Package : DIP28



VII.4 - Frame phase modulator

The Tranconductance Amplifier "A1" converts the differential input voltage into two output currents "I_{S1}" and "I_{S3}".

- A1 transconductance = $\frac{I_{S1}}{V_{IN}} = 10\mu A/mV$
- B transconductance = $\frac{I_{S2}}{V_2} = 40\mu A/V$
- Transfer characteristic = $\frac{\Delta t_{OUT}}{\Delta V_{IN}} = 6.4\mu s/mV$

The filter time constant is maximum near the operating point when $I_{S1} \cong I_{S2}$

In this case :

- The base current of T_1 = "I_{S2} - I_{S1}"
- The filter band-pass = 15kHz

The maximum conduction period of "40µs" is determined by the horizontal logic circuitry.

The frame frame flyback is detected by transistor "T3".

There is no feed-back during frame flyback and "I_{S3}" is maximum (higher than I_4) which will drive the "T3" into conduction.

Figure 73

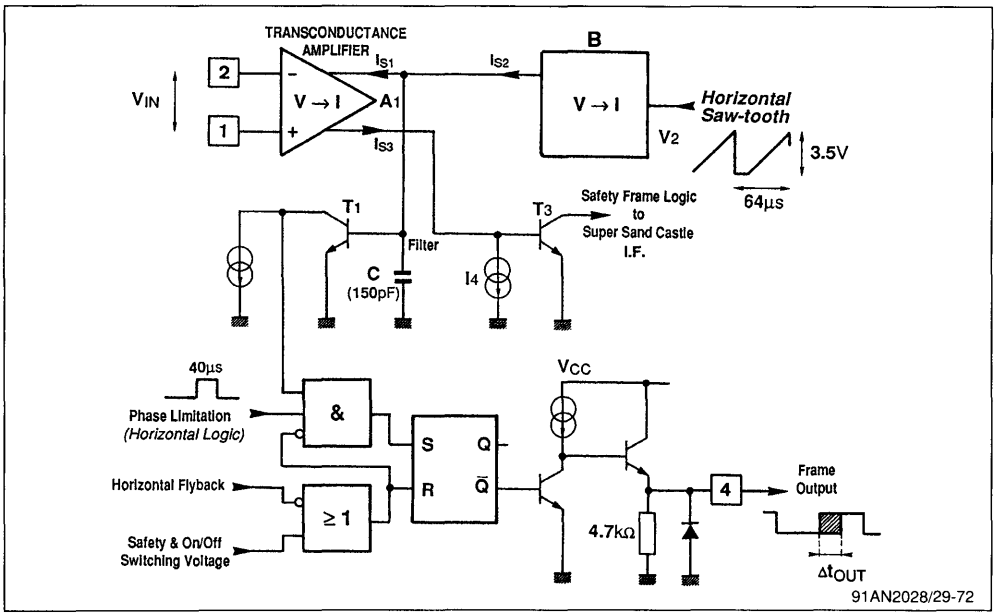
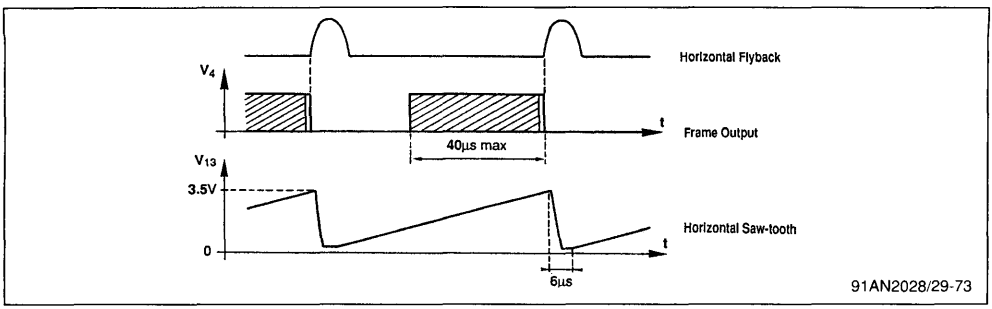


Figure 74

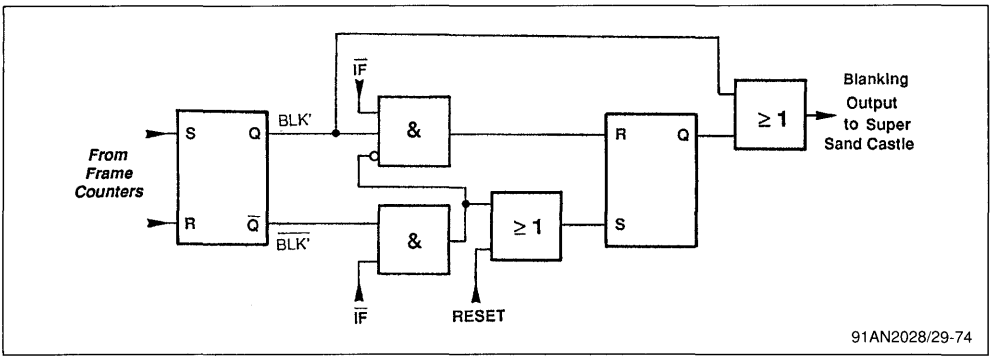


VII.5 - Frame blanking safety

- During trace : $I_{S3} < I_4 \Rightarrow$ T3 is blocked.
- During flyback : $I_{S3} > I_4 \Rightarrow$ T3 conducts.

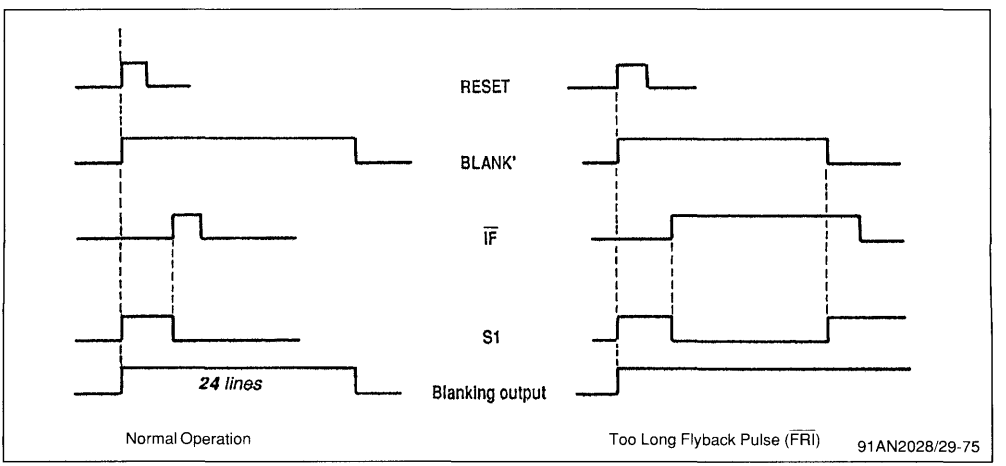
In the absence of flyback detection or if the flyback interval is longer than the blanking time, the sandcastle low level remains constant at 2.5V so as to protect the picture tube in the absence of frame scanning.

Figure 75 : Frame Blanking Safety Block Diagram



- "IF" signal is delivered by Frame Error Amplifier (see Frame phase modulator figure)
- $\overline{IF}$ is high during the Frame Flyback interval

Figure 76



VII.6 - On-chip line flip-flop

Figure 77

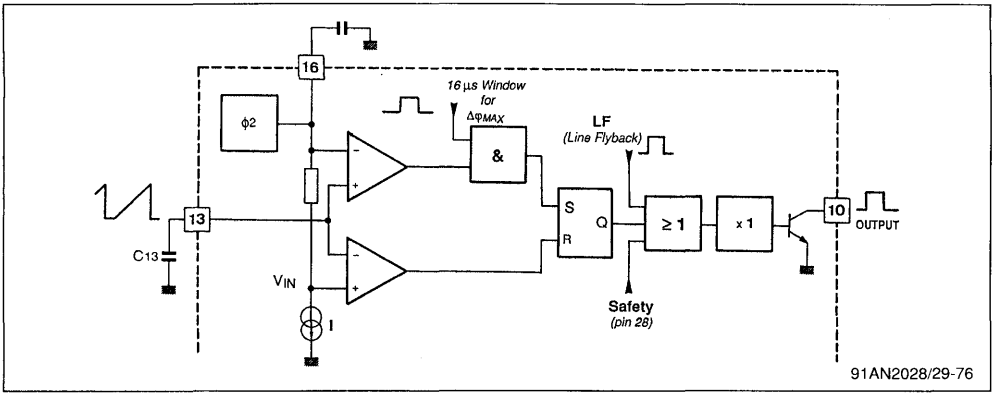
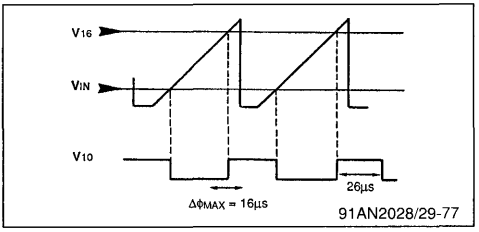


Figure 78



$T_{10} = 35 \times T_{VCO} - K \cdot R14 \cdot C13$

$= 70 \times 10^{-6} - 4R14 \cdot C13$

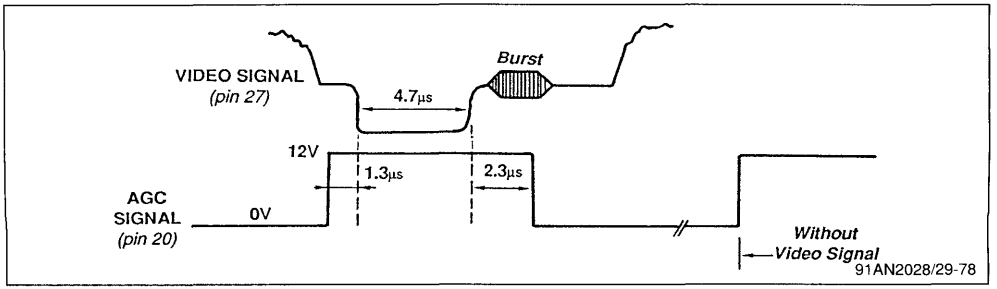
Where T_{VCO} is the V_{CO} period of oscillation on pin 18.

- If in synchronized mode :
- $T_{VCO} = 2\mu s$
- $R14 = 3.32k\Omega$
- $C13 = 3.3nF$

ThereforeT10 = 26µs (nominal value)

VII.7 - AGC key pulse

Figure 79



As illustrated below, this signal is used in some TV sets to perform sampling window for Automatic Gain Control of picture demodulation network.

This system is called "clamped" AGC, and locks the demodulated line sync amplitude and hence sets the video signal amplitude.

This signal generated by line logic circuitry is correctly positioned by the first phase locked loop "φ1" and includes the line sync pulse of the video signal. This is an open-collector output.

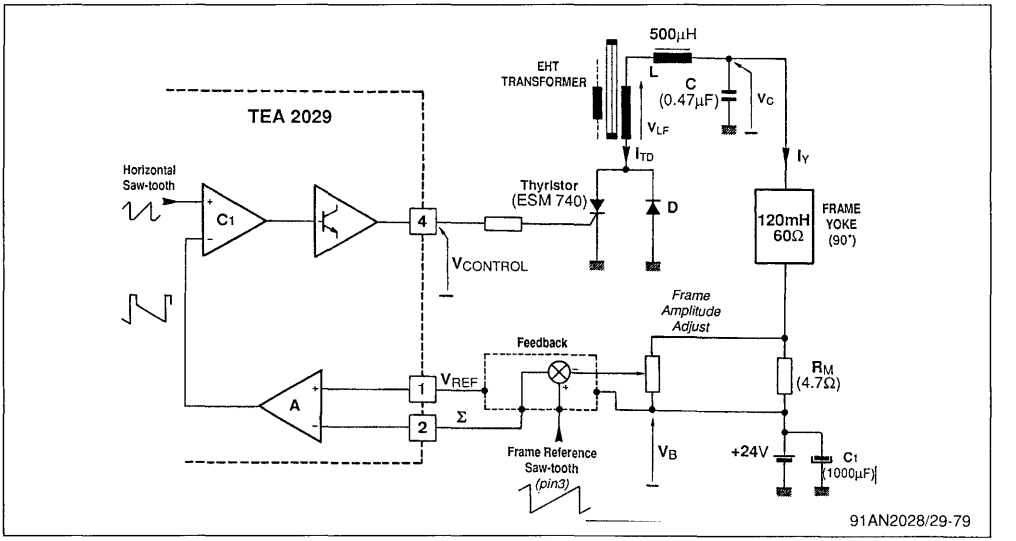
VIII - APPLICATION INFORMATION ON FRAME SCANNING IN SWITCHED MODE (TEA2029 ONLY)

VIII.1 - Fundamentals

The secondary winding of EHT transformer provides the energy required by frame yoke.

The frame current modulation is achieved by modulating the horizontal saw-tooth current and subsequent integration by a "L.C" network to reject the horizontal frequency component.

Figure 80 : Block diagram



VIII.2 - General description

The basic circuit is the phase comparator "C_1" which compares the horizontal saw-tooth and the output voltage of Error Amplifier "A".

The comparator output will go "high" when the horizontal saw-tooth voltage is higher than the "A" output voltage. Thus, the pin 4 output signal is switched in synchronization with the horizontal frequency and the duty cycle is modulated at frame frequency.

A driver stage delivers the current required by the external power switch.

The external thyristor provides for energy transfer between transformer and frame yoke.

The thyristor will conduct during the last portion of horizontal trace phase and for half of the horizontal retrace.

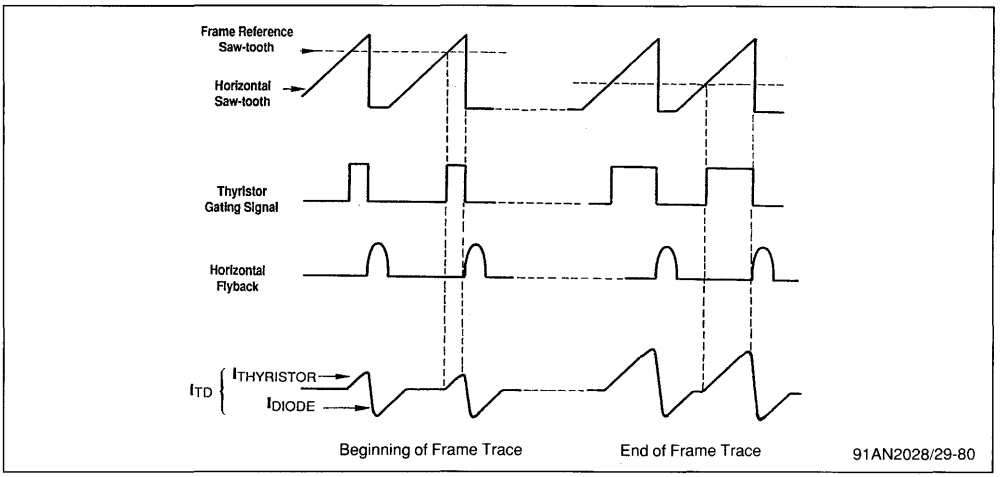
The inverse parallel-connected diode "D" conducts during the second portion of horizontal retrace and at the beginning of horizontal trace phase.

Main advantages of this system are :

- **Power thyristor soft "turn-on"**
  Once the thyristor has been triggered, the current gradually rises from 0 to IP, where IP will reach the maximum value at the end of horizontal trace. The slope current is determined by, the current available through the secondary winding, the yoke impedance and the "L.C." filter characteristics.
- **Power thyristor soft "turn-off"**
- The secondary output current begins decreasing and falls to 0 at the middle of retrace. The thyristor is thus automatically "turned-off".
- **Excellent efficiency of power stage** due to very low "turn-on" and "turn-off" switching losses.

VIII.3 - Typical frame modulator and frame output waveforms

Figure 81



VIII.4 - Frame power stage waveforms

Figure 82

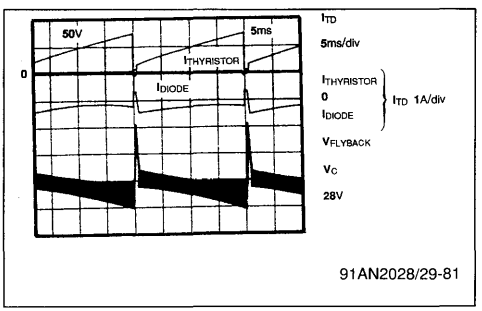


Figure 83

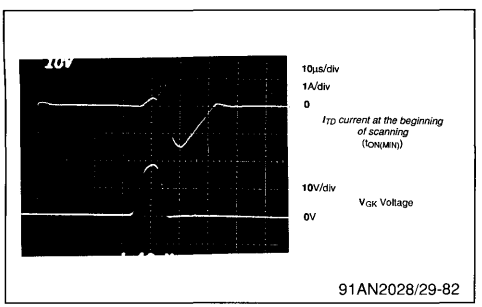


Figure 84

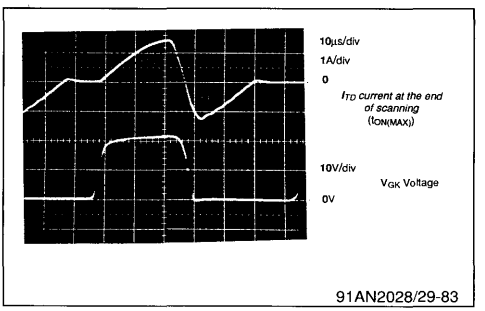


Figure 85 : Different horizontal conducting times during frame

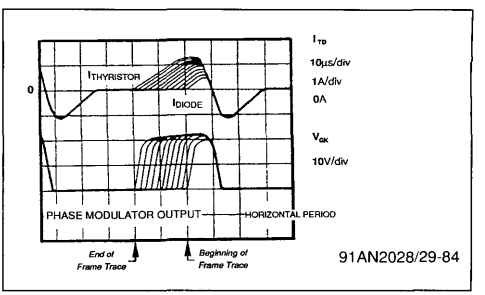
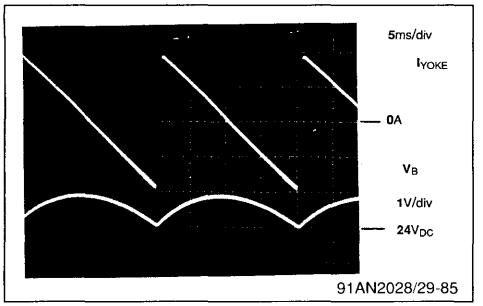


Figure 86



The bias voltage "V_B" is supplied by the secondary winding of EHT transformer. The parabolic effect is due to the integration of frame saw-tooth by the filtering capacitor "C1".

$$\Delta V_B = \frac{I_Y \cdot T}{8 \cdot C1} = 0.95V$$

Where :

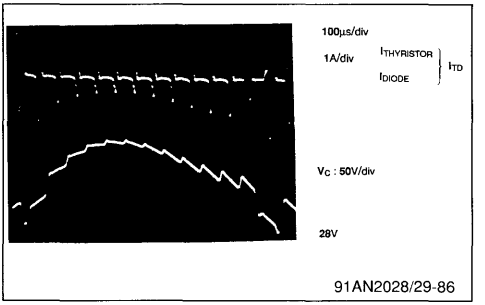
- I_Y : Peak-to-peak yoke current = 380mA$_{PP}$
- T : 20ms
- C1 = 1000µF

VIII.5 - Frame flyback

During flyback, due to the loop time constant, the frame yoke current cannot be locked onto the reference saw-tooth. Thus the output of amplifier "A" will remain high and the thyristor is blocked.

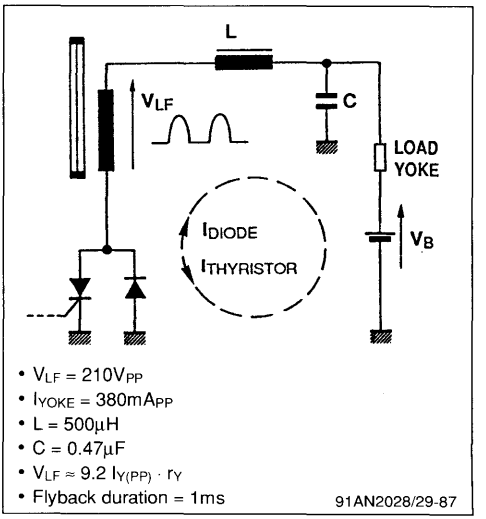
The scanning current will begin flowing through diode "D". As a consequence, the capacitor "C" starts charging up to the flyback voltage. The thyristor is triggered as soon as the yoke current reaches the maximum positive value.

Figure 87



EHT transformer winding
(for 90° tube : Yoke ⇒ L = 120mH, r_Y = 60Ω)

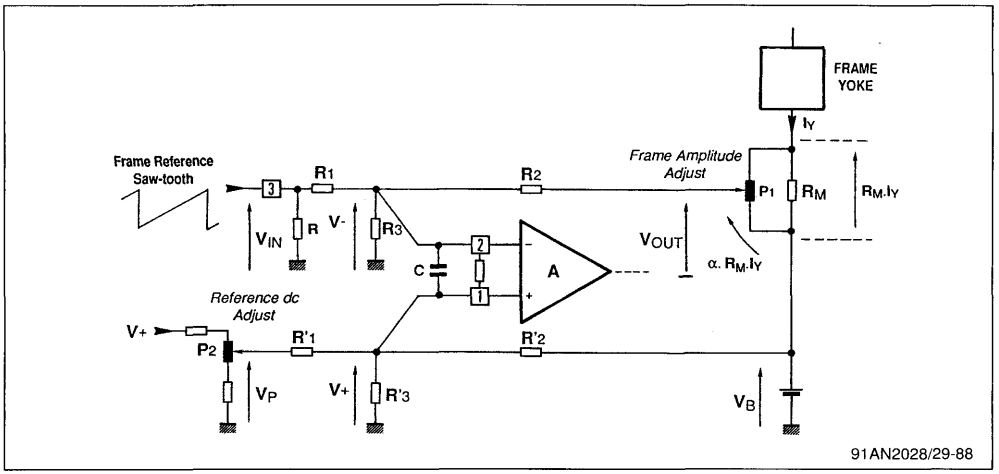
Figure 88



VIII.6 - Feed-back circuit

VIII.6.1 - Frame power in quasi-bridge configuration

Figure 89



This stage measures the frame scanning current in differential mode and compares it to the reference saw-tooth on pin 3.

The overall configuration is built around two symmetrical networks :

- "R_1, R_2, R_3" network : determines the dynamic saw-tooth voltage
- "R'_1, R'_2, R'_3" network : sets the bias voltage and the d.c. shift control.

a.c. gain : $G = \frac{R_2}{R_1} = \frac{I_Y}{V_{IN}} \cdot \alpha \cdot R_M$

where :

- I_Y : Peak-to-peak Yoke Current
- V_{IN} : Peak-to-peak saw-tooth voltage (pin 3)
- $\alpha \in [0,1]$: amplitude adjustment

VIII.6.1.1 - Choice of "R" value

The saw-tooth generator output is an emitter follower stage. Pin 3 output current must therefore be always negative.

$$R << R_1 \frac{V_{IN(MIN)}}{V_{BIAS} - V_{IN(MIN)}}$$

Where :

- V_{BIAS} : Bias voltage for pins 1 and 2
- $V_{IN(MIN)}$: Saw-tooth voltage low level

Example :

- $R1 = 22k\Omega$
- $V_{BIAS} = 5V$
- $V_{IN(MIN)} = 1.26V$

$$\Rightarrow R \approx \frac{R_1}{10}$$

VIII.6.1.2 - Influence of R_3 value

R_3 sets the bias voltage for pins 1 and 2. This voltage should be lower than 5.5V so as to enable the frame to function upon initial start-up at $V_{CC} = 6V$.

If the bias voltage is higher than this 5.5V level, the d.c. open-loop gain will fall thereby rendering the system more sensitive to d.c. drift.

Satisfactory results are obtained at V_{BIAS} values falling within 4V to 5V range.

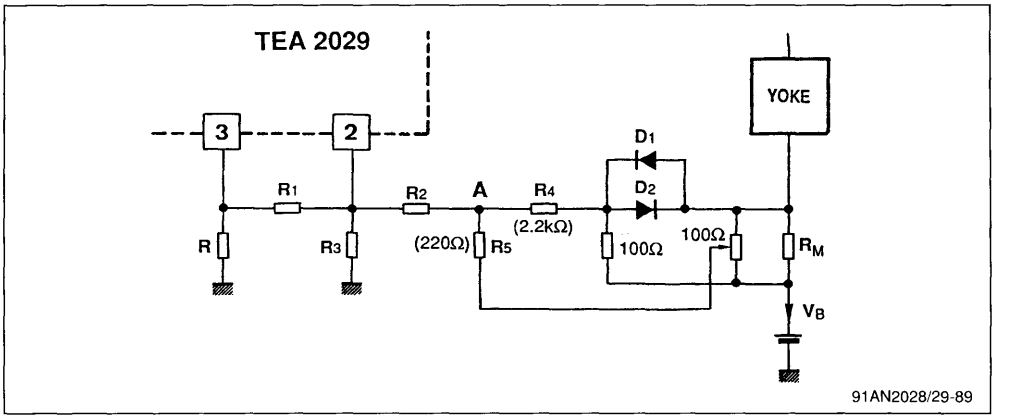
$$R_3 = R_2 \frac{V_{BIAS}}{V_B\,(V_{IN(MEAN)} \cdot G) - V_{BIAS}(1 - G)}$$

Where : $V_{IN(MEAN)}$: saw-tooth mean value (pin 3)

Capacitor "C" connected between pins 1 and 2 determines the system stability. Its value must be appropriately calculated as a function of "R_1, R_2 and R_3" values so as to reject the line frequency component.

VIII.6.1.3 - "S" Correction circuit in quasi-bridge configuration

Figure 90

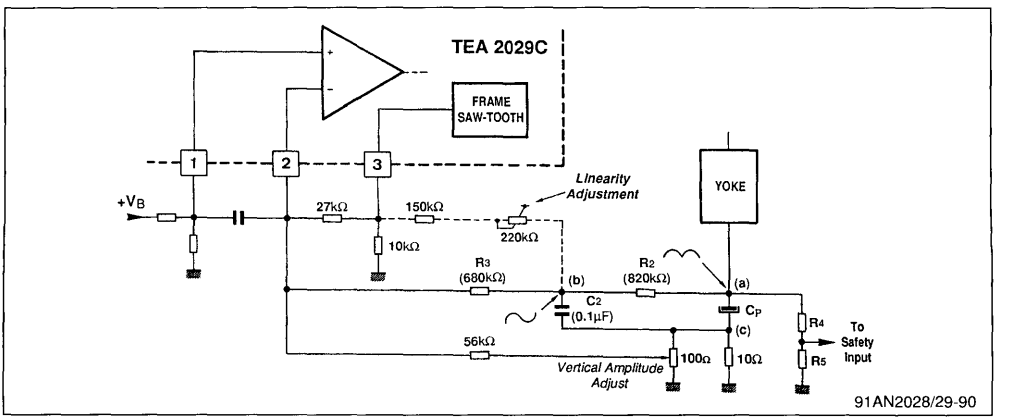


The "S" correction waveform is obtained using the non-linear "V_{DIODE}" versus "I_{DIODE}" characteristics of "D1" and "D2" diodes.

The signal pre-corrected by "D1", "D2" diodes and the feed-back signal through "R5", are summed at "A". The "S" correction level is determined by the ratio between "R4" and "R5" resistors.

VIII.6.2 - Frame scanning in switched mode using coupling capacitor

Figure 91



The parabolic voltage at (a) is integrated by "R2, C2" network and used for "S" correction.
The "S" waveform voltage at (b) is added to the saw-tooth voltage at (c). The "S" level is determined by "C2, R2, R3" network.

VIII.6.3 - Frame safety

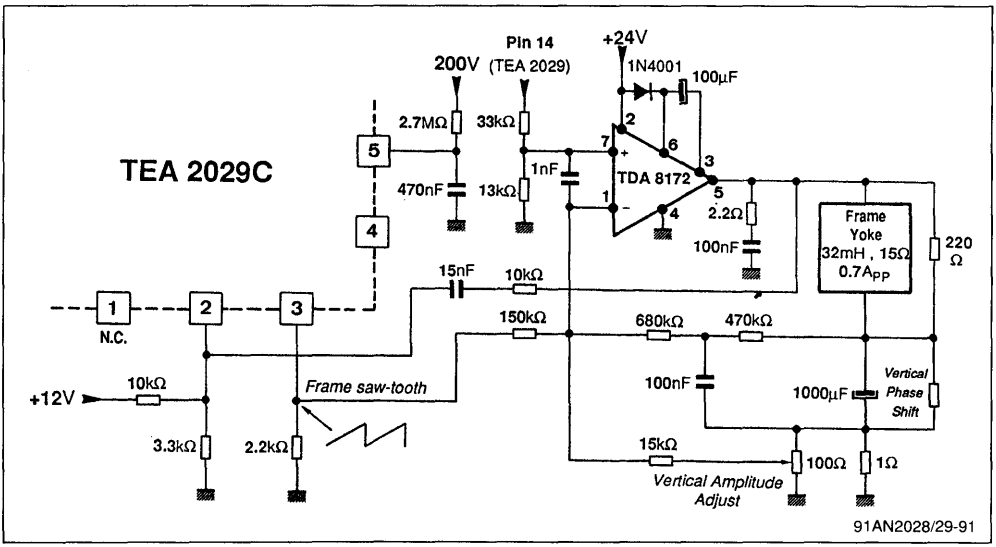
In case of failure in the loop, the thyristor may remain turned-off while the inverse parallel-connected diode conducts. This will result in a hazardeous situation where the voltage across the coupling capacitor "C_P" will reach an excessively high value.

To avoid such situation, the voltage at point (a) should be applied to the "Safety" input pin 28 after it has gone through the matching network "R4, R5".

VIII.7 - Frame scanning in class B with flyback generator

VIII.7.1 - Application diagram

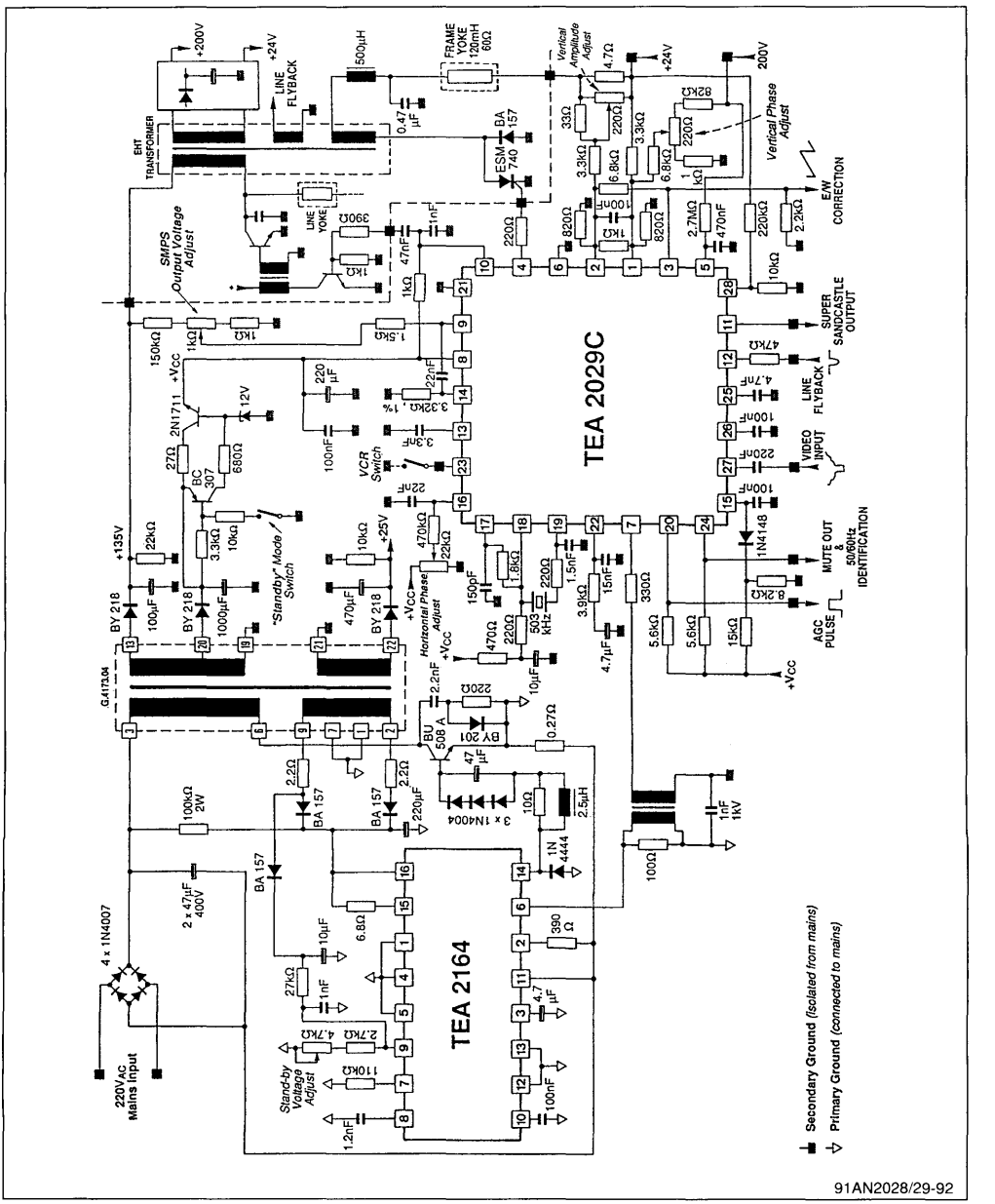
Figure 92



IX - TEA2029 APPLICATION DIAGRAM

Complete application with TEA2164

Figure 93



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA5170
SECONDARY CONTROLLER FOR MASTER-SLAVE STRUCTURE

By : T. PIERRE

SUMMARY

I - INTRODUCTION

The TEA 5170 is designed to work in the secondary part of SMPS, sending pulses to the slave TEA2164 which is located on the primary side of the main transformer.

The function of the regulation and synchronization are carried out by the TEA5170.

An accurate regulated voltage is obtained by duty cycle control.

The TEA5170 can be externally synchronized by a frequency higher or lower than the free-running frequency. This feature is particularly suitable for TV applications.

II - OPERATING PRINCIPLES OF MASTER-SLAVE STRUCTURE

This architecture offers two modes of operation :

- Master-slave mode (for normal operation)
- Burst mode (used during start-up and stand-by phases)

II.1 - Master-Slave mode

In this configuration, the master circuit located on the primary side, issues PWM pulses used for output voltage regulation. These pulses are sent via a pulse tranformer to the slave circuit (Figure 1). In this mode of operation, the falling edge of PWM signal may be synchronized by an external signal (e.g. by line flyback signal in TV applications).

II.2 - Burst Mode

During start-up and stand-by phases, no regulation pulses are issued by the master circuit and thus the slave circuit operates in burst mode. In this configuration, the slave circuit determines the switching frequency and the burst period. (See figure 2)

Figure 1

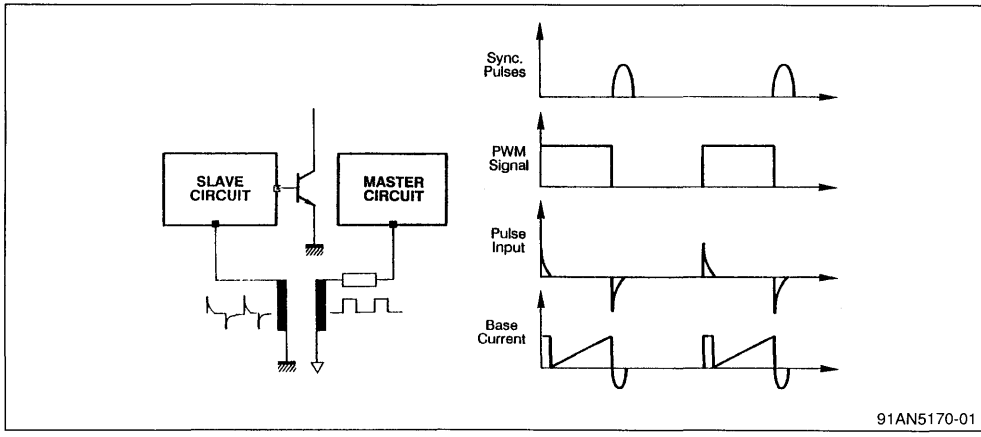
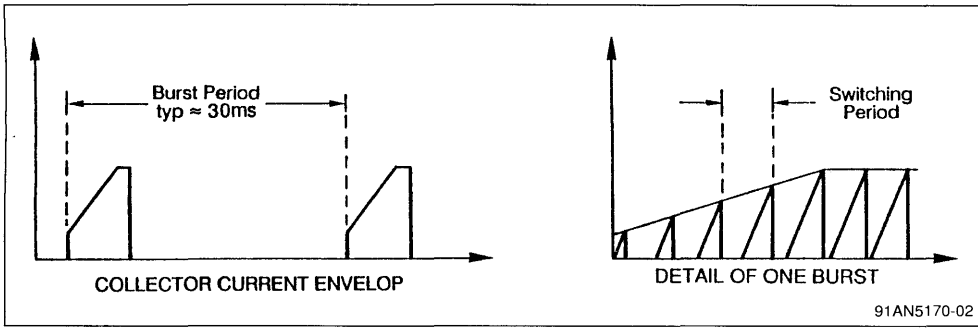


Figure 2 : Burst Mode Operation



II.3 - Operation of a Master-Slave Supply in TV Application

The arrangement generally employed is depicted in Figure 3. On the secondary side, a microcontroller is connected to the remote control receiver which issues control signals for stand-by and normal modes of operation. (Figure 4).

- In stand-by mode, the device power consumption is low (few Watts). The master will no longer send any control pulses to the slave which will consequently begin operating in burst mode.

Power supply regulation is performed by the slave circuit through the auxiliary winding.

- In normal mode of operation, the master circuit issues the PWM signal for regulation. The power supply operates in master-slave mode. The master circuit is simultaneously synchronized with the line flyback signal.
- Power supply start-up. As soon as the $V_{CC(START)}$ threshold is reached, the slave circuit begins operating in burst mode. While the secondary voltages are being stabilized, the microcontroller holds the TV set in stand-by mode.

Once the start-up phase is terminated, the set may remain in stand-by mode or switch into normal mode of operation.

Figure 3

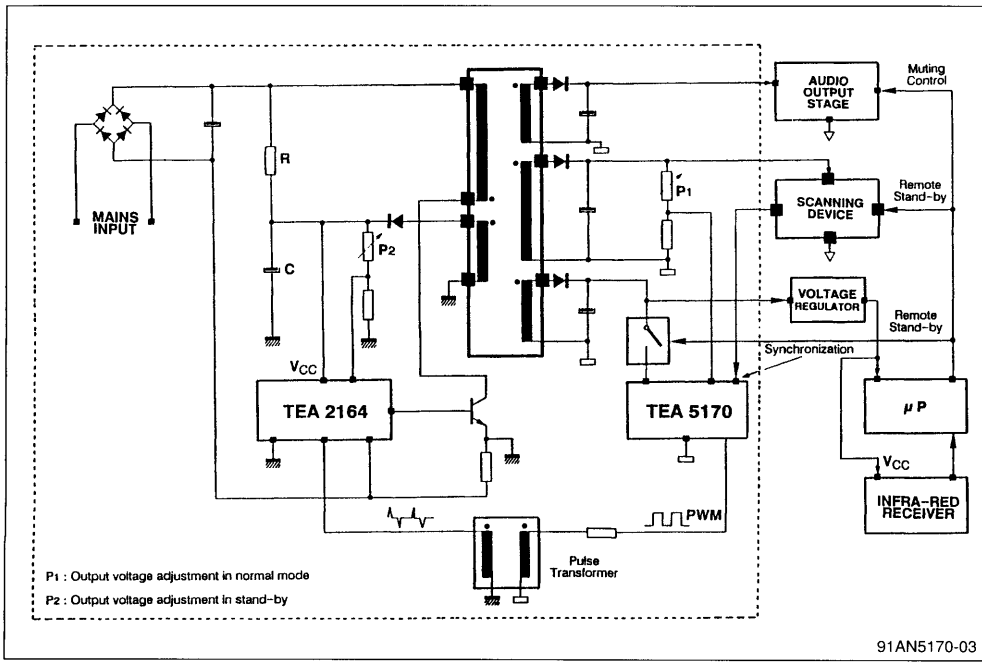
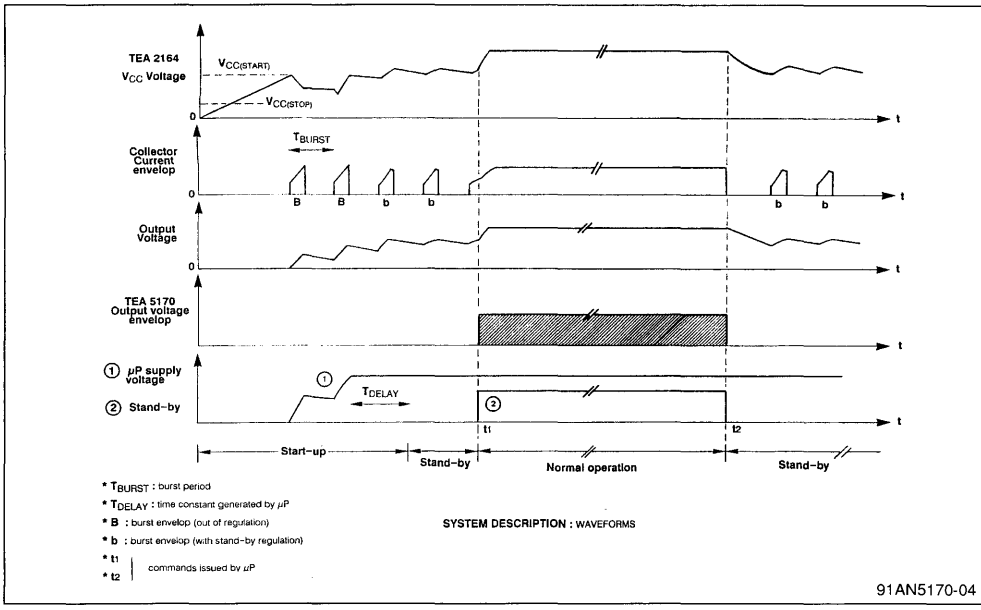


Figure 4

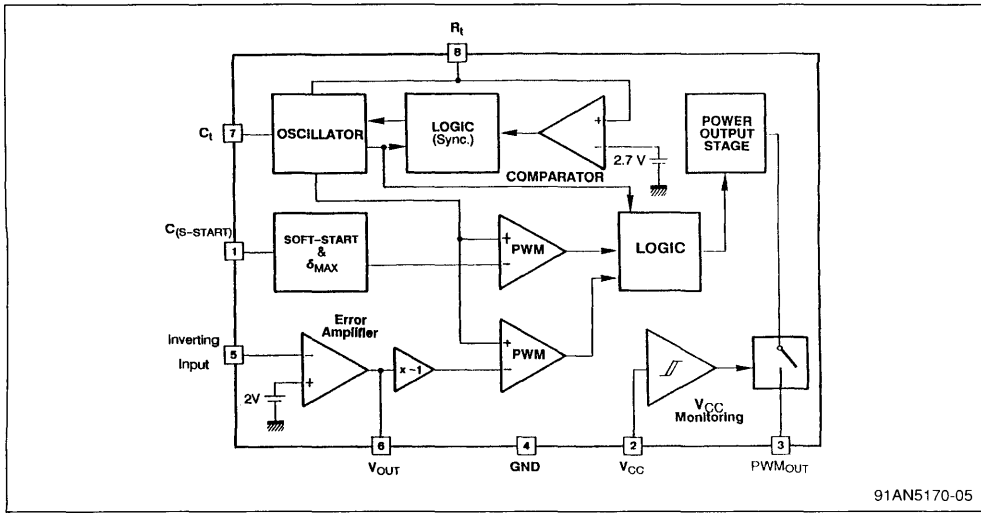


III - Description of TEA 5170

The TEA 5170 is a fixed frequency PWM signal generator operating in voltage mode regulation.

III.1 - Block Diagram

Figure 5



III.2 - Oscillator

The oscillator generates a linear saw-tooth signal and sets the free-running frequency. This oscillator can also operate in synchronized mode.

III.2.1 - Operation in free-running frequency mode. (See figure 6).

III.2.2 - Operation in synchronized mode

The oscillator is synchronized by forcing the saw-tooth return.

Enabling the synchronized mode (Figure 7)

The synchronized mode is enabled when the signal pulse on pin 8 (R_t) coincides with the oscillator saw-tooth return. The "C_t" capacitor charge current is then multiplied by a factor of 0.75.

The TEA 5170 will remain in synchronized mode as long as the synchronization pulses fall within the following window :

$(0.8\ T1 + T2) < T_{SYNC} < (1.33\ T1 + T2)$

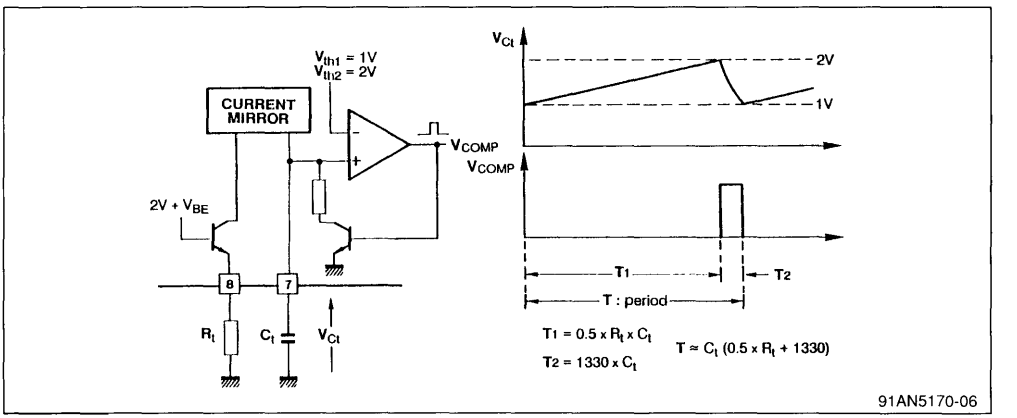
Where :

- T1 : C_t charge time in non synchronized mode.
- T2 : C_t discharge time

Synchronization signal (Figure 8)

Synchronization signal is applied to pin 8 "R_t" and the capacitor "C_t" is discharged when voltage "V_{Rt}" exceeds the "2.7 V" threshold.

Figure 6



Comment :

The internal current generator used to charge the "C_t" capacitor is disabled for the entire phase where "V_{Rt}" is higher than 2V. Thus, in order to maintain the saw-tooth shape of the oscillator signal, the "V_{Rt}" voltage should fall to 2V before the capacitor "C_t" full discharge.

Figure 7

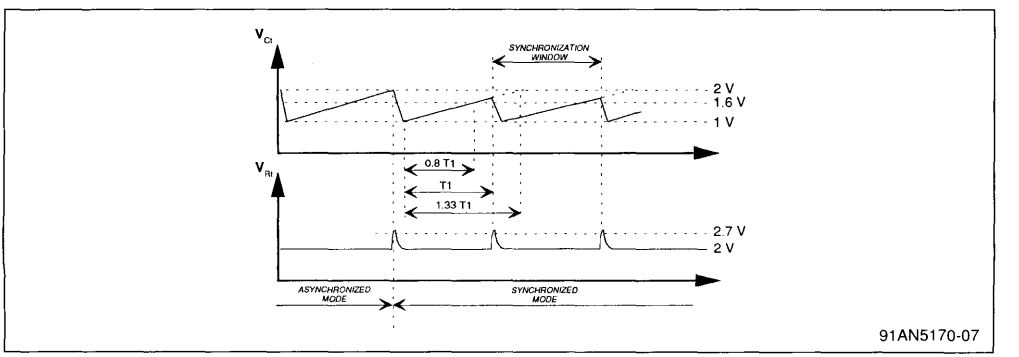
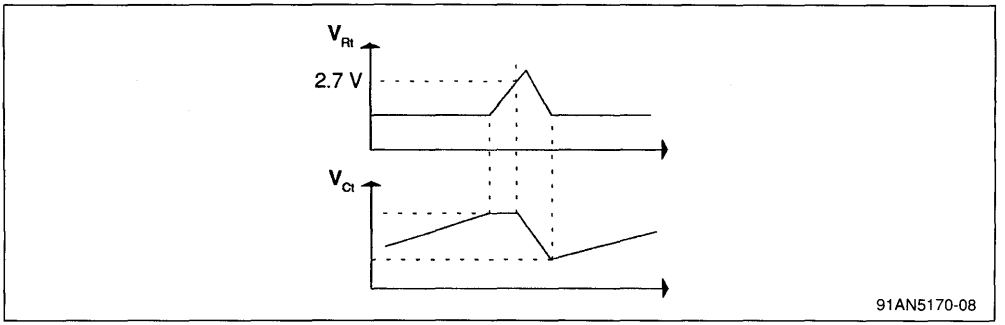


Figure 8



III.3 - Error Amplifier (Figure 9)

The on-chip error amplifier can be accessed through its inverting and output terminals.
The non-inverting input is internally tied to reference voltage level.

Comment :

An internal inverting amplifier sets the correct phase polarity of the error amplifier output signal for regulation.

III.4 - Pulse Width Modulation (Figure 9)

The TEA 5170 is a PWM signal generator operating in voltage mode. The pulse width is determined by comparing the error signal "V_{OM}" with the oscillator saw-tooth.

When the error signal "V_{OM}" exceeds the regulation range, internal threshold components will set a minimum conduction time $t_{ON(MIN)}$ and also limit the maximum conduction time $t_{ON(MAX)}$.

At initial start-up, a soft-start function implemented by linear charge of soft-start capacitor "$C_{(S\text{-}START)}$" is used to vary gradually the $t_{ON(MAX)}$ threshold. The output pulse width varies from $t_{ON(MIN)}$ to $t_{ON(MAX)}$ nominal value for $V_{C(S\text{-}START)}$ voltage variation of 0 to 2V.

Figure 9

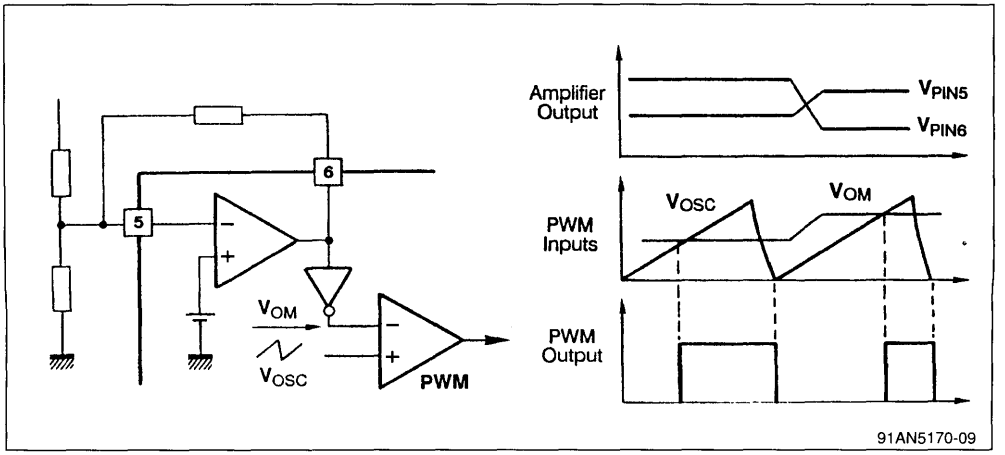
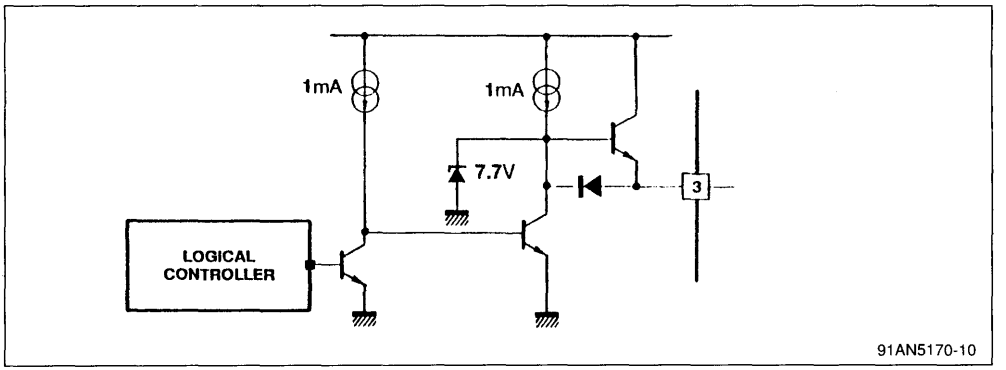


Figure 10



III.5 - Output Stage (see figure 10)

The output stage operates in on/off mode. For a supply voltage higher than 8V, the output signal value is independent of the supply voltage. (Typical value : 7V)

III.6 - V_{CC} Monitoring

V_{CC} Rising : When V_{CC} reaches the value "$V_{CC(START)}$", an internal switch enables the operation of the output stage and the soft-start capacitor begins charging.

The internal logic circuitry becomes operational before V_{CC} has reached the "$V_{CC(START)}$" value.

V_{CC} Falling : When V_{CC} falls below the "$V_{CC(STOP)}$" level, the negative output stage is switched-on, the transistor is turned off and the soft-start capacitor is discharged.

IV - TV POWER SUPPLY APPLICATION BUILT AROUND TEA5170 (Figure 15)

General structure and operational features of this power supply were outlined in section 1.

The details covered below apply to a power supply configuration using the slave "TEA2164" device.

(Refer to TEA2164 data sheet and application note "AN409/0591" for further details).

IV.1 - Main Application Characteristics

Characteristic	Value
Input voltage	$170V_{AC}$ to $270V_{AC}$
Output power	20W to 120W
Output power in stand-by mode	1W to 6W
Switching frequency	32kHz
Synchronization on line flyback signal (positive)	

IV.2 - Components External To TEA5170

Component Value Calculation

Also refer to TEA2164 application note "AN-409/0591" for calculation methods applicable to other power supply elements.

The external components determine the following parameters :

- Operating frequency
- $t_{ON(MIN)}$
- Soft-start
- Error amplifier gain

Ideal Values

- Period of operation "T_{OSC}" : 32µs
- $t_{ON(MIN)}$ duration : 1.2µs
- soft-start duration : 20ms
- Error amplifier gain :
  - DC gain G_{DC} = 35
  - AC gain at 1/10 x T_{OSC} : $G_{AC} = G_{DC}/5 = 7$

IV.3 - Free-Running Oscillation Frequency

For efficient use of TEA5170 and TEA2164 synchronization windows, the periods of both devices are determined as folows :

$$T_{OSC(5170)} = \frac{T_{SYNC}}{1.06}$$

$$T_{OSC(2164)} = \frac{T_{OSC(5170)}}{1.223}$$

Where :

- T_{SYNC} : line flyback signal period
- $T_{OSC(5170)}$: TEA5170 free-running period
- $T_{OSC(2164)}$: TEA2164 free-running period

Numerical Application

Period of synchronization signal being

$T_{SYNC} = 32\mu s$:

$$T_{OSC(5170)} = \frac{T_{SYNC}}{1.06} = 30.2\mu s$$

$$T_{OSC(2164)} = \frac{T_{OSC(5170)}}{1.223} = \frac{30.2}{1.223} = 24.7\mu s$$

The TEA5170 free-running period is determined as follows :

$T_{OSC(5170)} = C_t\ (0.5 \times R_t + 1330)$

Where :

$$C_t = \frac{t_{ON(MIN)} - 0.5 \times 10^{-6}}{1330}$$

- $R_t = 105k\Omega$ (1%)
- $C_t = 560$ pF (2%)

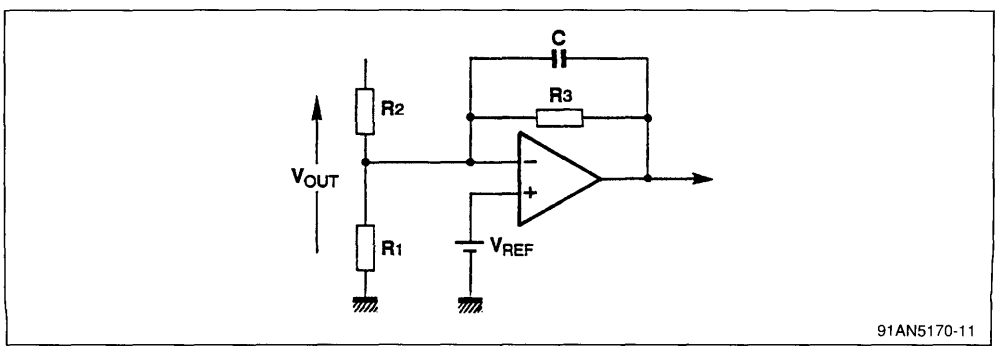
IV.4 - Error Amplifier Compensation

- A high DC gain is required for good accuracy.
- For stability reasons, the AC gain must be attenuated so as to avoid injection of the switching frequency component into the regulation loop.
- DC Gain : $G_{DC} = R3 \times \frac{R2 + R1}{R2 \times R1}$
- AC Gain : $G_{AC} = \frac{R3 \times \frac{1}{j\omega C}}{R3 + \frac{1}{j\omega C}} \times \frac{R2 + R1}{R2 \times R1}$

Assumptions :

- $R2 >> R1$ since $V_{OUT} > 10\ V_{REF}$ so the value of R2 does not modify the result of calculation and only R1 and R3 influence may be taken into consideration.
- $R1 = 2.2k\Omega$, $R3 = 75k\Omega$
- With cut-off frequency in AC regulation mode :
- $f_C = \frac{1}{10 \times T_{OSC}} \Rightarrow C = 2.2nF$

Figure 11



IV.5 - Synchronization Signal Matching Stage
(Figure 12)

The synchronization signal is generated from the line flyback.

The pulse amplitude is given by :

$$\frac{V_{PIN8(MAX)}}{V_{SYNC}} = \frac{R}{R + R_P} \text{ With } R_t >> R$$

The pulse time constant is $(R + R_P)C$ and should be lower than the saw-tooth fall time.

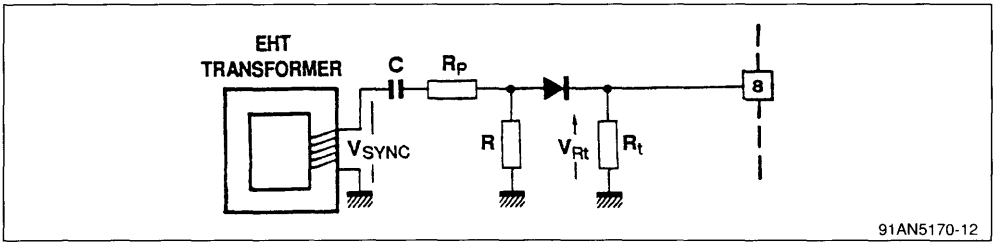
Thus, for a line flyback signal amplitude of 50V :

$R = 6.8k\Omega$, $R_P = 75k\Omega$, $C = 150pF$

Comment :

Practical and theoretical values may differ slightly since the rise time of the line flyback signal is not generally negligible.

Figure 12



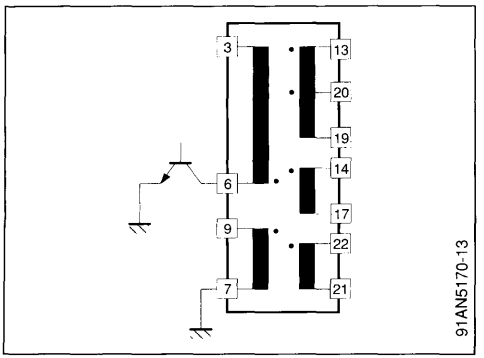
IV.6 - Soft-Start Period Duration

In this application, the duration of soft-start is around 20ms,

With :

- $C_{(S\text{-}START)} = T_{(S\text{-}START)} \times 2 \times 10^{-6} = 47nF$

Figure 13



IV.7 - Transformer Characteristics
(Reference : G4453-02 OREGA)

Winding	Pin	Inductance
n_P	3-6	680 µH
n_{AUX}	7-9	7 µH
n2	19-13	592 µH
n3	19-20	12 µH
n4	14-17	5 µH
n5	22-21	25 µH

IV.8 - Operation

IV.8.1 - Start-Up

The power supply of TEA5170 begins rising gradually upon initial start-up of the primary circuit. When V_{CC} reaches the value $V_{CC(START)}$ = 4V, the oscillator has already begun running and the soft-start capacitor "$C_{(S\text{-}START)}$" begins charging. The conduction time is $t_{ON(MIN)}$ and rises gradually.

IV.8.2 - Stand-By

This function is externally activated by grounding the *"stand-by"* input thereby disabling the power supply of TEA5170. (Figure 15).

To return to normal mode of operation, this pin should be left floating.

IV.8.3 - Synchronized Mode

The differentiator at synchronization input will transform the line flyback signal into a rectangular pulse whose time constant is around 1ms.

In this mode of operation, there is a lapse of time between the falling edge of the synchronization signal and the real transistor turn-off (Figure 13).

In TV applications, this time should be less than the line flyback duration so as to avoid the occurrence of on-screen visible disturbances.

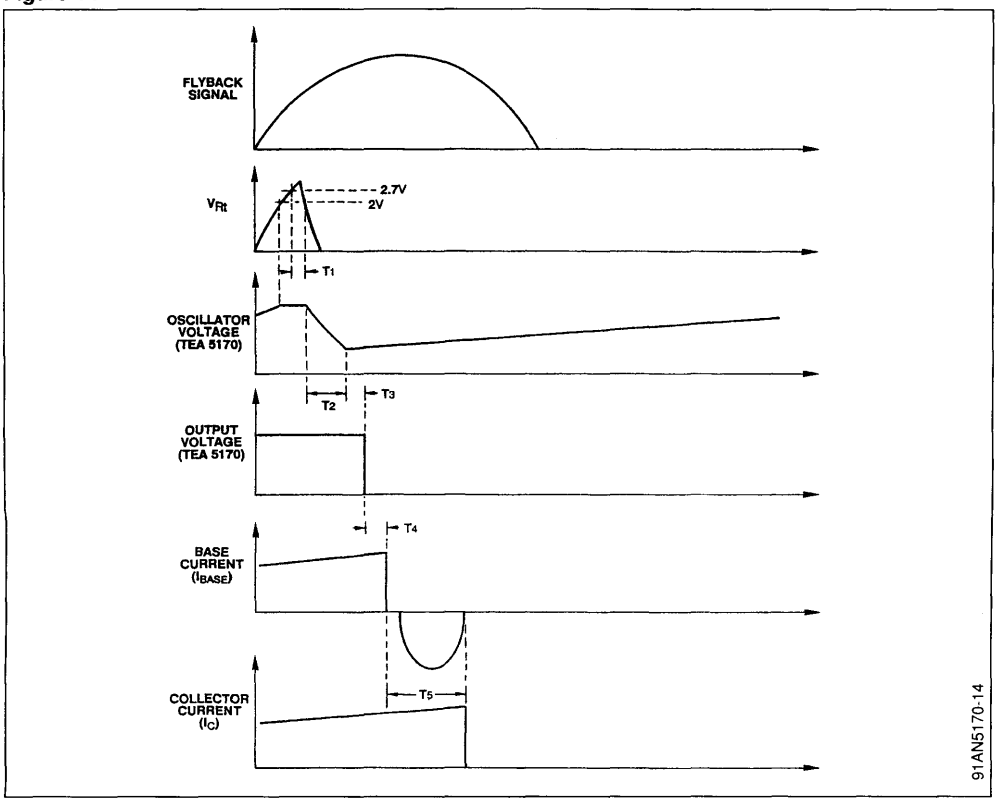
t1 and t3 times are specific to TEA5170 (t1 + t3 = 800ns typ.)

t4 is specific to the primary circuit (= 800ns typ. with TEA2164).

Only t2 = $t_{ON(MIN)}$ and t5 = t_{STG} of the switching transistor can be modified according to individual application requirements.

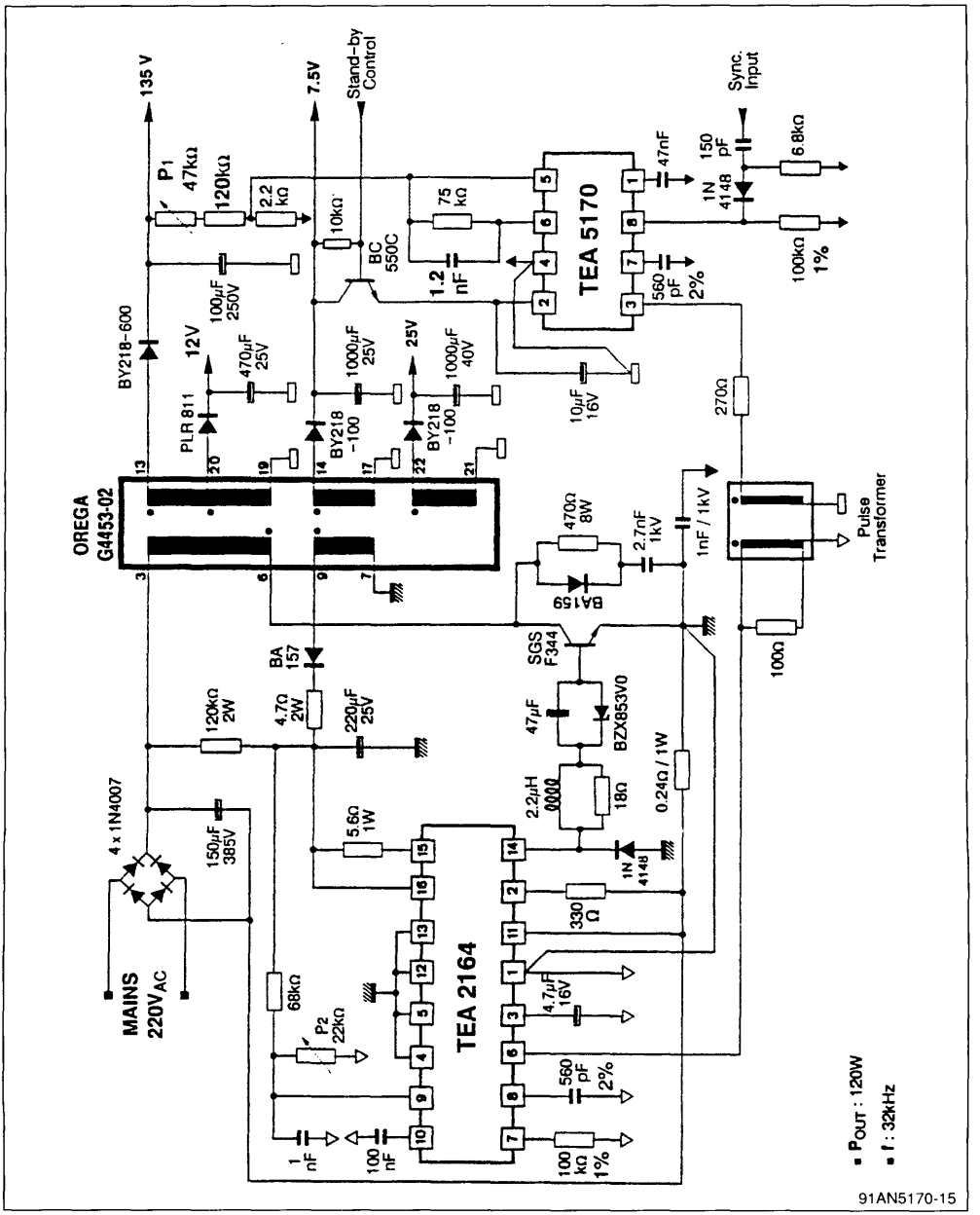
IV.9 - Delay Time In Synchronized Mode

Figure 14



IV.10 - Electrical Diagram

Figure 15



V - DC-DC CONVERTER

(9V ± 40% => 24V , 1.5W) (Figure 16)

This low power converter employs a transformer wound on a low-cost ferrite former.

The configuration is protected against open loads and short-circuits.

Transformer characteristics

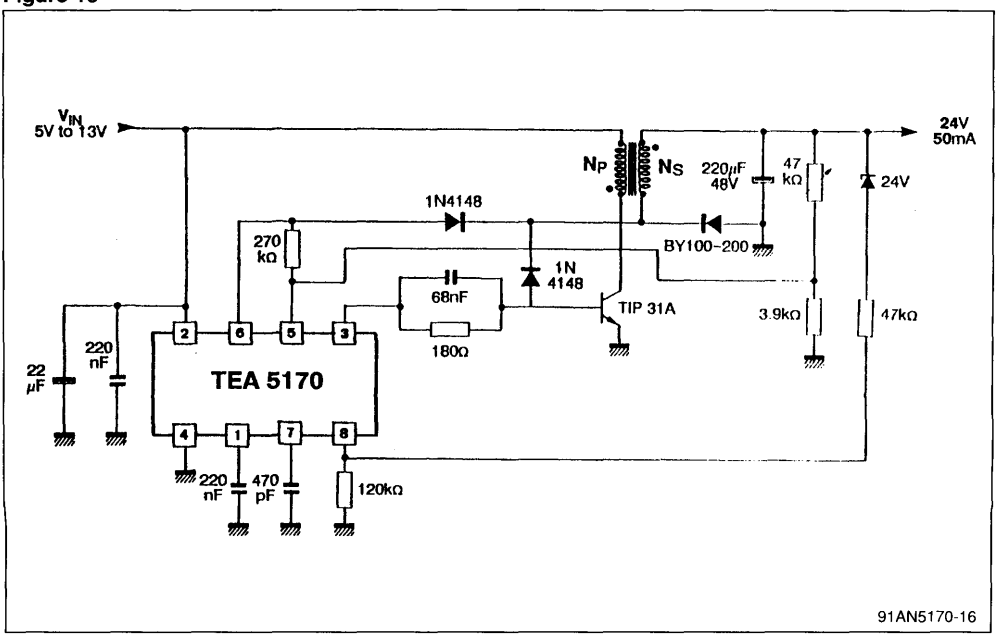
- Primary inductance : 53.5 µH
- Transformation ratio for 24V : n_S / n_P = 2

Regulation Characteristics

- Line regulation at 4.9V to 15V : 24V ± 0.22%
- Load regulation for (0.4P_{MAX} - P_{MAX}) : 24V ± 0.12%
- Power range : 0.24W to 1.6W
- Efficiency : 40%

V.1 - Electrical Diagram

Figure 16



V.2 - Operation

- The period of operation is determined by R_t and C_t components.
- Minimum conduction duration : 0.6 µs
- Free-running period : 29 µs
- Soft-start period duration : preset at 100 ms.

V.2.1 - Open-load Protection

In case of low load values, the minimum conduction time $t_{ON(MIN)}$ with respect to the period of operation is too high to maintain the output voltage at its nominal value. The only solution to stabilize the voltage is to increase the period of operation by reducing the charge current of the oscilator capacitor C_t. This is obtained by injecting additional current into resistor R_t as soon as the output voltage V_{OUT} rises.

V.2.2 - Short-circuit Protection

When the current through transistor becomes substantially high, the transistor is saturated and induces a high dI_C/dt . The diode on switching transistor base is then forward biased and begins deviating a portion of the base current. This phenomenon is self amplified and therefore results in rapid transistor turn-off.

V.2.3 - Demagnetization Monitoring

In order to avoid magnetic flux runaway, the transistor should be driven into conduction only once the transformer has been fully demagnetized.
While the transformer is being demagnetized, the secondary-connected rectifier diode is forward biased and thus maintains the error amplifier output at 0 potential. The allowed conduction period is consequently $t_{ON(MIN)}$.

VI - CONCLUSION

The TEA5170 requires a very simple configuration and yet offers excellent regulation quality combined with synchronization possibility for flyback-type converters.

The TEA5170 can be used in converters operating at 16 kHz to over 100 kHz frequency range.

Access to error amplifier and soft-start input are some of the remarkable features offered by this device whose application areas are by no means limited.

The TEA5170 belongs to the family of master controller devices characterized by their outstanding flexibility of use and application performances.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2164
MASTER-SLAVE SMPS FOR TV & VIDEO APPLICATIONS

By : B. D'HALLUIN

SUMMARY

SUMMARY *(continued)*

I - INTRODUCTION

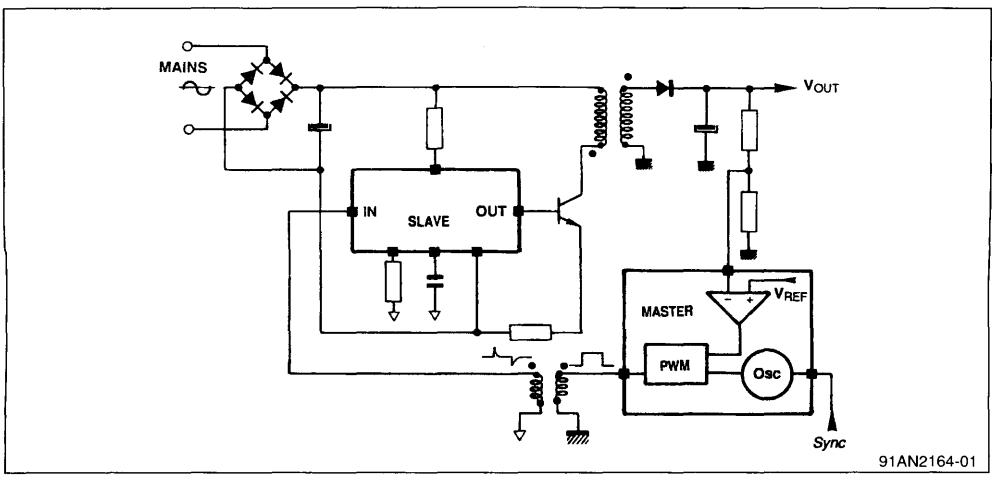
The TEA2164 is a Switching Power Supply Controller circuit designed to operate in Master-Slave structure.
This device is located on the primary side of power supply and requires the addition of other controller device such as TEA2028 or TEA5170 connected to the secondary side.

The main application of this circuit is in switching mode power supplies operating in discontinuous mode flyback configurations used in TV receivers at 60 W to 150 W power ratings.
The device incorporates a "Burst Mode" feature which offers excellent functional efficiency in "Stand-by" mode of operation.

I.1 - Master-slave structure

I.1.1 - Block diagram

Figure 1



I.1.2 - Fundamentals

The "Master" device located on the secondary side of the power *supply performs the following* functions :

- Output Voltage Control : Monitors the Conduction Period of the "Slave" circuit so as to provide Output Voltage Regulation as a function of Mains and Load variations.
- Switching Frequency Synchronization on Horizontal Scanning Frequency

The "Slave" circuit provides for the following functions :

- Power supply start-up
- Optimized Switching Transistor base drive
- Power supply regulation during stand-by operation
- Protection against
  - Overloads
  - Short-circuits
  - Open-loads
  - Missing control pulses normally delivered by secondary block.

I.1.3 - Principles of regulation

A fraction of the voltage to be regulated is obtained from a voltage divider network and compared to an internal reference voltage. The error voltage delivered by comparator is used to modulate the duration of the output pulse delivered by PWM (Pulse Width Modulation) Controller. The frequency of these pulses is determined by an internal oscillator synchronized on the horizontal scanning of the TV set.

PWM output signal is differentiated and forwarded towards the primary controller via a small low-cost pulse transformer which provides galvanic isolation between primary and secondary sections.

The differentiated positive signal pulse will turn the transistor on while the negative pulse will turn it off.

Conduction period variation will determine the amount of energy stored within the transformer during each cycle so as to maintain a constant output voltage whatever load and mains voltage variations.

I.1.4 - Advantages offered by this architecture

The "Master-slave" architecture offers the following advantages :

- Excellent output voltage regulation
- Main output voltage is not influenced by significant variations of auxiliary voltages (no sound interference within image display, even at audio power levels as high as 2 x 30 W).
- The coupling between transformer primary and secondary windings is no longer a critical requirement for regulation; which allows use of low-cost transformers (such as SMT5 series manufactured by OREGA)
- Synchronization on TV line scanning frequency will suppress any on-screen interference produced by power transistor turn-off, and eliminate the need of additional output voltage filtering components.
- All power supply protection features are implemented on primary side thereby allowing efficient and fast response to :
  - Current limitation
  - Overvoltage protection
  - Persisting overloads
- Other protections can be implemented to limit or disable the duration of regulation pulses issued by PWM, in case of failure detected within any section of the TV set.

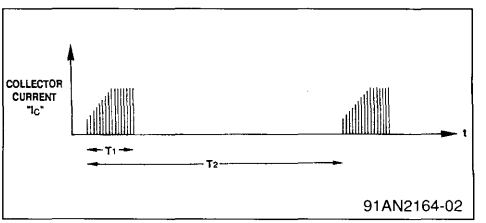
I.2 - Stand-by in burst mode

The secondary power required in stand-by mode is often quite low (1 W to 5 W in majority of cases).

Instead of operating the system at low t_{ON} duration, which is a difficult task with discontinuous mode transformer, the TEA2164 offers a "Burst Mode" to perform the stand-by function.

- T_1 : Burst duration

Figure 2



- T_2 : Burst period (period of VLF oscillator)

The T_1/T_2 ratio is fixed internally.

The TEA2164 allows the switching transistor to conduct only for typically 13% of the internal VLF oscillator period.

A pulse train "T_1" called "Burst" is thus obtained. The repetition period "T_2" can be set externally by capacitor "C_1" connected to pin 10.

In this mode of operation, the power transferred to the secondary windings is very low.

The collector current envelope has been optimized to yield efficient soft start and to minimize the audio

noise generated by switch mode transformer. Also, the free-running frequency "f_{OSC}" is shifted towards 20kHz so as to eliminate all audible noise in stand-by mode.

In this mode, the secondary output voltages are regulated by a feed-back loop on primary side. The TEA2164 will switch from synchronized mode (regulation by master circuit on secondary side) to burst mode (stand-by) as soon as the synchronization pulses, normally delivered by secondary block, are no longer available.

It is therefore obvious that the most efficient solution to implement the burst mode is to cut supply to master which will consequently be unable to deliver any synchronization pulse.

The stand-by function in burst mode offers the following advantages :

- Eliminates the need for auxiliary stand-by power supply and therefore its costly building elements such as stand-by mains transformer, relay or other specific components.
- Good power supply efficiency, thanks to burst mode, allows low mains power consumption in stand-by.

II - THE TEA2164 INTEGRATED CIRCUIT

II.1 - Description

The TEA2164 is cased in a 16-pin DIL package. The 4 center pins (2 on each side) are connected together and used to evacuate the heat.

The device includes the following functional blocks :

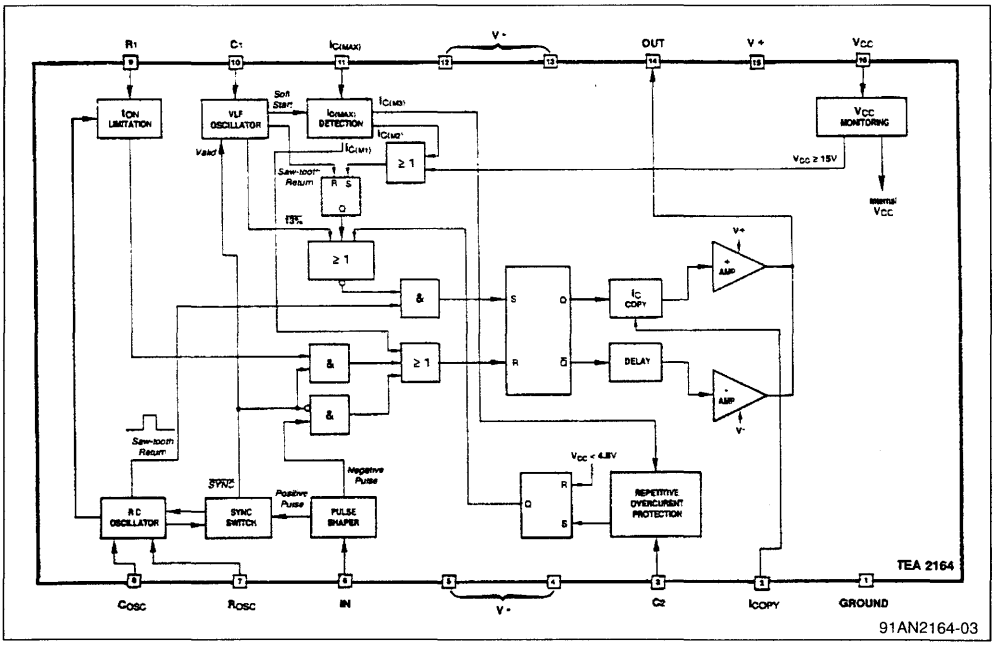
- A free-running oscillator which can be synchronized on the frequency of pulses issued from secondary.
- A Very Low Frequency (VLF) oscillator used for burst mode.
- An input stage to shape positive and negative input pulses.
- An output stage with two complementary amplifiers :
  - one, to provide the positive base current to turn the switching transistor on,
  - the other, to provide the negative base current required to turn the transistor off.

The positive base current is proportional to the collector current.

- A sophisticated protection system featuring :
  - Collector current limitation at 2 threshold levels
  - A device to memorize the occurrence of overloads and short-circuits, and to disable the power supply completely after a pre-determined time constant.
  - V_{CC} monitoring device with 2 thresholds :
    - Upper threshold : for overvoltage protection
    - Lower threshold with hysteresis : for system start-up
- Supply Voltages :
  - one pin for general supply (V_{CC})
  - one pin for power supply of the positive output stage (V^+)
  - four pins for power supply of the negative output stage (V^-)
    (according to application type, these pins can be grounded)
  - one pin for ground connection

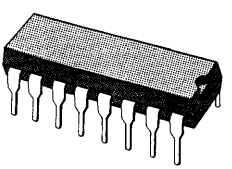
II.2 - TEA2164 Simplified block diagram

Figure 3



II.3 - Pin configuration

1	Ground
2	I_{COPY}
3	C_2
4	V^-
5	V^-
6	Input
7	R_{OSC}
8	C_{OSC}
9	R_1
10	C_1
11	I_{CMAX}
12	V^-
13	V^-
14	Output
15	V^+
16	V_{CC}



Batwing DIP16
(plastic package)

II.4 - Operating modes

II.4.1 - General description

The TEA2164 can operate in two distinct modes :

- "Normal" (or synchronized) mode :
  Synchronization and regulation by secondary controller circuit.
- "Burst" mode :
  In this mode, the TEA2164 operates as a stand-alone device.
  This mode is used upon start-up and in stand-by mode.

Two additional modes are also available :

- Long interval safety mode : the device is fully turned-off although it is correctly supplied (pin 3 capacitor has stored the occurrence of repetitive overcurrent)
- Start-up mode : the device is in low-consumption mode, its V_{CC} has not yet reached the $V_{CC(START)}$ threshold.

The normal start-up sequence is :

- Start-up Mode
- Burst Mode
- Synchronized Mode

II.4.2 - Synchronized mode

In synchronized mode, control pulses delivered by secondary block are differentiated and then applied to pin 6 input.

The positive pulse will synchronize the internal oscillator by discharging the "C_{OSC}" capacitor, which will generate a constant width pulse called "START" signal to be applied to positive stage output amplifier.

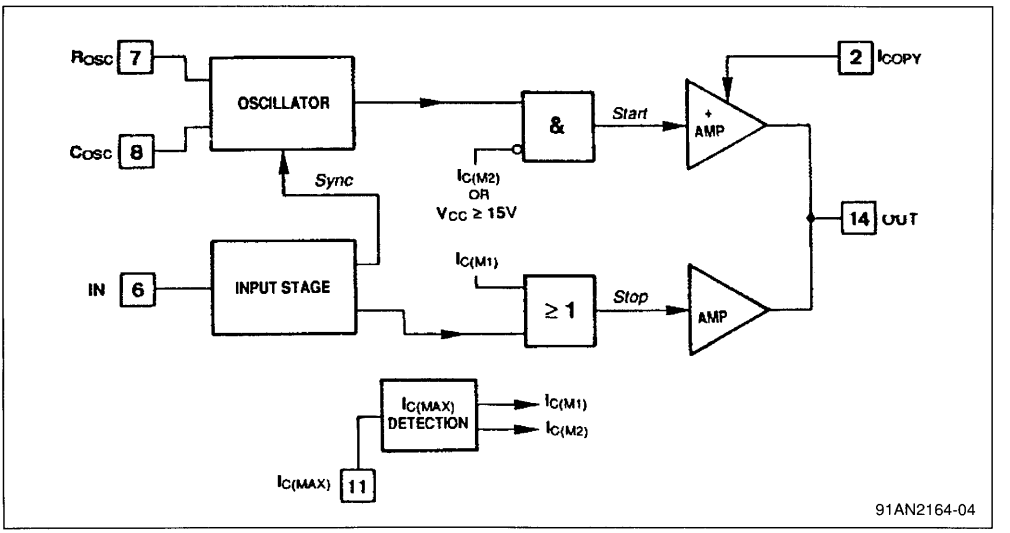
Similarly, the negative input pulse generates a "STOP" pulse which is applied to negative stage amplifier whose output is used to turn-off the switching transistor.

The "START" signal is disabled under following conditions :

- voltage applied to V_{CC} terminal is higher than +15V
- current protection device has detects a collector current higher than "$I_{C(M2)}$".

If the current reaches "$I_{C(M1)}$" threshold, the current limitation device will generate the "STOP" pulse.

Figure 4



II.4.3 - Burst mode

If no control pulses are present at device input terminal, the TEA2164 will operate as stand alone in burst mode.

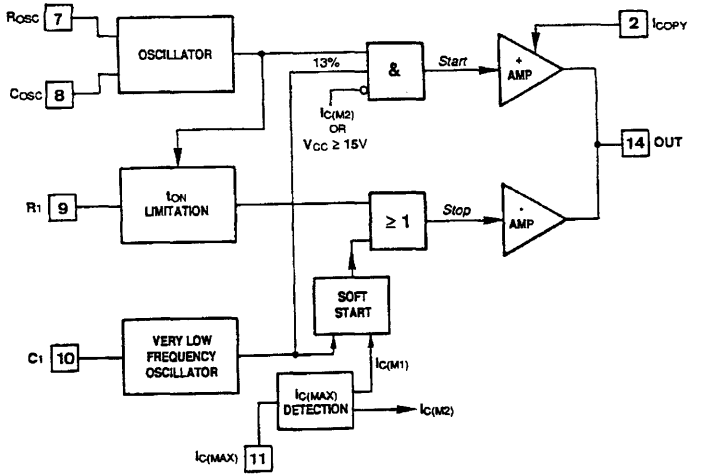
The switching frequency is given by the internal oscillator whose value depends on external components "R_{OSC}" (pin 7) and "C_{OSC}" (pin 8).

The "START" signal is generated by the oscillator and is used to turn the switching transistor on.

Transistor turn-off is performed by "$I_{C(M1)}$" current limitation through soft-start block or by "$t_{ON(MAX)}$" value set by resistor "R_1" connected to pin 9 (or voltage applied to pin 9).

The VLF oscillator will enable the "START" signal for 13% of its periode duration.

Figure 5



91AN2164-05

III - APPLICATION EXAMPLE
(120 W - Discontinuous mode flyback power supply with stand-by in burst mode)

III.1 - Characteristics & application diagram

III.1.1 - Characteristics

- Discontinuous mode flyback SMPS
- Standby function using the burst mode of TEA2164
- Switching frequency :
  - Normal mode : 15625Hz (synchronized on horizontal deflection frequency)
  - Stand-by mode : 19kHz
- Nominal mains voltage : $220V_{AC}$ (50Hz or 60Hz)
- Mains voltage range : $170V_{AC}$ to $270V_{AC}$
- Nominal output power : 120W
- Mains power consumption :
  - Normal mode : 150W max
  - Stand-by mode : 5W (with 3W at secondary side)
- Efficiency :
  - Normal mode : 85% (under nominal conditions)
  - Stand-by mode : 60%
- Regulation performance at high voltage output :
  - better than 0.5% versus mains variations of $170V_{AC}$ to $270V_{AC}$
  - better than 0.5% versus load variations of 35W to 120W
- Overload and short-circuit protection with complete power supply shut-down after a pre-determined time constant
- Open-load protection by output overvoltage detection

III.1.2 - Application diagram

The first diagram illustrates the primary block built around TEA2164.

The system is set into stand-by mode of operation by the switch connected to +15V supply.

Regulation pulses can be generated by a PWM device such as TEA5170 or delivered by a deflection circuit such as TEA2028 or TEA2029 which includes on-chip power supply regulation.

The second diagram depicts the full application diagram for a complete TV set power supply and scanning built around TEA2164 and TEA2029.

A microprocessor will introduce 100ms delay interval for the system to start-up in stand-by and then to switch into normal mode (synchronized and regulated by TEA2029).

Figure 6 : TEA2164 typical application

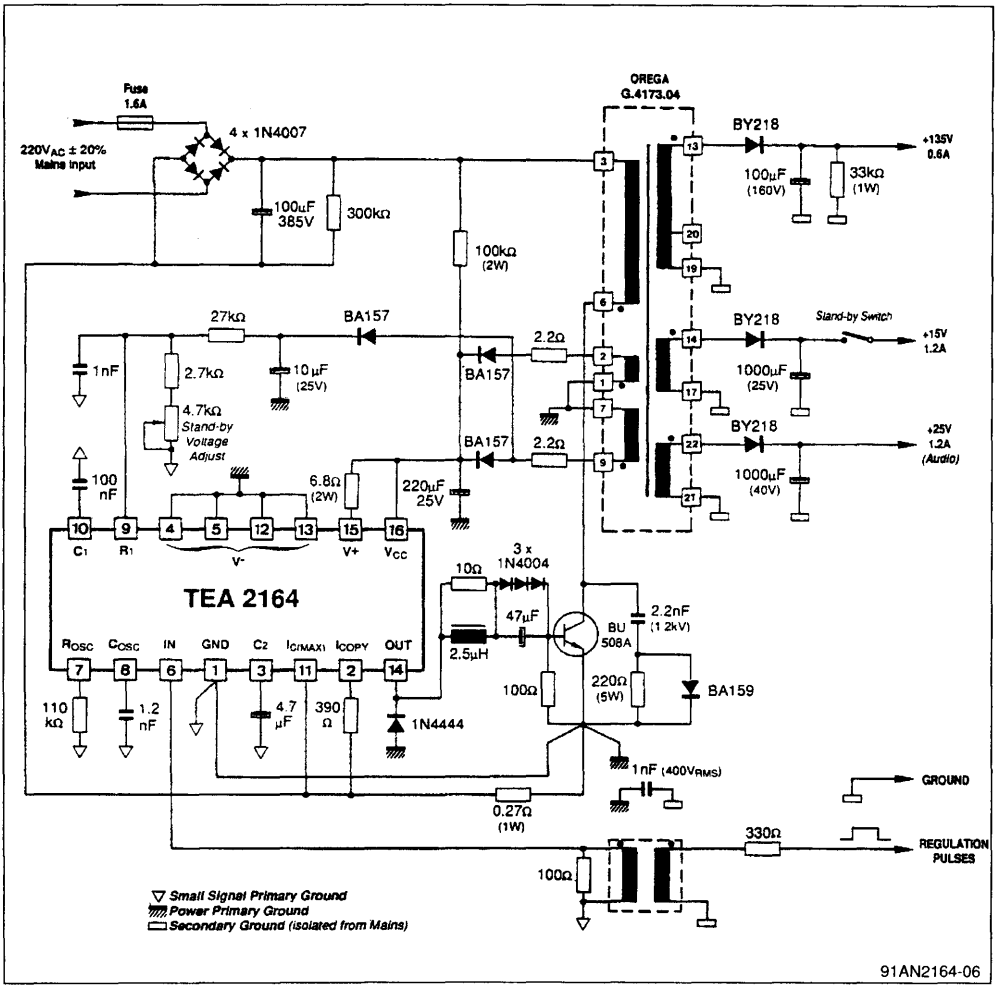
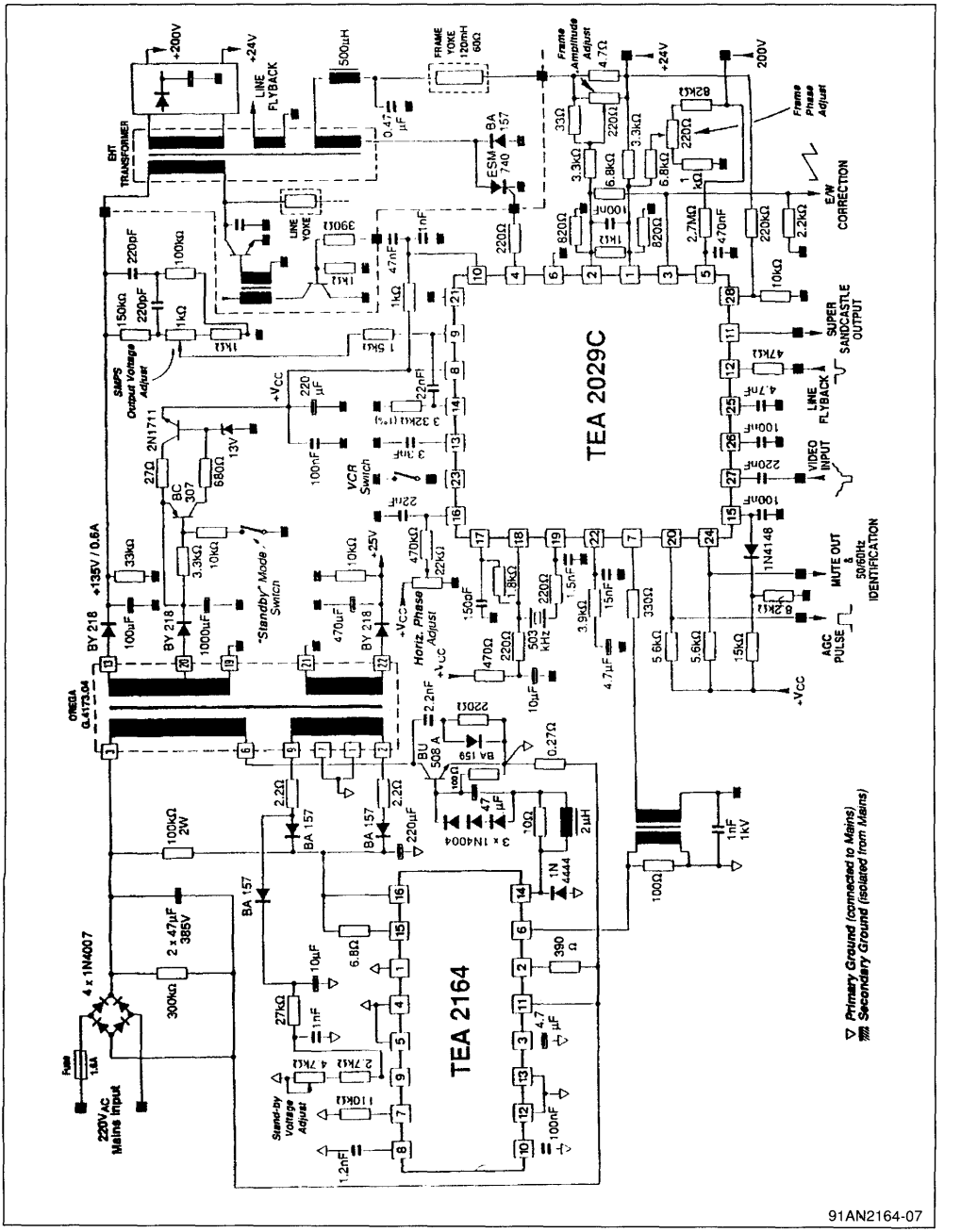


Figure 7 : SMPS & deflection complete application diagram

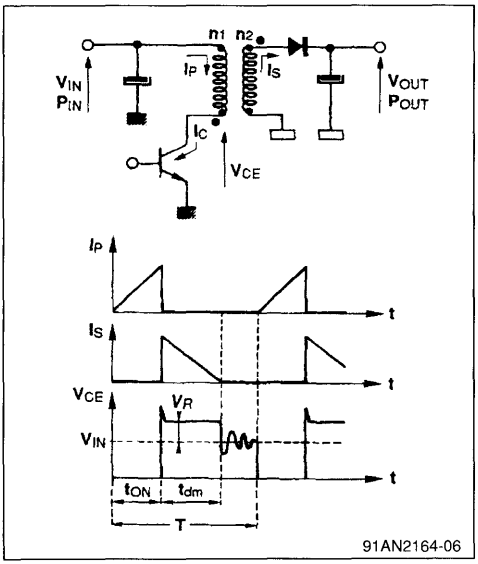


III.2 - Transformer calculation

The power supply must meet the following specification requirements :

- Mains voltage range : 170V_{AC} to 270V_{AC} (50Hz or 60Hz)
  i.e. 200V_{DC} to 380V_{DC} taking into account the supply ripple
- Output power : 10W to 120W max
  i.e. 150W at input
- Switching frequency : 15625Hz
- Main output voltage : +135V

Figure 8



The transformer primary inductance "L_P" and transformation ratio "n2/n1" are to be calculated while taking into consideration limits related to conduction time "t_{ON}" and switching transistor currents and voltages (I_C and V_{CE}).

Following conventional expressions are employed :

$$P_{IN} \approx \frac{L_P \times I_P^2}{2T} \quad (1)$$

$$I_P = \frac{V_{IN} \times t_{ON}}{L_P} \quad (2)$$

$$t_{dm} = \frac{n2}{n1} \times \frac{V_{IN} \times t_{ON}}{V_{OUT}} \quad (3)$$

combining (1) and (2)

$$t_{ON} = \frac{1}{V_{IN}} \times \sqrt{2P_{IN} \times T \times L_P} \quad (4)$$

combining (3) and (4)

$$t_{dm} = \frac{n2}{n1} \times \frac{1}{V_{OUT}} \sqrt{2P_{IN} \times T \times L_P} \quad (5)$$

First limit : The system should always operate in discontinuous mode

$$\text{therefore : } t_{ON(MAX)} + t_{dm(MAX)} \leq T \quad (6)$$

The worst case is specified with $P_{IN(MAX)}$ and $V_{IN(MIN)}$:

$$\left(\frac{1}{V_{IN(MIN)}} + \frac{\frac{n2}{n1}}{V_{OUT}}\right)\sqrt{L_p} \leq \sqrt{\frac{T}{2P_{IN(MAX)}}} \quad (7)$$

Second limit : Maximum voltage across the switching transistor :

$$V_{CE(MAX)} = V_{IN(MAX)} + V_R \quad (8)$$

where : $V_R = V_{OUT} \times \frac{n1}{n2}$

Third limit : Maximum current through the switching transistor :

$$I_{C(MAX)} = \sqrt{\frac{2P_{IN(MAX)}}{L_P} \times T} \quad (9)$$

To minimize the voltage across the power switch, we shall select a reflected voltage of V_R = 150V.

Therefore :

$$\frac{n2}{n1} = \frac{135V}{50V} = 0,9$$

- In order to take full advantage of the transformer ferrite core, one shall select the extreme limit of demagnetization :

therefore :

$t_{ON(MAX)} + t_{dm(MAX)} = T$

$$L_P = \frac{T}{2P_{IN(MAX)}} \times \left(\frac{V_{IN(MIN)} \times V_{OUT}}{V_{OUT} + \frac{n2}{n1} V_{IN(MIN)}} \right)^2 \quad (10)$$

$$L_P = \frac{64 \times 10^{-6}}{2 \times 150} \times \left(\frac{200 \times 135}{135 + 0.9 \times 200} \right)^2$$

$L_P = 1.55mH$

Characteristics of the ferrite core used in this case will require 80 primary and 72 secondary turns.

TRANSFORMER SPECIFICATIONS

- Reference : OREGA - SMT5 - G.4173-04
- Mechanical Data :
  - Ferrite : B50
  - 2 cores : 53 x 18 x 18 (THOMSON-LCC)
  - Airgap : 1.7 mm
- Electrical Data :

	Pin Number	Number of Turns	Wire Size (mm)	Inductance (µH)
Primary	3-6	80	0.45	1550
Forward	2-1	3	0.45	3
Flyback	7-9	7	0.45	14.5
Secondary				
+ 135V	19-13	72	0.45	1240
+ 15V	17-14	9	2 x 0.45	22
+ 25V	21-22	14	2 x 0.45	52

Using this transformer :

- maximum voltage across the switching transistor :

$$V_{CE(MAX)} = V_{IN(MAX)} + V_R$$

$V_{CE(MAX)} = 380 + 150 = 530V$

- maximum current :

$$I_{C(MAX)} = \sqrt{\frac{2P_{IN(MAX)}}{L_P} \times T}$$

$$I_{C(MAX)} = \sqrt{\frac{2 \times 150 \times 64 \times 10^{-6}}{1.55 \times 10^{-3}}} = 3.5A$$

- Maximum conduction time at $P_{IN(MAX)}$:

$$t_{ON(MAX)} = \frac{1}{V_{IN(MIN)}} \sqrt{2 \times P_{IN(MAX)} \times T \times L_P}$$

$$t_{ON(MAX)} = \frac{1}{200} \sqrt{2 \times 150 \times 64 \times 10^{-6} \times 1.55 \times 10^{-3}}$$

$t_{ON(MAX)} = 27.3\mu s$

- Minimum conduction time at $P_{IN(MIN)}$:

$$t_{ON(MIN)} = \frac{1}{V_{IN(MAX)}} \sqrt{2 \times P_{IN(MIN)} \times T \times L_P}$$

$$t_{ON(MIN)} = \frac{1}{380} \sqrt{2 \times 12.5 \times 64 \times 10^{-6} \times 1.55 \times 10^{-3}}$$

$t_{ON(MIN)} = 4.1\mu s$

Comment :

When using high value secondary filtering capacitors or if the switching transistor storage time is too long, the system start-up at high mains voltages may be difficult.

In fact, upon start-up, the secondary filtering capacitors are discharged which will result in very long demagnetization time. According to both, transformer characteristics and minimum conduction time, the transformer is magnetized and the peak primary current begins rising (the current does not any longer begin rising from zero).

In worst case, the current can reach the threshold level "$I_{C(M2)}$" which will consequently prevent the power supply start-up.

Two solutions are available :

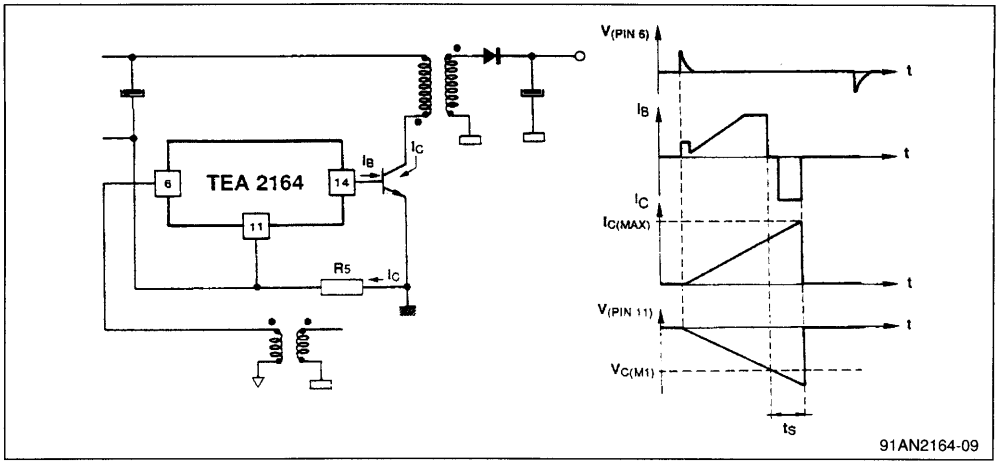
- Reduce the number of secondary turns which will decrease the demagnetization time (but also increase the switching transistor reflected voltage)
- Reduce the primary inductance while keeping the transformation ratio constant (which will also increase the RMS and peak current values)

Under all circumstances, an efficient transistor base drive combined with a not too long storage time (3.5µs to 4µs) are required.

III.3 - Switching transistor & its base drive

III.3.1 - Current limit calculation

Figure 9



The "R_S" resistor sets the switching transistor collector current limitation value. Power supply reliability is directly dependent on the value of this resistor, which is calculated as a function of the maximum power required from the secondary winding.

Lets set the secondary power limit at 150W value :

$$P_{IN} = \frac{P_{OUT}}{n} \Rightarrow P_{IN} = 175W$$

(with efficiency n = 0.85)

$$I_{C(MAX)} = \sqrt{\frac{2P_{IN(MAX)} \times T}{L_P}}$$

$$I_{C(MAX)} = \sqrt{\frac{2 \times 175 \times 64 \times 10^{-6}}{1.55 \times 10^{-3}}} = 3.8A$$

The storage time at this current value is approximately 4µs (with BU508A).

The collector current slope at nominal mains voltage is 0.2A/µs .

The current limitation threshold level must therefore be fixed at 3A.

The "$I_{C(M1)}$" voltage threshold is typically 0.84V :

$$\text{therefore : } R_s = \frac{0.84}{3} = 0.28\Omega$$

In practice, the selected value is $R_S = 0.27\Omega$

At minimum mains voltage level, the slope is smaller and the maximum current therefore becomes :

$$I_{C(MAX)} = \frac{0.84}{0.27} + \frac{200}{1.55 \times 10^{-3}} \times 4 \times 10^{-6} = 3.6A$$

At maximum mains voltage level, the slope is sharper and the maximum current therefore becomes :

$$I_{C(MAX)} = \frac{0.84}{0.27} + \frac{380}{1.55 \times 10^{-3}} \times 4 \times 10^{-6} = 4.1A$$

III.3.2 - Switching transistor

It was demonstrated that under normal operating conditions, the maximum collector current value is around 4.1A while the maximum collector voltage is approximately 530V.

Factors such as the overvoltage produced at the time of transistor turn-off, transformer leakage inductance and peak currents generated in the event of short-circuits, must be also taken into account.

At the time of transistor turn-off and under worst case conditions (maximum mains voltage, significant overload), the "V_{CE}" voltage across the transistor can reach 1000V.

Therefore, a transistor with $V_{CES} \geq 1200V$ must be selected.

In case of short-circuit, transformer is magnetized and the collector current value will reach 5A (with 0.27Ω measurement resistor and 1.35V typ. $V_{C(M2)}$ threshold).

Therefore, a transistor with $I_{C(MAX)} \geq 7A$ must be selected.

The BU508A and equivalents are perfectly suitable.

III.3.3 - Switching aid (snubber) network

The "Snubber" network is built using a combination of "R , C , D" components to limit the dV/dt slope and to reduce the collector current rise up at the time of transistor turn-off.

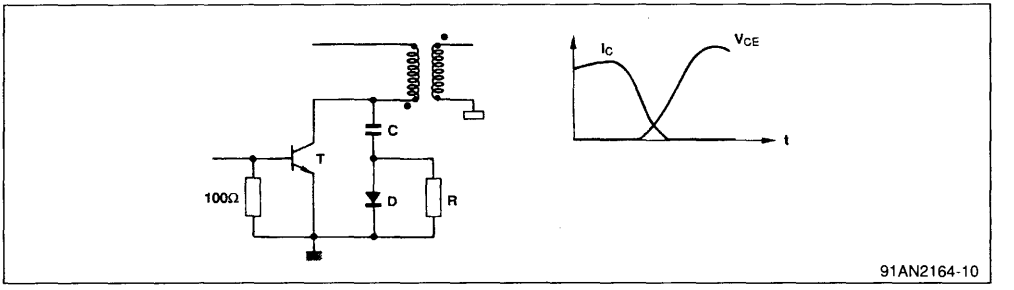
Switching losses at turn-off which are proportional to "V x I" product are thus minimized.

- C = 2.2nF
- R = 220Ω
- D : BA159
- T : BU508A

Whatever load and input voltage conditions, it must be ensured that the system will operate permanently within the safe operating area of the transistor.

A 100Ω resistor connected between transistor base and emitter terminals will improve the voltage behaviour.

Figure 10

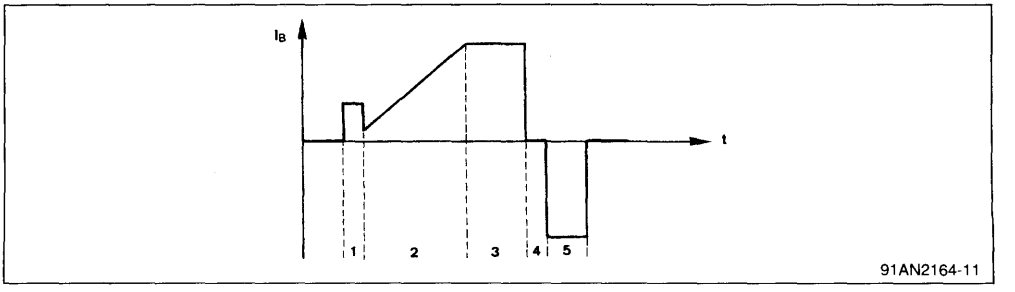


III.3.4 - Base drive

A bipolar switching transistor requires a positive base current to enter into saturation while a negative base current is necessary to turn it off.

The shape of base current waveform is illustrated in the following Figure.

Figure 11



1 - Constant amplitude pulse to turn the transistor on (duration depends on oscillator saw-tooth return)

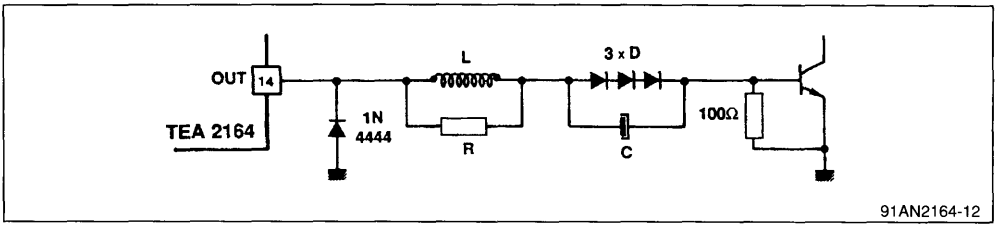
2 - Base current proportional to the collector current (I_{COPY} function on pin 2)

3 - Saturated base current to limit the circuit power dissipation (function implemented through the resistor in series with pin 15)

4 - On-chip delay interval of "0.7µs" to prevent simultaneous conduction of positive and negative stages

5 - Negative base current to remove the charge stored within base (storage time - duration of which depends on type of switching transistor)

Figure 12



- L = 2.5µH
- R = 10Ω
- C = 47µF
- D : 1N4001

The base drive circuit is a "capacitive coupled" device. There is therefore no need to apply a negative voltage "V -" to pins 4, 5, 12 and 13 which will be grounded. P.C.Board tracks connected to these pins must be wide enough to allow efficient evacuation of the power dissipated by device.

The positive base current goes through 3 diodes connected in series. Capacitor connected across these diodes will be charged to a value equal to 3 times forward diode voltage drop. This voltage is sufficient to turn the transistor off.

This capacitor must be selected to withstand the effective current through it, which is mainly the negative turn-off current.

The inductor in series with base, limits the dIB/dt slope and thus the base current, at the time of transistor turn-off. The inductance value must be adjusted to yield efficient turn-off while the negative current delivered by TEA2164 should not exceed -1.7A . The 10Ω resistor connected across this inductor helps the damping of base current oscillations at the beginning of transistor conduction.

Comment :

In order to avoid all problems at TEA2164 output stage, it is recommended to connect a 1N4444 diode between the output terminal (pin14) and the ground, as illustrated in Figure 12 above.

In case of capacitive drive and if a negative voltage appears across output terminal (due to inductor L), this diode will deviate the current towards ground thereby preventing reverse bias of the negative output stage.

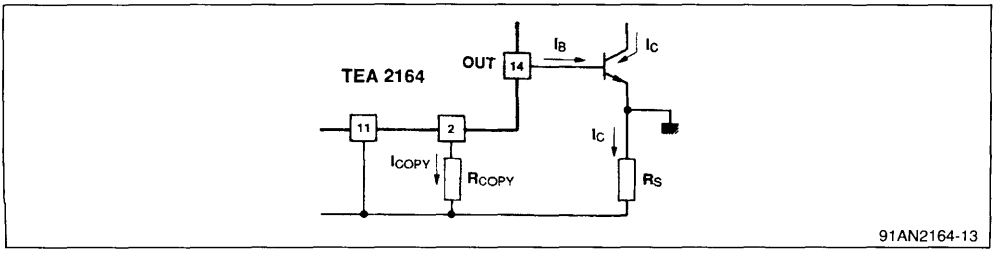
III.3.5 - R_{COPY} Resistor Calculation

This input is used to set the switching transistor forced gain, that is, to deliver the base current necessary for a required collector current.

Input pin 2 can be considered as a virtual ground terminal and therefore :

$R_S \times I_C = R_{COPY} \times I_{COPY}$

Figure 13



Also, the current gain between input (pin 2) and the output (pin 14) is :

$1000 \Rightarrow I_B = 1000 \times I_{COPY}$

The forced gain is therefore :

$$\frac{I_C}{I_B} = \frac{R_{COPY}}{R_S} \times \frac{1}{1000}$$

A forced gain of 2.25 (BU508A) with $R_S = 0.27\Omega$ will yield : $R_{COPY} = 600\Omega$

In practice, one would select the optimal value by observing the dynamic aspect of the saturation voltage on an oscilloscope. This is why R_{COPY} = 390Ω is selected with BU508A.

III.3.6 - Calculating the value of resistor connected to v+

In order to prevent high current flow through the integrated circuit and also to limit the power dissipation, the output stage is operated in saturated mode in high positive output currents.

The maximum recommended positive base current is 1.2A.

Selected maximum power supply voltage is +12V.

Lets calculate the resistor value required to yield a maximum current of +1A.

The voltage drop across three diodes connected in series is typically 0.9V x 3 = 2.7V at 1A.

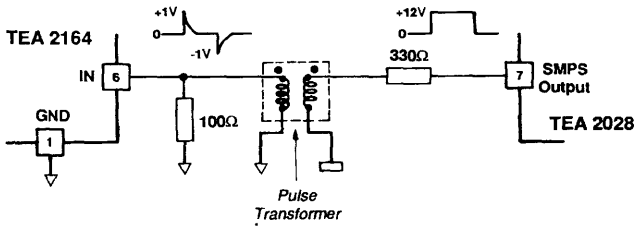
The base-emitter saturation voltage of BU508A is around 1V. The TEA2164 output stage voltage drop is approximately 1.4V.

Therefore :

$$R_{V+} = \frac{12V - 1V - (3 \times 0.9V) - 1.4V}{1A} = 6.9\Omega$$

Preferred value $R_{V+} = 6.8\Omega$ is selected.

Figure 14



91AN2164-14

Comment :

- It is obvious that the maximum I_{B+} value is directly dependent on the power supply voltage. Therefore, V_{CC} variations as a function of mains voltage, through the forward self-supply winding, must be taken into consideration.
- All calculated values must be optimized on the prototype board by taking into account all operating conditions of the switching transitor to be used.

III.4 - Input pulses & oscillator

III.4.1 - Input pulses (pin 6)

The regulation PWM and sync pulses issued by the controller circuit on secondary side are sent to the primary side through a pulse transformer that ensures galvanic isolation between primary and secondary sections. The PWM pulse is differentiated by the pulse transformer.

The input signal (pin 6 of TEA2164) frequency must fall within the sync window :

$0.65\ f_{OSC} < f_{SYNC} < f_{OSC}$

The positive drive pulse will turn the transistor on while the negative pulse will turn it off. Prior to transistor turn-off, the positive base current is interrupted and then after a constant time interval, the negative base current is applied to turn the transistor off.

For appropriate system operation, the amplitude of pulses applied to input pin 6 must fall within ± 0.5V to ± 1V range.

The pulse transformer can be built by 2 few turn windings wound on a tore or ferrite rod.

III.4.2 - Oscillator (R_{OSC} , C_{OSC} - pin 7 and pin 8)

The free-running frequency is given by :

$$f_{OSC} = \frac{1}{0.4 \times R_{OSC} \times C_{OSC} + 470 \times C_{OSC}}$$

Choice of f_{OSC} must take into account the following constraints :

- f_{OSC} must fall within the sync range :
  $0.65 \times f_{OSC} < f_{SYNC} < f_{OSC}$
- the free-running frequency f_{OSC} must not fall inside audible frequency range in stand-by mode :
  $f_{OSC} \geq 20kHz$

The sync frequency value used in TV applications is 15.7kHz.

The free-running frequency "f_{OSC}" value is selected to be 19kHz so as to fall at the center of sync frequency range. This frequency is close to 20kHz and is therefore not audible.

The value of "C_{OSC}" capacitor determines the oscillator saw-tooth discharge time. This time has a direct influence on "$t_{ON(MIN)}$" used by TEA2164 and therefore should not be too long so as to allow a

low "$t_{on(min)}$".
We shall select C_{OSC} = 1.2nF
The corresponding value of R_{OSC} is calculated as follows :

$$R_{OSC} = \frac{1}{0.4 \times 19 \times 10^3 \times 1.2 \times 10^{-9}} - \frac{470}{0.4} = 108k\Omega$$

Selected value is : R_{OSC} = 110kΩ
The tolerance of these components is calculated as a function of maximum admissible free-running frequency dispersion while also taking into account the minimum and maximum limits of the horizontal scanning frequency.

III.5 - Stand-by

The system will enter into stand-by mode by simply disconnecting the power supply to the secondary-connected PWM regulation device (TEA5170 or TEA2028). In the absence of control pulses normally delivered by the secondary block, the TEA2164 will switch to "burst" mode in which case, the power transfer falls to a low value.

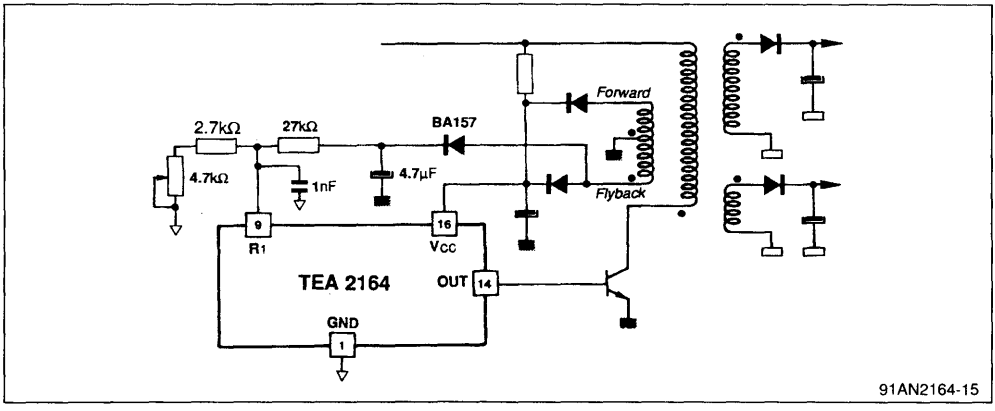
III.5.1 - Very low frequency oscillator

The period of this VLF Oscillator is determined by capacitor "C_1" connected to pin 10.
For C_1 = 100nF, the VLF oscillator period is approximately 30ms. The typical burst duration is therefore 3.9ms - which is 13% of the VLF oscillator period.
The ripple ratio of secondary output voltages in stand-by mode depends on VLF oscillator period and hence on the value of capacitor C1.

III.5.2 - Regulation in stand-by mode

A feed-back loop connected to pin 9 is used to modify the maximum conduction period in burst mode and to allow the regulation of secondary output voltages in stand-by.
The feed-back information is delivered by the self-supply flyback winding of TEA2164. This signal, once rectified and filtered, is an image of secondary voltages. This voltage is applied to an adjustable

Figure 15



divider bridge and then to pin 9 which is used for output voltage adjustment in stand-by operation. It is recommended to choose the voltage values in stand-by slightly lower than nominal values used under normal operating conditions. A 1nF capacitor has been added to pin 9 which will improve the filtering of the regulation voltage.

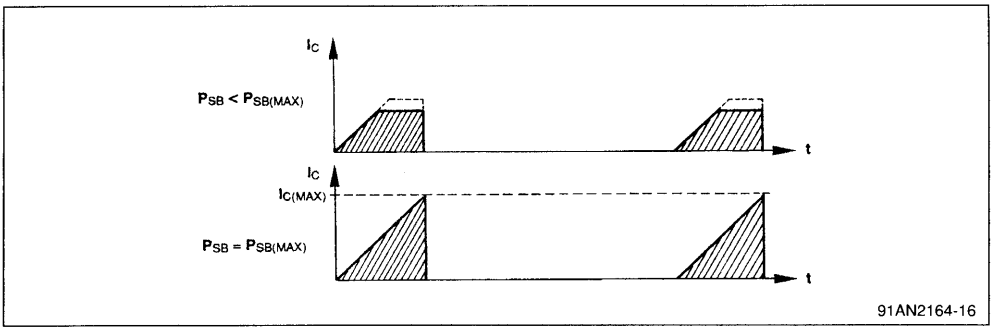
III.5.3 - Maximum power in stand-by operation

The collector current envelope shape varies as a function of the secondary power consumption in stand-by.

It follows that the power which may be tranferred to the secondary winding in stand-by is therefore limited.

The maximum power in stand-by can be estimated as follows :

Figure 16



$$P_{SB(MAX)} \approx \frac{P_{MAX}}{3} \times 0.13 \times \frac{f_{SB}}{f_{SYNC}}$$

$$\Rightarrow P_{(SBMAX)} \approx \frac{150}{3} \times 0.13 \times \frac{19 \times 10^3}{15.7 \times 10^3} = 8W$$

Comment :

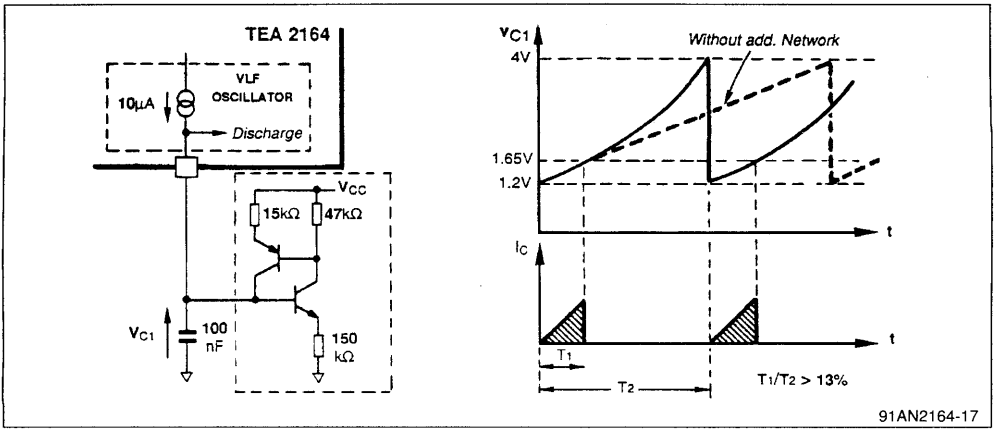
- at $P_{SB} = P_{SB(MAX)}$, C_3 capacitor (pin3) is slowly charged and the voltage on pin 3 will reach the protection threshold value (3V typ.) and the SMPS is shut down.

III.5.4 - Booster circuit for higher stand-by output power

When higher stand-by output power is required, it is possible to add a network on pin 10, which modifies the shape of the VLF oscillator saw-tooth and increase the T1/T2 ratio.

The burst duration "T1" is not modified, only the VLF oscillator period "T2" is shorter, which will increase the available stand-by output power.

Figure 17

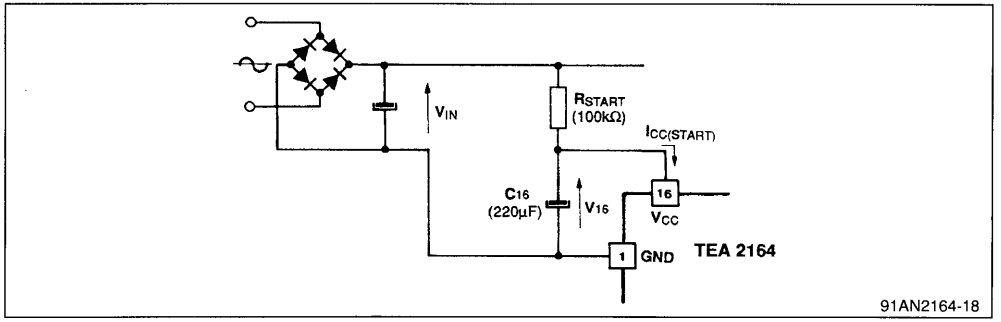


III.6 - Start-up

III.6.1 - Start-up resistor

Upon initial system start-up, the mains filtering capacitor is charged through the rectifier diode bridge.

Figure 18



- The capacitor charge up time is given by :

$$t_{CHARGE} = \frac{V_{CC(START)} \times C_{16}}{\frac{V_{IN}}{R_{START}} - I_{CC(START}}$$

$$t_{CHARGE} = \frac{9 \times 220 \times 10^{-6}}{\frac{310}{100 \times 10^{-3}} - (0.8 \times 10^{-3})} = 0.85s$$

At minimum mains voltage level : t_{CHARGE} = 1.2s

- The power dissipated within "R_{START}" resistor is :

$$P = \frac{(V_{IN} - V_{CC})^2}{R_{START}}$$

$$P = \frac{(310 - 12)^2}{100 \times 10^3} = 0.9W \text{ (P = 1.4W at Mains max level)}$$

An application variant is when the start up resistor is directly connected to non-rectified mains.

In this case and in order to obtain an identical start-up time, the value of "R_{START}" resistor must be divided by π. The power dissipation is thus reduced by approximately 30%.

III.6.2 - Self-supply

As soon as the voltage on pin 16 reaches the $V_{CC(START)}$ level of 9V, the TEA2164 will start-up and deliver the base drive pulses to the switching transistor at internal oscillator frequency (set by R_{OSC} and C_{OSC}). The duty cycle of these pulses gradually increases (soft-start). During this cycle of operation, the device does not receive any control pulse from the secondary controller circuit and therefore operates in "Burst mode".

The start-up will correcty take place if the device is rapidly self-supplied, that is, before the voltage across the supply capacitor on pin 16 falls below $V_{CC(STOP)}$ threshold.

The TEA2164 is supplied by two distinct secondary windings, one connected in flyback and the other in forward configuration.

The forward voltage will rapidly provide the supply required by TEA2164 whereas the flyback voltage will begin rising slowly and depends on various secondary time constants.

Main advantage of the flyback voltage is that it provides a regulated supply voltage proportional to the secondary voltages.

A +12V voltage has been selected for device power supply at nominal mains voltage level. A lower value such as +10V can be selected which will also reduce the power dissipation. Note however that since the overvoltage protection threshold is internally set at +15V, then the lower is the supply voltage level the greater will become threshold margin.

At nominal mains voltage, the forward voltage value is selected to be 1V below the flyback voltage value so that, the supply voltage at maximum mains voltage, will not rise much above its nominal value (and will remain below 15V threshold level).

III.6.3 - Secondary controller circuit start-up

After a time interval required for the secondary

power supply capacitors to charge up, the secondary-connected regulation controller circuit will be powered and as soon as its supply voltage "V_{CC}" reaches the "$V_{CC(START)}$" level, it will begin delivering regulation and synchronization pulses. The TEA2164 will receive these pulses and will consequently switch from "Burst Mode" to "Normal Mode" synchronized and regulated by the secondary controller circuit.

The secondary controller circuits (TEA2028, TEA2029 and TEA5170) have a "soft-start" function. This system allows better transition when switching from stand-by mode to normal mode.

The TEA2028 and TEA2029 controllers have no "$t_{ON(MIN)}$" function, and for this reason, it is necessary to choose lower voltage in stand-by mode than in normal mode. Otherwise, switching from stand-by mode to normal mode will not be possible (secondary controller circuit will not issue regulation pulses as long as the output voltage remains above its nominal value).

The TEA5170 has a "$t_{ON(MIN)}$" function, but it is also recommended to choose the stand-by voltage under the nominal value so as to avoid overvoltage when switching from stand-by mode to normal mode.

For further details on secondary controller circuits, please refer to TEA5170 and TEA2028-TEA2029 Application Notes (AN407/0591).

III.7 - Protection features

III.7.1 - Overload protection

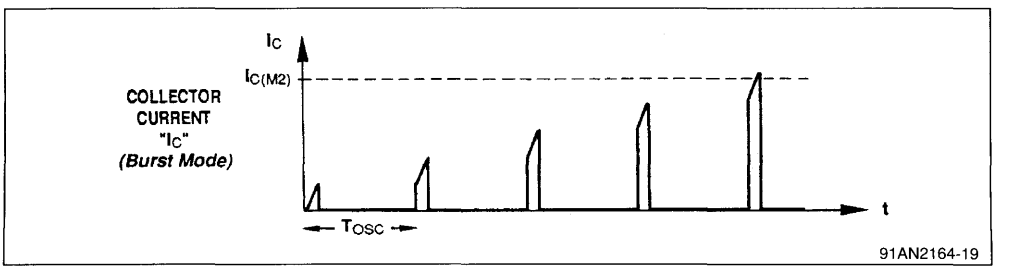
The current limitation is set by resistor "R_S" as a function "$I_{C(M1)}$" threshold, such that the power transfer is limited at 150W. If the load connected to secondary requires higher power, the current limitation is activated and will limit the power transfer by lowering the output voltage.

III.7.2 - Short-circuit protection

In case of short-circuit, the secondary voltage falls to zero and the time required for the transformer to demagnetize becomes very long. The collector current will no longer start at zero level but at the final value of the preceding period. The current value will rapidly reach "$I_{C(M1)}$" and then "$I_{C(M2)}$" threshold levels.

Only the "$I_{C(M2)}$" threshold will disable the device and switch it into "Burst Mode". The device will re-start at the beginning of the following VLF oscillator period. However, if the short-circuit still persists, the "$I_{C(M2)}$" protection threshold is once again activated.

Figure 19



III.7.3 - Repetitive overcurrent protection

Each time that "$I_{C(M1)}$" or "$I_{C(M2)}$" thresholds are reached, an event counter will charge up the capacitor "C2" connected to pin 3. If the overload persists, the voltage across capacitor will reach the 3V threshold level and TEA2164 is consequently disabled (no power transfer to secondary will take place).

To exit this protection mode, the mains voltage must be disconnected during a time interval long enough for all capacitors to fully discharge. The system can re-start only once the capacitors have been discharged.

III.7.4 - Overvoltage protection

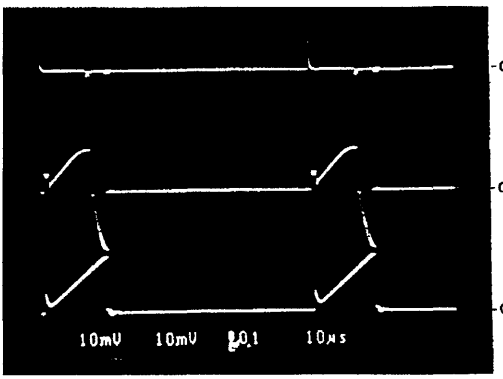
If an overvoltage (produced by improper adjustment or failure) appears at secondary terminals, the primary flyback voltage will rise and if the +15V threshold level is reached, the TEA2164 is disabled.

An overvoltage would be also generated if the load on secondary terminals is disconnected. In this case, if the secondary controller device is not equiped with $t_{ON(MIN)}$ feature (TEA2028 , TEA2029), it will stop sending the regulation pulses and the TEA2164 will consequently enter into "Burst Mode".

If the secondary controller device has a "$t_{ON(MIN)}$" function (TEA5170), the protection is performed at the primary side by the +15V overvoltage threshold level.

III.8 - Oscillograms

Figure 20



1 - NORMAL MODE : *Base Current*

$V_{PIN\ 6}$: 1V/div

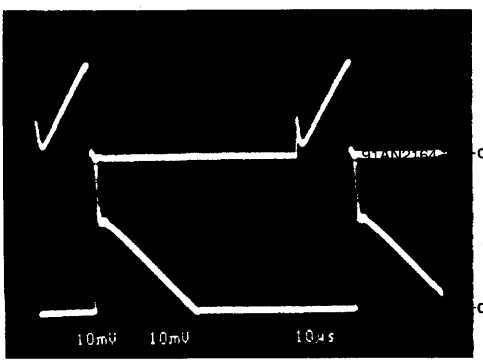
I_B : 1A/div

I_C : 2A/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

Figure 21



2 - NORMAL MODE : *Primary and Secondary Currents*

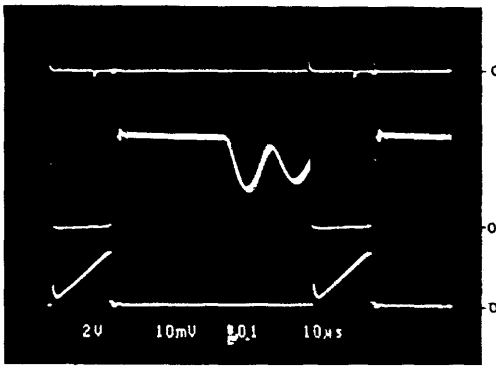
I_C : 1A/div

I_S : 1A/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

Figure 22



3 - NORMAL MODE : *Collector-emitter Voltage*

$V_{PIN\ 6}$: 1V/div

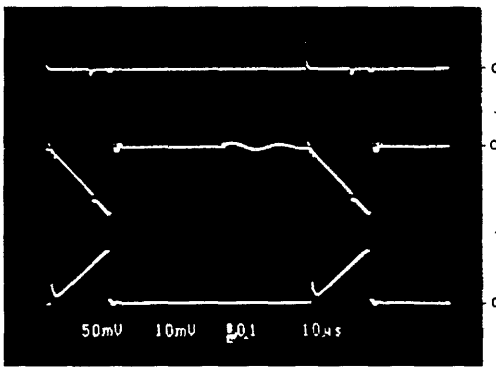
V_{CE} : 200V/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

I_C : 2A/div

Figure 23



4 - NORMAL MODE : *Current Limitation Voltage*

$V_{PIN\ 6}$: 1V/div

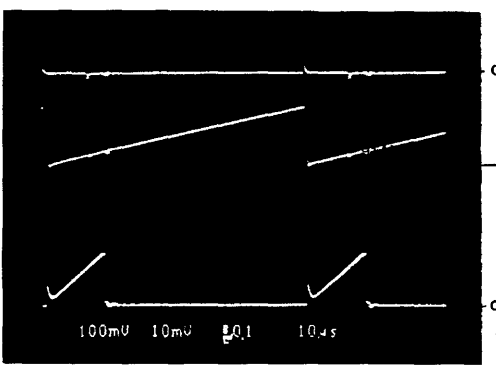
$V_{PIN\ 11}$: 0.5V/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

I_C : 2A/div

Figure 24



5 - NORMAL MODE : *Oscillator Saw-tooth*

$V_{PIN\ 6}$: 1V/div

$V_{PIN\ 8}$: 1V/div

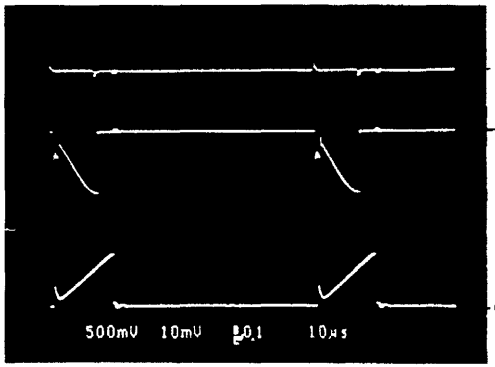
1.6V

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

I_C : 2A/div

Figure 25



6 - NORMAL MODE : *V+ Supply Voltage*

$V_{PIN\ 6}$: 1V/div

12V

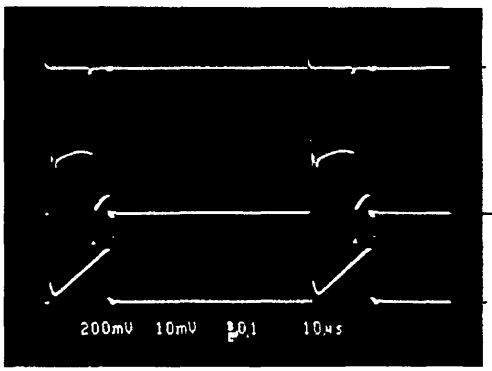
$V_{PIN\ 15}$: 5V/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

I_C : 2A/div

Figure 26



7 - NORMAL MODE : *Output Voltage*

$V_{PIN\ 6}$: 1V/div

$V_{PIN\ 14}$: 2V/div

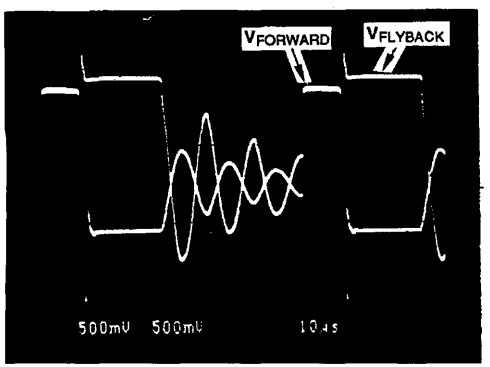
0.5V

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

I_C : 2A/div

Figure 27



8 - NORMAL MODE : *Flyback and Forward Voltages*
(TEA 2164 Power Supply)

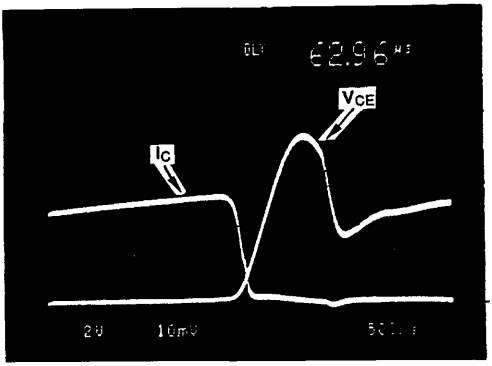
$V_{FORWARD}$: 5V/div

$V_{FLYBACK}$: 5V/div

Mains : 220V_{AC}
Load : 90W

Scale : 10µs/div

Figure 28



9 - NORMAL MODE : *Transistor turn-off*

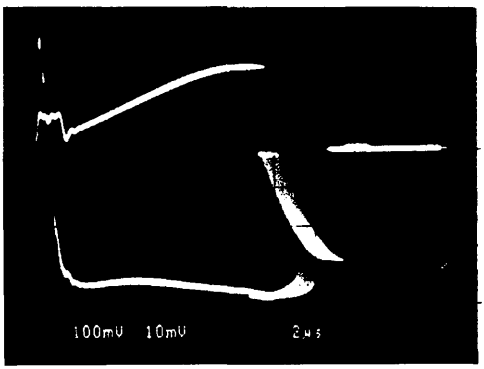
V_{CE} : **200**V/div

I_C : **1**A/div

Mains : **220**V_{AC}
Load : **90**W

Scale : **500**ns/div

Figure 29



10 - NORMAL MODE : *Saturation Voltage*

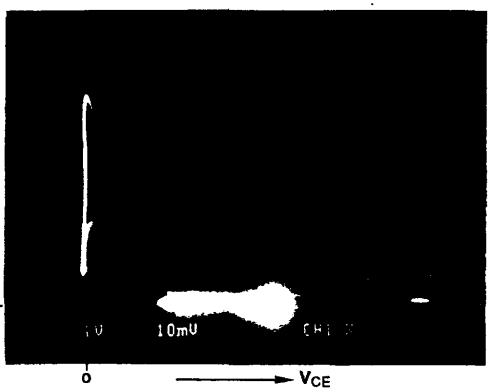
I_B : **0.5**A/div

Mains : **220**V_{AC}
Load : **90**W

Scale : **2**µs/div

$V_{CE(SAT)}$: **1**V/div

Figure 30



11 - NORMAL MODE : *Safe Operating Area*

Mains : **220**V_{AC}
Load : **90**W

I_C : **0.5**A/div

V_{CE} : **100**V/div

Figure 31

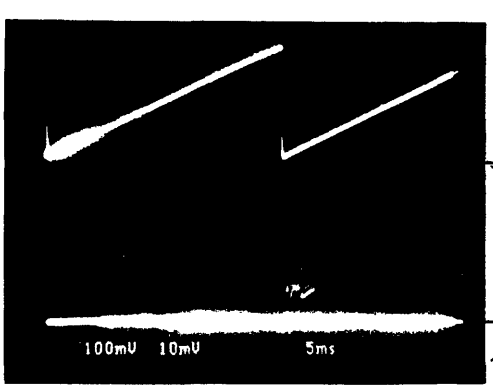


Figure 32

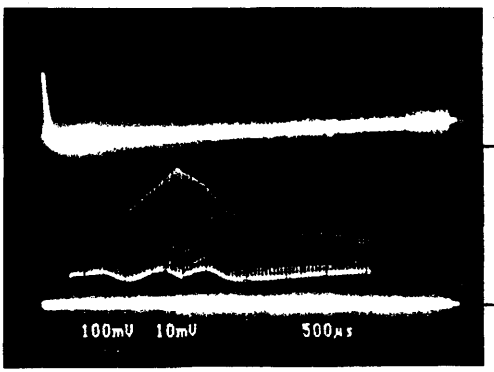


Figure 33

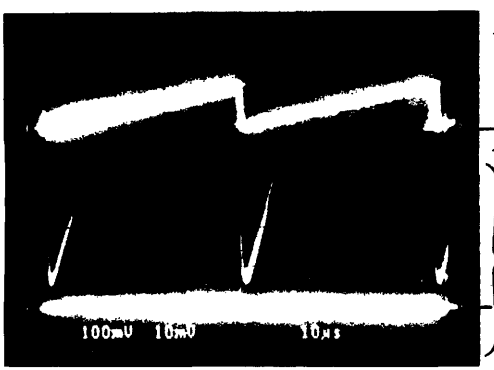


Figure 34

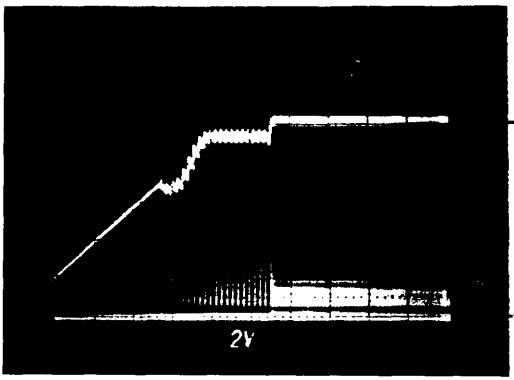


Figure 35

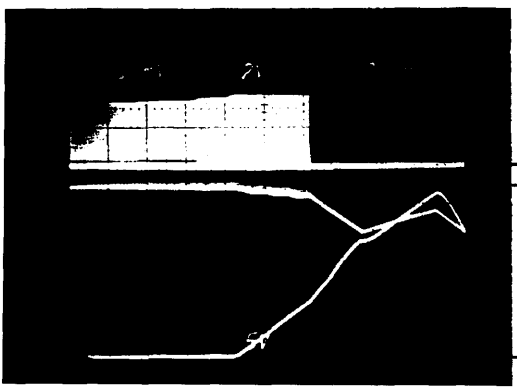
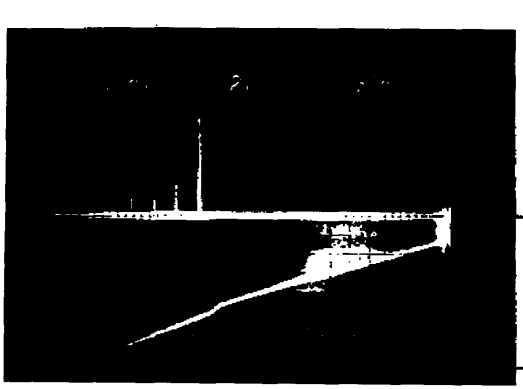


Figure 36



IV - APPLICATION VARIANTS

V.1 All mains application

IA wide input voltage range application can be configured around TEA 2164. We have built a power supply delivering 90W output power at mains input voltage range of $90V_{AC}$ to $260V_{AC}$.
Difficulties encountered in such application are given below :

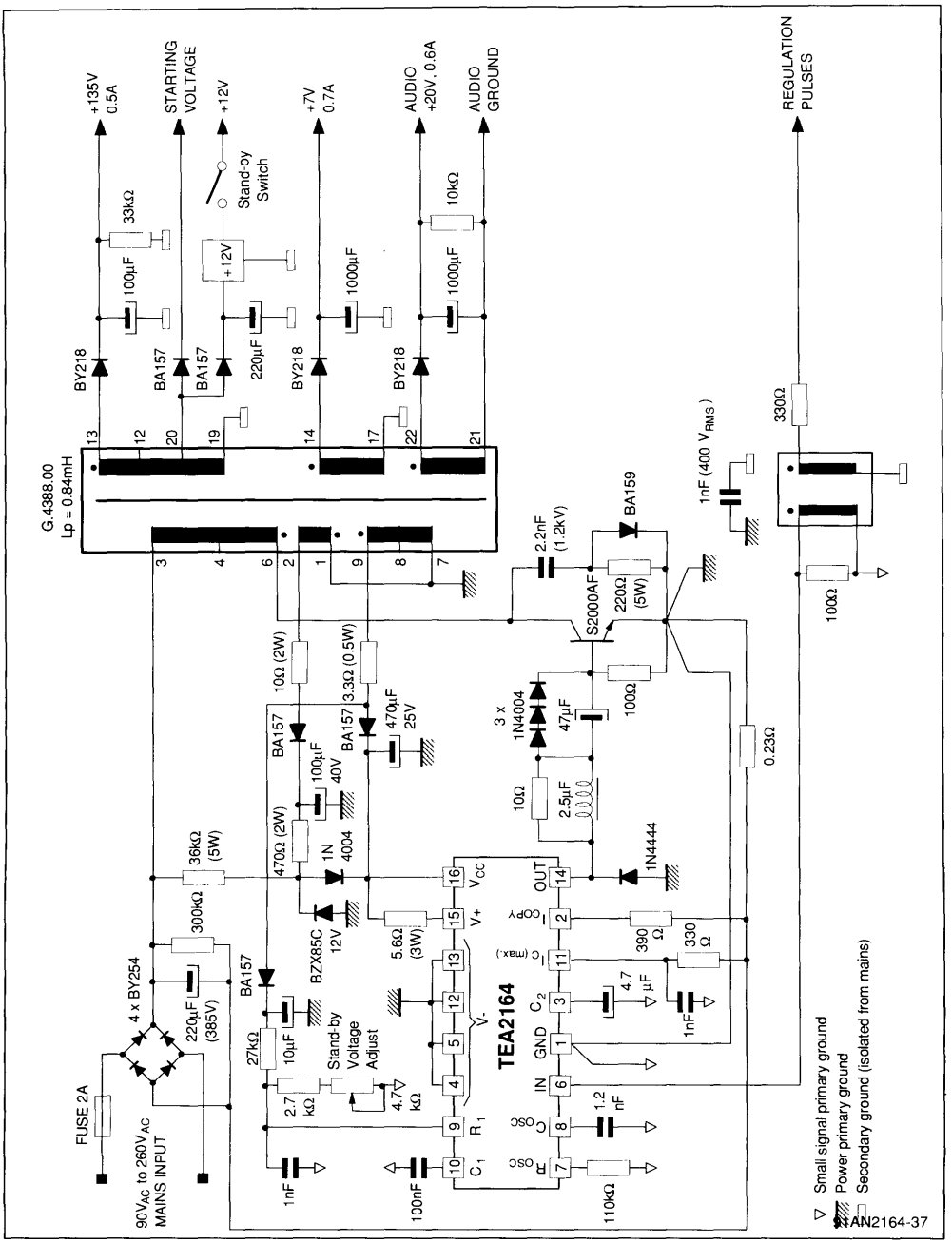
- Very wide regulation range : if a discontinuous mode flyback transformer is employed, the conduction time would be highly variable.
  The "$t_{ON(MAX)}$" duration is determined as a function of maximum power output and the minimum mains voltage level.
  The "$t_{ON(MIN)}$" duration is determined as a function of minimum power output and the maximum mains voltage level.
- Start-up at minimum mains level : appropriate selection of start-up resistor and self-supply windings.
- Optimized switching transistor base drive and appropriately dimentioned protection features to operate over the whole mains voltage range :

both, the base current, and supply voltage values and hence the self-supply windings, must be appropriately calculated.

FEATURES

- Discontinuous mode flyback SMPS (L_P = 0.84mH)
- Standby function using the burst mode of TEA2164
- Switching frequency :
  - Normal mode : 15625 Hz (synchronized on horizontal deflection frequency)
  - Stand-by mode : 19 kHz
- Mains voltage range : 90 V_{AC} to 260 V_{AC}
- Mains power consumption :
  - Normal mode : 110 W max
  - Stand-by mode :
    6.7W (at 110V)
    9.8W (at 220V)
    (without degaussing coil)
- Efficiency :
  - Normal mode :
    83% (at 110V)
    80% (at 220V)
    (measured with 86W output power)

Figure 37 : 90 Volts to 260 Volts Application Diagram



IV.2 - 117 Volts application

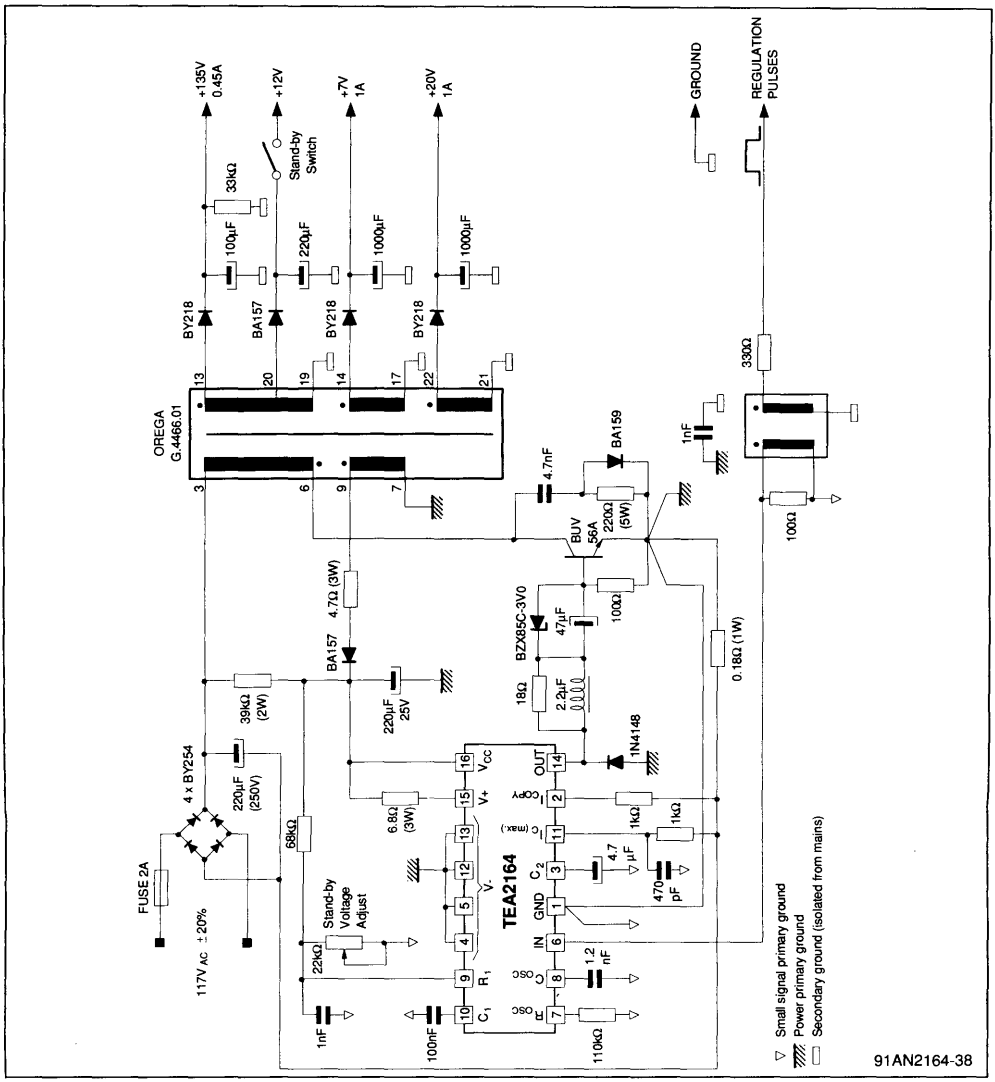
Main Features :

- Discontinuous mode flyback SMPS (L_P = 0.62mH)
- Switching Frequency : 15.7kHz
- Mains Voltage Range : 90V_{AC} to 140V_{AC}
- Output Power : 90W
- Stand-by using the burst mode of TEA2164

Comment :

An optimization of the start up has permitted to eliminate the need of the self-supply forward winding and therefore to *suppress* some components.

Figure 38 : 117 Volts Application Diagram

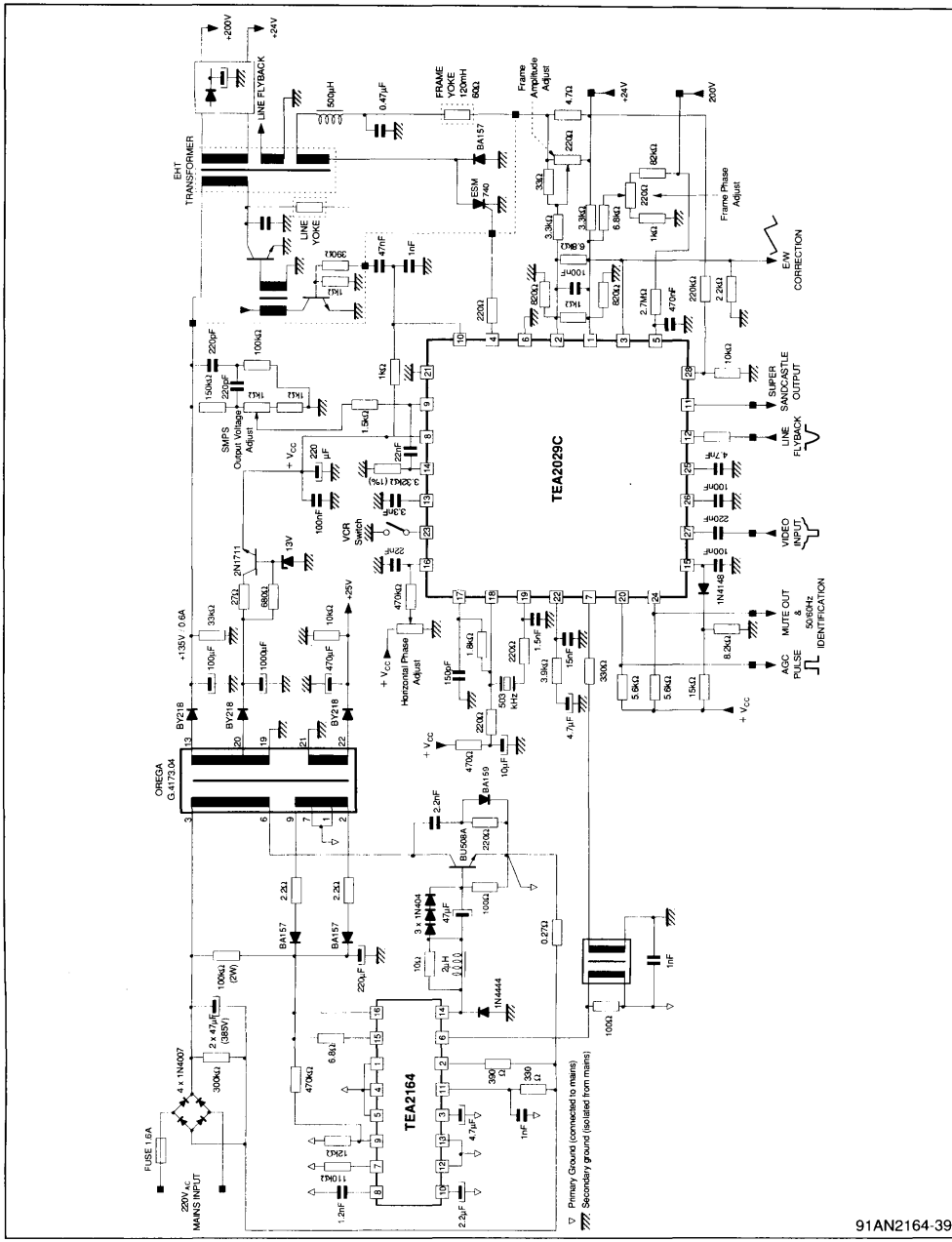


IV.3 - Application without stand-by

The application arrangement is simplified if the stand by function is not required :

- The "Master" circuit on the secondary side is permanently powered and as a consequence the transistors used to cut its power supply are no longer needed and can be eliminated.
- The feedback used for "stand-by" regulation function on the primary side configured around pin 9 of TEA 2164, can be simplified.
- The value of "C1" capacitor connected to pin 10 of TEA 2164 used to set the burst period and therefore its duration, is increased (1µF or 2.2µF) so as to enable full load system start-up as soon as the first burst is available.

Figure 39 : Complete Application Diagram (SMPS + Deflection)
(Without Stand-by Function)



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2037
HORIZONTAL & VERTICAL DEFLECTION CIRCUIT

By : B. D'HALLUIN

SUMMARY

I - INTRODUCTION

The TEA2037 is a horizontal and vertical deflection circuit for monitors and black and white TV sets.

This device includes all functions required for deflection, namely :

- Line and frame sync separation
- Line oscillator with phase comparator
- Driver stage for line deflection darlington transistor
- Frame oscillator
- Frame amplifier with flyback generator for direct drive of the vertical deflection yoke.

The TEA2037 is particularly well-suited for low-cost monitors since it is cased in a low-cost package and requires a few number of external components and hence optimized for small displays.

However, application areas are by no means limited. Sophisticated applications requiring various adjustment possibilities such as for display geometry and centering settings (amplitude, linearity,...) and operating at different line and frame frequencies (line frequencies up to 64kHz), are readily configured around TEA2037.

In large screen applications, addition of a heatsink mounted on TEA2037 will enable the vertical deflection yoke current to be boosted to 2A peak-to-peak.

II - FUNCTIONAL DESCRIPTION OF TEA 2037

II.1 - General description

The TEA2037 is a 16-pin DIP package. The 4 center pins (2 on each side) are connected together and used as heatsink.

From composite video or TTL-compatible sync. signals, the device will extract and generate all signals required for the line scanning darlington transistor and direct drive of the frame yoke.

The following functional blocks are implemented on-chip :

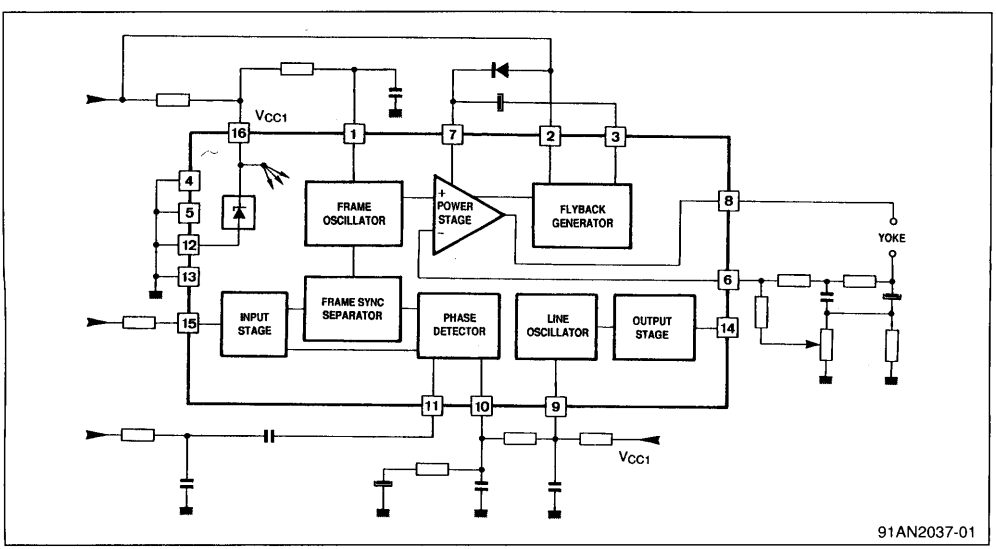
- Line and frame sync. separator
- Line oscillator
- Line phase comparator
- Line output stage
- Frame oscillator
- Frame amplifier
- Frame flyback generator
- Shunt regulator

The common device power supply is implemented by the on-chip shunt regulator.

In order to optimize the drive to frame deflection yoke and also enable appropriate use of the flyback generator, the frame amplifier is powered by an independent supply.

The ground is connected to the 4 center pins of the device.

Figure 1 : Block Diagram

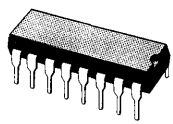


Pin description

1	Frame *Oscillator*
2	V_{CC2} (Flyback generator power supply)
3	Flyback generator output
4, 5	Ground
6	Frame feed-back (frame amplifier inverting input)
7	V_{CC2} (positive power supply for frame output stage)
8	Frame output (direct drive to frame yoke)
9	Line oscillator
10	Phase comparator output
11	Phase comparator input (line flyback)
14	Line output (drive to line darlington transistor)
15	Video input (or TTL-compatible sync.)
16	V_{CC1} (shunt regulator)

Package

Batwing DIP16
(plastic package)



II.2 - Sync. pulse separator

The TEA2037 extracts, first the line and frame sync. pulses from the composite video signal and then the largest pulses, i.e., the frame syncs.

II.2.1 - Extraction of sync. pulses from the composite video signal (TV application).

Figure 2

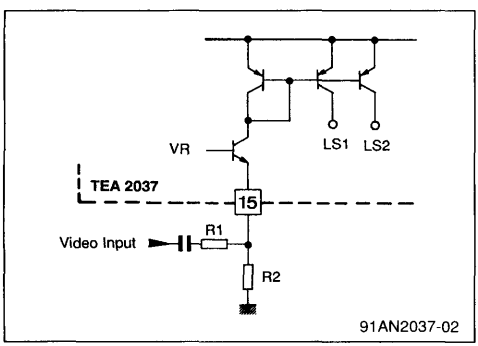
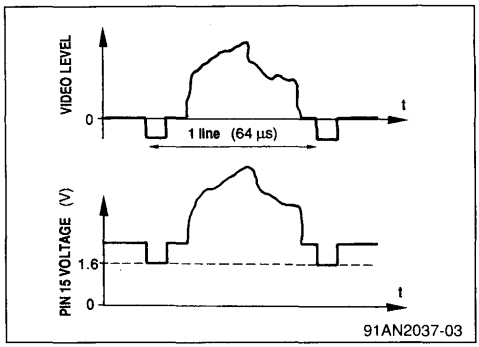
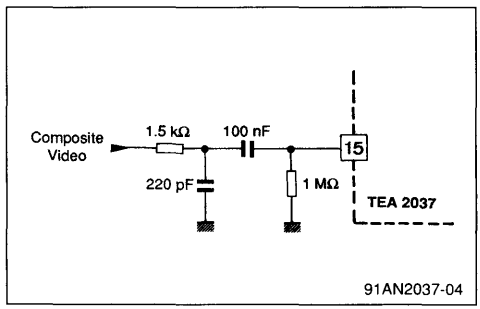


Figure 3



- The sync. detection level is set at 1.6 V.
- The value of R2 is typically 1 MΩ (fixed for a good internal bias).
- Resistor R1 limits the output current of pin 15.

Figure 4



As illustrated in the above Figure, it is recommended to employ a low-pass filter which will suppress high-frequency harmonics susceptible to produce jitters on line sync signal in composite video TV applications.

II.2.2 - Negative TTL SYNC. (Monitor application)

Figure 5

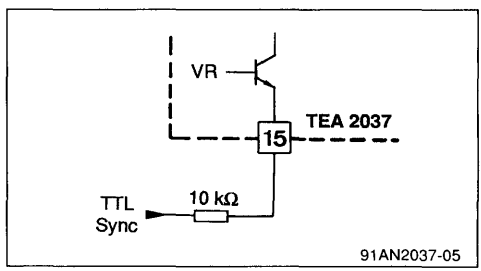
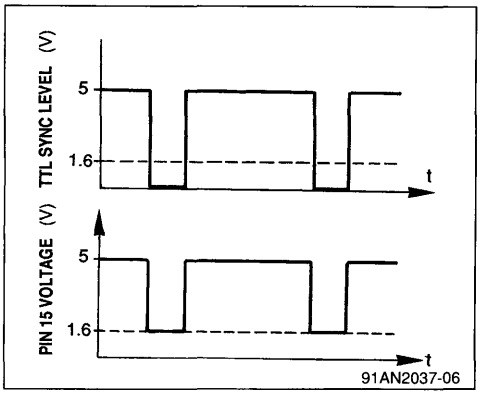


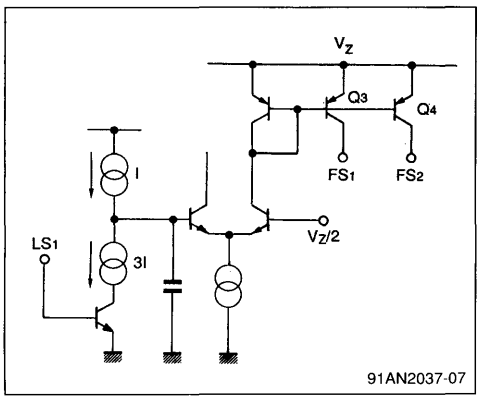
Figure 6



In monitor application, the sync. signal is generally separated from the video signal.
In this case, the sync. signal is applied to pin 15 through a single limiting resistor. Similar to the former case, the sync. is detected when the input voltage falls below 1.6 V level.

II.2.3 - Frame sync. extraction

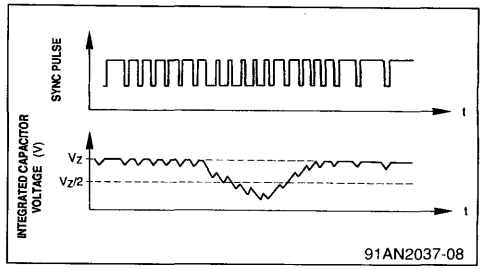
Figure 7



This function is processed internally and hence does not require any external component. Line and frame sync. pulses are distinguished by an integrated capacitor which is more or less discharged during each sync. pulse interval as follows :

- if the sync pulse duration is short, i.e. it is line sync, then the capacitor is slightly discharged
- on the other hand, if the pulse width is larger, the capacitor is fully discharged and an internal frame signal is thus generated.

Figure 8



II.3 - Line oscillator

Figure 9

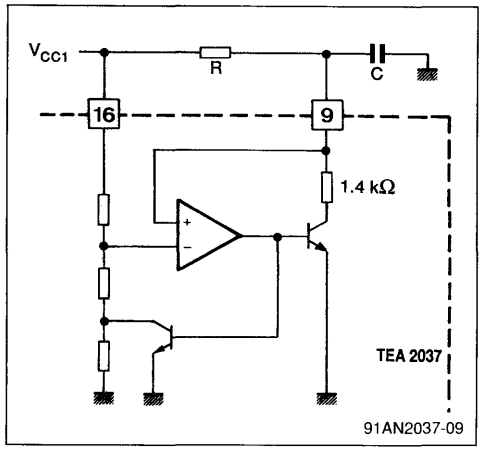
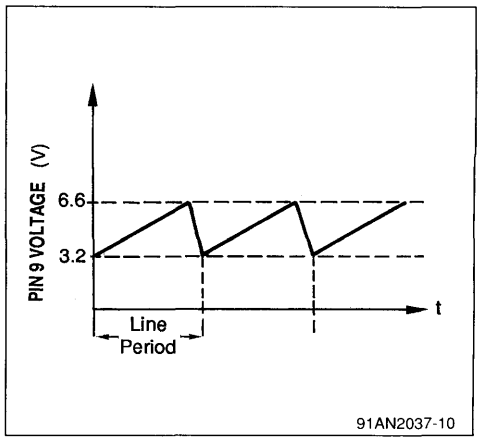


Figure 10



The line saw-tooth is generated by charging an external capacitor on pin 9 via a resistor connected to V_{CC1} (pin 16).

The capacitor is discharged via an internal 1.4 kΩ resistor. The saw-tooth amplitude is set by two on-chip threshold levels :

- lower threshold : 3.2 V
- higher threshold : 6.6 V

The free-running period is approximately given by the following relationship :

$$T_{OSC} \approx 0.85\ RC$$

The phase comparator will modify the capacitor charge by injecting a positive or negative current so as to produce correct phase and frequency relationships with respect to the synchronization signal.

II.4 - Line output stage

The line output stage has been designed for direct base drive of the horizontal scanning darlington transistor.

The low level interval on pin 14, i.e. the power line transistor blocking period, is determined by the time when the voltage of the line oscillator capacitor (pin 9) is below 4.8 V (internally set threshold level). In a typical application, this interval corresponds to 22µs at 64µs free-running period.

Figure 11

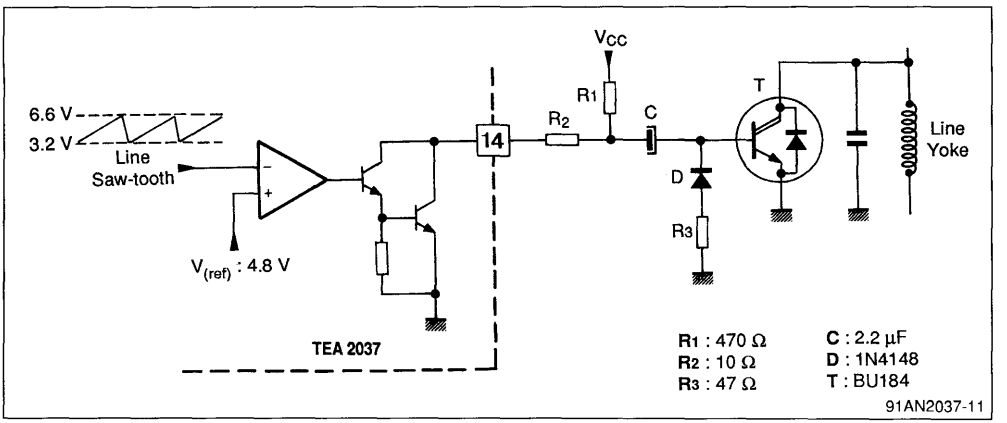
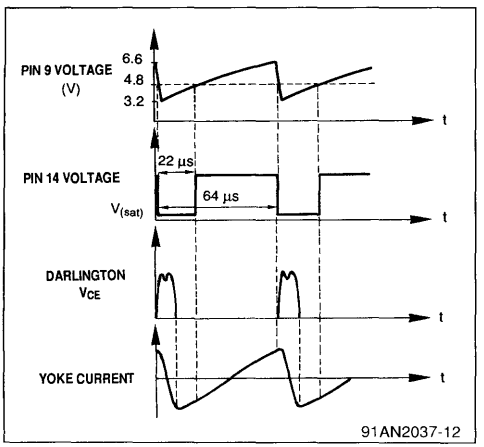


Figure 12

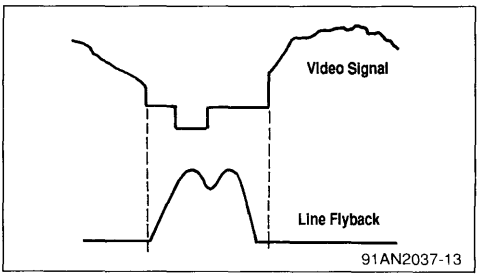


II.5 - Phase comparator (PLL)

II.5.1 - Functional description

The duty of phase comparator is to synchronize the horizontal scanning with the line sync pulse and ensure correct line flyback during the horizontal blanking phase.

Figure 13



The line flyback signal (i.e. the pulse on the collector of the line scanning transistor) is compared with the line sync. signal issued by sync. separator. If the detected coincidence is incorrect, the comparator will then generate an appropriate positive or negative current so as to charge or discharge the line oscillator capacitor thereby providing for frequency and phase locking.

II.5.2 - Phase comparator operation

Figure 14

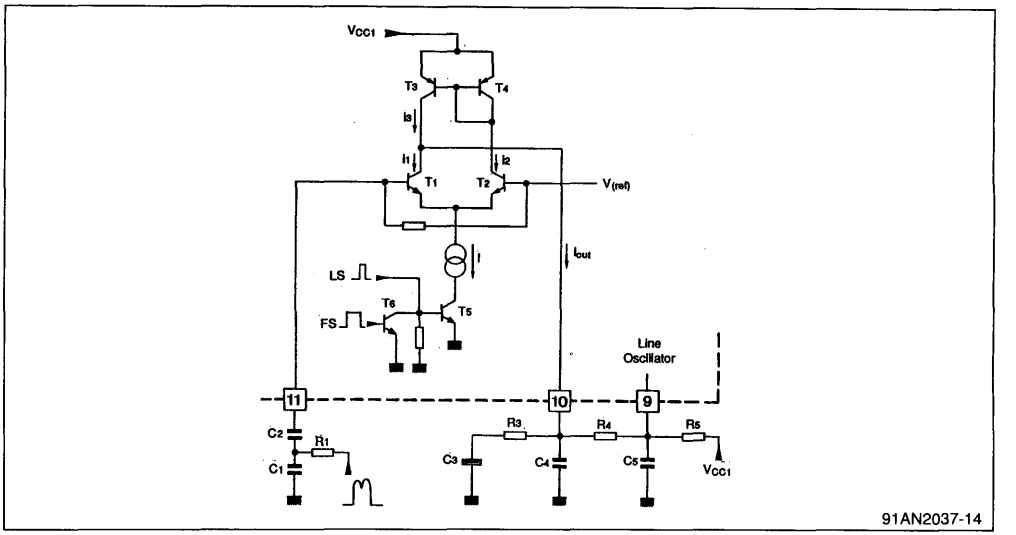
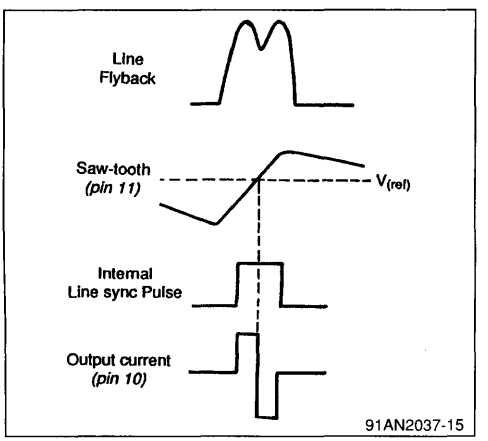


Figure 15



The line flyback signal goes through integrator network R1C1 the output of which, a saw-tooth signal, is applied to comparator input (pin 11) via capacitor C2.

The comparator input stage is formed by the differential pair T1 and T2. T3 and T4 transistors are arranged in current mirror configuration and thus : $i_3 = i_2$

The sum of currents going through T1 and T2 transistors is determined by the current generator "I" so that : $I = i_1 + i_2$.

The comparator output current is the difference current through the differential pair, i.e. :

$$i_{OUT} = i_2 - i_1$$

The comparator is enabled by T5 transistor only during the line sync. interval.

Transistor T6 inhibits the phase comparison during the frame sync. interval.

During the first portion of the flyback, the voltage at comparator input (pin 11) is lower than the reference voltage. T1 is off and T2 conducts ; consequently the comparator output goes positive :

$$i_{OUT} = +I$$

During the second portion, the input voltage ex-

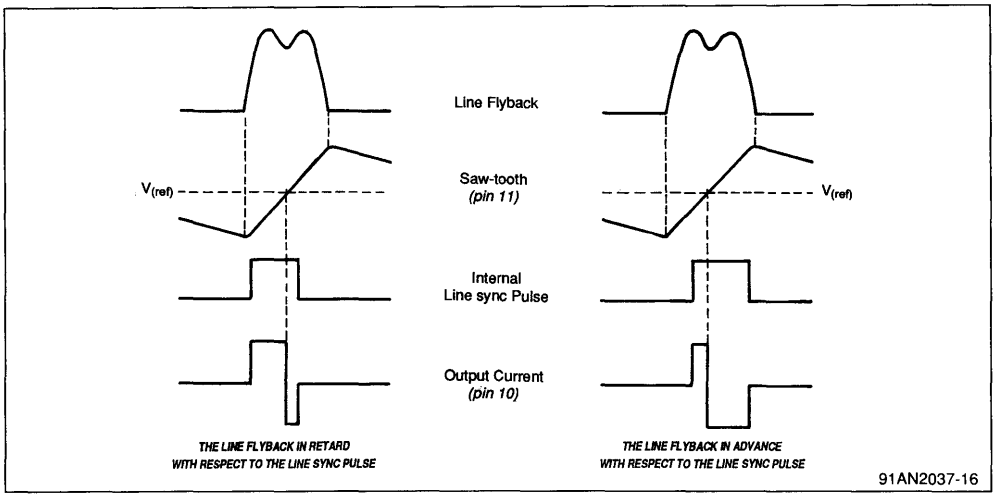
ceeds the reference voltage and as a result, the comparator ouput falls to negative level :

$$i_{OUT} = -I$$

If the line flyback is in retard with respect to the horizontal sync. pulse (which is the case of too long line periods), the interval for which the phase comparator's output current is positive would increase. This current is then filtered and applied to the line oscillator capacitor (C5) thereby accelerating its charge-up phase and hence reducing the line period.

Inverse action takes place if the line flyback is in advance - the negative current at comparator's output will rise, C5 is charged more slowly and the line period is thus increased.

Figure 16



II.5.3 - Output filter

Figure 17

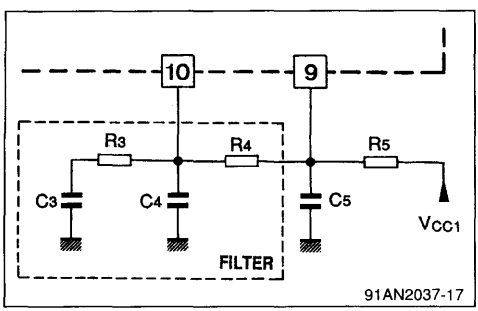
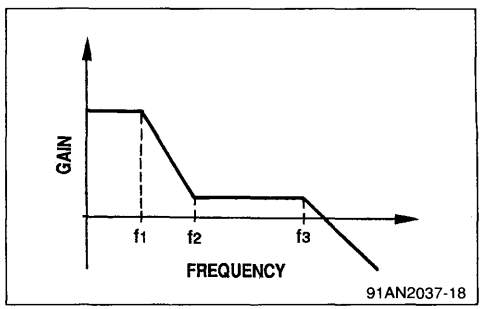


Figure 18



$$f_1 = \frac{1}{2\pi\,(R3 + R4)\,C3} \qquad f_2 = \frac{1}{2\pi R3C3} \qquad f_3 = \frac{R3 + R4}{2\pi R3R4C4}$$

The duty of the output filter is to ensure the stability of the locked loop and its characteristics will have a partial influence on capture range and also on capture time.
The holding range, which is larger than the capture range, depends on the ratio of the current available at the comparator output and the charging current of the line oscillator. The holding range does not depend directly on the cut-off frequencies of the output filter. But, as the voltage range at the comparator output is limited, a too high value for R4 will limit the holding range.
The sync. pulse duration has significant influence on capture range and also on the holding range of the device. The output current duration is directly related to synchronization pulse width.

- First the R5 x C5 product is selected to yield the required free-running line oscillator frequency.
- Then, the value of C5 capacitor is selected as follows :
  - for monitor applications (large holding range) low value; e.g. :2.2 nF @ 16 kHz, 1 nF @ 32 kHz
  - for TV applications higher value; e.g. : 4.7 nF @ 16 kHz
- Finally, the filter components are selected to match the required capture range. (R4 ≤ 100 kΩ to prevent comparator output saturation)

II.6 - Frame oscillator

Similar to line oscillator, the frame saw-tooth is generated by charging an external capacitor on pin 1 through a resistor connected to V_{CC1}.

Figure 19

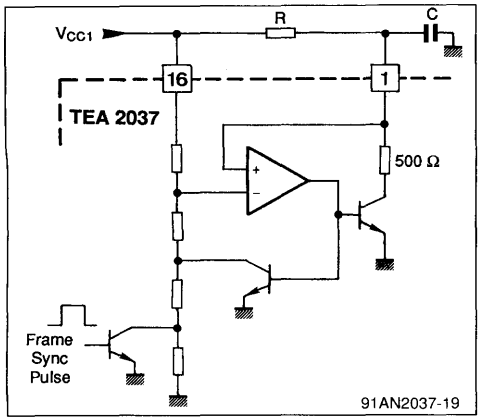
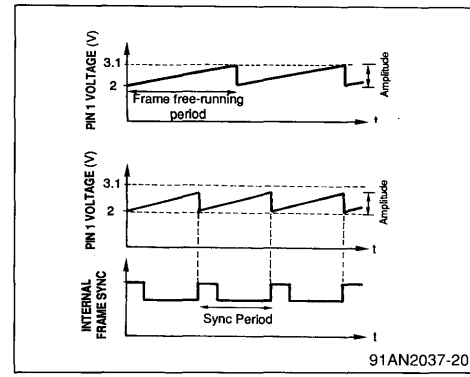


Figure 20



The capacitor is discharged via an internal 500 Ω resistor. The saw-tooth amplitude is set at two on-chip threshold levels.
The free-running period is approximately given by :

$$T_{OSC} \approx 0.15\ RC$$

Synchronization is achieved by period reduction.
The frame sync. pulse issued by the sync. separator will modify the current through the resistor bridge which is used to set the saw-tooth threshold levels.
The minimum synchronized frame period (MSFP) is given by :

$$MSFP \approx \frac{T_{OSC}}{1.8}$$

II.7 - Frame output amplifier

The frame saw-tooth generated by frame oscillator is first inverted (Gain : - 0.4) and then applied to the non-inverting input of the frame amplifier. The output current capability of this amplifier is as high as ± 1A thus enabling to drive vertical deflection yokes requiring 2A peak-to-peak.
As a function of dissipated power, the device may require the addition of a heatsink.
A feed-back loop is connected to the inverting input of the frame amplifier (pin 6).
As the CRT screen is not part of a sphere centered on the deflection center point, if the yoke is actually driven by a saw-tooth waveform, the image is expanded at the top and bottom. The yoke must therefore be provided with an "S" waveform current, by applying linearity correction.
The circuit configuration depicted above does not require any linearity adjustment - only an amplitude

Figure 21

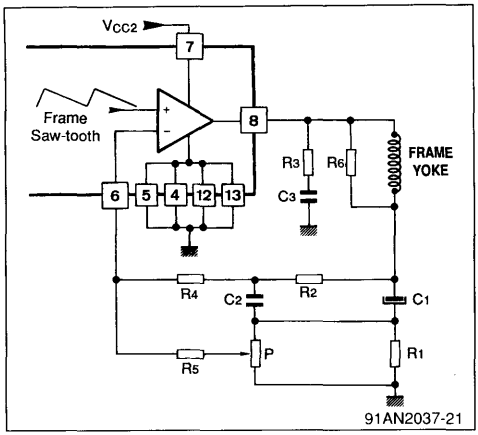
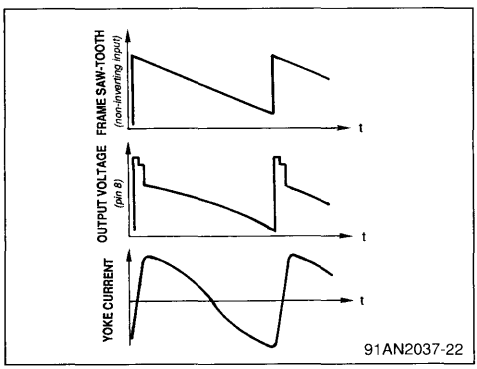


Figure 22



adjustment potentiometer "P" has been provided for.

- **D.C. Feedback :** The C1 capacitor is charged to approximately 1/2 x V_{CC2}. Divider bridge formed by R2 + R4 and R5 networks will set the d.c. feedback. The component values of this divider network will be choosen to avoid saturation at top and bottom of the output voltage. (pin 6 biasing voltage is approximately 0.6 V)
- **Linearity Correction :** A parabolic signal at frame frequency is available on "+" terminal of the C1 capacitor. This signal is integrated by R2, C2 network. An "S" waveform is thus obtained, which is applied to pin 6 via resistor R4.

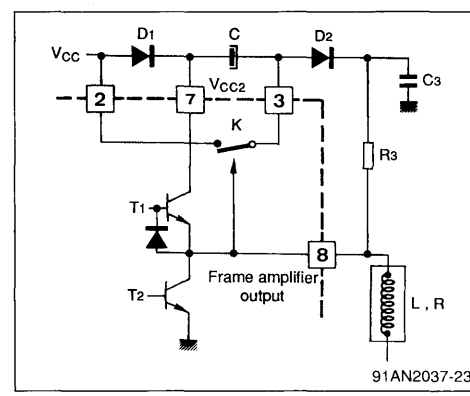
  Any correction to this "S" waveform depends on C1 and C2 values. The linearity correction depends on ratio : R2/R4
- **Vertical Amplitude :** Frame current amplitude is determined by the value of measurement resistor "R1", potentiometer "P" settings and the value of "R5" resistor.

II.8 - Frame flyback generator

The output stage of the vertical amplifier includes a frame flyback generator connected to pin 3. During the vertical scanning flyback time, the value of the yoke inductance "L" must be taken into account since the time constant L/R is no longer negligible. In television applications, the frame blanking time is 1.6 ms. Thus when $L/R > 1.6 \times 10^{-3}$, it is necessary to increase the supply voltage to the frame output amplifier so as to reduce the flyback time. This surplus is required only for the frame flyback and energy is wasted by boosting the supply to the amplifier at all times (during the frame scanning time, the minimum voltage is substantially RI, where I is peak-to-peak frame current).

The configuration of the flyback generator is depicted in Figure below :

Figure 23

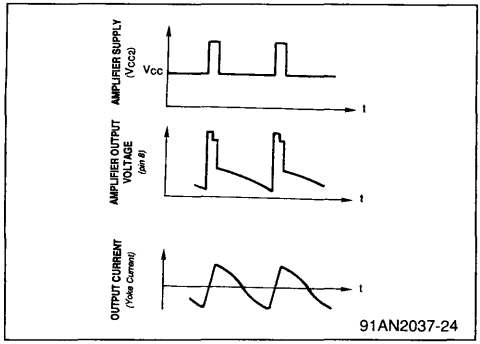


During the second half of the vertical scanning time, transistor T2 conducts and capacitor C is charged to V_{CC} through D1, D2, R3 and T2. (Switch K open)

On flyback, switch K closes and pin 3 is connected to V_{CC}. The voltage at pin 7 (V_{CC2}), which was equal to V_{CC} - V_{D1}, is almost doubled during the flyback time. The only external components required are therefore D1, D2 and C.

In addition to reducing the flyback time, the flyback generator reduces the power consumed by the power stage, and can in certain cases avoid the

Figure 24

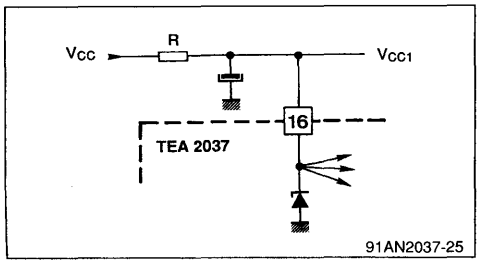


need to use a heatsink.
Diode D2 is a low-signal diode (1N4148) but diode D1 must be appropriately rated since the positive current in the first part of the saw-tooth is supplied to the yoke through D1 and T1. A 1N4001 is generally used.

II.9 - The shunt regulator

The TEA2037 incorporates an internal shunt regulator which delivers the common supply voltage V_{CC} to various blocks such as oscillators, comparator, sync separator and so on.
The voltage on pin 16 is 9.7 V (9 V min, 10.5 V max). The value of the series resistor R must be so calculated to obtain a 15 mA current on pin 16 - this

Figure 25



current can be 10 mA min. and 20 mA max.
The external current supply from V_{CC1} to both oscillators (i.e. line and frame) can be neglected in majority of cases.
The resistor value is found to be 1.2 kΩ at V_{CC} = +28V.
At V_{CC} = + 12 V, and taking into account the voltage tolerance on pin 16, a 150 Ω series resistor must be used.

II.10 - Thermal considerations

In order to ensure reliable device operation, the dissipated power should be accurately determined. Calculation will allow an evaluation of the dissipated power and should be completed by package temperature measurements in actual applications. According to results obtained, a heatsink may or may not be required.

■ Power drawn from V_{CC1} supply :

$$P1 = V_{CC1} \cdot I_1$$

Where I_1 is the current through the shunt regulator (pin 16)

■ Power drawn from V_{CC2} supply :

$$P2 = V_{CC2}\left(\frac{I_{PP}}{8} + I_2\right)$$

Where :

- Ipp = peak-to-peak current through the vertical deflection yoke.
- I_2 = Pin 7 quiescent current.
- V_{CC2} = Pin 7 voltage.

■ Power dissipated in deflection yoke and the measurement resistor :

$$P_Y = (R_Y + R_M)\frac{I^2pp}{12}$$

Where :

- R_y = Frame deflection yoke resistance
- R_M = Measurement resistor value

Thus, the overall power dissipated in the integrated circuit is :

$$P_D = P1 + P2 - P_Y$$

$$P_D = \left[V_{CC1} \cdot I_1\right] + \left[V_{CC2}\left(\frac{Ipp}{8} + I_2\right)\right] - \left[(R_Y + R_M)\frac{I^2pp}{12}\right]$$

In application using the flyback generator, the V_{CC2} specified above becomes "V_{CC2} - V_D", where V_D is the voltage drop across the series diode.

Figure 26

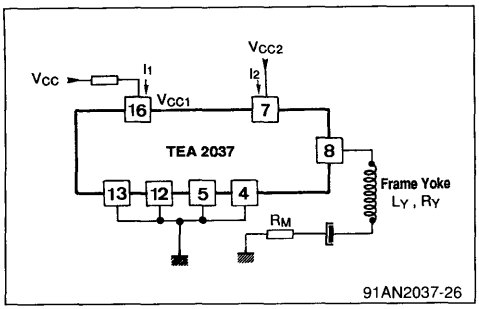
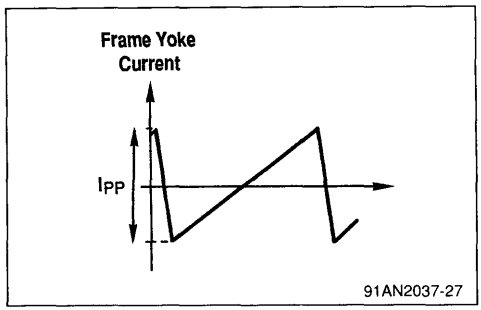


Figure 27



III - APPLICATION EXAMPLES

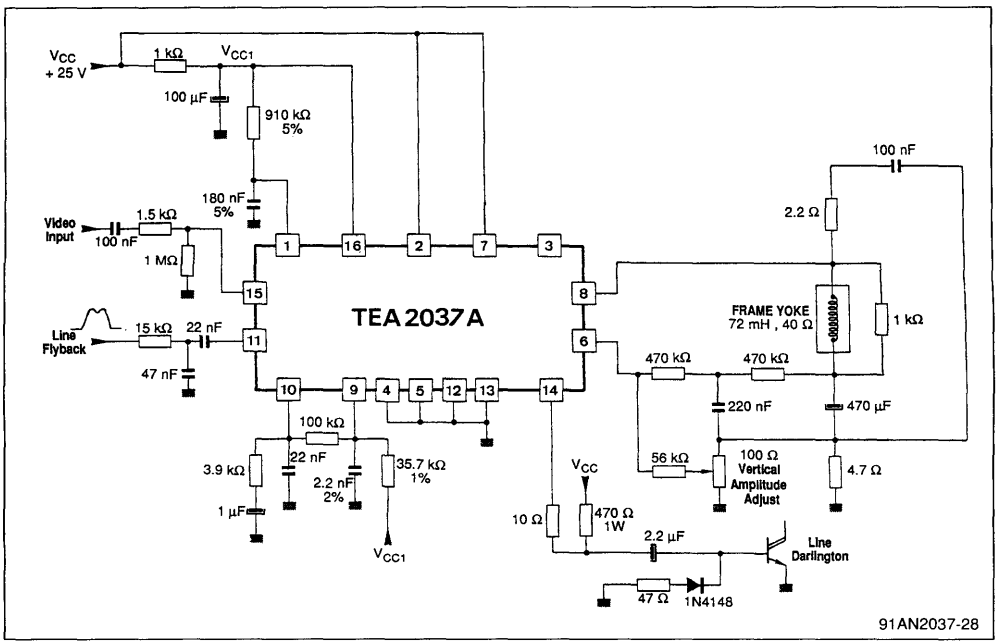
III.1 - Monitor applications

III.1.1 - Low-cost monitor (French Minitel Type)

CHARACTERISTICS

- Screen : 9" Monochrome
- Frame deflection yoke : 72 mH, 40 Ω, 220 mA peak-to-peak
- V_{CC} = + 25 V without flyback generator
- Frame flyback time : 1.2 ms
- Vertical frequency : 50 Hz (20 ms)
- Vertical free-running period : 24.5 ms
- Horizontal frequency : 15 625 Hz
- Capture range : ±5µs
- Holding range : ±10µs
- Input signal : composite video
- Dissipated power : 1.15 W
- Only one adjustment : vertical amplitude

Figure 28



- This is a low-cost application used in French Minitel type configurations and requires minimum number of additional components and adjustments. The input is a composite video signal at line frequency = 15 625 Hz and frame frequency of 50 Hz.
- The free-running horizontal frequency is determined by the component values of RC network on pin 9. Since no adjustment is available, precision components must be used to ensure correct synchronization :

[R = 35.7kΩ, 1% and C = 2.2nF, 2% for f_H = 15 625Hz]

The capture range is large enough to compensate for possible variations.

- Synchronization range of the vertical oscillator is quite large which consequently allows use of less accurate components :

[R = 910 kΩ, 5 % and C = 180 nF, 5 %]

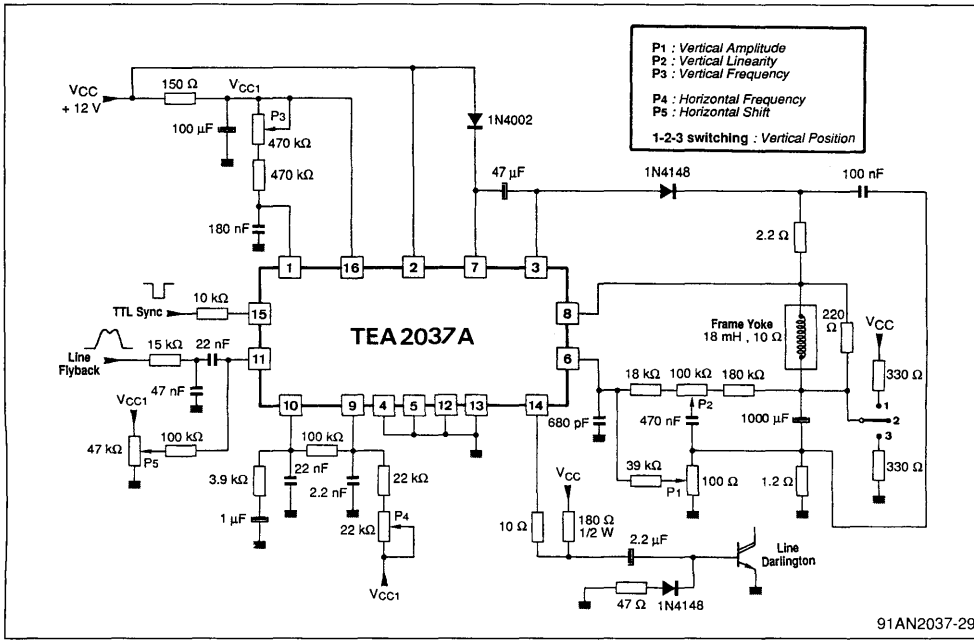
- Since the frame flyback time is short enough at supply voltage used here, the flyback generator is not used in this application.

III.1.2 - Monitor with geometry and frequency adjustments

CHARACTERISTICS

- Screen : 12" Colour
- Frame deflection yoke : 18 mH, 10Ω, 500 mA peak-to-peak
- V_{CC} = + 12V with flyback generator
- Frame flyback time : 0.7 ms
- Vertical frequency : 50/60 Hz
- Vertical free-running period : 23 ms (adjustable)
- Horizontal frequency : 15.7 kHz (adjustable)
- Capture range : = ±5µs
- Holding range : ±10µs
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 0.9 W
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Vertical frequency
  - Horizontal frequency
  - Horizontal phase-shift

Figure 29

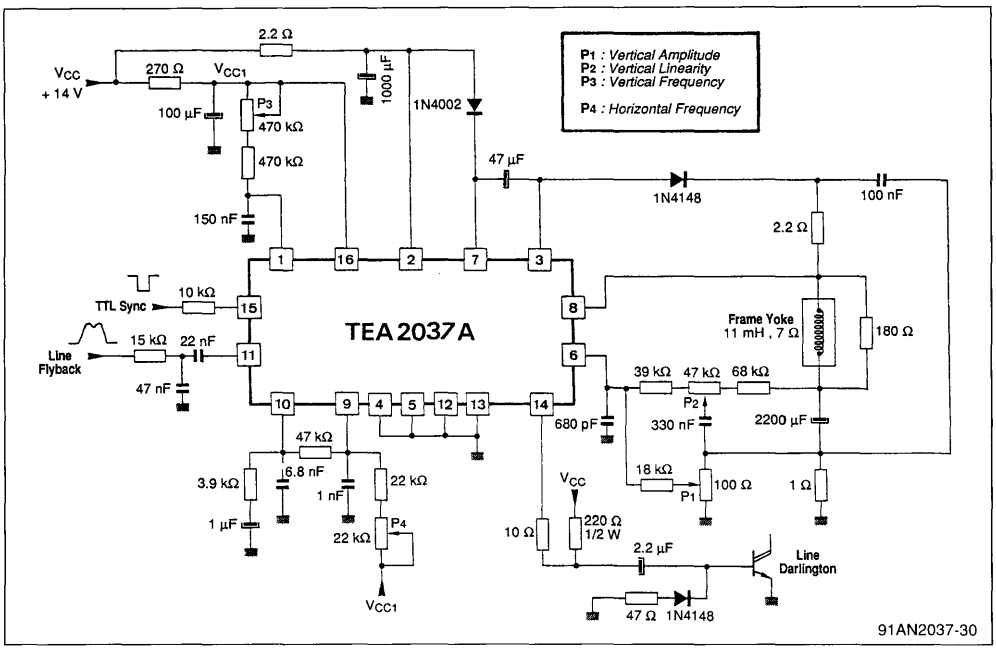


III.1.3 - High frequency monitor

CHARACTERISTICS

- Screen : 14" Colour
- Frame deflection yoke : 11 mH, 7 Ω, 750 mA peak-to-peak
- V_{CC} = + 14 V with flyback generator
- Frame flyback time : 0.6 ms
- Vertical frequency : 72 Hz
- Vertical free-running period : 16 ms (adjustable)
- Horizontal frequency : 35 kHz (adjustable)
- Line flyback time : 5.5µs
- Capture range : 5µs (@sync pulse = 4.7µs)
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 1.4 W (heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Vertical frequency
  - Horizontal frequency

Figure 30

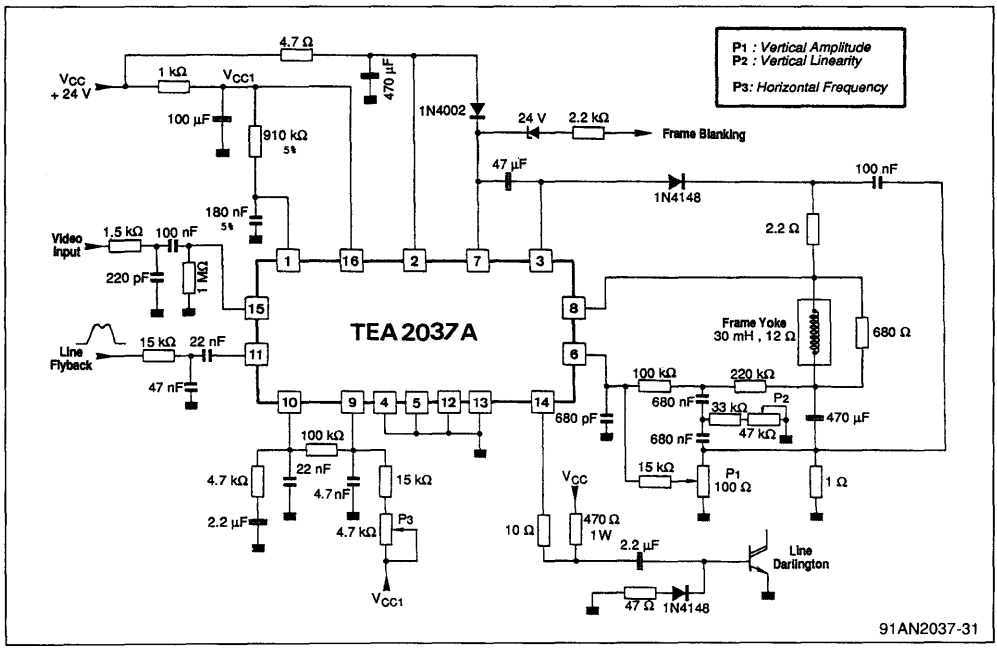


III.2 - Black & white TV application

CHARACTERISTICS

- Screen : 20" B & W 110°
- Frame yoke : 30mH, 12Ω, 850mA peak-to-peak
- V_{CC} = + 24 V with flyback generator
- Frame flyback time : 1ms
- Vertical frequency : 50Hz
- Vertical free-running period : 24.5 ms
- Horizontal frequency : 15 625 Hz (adjustable)
- Capture range : ±2 µs
- Holding range : ±4.5 µs
- Input signal : composite video
- Dissipated power : 2.3 W (10°C/W - heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical linearity
  - Horizontal frequency

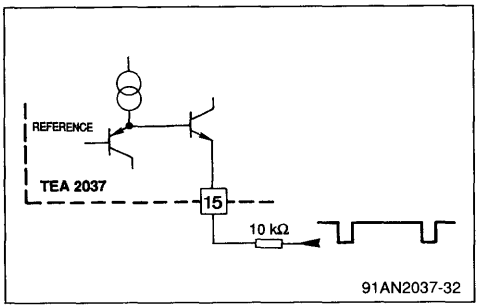
Figure 31



III.3 - Using composite TTL synchronization

Since the threshold level on input pin 15 is internally set at 1.6 V, the device can directly accept TTL signals.
However, a series resistor is required to limit the current sunk by the on-chip transistor (pin 15).

Figure 32



If composite sync signal is not available, line and frame sync signals can be recombined at circuit input as illustrated below.

Figure 33

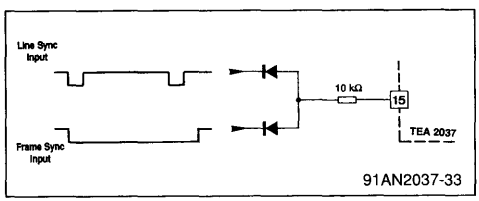
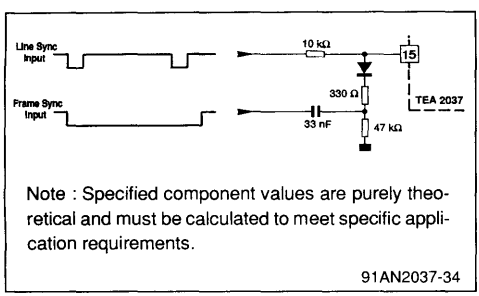


Figure 34 : Application example

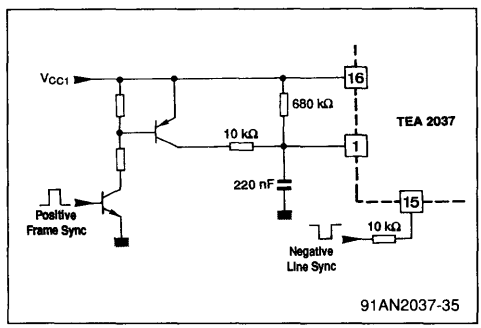


This arrangement is particularly interesting in applications where the available signals differ from those commonly used. An example is the case where the frame signal is of quite long duration (sometimes as long as frame blanking period). In such case, efficient synchronization can be achieved by differentiating the signal so that it will behave as a signal of only few lines duration which is the condition required for appropriate frame and line sync separation and also a picture without flag effect.

III.4 - Direct frame synchronization

The vertical scanning can be directly synchronized by the frame oscillator (pin 1) and without any need of using the synchronization input (pin 15).
Figure 35 illustrates an example :
In this case, only the line sync pulse is applied to pin 15.

Figure 35



III.5 - Constant amplitude 50/60 Hz switching

In applications requiring 50/60 Hz standard switching feature, the arrangement shown below allows to maintain the amplitude of the oscillator sawtooth (pin 1) constant thus yielding uniform vertical scanning.

Figure 36

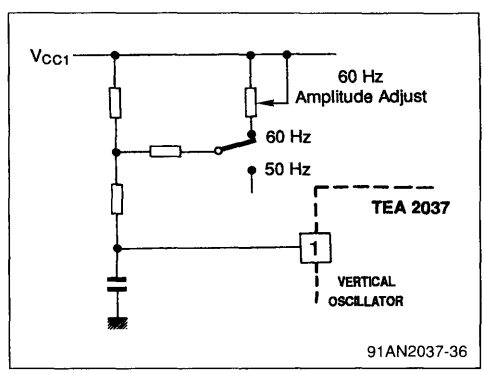
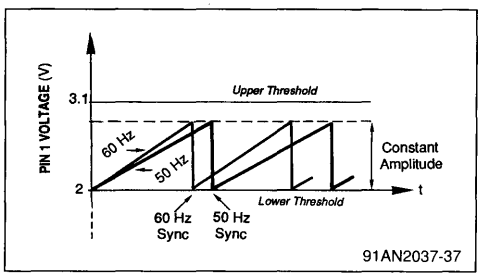
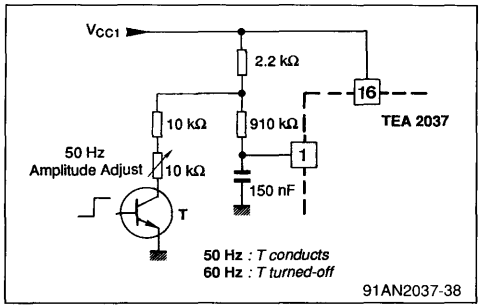


Figure 37



A practical application configuration is illustrated below.

Figure 38



III.6 - Modifying the line output duration

The line output pulse duration is determined by two internally set threshold levels. This interval can be altered by modifying the charge current of the line oscillator (pin 9)

Figure 39

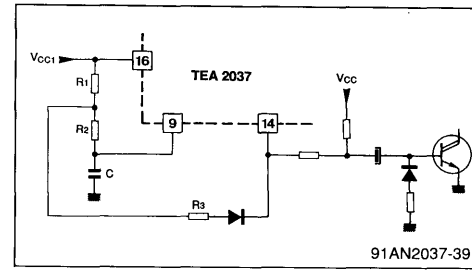
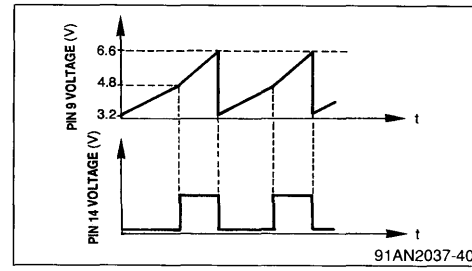


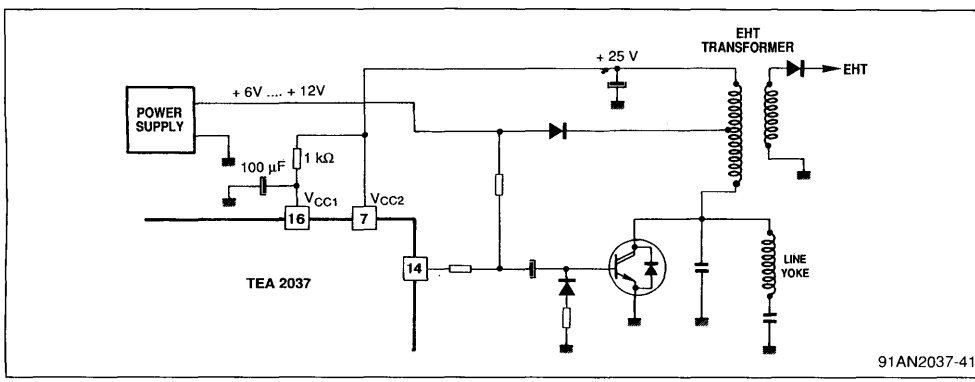
Figure 40



III.7 - Starting the TEA2037 from a +6V power supply

The line oscillator of TEA2037 is capable of starting at a low supply voltage (< 6V). The period of oscillation is practically the same as at nominal operation. It is thus possible to initiate the line scanning at a reduced supply voltage (e.g. +6V) and then supply the overall configuration by the power available on the line transformer.

Figure 41



IV - DESIGN CONSIDERATIONS

IV.1 - Precautions for interlaced scanning

- The links interconnecting the ground terminals of V_{CC} and V_{CC1} power supplies, as well as those of device decoupling capacitors, must be kept to as short as possible
- A high value decoupling capacitor can be used for V_{CC} supply, provided that a good quality low series resistance capacitor is employed. Interlacing is very sensitive to decoupling quality. The value of the decoupling capacitor can vary from 22µF to 100µF.
- The interconnecting links between the frame oscillator capacitor, the line oscillator capacitor and TEA2037 grounds must be kept to as short as possible.

Perfect line and frame synchronization is achieved by observing the above guidelines and recommendations.

IV.2 - Printed circuit board layout

- The usual precautions observed in design of TV timebase pc boards must be employed
- The line output stage handles high amounts of voltage and current. Components employed must therefore be appropriately rated, the width of and the clearance between the wiring tracks should be carefully selected. All connections must be as short as possible and all signals at the line frequency gathered at this section.
- The supply to the frame scanning section of the circuit must not be influenced by the horizontal scanning function, particularly when interlaced scanning is used.
- Generally speaking, interactions on the pc board between the high-gain/low-level and the high-current sections of the output stages must be minimized by as much as possible.
- As indicated in previous chapters, the four center pins of the device must be earthed. The pad used for this purpose must be as large as possible since it acts as the heatsink for the device. A cruciform pad underlying the circuit should be employed.
- There should be a single connection to the chassis earth terminal.

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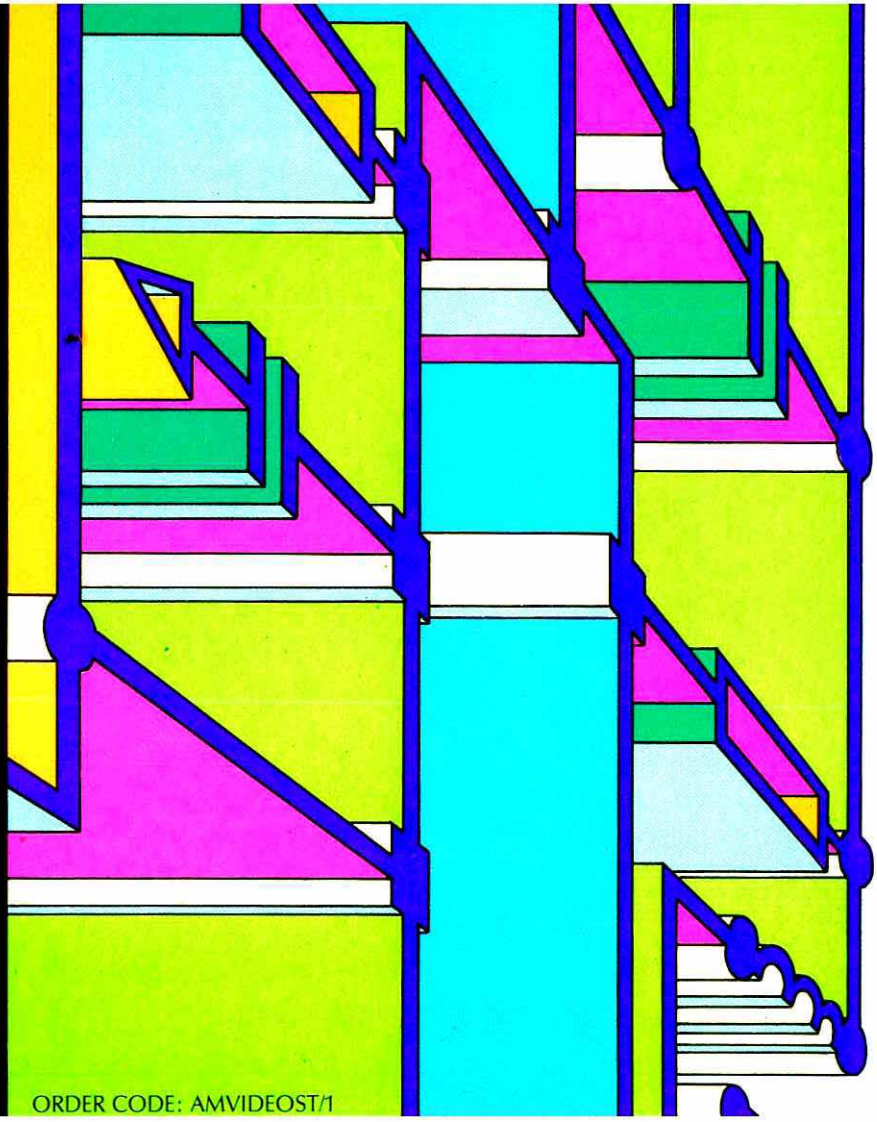

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