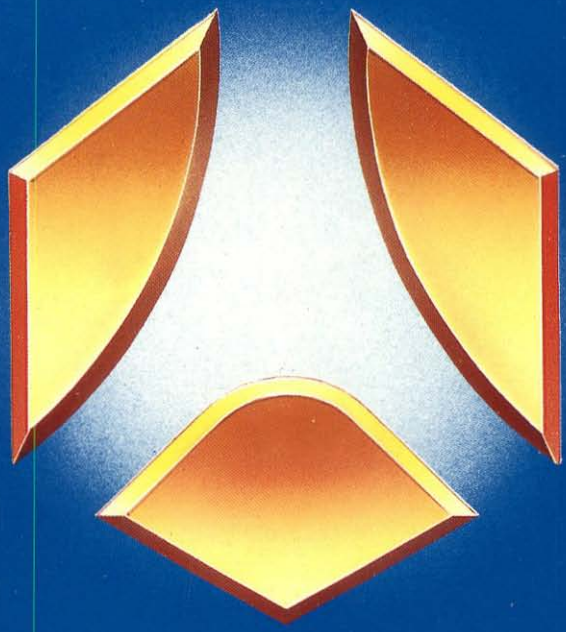
CONSUMER INTEGRATED CIRCUITS

THOMSON SEMICONDUCTORS



DATA BOOK

THOMSON COMPONENTS

THOMSON SEMICONDUCTORS

Formed by combining Efcis, Eurotechnique and Semiconducteurs Alcatel with THOMSON'S Discrete and Bipolar Integrated Circuits divisions into a single operating entity, THOMSON SEMICONDUCTORS has been able to implement a whole set of strategies, technologies, production capabilities, technical and commercial services and to focus on delivering effective answers to the multiple challenges facing today's electronics industry.

With seven research and development laboratories and those of the THOMSON Group—one of the world leaders in electronics: 110.000 people/near 6000 M$ turnover—THOMSON SEMICONDUCTORS offers its customers the benefits of the latest advances in technology: development of new products, innovations in MOS and Bipolar technologies for linear and digital LSI and power semiconductors, new packaging processes, solid state physics, etc... 20% of THOMSON SEMICONDUCTORS revenues are reinvested in Research and Development.

6000 people trained to our exacting professional standards, the latest state of the art production and control equipment, product design aided by powerful data processing ressources—all these make it possible to produce millions of integrated circuits and discrete components together with systems and OEM boards.

In our 7 plants (one located in the U.S.A.) and in all our test and assembly centers, the same quality assurance policy is implemented from product design to the finished product.

Finally with operations in almost any country and an international distribution network of more than 150 companies, THOMSON SEMICONDUCTORS has one of the most comprehensive commercial forces in the world.

THOMSON SEMICONDUCTORS

CONSUMER INTEGRATED CIRCUITS

1983
DATA BOOK

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Application	Function	Part number	Page
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	Power supply control	TEA2019	581

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Application	Function	Part number	Page
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	A.F amplifier	TBA820	429
	A.F amplifier	TBA820M	437
	A.F amplifier	TCA830SM	447
	Dual A.F amplifier	TEA2025	557
	Medium power A.F amplifier (> 3 W, < 8 W)		
	A.F amplifier	TBA810P,AP	411
	A.F amplifier	TBA810S,AS	421
	A.F amplifier	TCA830SR	455
	A.F amplifier	TEA2021	539
	Dual A.F amplifier	TEA2024	547
CAR RADIO	**Medium power A.F amplifier** (> 3 W ; < 8 W)		
	A.F amplifier	TBA810P,AP	411
	A.F amplifier	TBA810CB,ACB	399
	A.F amplifier	TEA2021	539
	High power A.F amplifier (> 8 W)		
	A.F amplifier	TDA2003V,H	499
TV RECEIVERS	**Medium power A.F amplifier** (> 3 W ; < 8 W)		
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	A.F amplifier	TCA940,E	461
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	A.F amplifier	TDA2006	513
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FUNCTIONAL INDEX

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ALPHANUMERIC LISTING

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9366	Graphic display processor	289
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810P,AP	Medium power A.F amplifier	411
810S,AS	Medium power A.F amplifier	421
820	Low power A.F amplifier	429
820M	Low power A.F amplifier	437
920,S	Horizontal processor	17
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TCA830SM	Low power A.F amplifier	447
830SR	Medium power A.F amplifier	455
940,E	Medium power A.F amplifier	461
TDA1041	Flexible speed regulator	611
1048	I.F sound and AM demodulation	31
1102	High power A.F amplifier	471
1111	High power A.F amplifier	489
1154	Speed regulator	615
1170LN,LNH	Low-noise vertical deflection	35
1170S,SH	Vertical deflection	47
TDA2003V,H	High power A.F amplifier	499
2006V, H	High power A.F amplifier	513
2030V,H	High power A.F amplifier	525
2540	I.F video with AFC	61
2541	I.F video with AFC	61
2542	I.F video with AFC	69
2593	Colour TV horizontal processor	75
3300B	PAL-NTSC decoder and processor	89
TEA1001	SMPS control IC (I_O max : ± 3 A)	565
1014	Video and A.F switch	97
1020	Fully protected vertical deflection	103
1030B	Video processor	119
1035	Multichannel A.F stereo switch	129

ALPHANUMERIC LISTING

Part number	Function	Page
TEA2014	Video switch	139
2015A	Vertical deflection	143
2017	Complete H & V deflection	361
2018	Power supply control	577
2019	Power supply control	581
2021	Medium power A.F amplifier	539
2024	Medium power dual A.F amplifier	547
2025	Low power dual A.F amplifier	557
2585	Digital data extractor	371
2586	Data slicer	379
3717	Stepper motor drive	621
TEA5030	Video processor	159
5620	PAL decoder	169
5630	SECAM decoder	185
TEB1013	Quad. Darlington	629
UAA4000	PPM transmitter	197
4000S	PPM transmitter	203
4001	SMPS control IC (I_O max : ± 1 A)	587
4003	Switch mode regulator (I_O max : 1.5 A)	633
4006	SMPS control IC (I_O max : ± 1.5 A)	599
4009	Complete receiver	207

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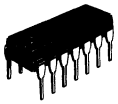
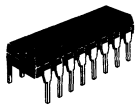
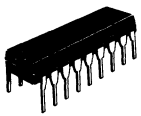
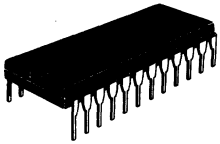
TELEVISION

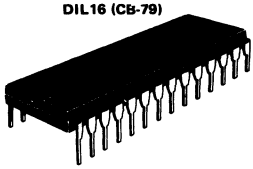

DIL8 (CB-98)


DIL14 (CB-2)


DIL16 (CB-79)


DIL18 (CB-225)


DIL24 (CB-68)

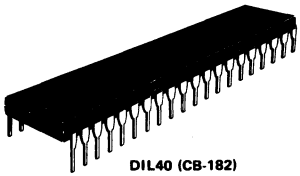

DIL28 (CB-132)

DEFLECTION CIRCUITS

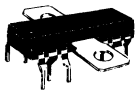
Function	Main features	Part number	Package	Page
HORIZONTAL	Line oscillator, sync. separator, phase comparator for monochrome TV sets.	TBA920 TBA920S	DIL16 (CB-79)	17 17
	Line oscillator combination, burst, blanking and frame pulse separation for color TV sets.	TDA2593	DIL16 (CB-79)	75
VERTICAL	Synchronized oscillator, power amplifier, fly-back generator (maximum output current : 1.5 A).	TDA1170S TDA1170SH	QUIL12(CB-109) QUIL12(CB-155)	47 47
	Low noise integrated circuit for monitors. Synchronized oscillator, power amplifier, fly-back generator (maximum output current : 1.5 A).	TDA1170LN TDA1170LNH	QUIL12(CB-109) QUIL12(CB-155)	35 35
	Synchronized oscillator, power amplifier, fly-back generator (maximum output current ± 2.5 A) and blanking generator.	TEA2015A	SIL13(CB-230)	143
	Fully protected vertical deflection system with a blanking pulse generator and safety systems (maximum output current : ± 2.5 A).	TEA1020	SIL17(CB-215)	103
HORIZONTAL AND VERTICAL	Complete horizontal and vertical deflection circuit. Direct drive of frame yoke (maximum output current : ± 1.5 A), direct drive of line Darlington, muting output.	TEA2017	SIL15(CB-501)	361

CHROMA CIRCUITS

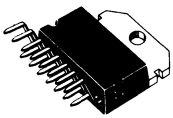
Function	Main features	Part number	Package	Page
PAL DECODER	Complete PAL decoding system.	TEA5620	DIL18(CB-225)	169
SECAM DECODER	Complete SECAM decoding system. Can be combined with PAL decoder for PAL/SECAM applications (automatic PAL/SECAM switching).	TEA5630	DIL24(CB-68)	185
VIDEO PROCESSOR	In conjunction with PAL and/or SECAM decoder, each of these circuits constitutes a complete and flexible color TV chroma system featuring : on screen display inputs, electronic control of contrast, brightness and saturation, automatic cut-off adjustment, low dissipation, and • positive color difference inputs • negative color difference inputs	 TEA5030 TEA1030B	 DIL28(CB-132) DIL28(CB-132)	 159 119
PAL - NTSC DECODER & PROCESSOR	One-chip PAL system with on screen display, electronic controls, automatic cut-off adjustment and beam current limitation.	TDA3300B	DIL40(CB-182)	89


DIL40 (CB-182)


QUIL12 (CB-109)


QUIL12 (CB-155)


SIL17 (CB-215)


SIL15 (CB-501)


SIL13 (CB-230)

VIDEO AND SOUND IF CIRCUITS

Function	Main features	Part number	Package	Page
VIDEO IF	IF amplifiers with demodulator for : • PNP tuners • NPN tuners	 TBA1440G TBA1441	 DIL16(CB-79) DIL16(CB-79)	 25 25
	IF amplifiers with demodulator and AFC (CCIR standard) for : • NPN tuners • PNP tuners	 TDA2540 TDA 2541	 DIL16(CB-79) DIL16(CB-79)	 61 61
	IF amplifier with demodulator and AFC (French standard)	TDA2542	DIL16(CB-79)	69
SOUND IF	IF amplifier and AM demodulator with volume adjustment by electronic potentiometer.	TDA1048	DIL16(CB-79)	31

PERITELEVISION INTERFACE CIRCUITS

Function	Main features	Part number	Package	Page
VIDEO SWITCH	Switched 2 Vpp Video output. Not switched 75 Ω. 1 Vpp video output.	TEA 2014	DIL8(CB-98)	139
VIDEO AND AF SWITCH	For monosound TV sets. Follows the SCART specification n° 108.	TEA1014	DIL14 (CB-2)	97
MULTI CHANNEL AF STEREO SWITCH	Up to five stereo channel switch.	TEA1035	DIL14 (CB-2) DIL18(CB-225) DIL24(CB-68)	129

REMOTE CONTROL CIRCUITS

Function	Main features	Part number	Package	Page
TRANSMITTER	For ultra-sonic or infra-red transmission. 32 command capability. Pulse position modulation provides excellent noise immunity.	UAA4000 UAA4000S	DIL18(CB-225) DIL18(CB-225)	197 203
RECEIVER	Complete circuit for PPM demodulation. 12 channel tuning voltage switch (remote and keyboard), one DC voltage output for volume adjustment, standby information.	UAA4009	DIL18(CB-225)	207

AF CIRCUITS FOR TV : See section 4 page 387

SWITCH MODE POWER SUPPLIES : See section 5 page 563.

THOMSON SEMICONDUCTORS

TBA920
TBA920 S

LINE OSCILLATOR COMBINATION FOR TV SETS
BASE DE TEMPS LIGNES POUR TV (JUNGLE)

The line oscillator combination TBA920 is a monolithic integrated circuit intended for the horizontal deflection of the black and white and colour TV SETS picture tube.

This circuit is able to perform the following functions (see block diagram, page 5) :

- **Sync-pulse separation**
- **Optional noise inversion**
- **Generation of a line frequency voltage by means of on oscillator**
- **Phase comparaison between sync-pulse and the oscillator waveform**
- **Phase comparaison between the oscillator waveform and the middle of the line fly-back pulse**
- **Automatic switching of the variable transconductance and the variable time constant to achieve noise suppression and, by switching off, possibility of tape-video-registered reproduction**
- **Shaping and amplification of the oscillator waveform to obtain pulses for the control of driving stages in horizontal, deflection circuits using either transistors or thyristors.**

Le TBA920 est un circuit intégré monolithique permettant de réaliser la base de temps lignes dans les récepteurs de télévision en noir et blanc et en couleur.

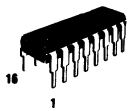
Il remplit les fonctions suivantes:

- Séparateur signal-synchro
- Porte de bruit
- Oscillateur de ligne
- Comparateur de phase entre l'impulsion de synchro de lignes et l'oscillateur
- Comparateur de phase entre l'impulsion de retour de lignes et la période équivalente du signal vidéo
- Constante de temps et gain de boucle variables permettant la suppression des bruits avec la possibilité de reproduction des enregistrements vidéo sur bande magnétique
- Etage de sortie permettant la commande soit de thyristors, soit de transistors, soit de tubes.

LINE OSCILLATOR COMBINATION FOR TV SETS
BASE DE TEMPS LIGNES POUR TV (JUNGLE)

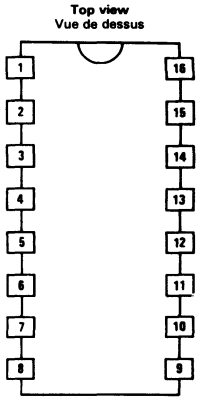
2

CASE/BOITIER CB-79



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE

PIN CONFIGURATION
BROCHAGE



1 **Positive supply**
Alimentation positive

2 **Driver line stage pulse, driving and output stage**
Sortie des impulsions de commande de lignes

3 **Input control voltage for pulse width**
Entrée de commande de largeur des impulsions de sortie

4 **Phase discriminator output between fly-back pulse and oscillator**
Sortie du comparateur de phase entre l'impulsion de retour de lignes et l'oscillateur

5 **Fly-back pulse input**
Entrée de l'impulsion de retour de lignes

6 **Synchro pulse input**
Entrée de l'impulsion de synchro

7 **Synchro pulse output**
Sortie du séparateur signal-synchro

8 **Video signal input**
Entrée su signal vidéo (séparateur signal-synchro)

9 **Noise gate input**
Entrée porte de bruit (non utilisée en modulation positive)

10 **Switch emission-magnetoscope**
Commutation émission/magnétoscope

11 **Time constant switch**
Voie de communication des constantes de temps

12 **Oscillator control voltage loop**
Sortie du comparateur de phase entre l'impulsion de synchro et l'oscillateur (tension de commande de l'oscillateur)

13 **Oscillator decoupling**
Découplage de l'oscillateur

14 **Tuning oscillator capacitor**
Branchement du condensateur d'accord de l'oscillateur

15 **Oscillator control voltage**
Tension de commande de l'oscillateur

16 **Ground**
Masse.

NT 7560

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THOMSON COMPONENTS

LIMITING VALUES
VALEURS LIMITES ABSOLUES

(Unless otherwise stated)
(Sauf indications contraires)

PARAMETERS *PARAMETRES*		SYMBOLS *SYMBOLES*	MIN.	TYP.	MAX.	UNITS *UNITES*
Power supply voltage *Tension d alimentation*	V_{1-16}	V_{CC}	4		14	V
Power dissipation *Dissipation de puissance*		P_{tot}			600	mW
Ambiant température *Température ambiante de fonctionnement*		T_{amb}	−20		+60	°C
Storage temperature *Température de stockage*		T_{stg}	−55		+150	°C

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C V_{CC} = 12 V

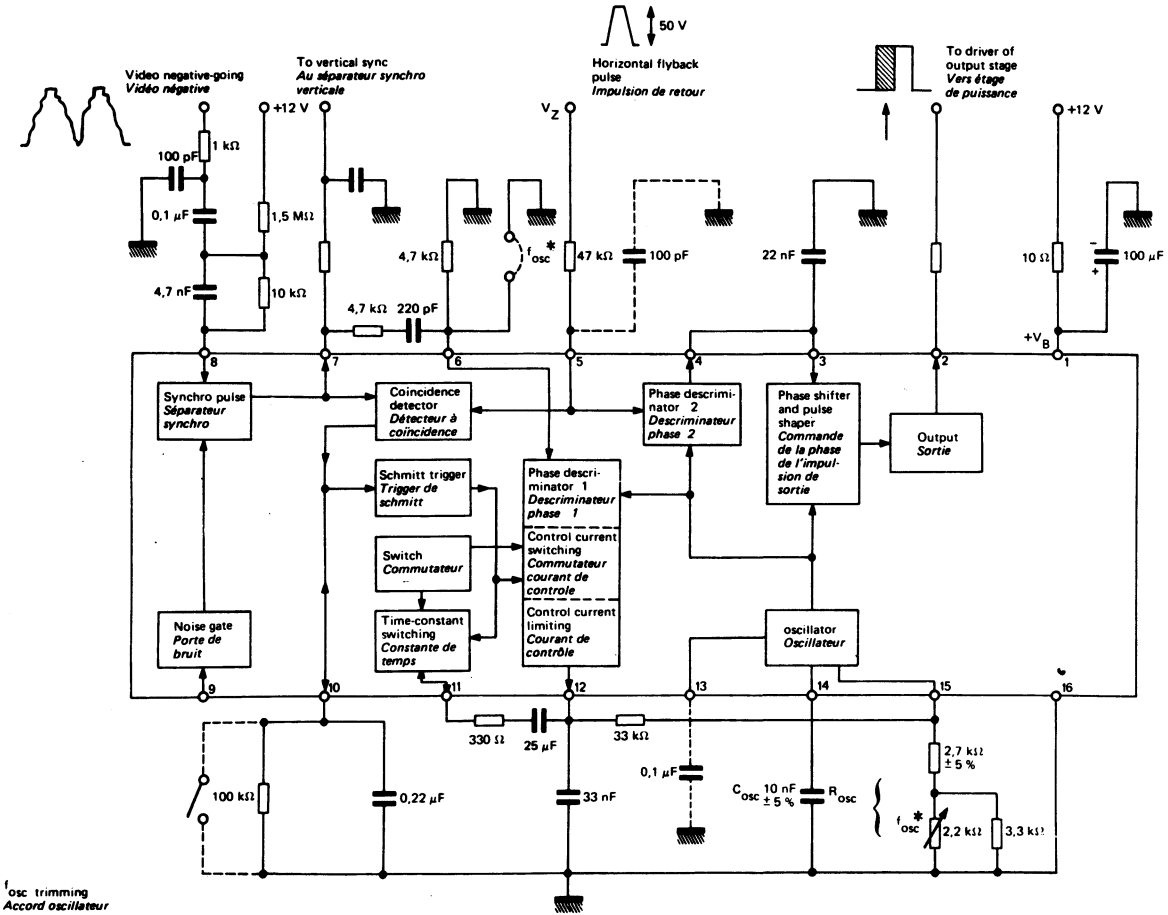
PARAMETERS *PARAMETRES*	TEST CONDITIONS *CONDITIONS DE MESURE*	SYMBOLS *SYMBOLES*	Pins *Broches*	MIN.	TYP.	MAX.	UNITS *UNITES*
Inputs *Entrées*							
Video signal *Signal vidéo*							
Input voltage (positive synchro-pulse) *Tension d'entrée (impulsions de synchro positives)*		V_I	8-16	1	3	7	V
Input current *Courant d'entrée*		I_I	8			0,2	mA
Flyback pulse *Impulsion de retour de lignes positives*							
Input current *Courant d'entrée*		I_I	5	0,1	1	2	mA
Input voltage *Tension d'entrée*		V_I	5-16		±0,8		V
Input resistance *Impédance d'entrée*		Z_I	5-16		0,4		kΩ
Noise gate *Porte de bruit*							
Input current *Courant d'entrée*		I_I	9		20		μA
Input voltage *Tension d'entrée*		V_I	9-16		0,7		V
Outputs *Sorties*							
Synchro pulse *Impulsions de synchro positives*							
Output voltage *Tension de sortie*		V_O	7-16	9	10		V
Output impedance on rise time *Impédance de sortie sur le front avant*		Z_O	7-16		50		Ω
Output impedance on fall time *Impédance de sortie sur le front arrière*		Z_O	7-16		2,2		kΩ

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C V_{CC} = 12 V (Unless otherwise stated) *(Sauf indications contraires)*

PARAMETERS *PARAMETRES*	TEST CONDITIONS *CONDITIONS DE MESURE*	SYMBOLS *SYMBOLES*		MIN.	TYP.	MAX.	UNITS *UNITES*
Line amplifier *Amplificateur de lignes*	Peak to peak						
Output current and voltage *Courant et ension de sortie*		I_O			25	200	mA
		V_O		9	10		V
Output pulse duration (adjust by V_{3-16}) *Durée des impulsions de sortie (ajustable par V_{3-16})*		t_p		12		32	µs
Flyback pulse phase control *Commande de la phase des impulsions de retour de lignes*							
Delay accepted between output pulse and flyback pulse *Retard acceptable entre l'impulsion de sortie et l'impulsion de retour de lignes*				0		15	µs
Output current during flyback pulse *Courant de sortie pendant l'impulsion de retour de lignes* I_4		I_O			±0,5		mA
Line oscillator (no synchronised) *Oscillateur de lignes (non synchronisé)*							
for 625 lines *pour 625 lignes*					15625 ±5 %		Hz
for 819 lines *pour 819 lignes*					20475 ±5 %		Hz
At supply cut-off, without synchronised *A la coupure de la tension d alimentation non synchronisé*							
for 625 lines *pour 625 lignes*					15625 ±10 %		Hz
for 819 lines *pour 819 lignes*					20475 ±10 %		Hz
Phase control between oscillator and synchro-pulse *Asservissement de phase entre l'oscillateur et les impulsions de synchro*							
With emission *Sur émission*							
Pull in range *Plage de capture*					±1		kHz
Keep in range *Plage de maintien*					±1		kHz
Sensibility *Sensibilité*		S			3		kHz/µs
With magnetoscope *Sur magnétoscope*							
Keep in range *Plage de maintien*					±350		Hz
Pull in range *Plage de capture*					±350		Hz
Sensibility *Sensibilité*		S			±1		kHz/µs

APPLICATION SCHEMA
SCHEMA D'APPLICATION



PARAMETERS *PARAMETRES*	TEST CONDITIONS *CONDITIONS DE MESURE*	SYMBOLS *SYMBOLES*	Pins *Broches*	MIN. TYP. MAX.	UNITS *UNITES*
Oscillator *Oscillateur*					
Oscillator frequency spead *Dispersion de la fréquence de l'oscillateur*	$R_{15-16} = 3{,}3\ k\Omega$ $C_{14-16} = 10\ nF$	ΔF_O	14-16	$\leqslant 1{,}5$	%
Oscillator frequency range *Gamme de réglage de la fréquence de l'oscillateur*	fig. 1 fig. 2	ΔF_O	14-16	± 5	%
Phase position *Position de la phase*					
Phase spead between front end synch pulse and flyback pulse center *Dispersion de la phase entre le front avant de l'impulsion de synchronisation et le milieu de l'impulsion de retour (flyback)*	fig. 1	Δt	6-16 5-16	$\leqslant \pm 0{,}4$	µs

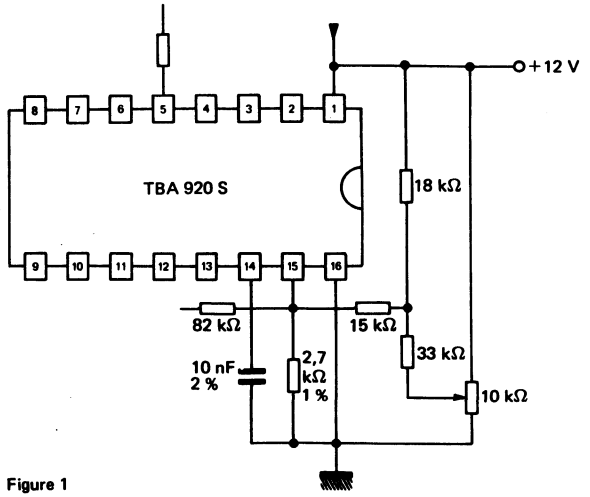
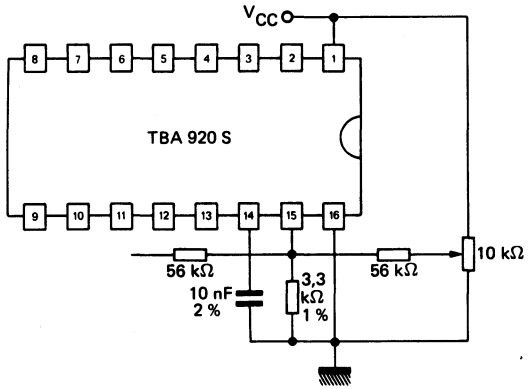


Figure 1

APPLICATION : EUROPEAN STANDARD 625 LINES
APPLICATION : NORMES EUROPEENNES 625 LIGNES

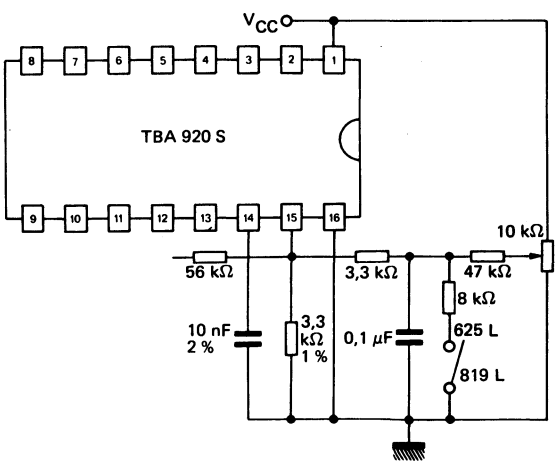


Réglage : $\Delta_f = \pm 5\ \%$
Control

Figure 2

APPLICATION : FRENCH STANDARD 625 - 819 LINES
APPLICATION : NORMES FRANCAISES 625 - 819 LIGNES

Progressive change 655 819 lignes
Changement progressif 625 819 lignes



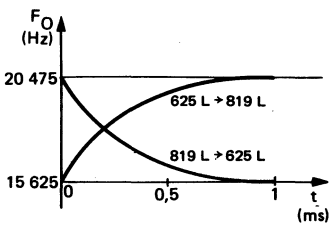
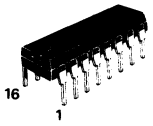
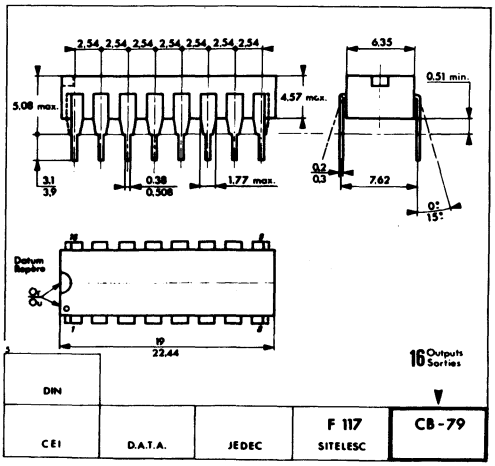


Figure 3

CASE/BOITIER CB-79



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

TBA1440 G
TBA1441

VIDEO IF AMPLIFIERS
AMPLIFICATEURS FI VIDEO

The integrated circuits TBA1440 G and TBA1441 perform the same functions and are interchangeable. The following advantages can be provided:

- **Decreasing residual IF at video-outputs**
- **Decreasing residual IF at pin 13 (supply)**
- **Excellent demodulation linearity**
- **Increasing the output current at the pin 4**

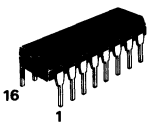
Les circuits intégrés TBA1440 G et TBA1441 sont destinés à remplacer les TBA440 P et TBA440 N, ils sont interchangeables. Les améliorations par rapport aux types précédents sont les suivantes:

- Diminution du résidu FI sur les sorties 11 et 12
- Diminution du résidu FI sur la broche d'alimentation 13
- Meilleure linéarité de démodulation
- Augmentation du courant de charge de la capacité branché sur la borne 4.

VIDEO IF AMPLIFIERS
AMPLIFICATEURS FI VIDEO

2

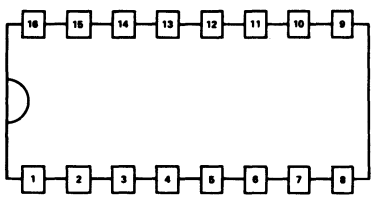
CASE/BOITIER CB-79



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE

PIN CONFIGURATION
BROCHAGE

Top view
Vue de dessus



1 **IF input**
Entrée FI

2 **Decoupling**
Découplage

3 **Ground**
Masse

4 **ACG filter**
Filtre de CAG

5 **Tuner ACG control**
Commande de CAG tuner

6 **Tuner ACG delay time adjustment**
Réglage du retard CAG tuner

7 **ACG gate**
Porte CAG

8 **Tuned circuit for carrier recovery**
Circuit accordé de récupération de porteuse

9 **Tuned circuit for carrier recovery**
Circuit accordé de récupération de porteuse

10 **ACG amplifier input**
Entrée amplificateur de CAG

11 **Video negative output**
Sortie Vidéo négative

12 **Vidéo positive output**
Sortie Vidéo positive

13 V_{CC}

14 **Output DC voltage adjustment**
Réglage tension continue de sortie

15 **Decoupling**
Découplage

16 **IF input**
Entrée FI

NT7740

THOMSON SEMICONDUCTORS
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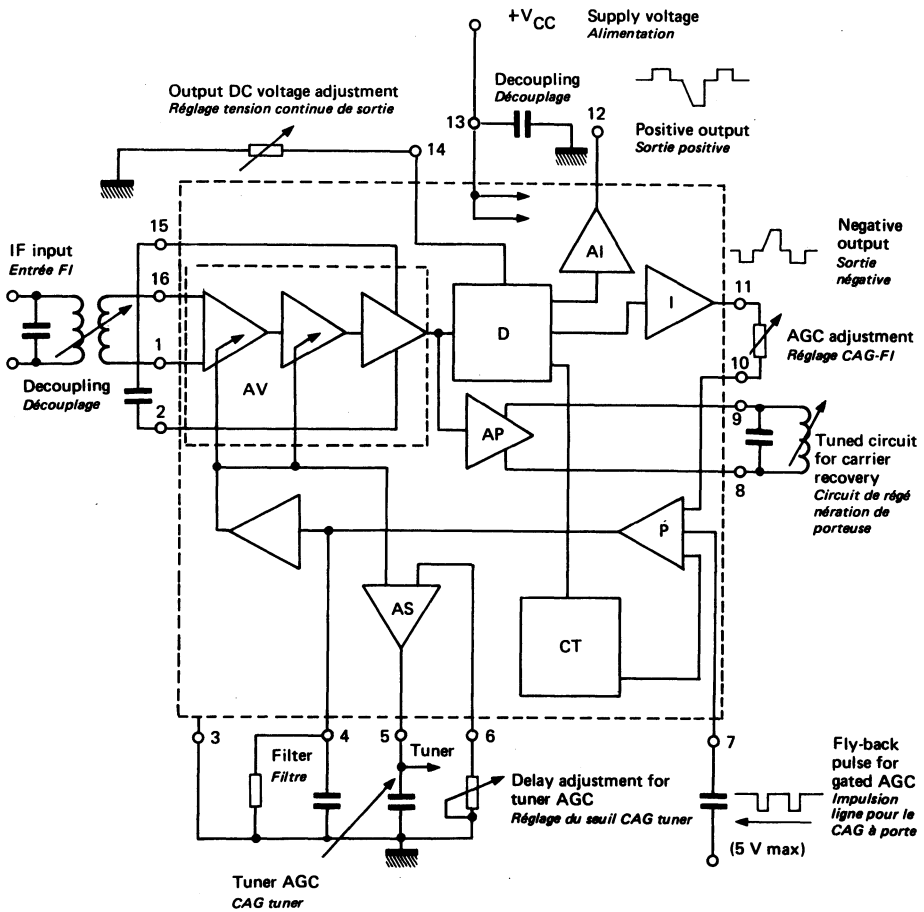
THOMSON COMPONENTS

BLOCK DIAGRAM
SCHEMA BLOC

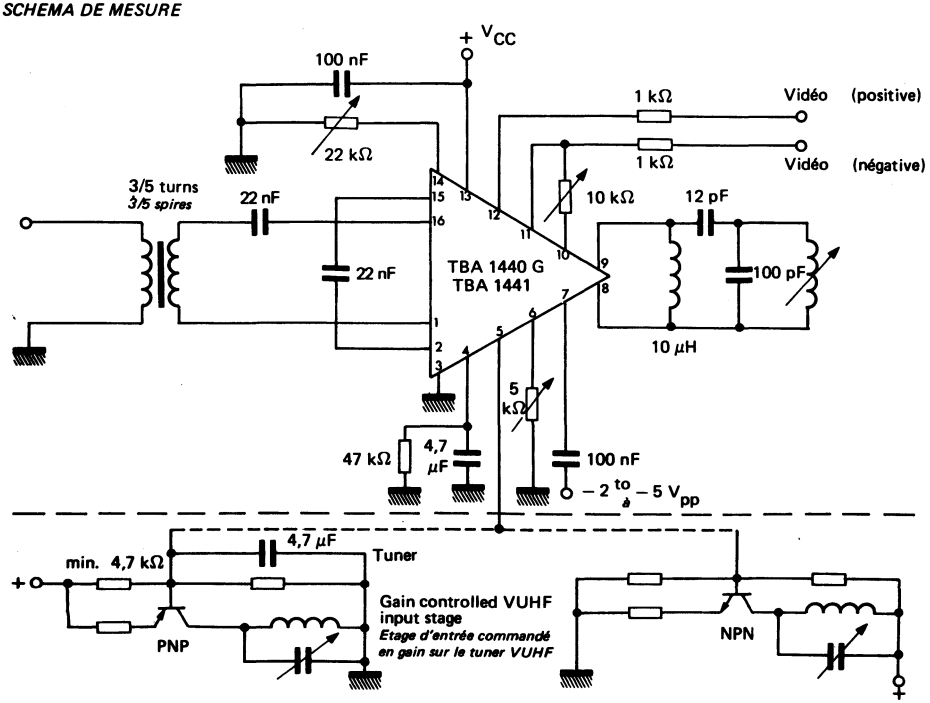


D	Demodulator *Démodulateur*	P	ACG gate *Porte de CAG*
AI	Impedance buffer *Adaptateur d'impédance*	CT	Temperature compensation *Compensation de température*
I	Inverter and impedance buffer *Inverseur et adaptateur d'impédance*	AS	Threshold amplifier *Amplificateur à seuil*
AP	Carrier amplifier *Amplificateur de porteuse*	AV	IF amplifier *Amplificateur FI*

ABSOLUTE RATINGS (LIMITING VALUES)
VALEURS LIMITES ABSOLUES D'UTILISATION

	SYMBOLS *SYMBOLES*	PINS *BROCHES*	Min.	Typ.	Max.	
Supply voltage $t_p < 10$ s *Tension d'alimentation*	V_{CC}	13	10,5		15	V
Maximum voltage on pin 5 (tuner AGC) *Tension max. sur la broche 5 (CAG tuner)*	V	5			20	V
Ohmic resistance between pin 8 and pin 9 *Résistance ohmique entre les broches 8 et 9*	R_R	8 – 9	0		20	Ω
Maximum voltage on pins 4 and 14 *Tension max. sur les broches 4 et 14*	V	4 – 14			5	V
Power dissipation $T_{amb} \leqslant 55°C$ *Dissipation de puissance*	P_{tot}			0,7		W
Operating ambient temperature *Température ambiante de fonctionnement*	T_{amb}		−25		+60	°C
Junction temperature *Température de jonction*	T_j				+150	°C
Junction ambient thermal resistance *Résistance thermique jonction ambiante*	$R_{th(j-a)}$				100	°C/W

TEST CIRCUIT
SCHEMA DE MESURE

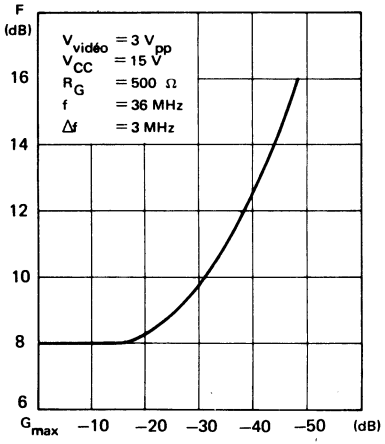


STATIC CHARACTERISTICS
CARACTERISTIQUES STATIQUES

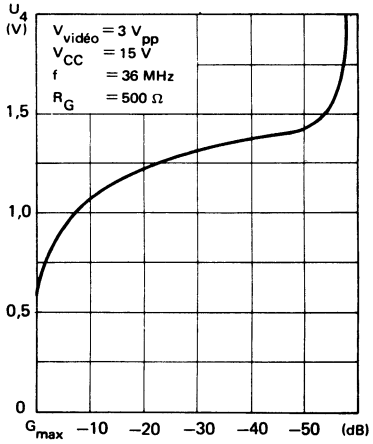
$T_{amb} = 25°C$ $V_{CC} = 13\ V$

	Test conditions *Conditions de mesure*		Pins *Broches*	Min.	Typ.	Max.	
Supply current *Courant d'alimentation*		I_{CC}	13		42		mA
Tuner control current capability *Courant de commande du tuner disponible*	$V_5 > 2V$	I	5	10	15		mA
IF ACG voltage *Tension de CAG FI*	max gain *Gain max.*	V	4	0		0,5	V
	min gain *Gain min.*	V	4	2,5		5	V
Clock pulse voltage *Amplitude de l'impulsion de porte CAG*			7	−2		−5	V
Output resistance *Résistance extérieure de sortie*	$V_{(11)} = 3\ V_{pp}$	R_O	10 - 11		3		kΩ
Output current to ground *Courant de sortie vers la masse*		I_O	11 - 12			5	mA
Output current to positive supply *Courant de sortie vers l'alimentation positive*		I_O	11 - 12			−1	mA
Input impedance *Impédance d'entrée*	max gain *Gain max.*	Z_I	1 - 16		1,8 2		kΩ pF
	min gain *Gain min.*	Z_I	1 - 16		1,9 0		kΩ pF
Input voltage *Tension d'entrée*	3 V_{pp} Video output *Sortie Vidéo*	V_I	1 - 16	70	100	300	μV
Video band width *Largeur de bande video*		B		6	7		MHz
Range of regulation *Dynamique de CAG*		$\frac{Gmax}{Gmin}$		52	56		dB
Residual IF *Résidu FI*		V	11 12		10		mV
Output voltage pin 11 *Tension continu sur la sortie 11*	$R_{14-3} = \infty$ $R_{14-3} = 0$	V V	11 11		5,5 9,6		V V
Output voltage pin 12 *Tension continu sur la sortie 12*	$R_{14-3} = \infty$ $R_{14-3} = 0$	V V	12 12		1,9 2,5		V V

NOISE FACTOR F = f (a)
FACTEUR DE BRUIT F = f(a)

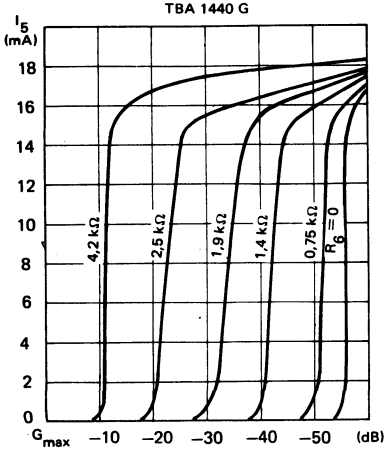


IF AGC VOLTAGE
TENSION DE CAG FI



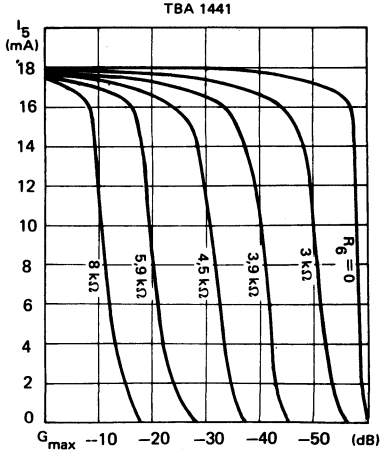
UVHF AGC current I_5
COURANT DE COMMANDE CAG TUNER (broche 5)

TBA 1440 G

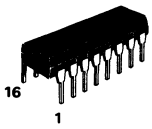


UVHF AGC current I_5
COURANT DE COMMANDE CAG TUNER (broche 5)

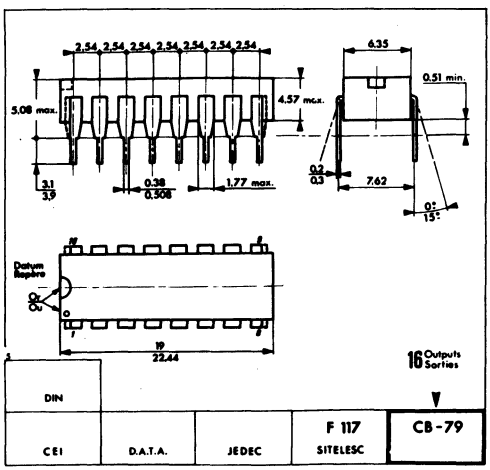
TBA 1441



CASE/BOITIER CB-79



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE



These specifications are subject to change without notice.
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THOMSON SEMICONDUCTORS

TDA1048

IF AMPLIFIER AND AM DETECTOR

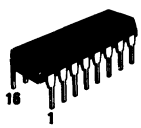
The inegrated circuit TDA1048 is intended for use in the french sound section of TV receivers (AM) ; this circuit includes the following functions :

- IF amplifier with automatic gain control
- AM detector with low distorsion
- Electronic potentiometer (Audio frequency volume control by variation of DC voltage).

IF AMPLIFIER AND AM DETECTOR

2

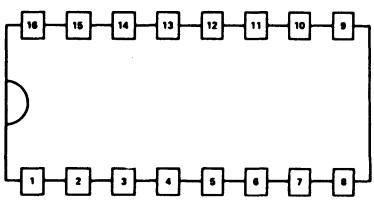
CASE CB-79



DP SUFFIX
PLASTIC PACKAGE

PIN CONFIGURATION

Top view



1	Ground	9	DC control input of AF pre-amplifier
2	Decoupling	10	AF output after electronic potentiometer
3	AF constant level output	11	Output regulated voltage
4	AF constant level input	12	Supply voltage
5	IF input for demodulation	13	Decoupling
6	Filtering condensator	14	Decoupling
7	IF output	15	HF input
8	Supply voltage of IF output amplifier	16	Decoupling

NT7844R1-A

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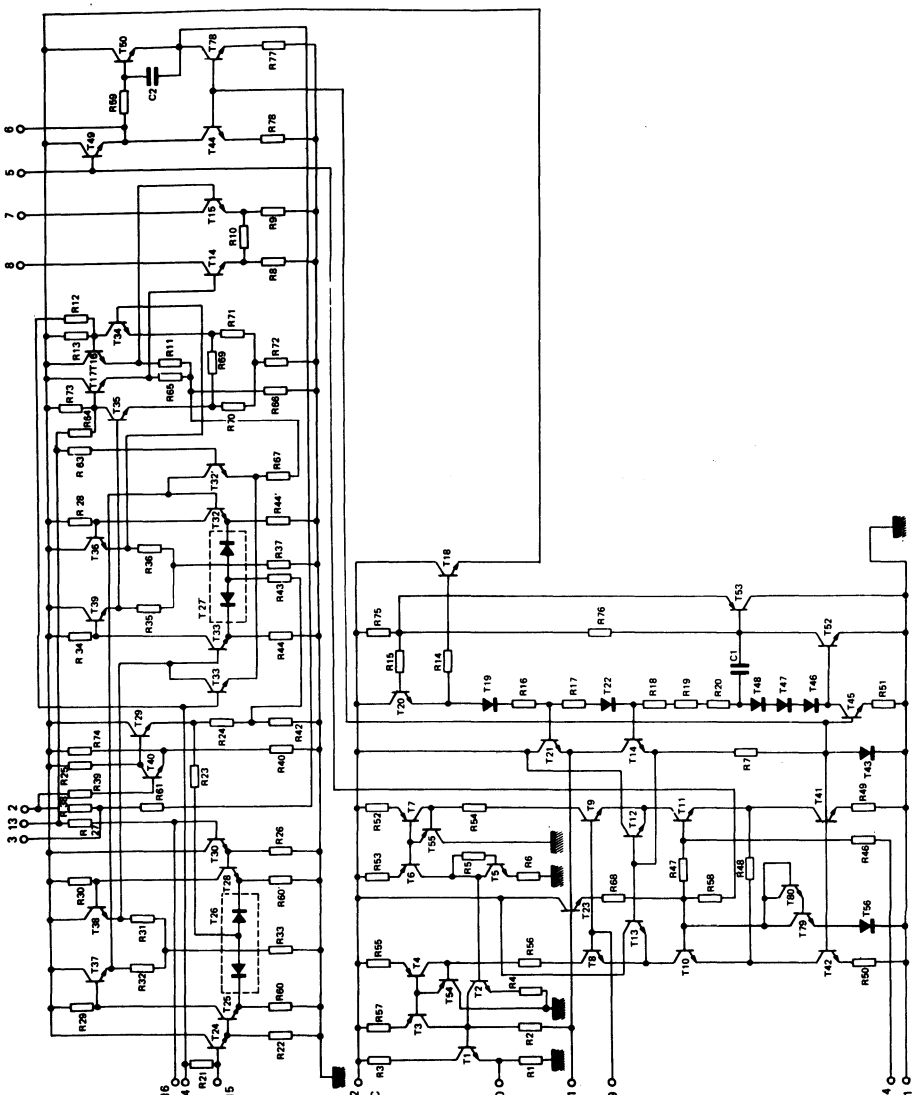
THOMSON COMPONENTS

ELECTRIC DIAGRAM



MAXIMUM RATINGS (Transformer input 3 : 5)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	16.5	V
Power dissipation	P_{tot}	700	mW
Ambient operating temperature	T_{amb}	0 to 60	°C
Storage temperature	T_{stg}	- 40 + 125	°C
Maximum junction temperature	T_j	125	°C
Available current at the pin 11 (regulated internal power voltage)		5	mA

THERMAL CHARACTERISTICS

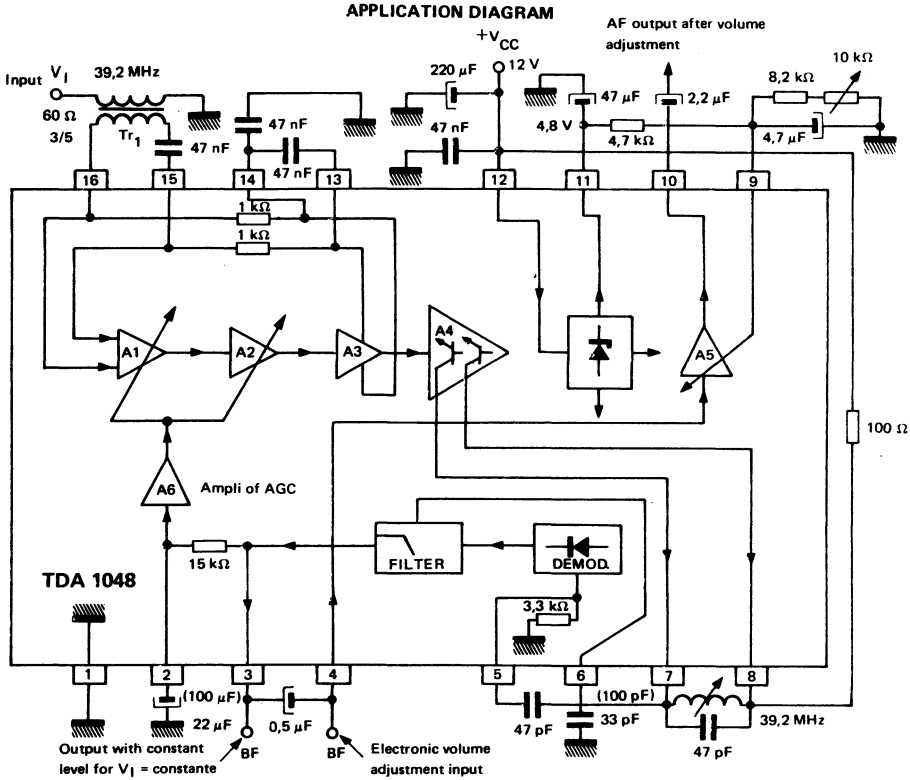
Characteristic	Symbol	Value	Unit
Junction ambient, thermal resistance	$R_{th(j-a)}$	100	°C/W

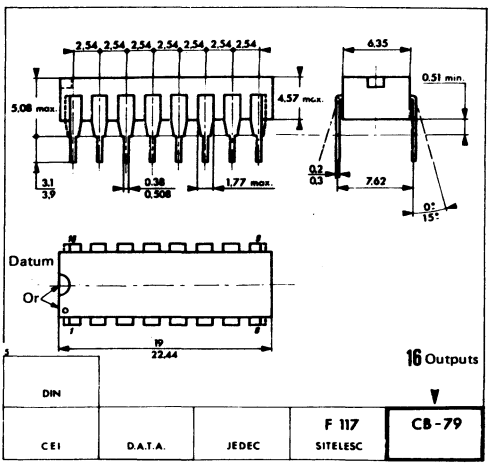
ELECTRICAL CHARACTERISTICS

$T_{amb} = +25°C$; $V_{CC} = 12$ V ; $F_{IF} = 40$ MHz

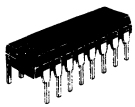
Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage	Pin 12	V_{CC}	10	–	15	V
Supply current	Pins 7, 8, 12		29	37	48	mA
IF constant output current (I7 = I8)	Pins 7, 8		–	4	–	mA
Input regulation voltage (threshold) (AF_{nom} – 3 dB)	Pins 15, 16	V_I to 60 Ω	100	–	–	μV_{eff}
AF output voltage m = 80 % m = 50 % m = 30 %	Pin 10	V_{AF}	0.9 – –	1.4 900 500	1.5 – –	V_{eff} mV_{eff} mV_{eff}
Maximum AF attenuation (11 = 47 μF)	Pin 10	$\frac{V_{AF\ max}}{V_{AF\ min}}$	70	80	–	dB
AF output impedance constant level (before volume adjustment)	Pin 3		–	200	300	Ω
AF output impedance (after volume adjustment)	Pin 10		–	130	150	Ω
Load impedance	Pin 3	R_L	3.3	–	–	kΩ
Load impedance	Pin 10	R_L	3.3	–	–	kΩ
Available regulated output voltage	Pin 11		4.4	5.1	5.8	V
Temperature coefficient of regulated voltage (between + 20° and + 70°)	Pin 11		–1	–	+ 1	mV/°K
AF distorsion for m = 30 %			–	–	1	%
AF distorsion for m = 50 %			–	–	1.6	%
AF distorsion for m = 80 %			–	–	2	%
Output AF level variation for 55 dB of IF signal input variation			–	3	–	dB
AF amplification	Pin 4 to 10		6	7	–	dB
Input impedance	Pin 4		6.5	9	11.5	kΩ
AF output level tolerance	Pin 10		–2	–	+ 2	dB
Input impedance for maximum gain			1.35 1.9	1.8 2.4	2.25 2.9	kΩ pF
Input impedance minimum gain			1.05 2.3	1.4 2.8	1.75 3.3	kΩ pF
Resistance of volume control potentiometer for -30 dB AF level maximum		R_{pot}	4	–	5	kΩ

APPLICATION DIAGRAM





CASE CB-79



DP SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TDA1170 LN
TDA1170 LNH

LOW NOISE T.V VERTICAL DEFLECTION SYSTEM

The TDA1170 LN , LNH is a silicon monolithic integrated circuit in a 12 lead dual in line plastic package. It is intended for use in black and white and colour TV receivers. Low - noise features make this device particulary suitable for use in monitors.

The functions incorporated are:

- synchronization circuit
- oscillator and ramp generator
- high power gain amplifier
- fly back generator
- voltage stabilizer
- Max supply voltage 35 V
- Max fly back voltage 60 V
- Max peak to peak deflecting current 50 Hz 1.5 A

LOW NOISE
TV VERTICAL
DEFLECTION SYSTEM

2

CASES

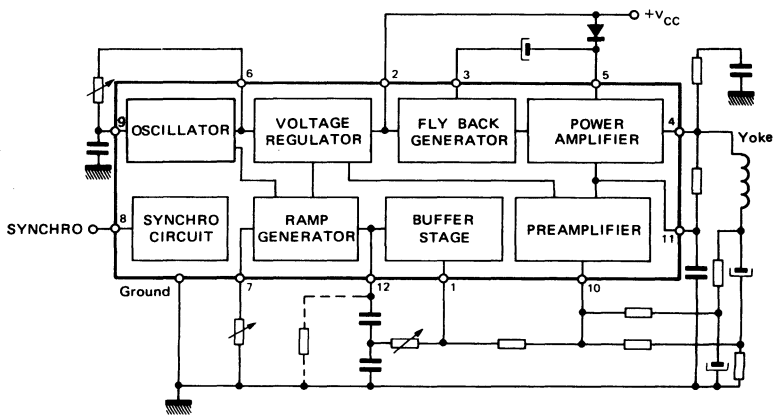
CB- 109

TDA1170 LN

CB- 155

TDA1170 LNH

TYPICAL APPLICATION CIRCUIT



NT8316-A

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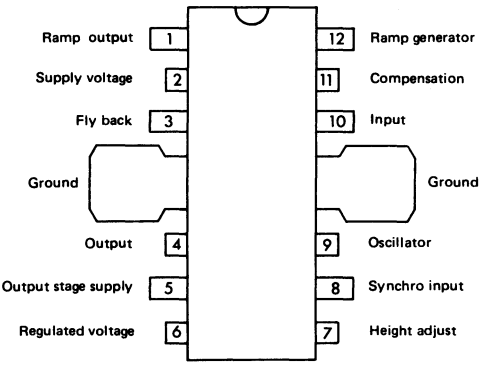
THOMSON COMPONENTS

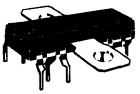
PIN CONFIGURATIONS

CASE CB-109

TDA1170 LN

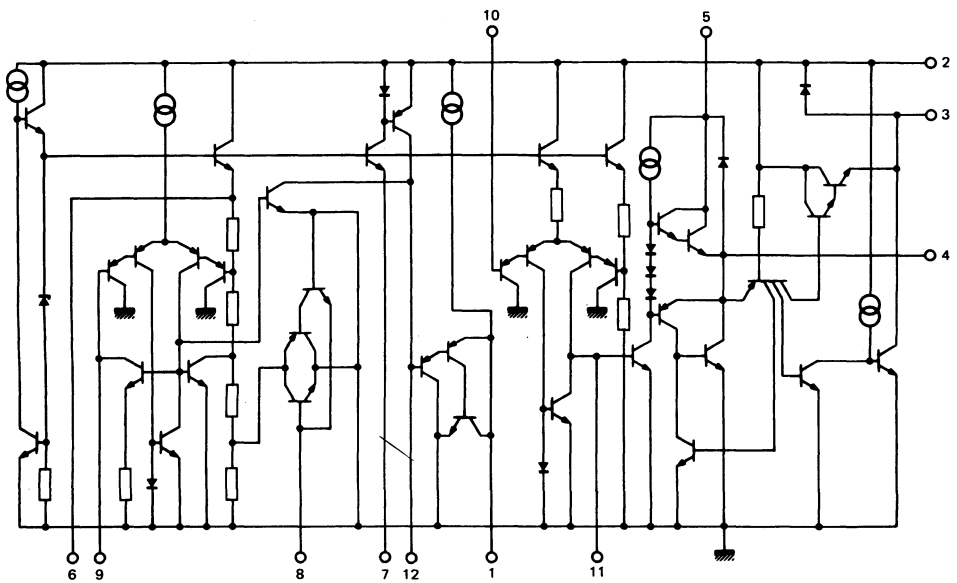


CASE CB-155



TDA1170 LNH

SCHEMATIC DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage at pin 2	V_{CC}	35	V
Fly-back peak voltage	V(4), V(5)	60	V
Power amplifier input voltage	V(10)	+10, −0.5	V
Output peak current (non repetitive) t = 2ms	I_O	2	A
Output peak current at f = 50 Hz ; t ⩽ 10 μs	I_O	2.5	A
Output peak current at f = 50 Hz ; t > 10 μs	I_O	1.5	A
Pin 3 DC current at V4 < V2	I(3)	100	mA
Pin 3 peak to peak fly-back current for f = 50 Hz and t ⩽ 1.5ms	I(3)	1.8	A
Pin 8 current	I(8)	± 20	mA
Power dissipation at $T_{tab} = 90°C$	P_{tot}	5	W
Power dissipation at $T_{amb} = 80°C$ (free air)	P_{tot}	1	W
Storage and junction temperature	T_{stg}, Tj	− 40 to 150	°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Junction-tab thermal resistance	TDA1170LN	$R_{th(j-c)}$	12	°C/W
	TDA1170LNH		10	
Junction-ambient thermal resistance	TDA1170LN	$R_{th(j-a)}$	70	°C/W
	TDA1170LNH		80	

FIGURE 1 – STATIC TEST CIRCUITS

Fig. 1 a

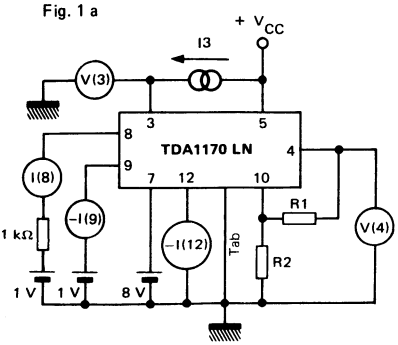


Fig. 1 b

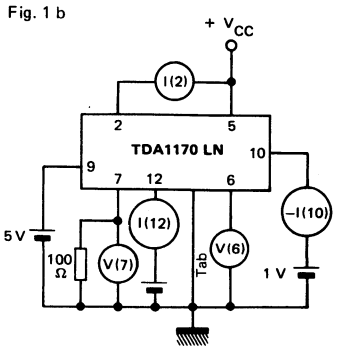


Fig. 1 c

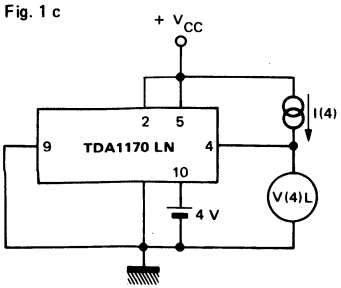
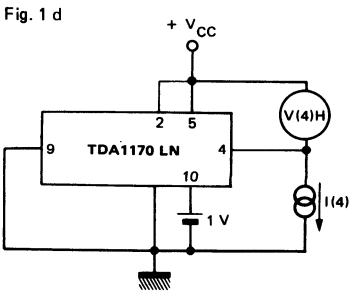


Fig. 1 d



STATIC CHARACTERISTICS

V_{CC} = 35 V, T_{amb} = 25° C, (Unless otherwise specified)

characteristic		Symbol	Min.	Typ.	Max.	Unit.
Pin 2 quiescent current (I(3) = 0)	Fig. 1b	I(2)	–	7	14	mA
Pin 5 quiescent current (I(4) = 0)	Fig. 1b	I(5)	–	8	15	mA
Oscillator bias current (V(9) = 1V)	Fig. 1a	– I(9)	–	0.1	1	μA
Amplifier input bias current (V(10) = 1V)	Fig. 1b	– I(10)	–	0.1	1	μA
Ramp generator bias current (V(12) = 0)	Fig 1a	– I(12)	–	0.02	0.3	μA
Ramp generator current (I(7) = 20 μA ; V(12) = 0)	fig 1b	–I(12)	19	20	24	μA
Ramp generator non linearity (ΔV(12) = 0 to 12 V ; I(7) = 20 μA)	Fig 1b	$\frac{\Delta I(12)}{I(12)}$	–	0.2	1	%
Supply voltage range		V_{CC}	10	–	35	V
Pin 1 saturation voltage to ground (I(1) = 1 mA)		V(1)	–	1	1.4	V
Pin 3 saturation voltage to ground (I(3) = 10 mA)	Fig. 1a	V(3)	–	1.7	2.6	V
Quiescent output voltage	Fig 1a	V(4)				V
V_{CC} = 10 V ; R(1) = 10 kΩ ; R(2) = 10 kΩ			4.15	4.4	4.6	
V_{CC} = 35 V ; R(1) = 30 kΩ ; R(2) = 10 kΩ			8.3	8.8	9.2	
Output saturation voltage to ground	Fig.1c	V(4)L				V
–I(4) = 0.1 A			–	0.9	1.2	
–I(4) = 0.8 A			–	1.9	2.3	
Output saturation voltage to supply	Fig. 1d	V(4) H				V
I(4) = 0.1 A			–	1.4	2.1	
I(4) = 0.8 A			–	2.8	3.2	
Regulated voltage at pin 6	Fig 1b	V(6)	6.1	6.5	6.9	V
Regulated voltage at pin 7 (I(7) = 20 μA)	Fig 1b	V(7)	6.2	6.6	7	V
Regulated voltage drift with supply voltage ΔV_{CC} = 10 to 35 V	Fig. 1b	$\frac{\Delta V(6)}{\Delta V_{CC}}, \frac{\Delta V(7)}{\Delta V_{CC}}$	–	1	–	mV/V
Amplifier input reference voltage		V(10)	2.07	2.2	2.3	V
Pin 8 input resistance (– V(8) ⩽ 0.4 V)	Fig. 1a	R(8)	1	–	–	MΩ

DYNAMIC CHARACTERISTICS

f = 50 Hz ; V_{CC} = 25 V (Unless otherwise specified)

characteristic		Symbol	Min	Typ	Max	Unit
Supply current (I_y = 1 Ap.p))	Fig. 2	I_{CC}	–	140	–	mA
Synchro input current (positive or negative)	Fig. 2	I(8)	500	–	–	μA
Fly back voltage (I_y = 1Ap.p)	Fig. 2	V(4)	–	51	–	V
Peak to peak output noise (Bw = 20 – 20000 Hz)	Fig. 2	V_{on}	–	–	50	mV
Fly back time (I_y = 1 Ap.p)	Fig. 2	t_{fly}	–	0.7	–	ms
Free running frequency	Fig. 2	f_o				Hz
R = 300 kΩ ; C = 100 nF			–	43.7	–	
R = 260 kΩ ; C = 100 nF			–	52.4	–	
Synchronization range (I(8) = 0.5 mA)	Fig. 2	Δf	14	–	–	Hz
Frequency drift with supply voltage V_{CC} = 10 to 35 V	Fig. 2	$\frac{\Delta f}{\Delta V_{CC}}$	–	0.005	–	Hz/V
Frequency drift with tab temperature T_{tab} = 40 to 120° C	Fig. 2	$\frac{\Delta f}{\Delta T_{tab}}$	–	0.01	–	Hz/°C

FIGURE 2 – DYNAMIC TEST CIRCUIT

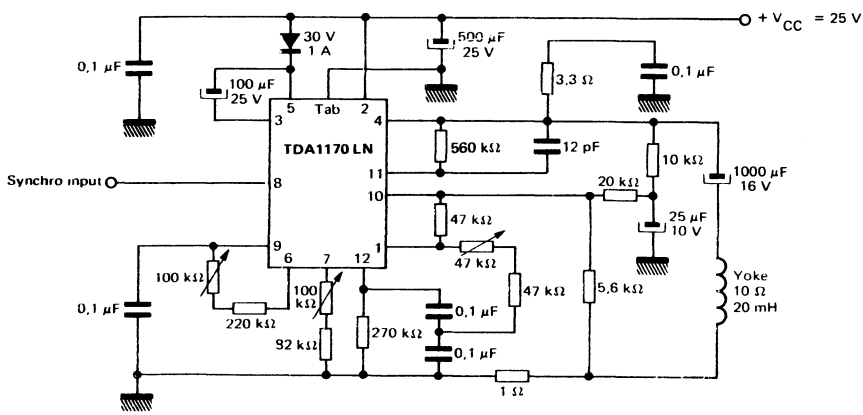
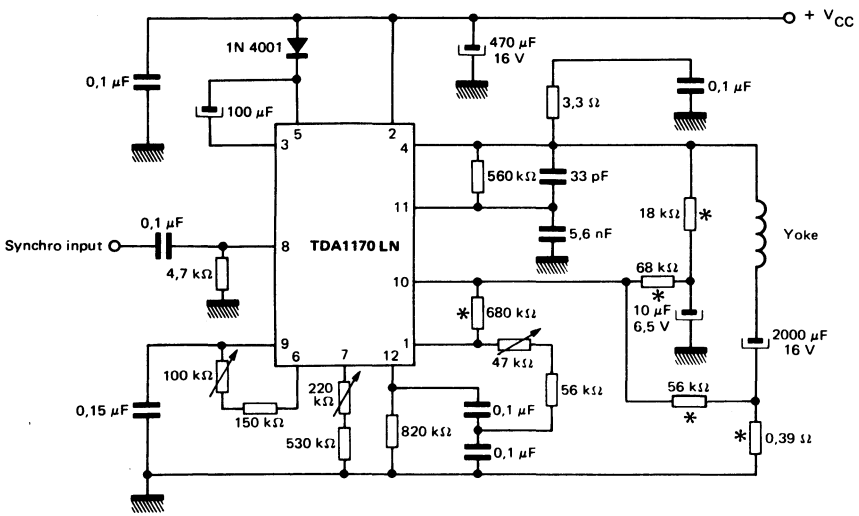


FIGURE 3 – TYPICAL APPLICATION CIRCUIT FOR SMALL SCREEN B/W TV SET

($R_Y = 2.9\ \Omega$; $L_Y = 6$ mH ; $I_Y = 1.1$ Ap.p)



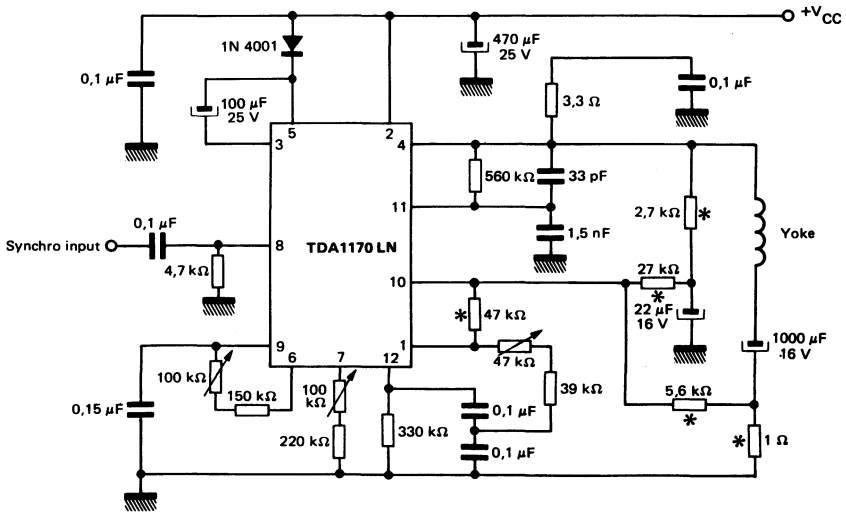
*Tolerance 5 %

TYPICAL PERFORMANCES

– Operating supply voltage	10.8 V
– Supply current	155 mA
– Fly back time	0.5 ms
– IC power dissipation	1.35 W
– Maximum scanning current (peak to peak)	1.30 Ap.p
– For safe working up to a heatsink of $R_{th} = 30°$ C/W is required	$T_{amb} = 60°C$

FIGURE 4 – TYPICAL APPLICATION CIRCUIT FOR SMALL SCREEN 90° PIL TVC SET

($R_Y = 12.5\ \Omega$; $L_Y = 31$ mH ; $I_Y = 0.8$ Ap.p)



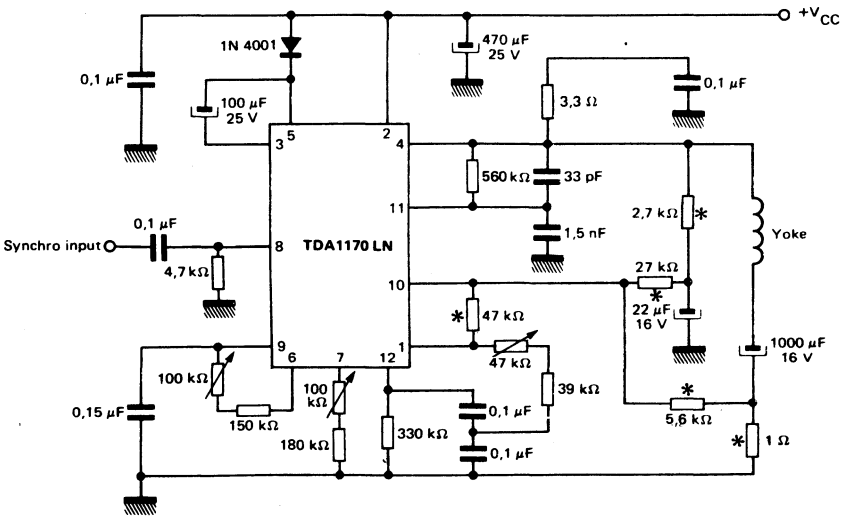
*Tolerance 5 %

TYPICAL PERFORMANCES

– Operating supply voltage	22 V
– Supply current	120 mA
– Fly back time	0.8 ms
– IC power dissipation	1.95 W
– Maximum scanning current (peak to peak)	1.0 A
– For safe working up to a heatsink of $R_{th} = 18°$ C/W is required	$T_{amb} = 60°C$

FIGURE 5 – TYPICAL APPLICATION CIRCUIT FOR LARGE SCREEN B/W TV SET

($R_Y = 10\ \Omega$; $L_Y = 20$ mH ; $I_Y = 1$ Ap.p)



* Tolerance 5 %

TYPICAL PERFORMANCES

– Operating supply voltage	22 V
– Supply current	145 mA
– Fly back time	0.7 ms
– IC power dissipation	2.3 W
– Maximum scanning current (peak to peak)	1.2 V
– For safe working up to a heatsink of $R_{th} = 14°$ C/W is required	$T_{amb} = 60°C$

THERMAL CHARACTERISTICS OF TDA1170 LN

FIGURE 6 – EXAMPLE OF TDA1170 LN WITH EXTERNAL HEATSINK

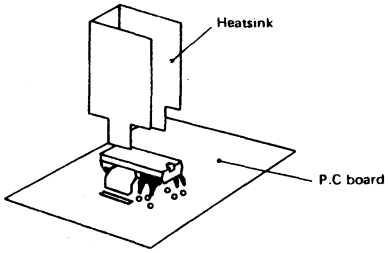
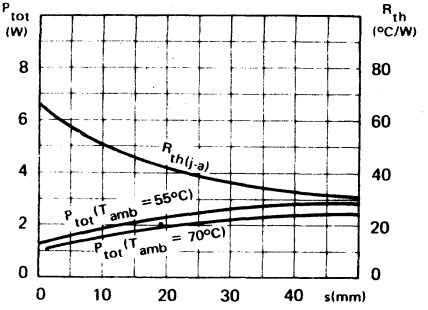
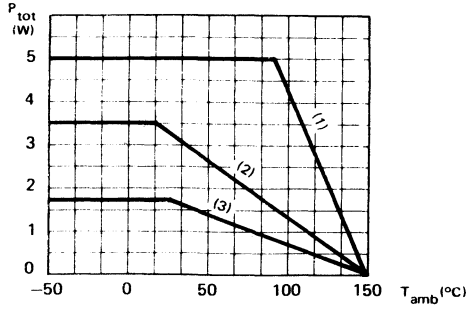


FIGURE 7 – MAXIMUM POWER DISSIPATION AND JUNCTION-AMBIENT THERMAL RESISTANCE VS. "s"



(See fig. 12)

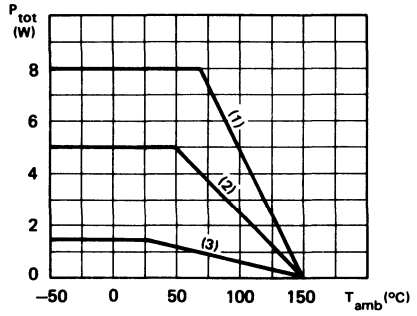
FIGURE 8 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



(1) With infinite heat sink
(2) With heat sink 25°C/W
(3) Free air

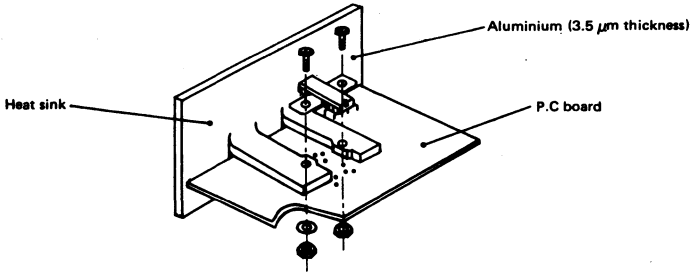
THERMAL CHARACTERISTICS OF TDA1170 LN, LNH

FIGURE 9 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



(1) With infinite heat sink
(2) With heat sink 25° C/W
(3) Free air

FIGURE 10 – MOUNTING EXAMPLE



MOUNTING INSTRUCTIONS

During soldering the tab temperature must not exceed 260° C and the soldering time must not be longer than 12 seconds.

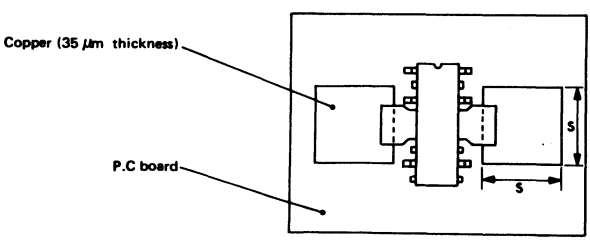
The external heatsink or printed circuit copper area must be connected to electrical ground.

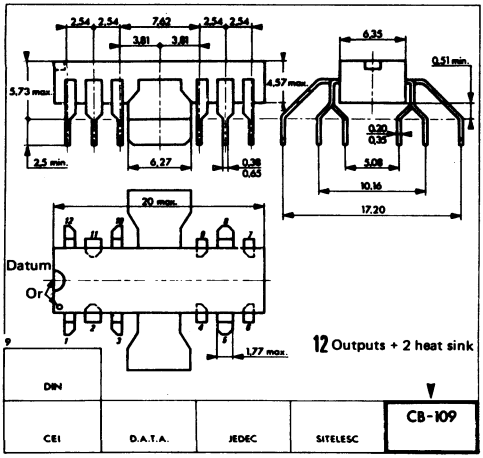
TDA1170 LN

The junction to ambient thermal resistance of the TDA1170 LN can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 11) or to an external heatsink (fig. 6).

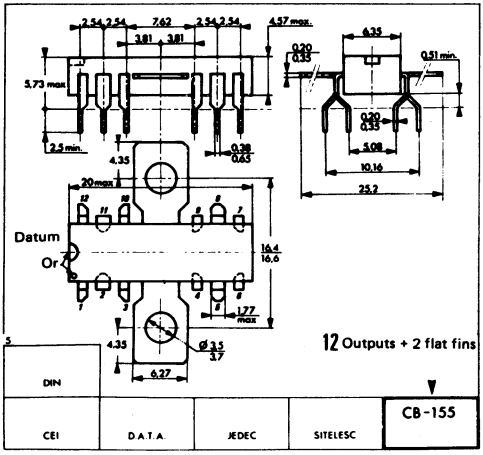
The diagram of fig. 7 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "S" of two equal square copper areas having a thickness of 35 μ (1.4 mil).

FIGURE 11 – EXAMPLE OF P.C BOARD COPPER AREA USED AS HEATSINK

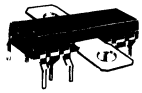




CASE / CB- 109



CASE / CB- 155



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

TDA1170S TDA1170SH

TV VERTICAL DEFLECTION SYSTEM

The TDA 1170 S, SH is a silicon monolithic integrated circuit in a 12 lead dual in line plastic package. It is intended for use in black and white and colour TV receivers.

The functions incorporated are:

- synchronization circuit
- oscillator and ramp generator
- high power gain amplifier
- fly back generator
- voltage stabilizer.
- Max supply voltage 35 V
- Max fly back voltage 60 V
- Max peak to peak deflecting current 50 Hz 1.5 A

TV VERTICAL DEFLECTION SYSTEM

2

CASES

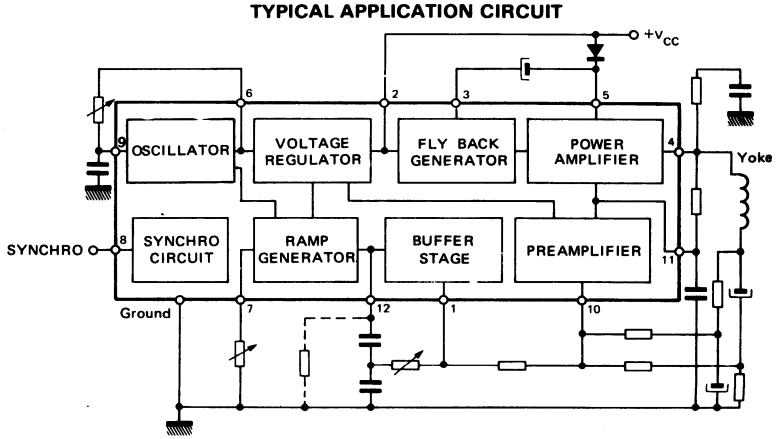
CB- 109

TDA 1170 S

CB- 155

TDA 1170 SH

TYPICAL APPLICATION CIRCUIT

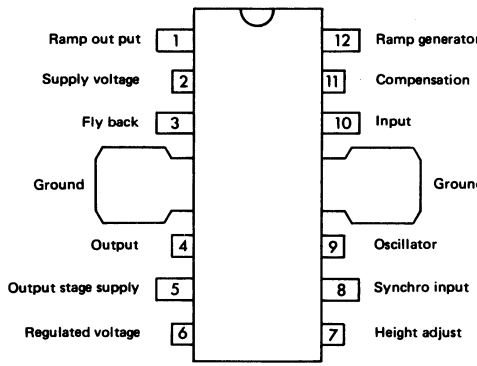


NT8150-A

PIN CONFIGURATIONS

CASE CB-109

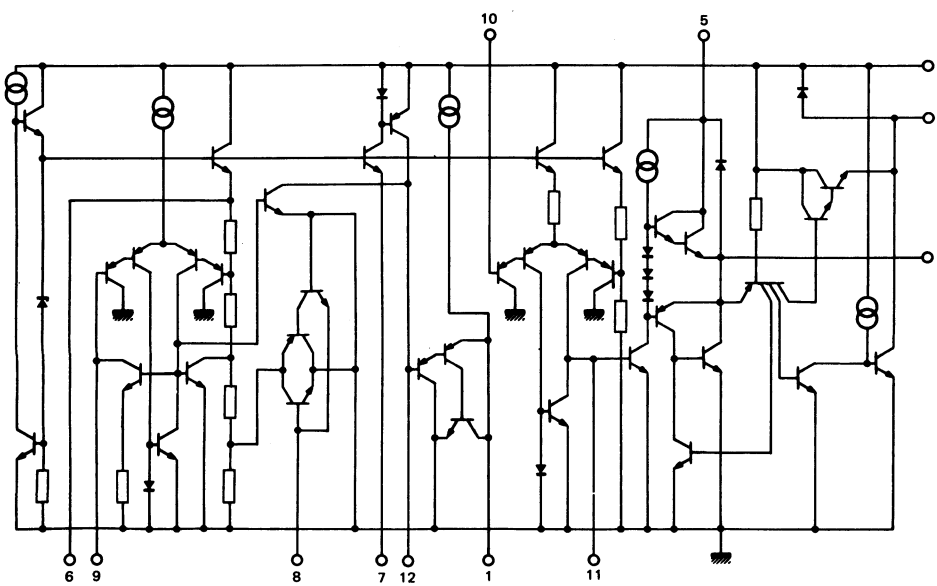
TDA1170 S



CASE CB-155

TDA1170 SH

SCHEMATIC DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage at pin 2	V_{CC}	35	V
Fly-back peak voltage	V(4), V(5)	60	V
Power amplifier input voltage	V(10)	+10, −0.5	V
Output peak current (non repetitive) t = 2ms	I_O	2	A
Output peak current at f = 50 Hz ; t ⩽ 10 µs	I_O	2.5	A
Output peak current at f = 50 Hz ; t > 10 µs	I_O	1.5	A
Pin 3 DC current at V4 < V2	I(3)	100	mA
Pin 3 peak to peak fly-back current for f=50 Hz and t⩽1.5ms	I(3)	1.8	A
Pin 8 current	I(8)	± 20	mA
Power dissipation at $T_{tab} = 90°C$	P_{tot}	5	W
Power dissipation at $T_{amb} = 80°C$ (free air)	P_{tot}	1	W
Storage and junction temperature	T_{stg}, Tj	− 40 to 150	°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Junction-tab thermal resistance	TDA1170S	$R_{th(j-c)}$	12	°C/W
	TDA1170SH		10	
Junction-ambient thermal resistance	TDA1170S	$R_{th(j-a)}$	70	°C/W
	TDA1170SH		80	

FIGURE 1 – STATIC TEST CIRCUITS

Fig. 1 a

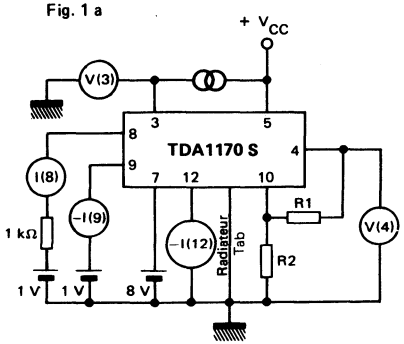


Fig. 1 b

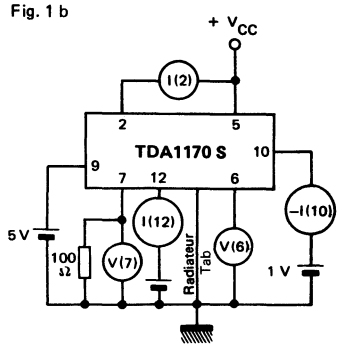


Fig. 1 c

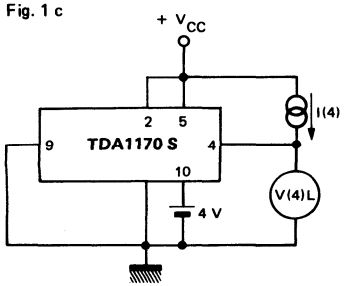
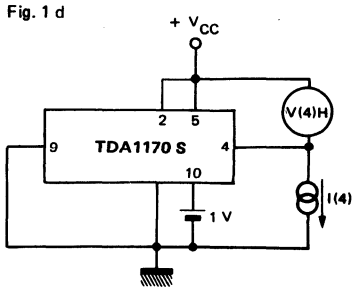


Fig. 1 d



STATIC CHARACTERISTICS

V_{CC} = 35 V, T_{amb} = 25° C, (Unless otherwise specified)

characteristic		Symbol	Min.	Typ.	Max.	Unit.
Pin 2 quiescent current (I(3) = 0)	Fig. 1b	I(2)	–	7	14	mA
Pin 5 quiescent current (I(4) = 0)	Fig. 1b	I(5)	–	8	15	mA
Oscillator bias current (V(9) = 1V)	Fig. 1a	– I(9)	–	0.1	1	μA
Amplifier input bias current (V(10) = 1V)	Fig. 1b	– I(10)	–	0.1	1	μA
Ramp generator bias current (V(12) = 0)	Fig. 1a	– I(12)	–	0.02	0.3	μA
Ramp generator current (I(7) = 20 μA ; V(12) = 0)	fig 1b	–I(12)	19	20	24	μA
Ramp generator non linearity (ΔV(12) = 0 to 12 V ; I(7) = 20 μA)	Fig 1b	$\frac{\Delta I(12)}{I(12)}$	–	0.2	1	%
Supply voltage range		V_{CC}	10	–	36	V
Pin 1 saturation voltage to ground (I(1) = 1 mA)		V(1)	–	1	1.4	V
Pin 3 saturation voltage to ground (I(3) = 10 mA)	Fig. 1a	V(3)	–	1.7	2.6	V
Quiescent output voltage	Fig 1a	V(4)				V
V_{CC} = 10 V ; R(1) = 10 kΩ ; R(2) = 10 kΩ			4.15	4.4	4.6	
V_{CC} = 35 V ; R(1) = 30 kΩ ; R(2) = 10 kΩ			8.3	8.8	9.2	
Output saturation voltage to ground	Fig.1c	V(4)L				V
–I(4) = 0.1 A			–	0.9	1.2	
–I(4) = 0.8 A			–	1.9	2.3	
Output saturation voltage to supply	Fig. 1d	V(4) H				V
I(4) = 0.1 A			–	1.4	2.1	
I(4) = 0.8 A			–	2.8	3.2	
Regulated voltage at pin 6	Fig 1b	V(6)	6.1	6.5	6.9	V
Regulated voltage at pin 7 (I(7) = 20 μA)	Fig 1b	V(7)	6.2	6.6	7	V
Regulated voltage drift with supply voltage ΔV_{CC} = 10 to 35 V	Fig. 1b	$\frac{\Delta V(6)}{\Delta V_{CC}} \cdot \frac{\Delta V(7)}{\Delta V_{CC}}$	–	1	–	mV/V
Amplifier input reference voltage		V(10)	2.07	2.2	2.3	V
Pin 8 input resistance (– V(8) ≤ 0.4 V)	Fig. 1a	R(8)	1	–	–	MΩ

DYNAMIC CHARACTERISTICS

f = 50 Hz ; V_{CC} = 25 V (Unless otherwise specified)

characteristic		Symbol	Min	Typ	Max	Unit
Supply current (I_y = 1 Ap.p))	Fig. 2	I_{CC}	–	140	–	mA
Synchro input current (positive or negative)	Fig. 2	I(8)	500	-	–	μA
Fly back voltage (I_y = 1Ap.p)	Fig. 2	V(4)	–	51	–	V
Peak to peak oscillator sawtooth voltage	Fig. 2	V(9)	–	2.4	–	V
Fly back time (I_y = 1 Ap.p)	Fig. 2	t_{fly}	–	0.7	–	ms
Free running frequency	Fig. 2	f_o				Hz
R = 300 kΩ ; C = 100 nF			–	43.7	–	
R = 360 kΩ ; C = 100 nF			–	52.4	–	
Synchronization range (I(8) = 0.5 mA)	Fig. 2	Δf	14	–	–	Hz
Frequency drift with supply voltage V_{CC} = 10 to 35 V	Fig. 2	$\frac{\Delta f}{\Delta V_{CC}}$	–	0.005	–	Hz/V
Frequency drift with tab temperature T_{tab} = 40 to 120° C	Fig. 2	$\frac{\Delta f}{\Delta T_{tab}}$	–	0.01	–	Hz/°C

FIGURE 2 – DYNAMIC TEST CIRCUIT

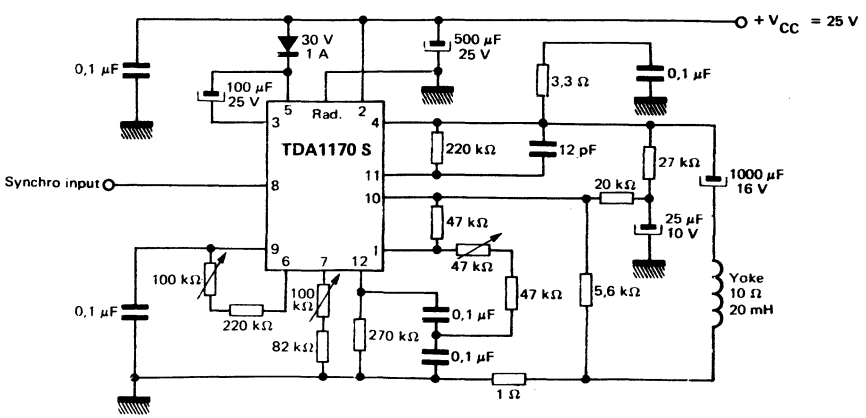
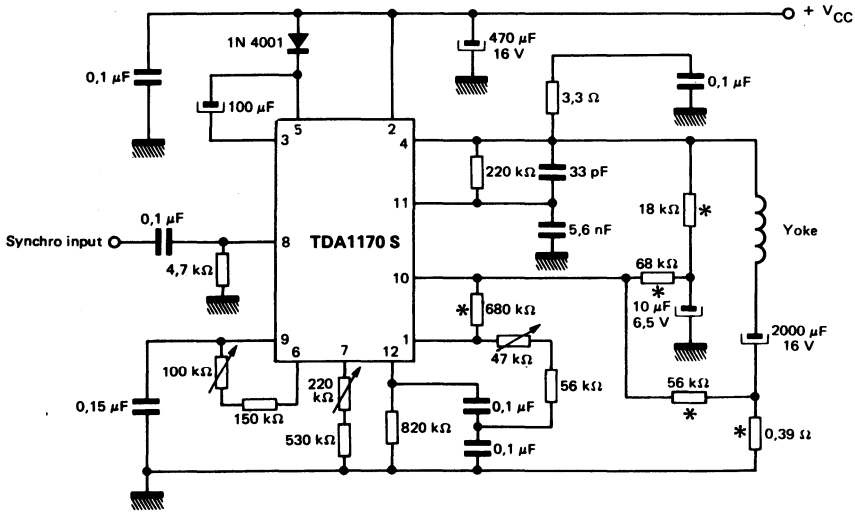


FIGURE 3 – TYPICAL APPLICATION CIRCUIT FOR SMALL SCREEN B/W TV SET

($R_Y = 2.9\ \Omega$; $L_Y = 6$ mH ; $I_Y = 1.1$ Ap.p)



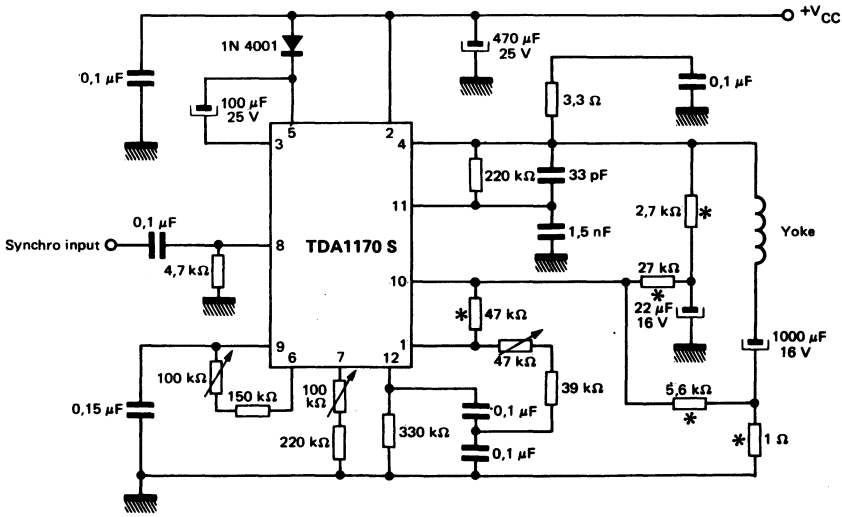
*Tolerance 5 %

TYPICAL PERFORMANCES

– Operating supply voltage	10.8 V
– Supply current	155 mA
– Fly back time	0.5 ms
– IC power dissipation	1.35 W
– Maximum scanning current (peak to peak)	1.30 Ap.p
– For safe working up to a heatsink of $R_{th} = 30°$ C/W is required	$T_{amb} = 60°C$

FIGURE 4 – TYPICAL APPLICATION CIRCUIT FOR SMALL SCREEN 90° PIL TVC SET

($R_Y = 12.5\ \Omega$; $L_Y = 31$ mH ; $I_Y = 0.8$ Ap.p)



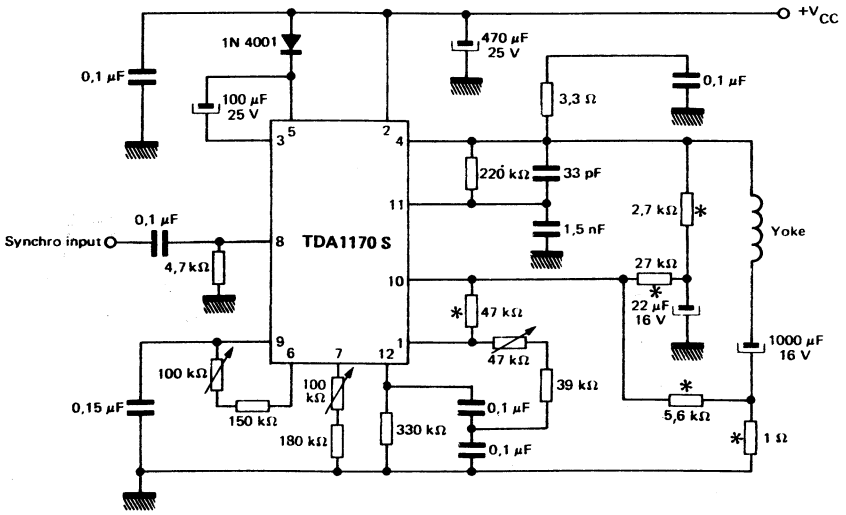
*Tolerance 5 %

TYPICAL PERFORMANCES

– Operating supply voltage	22 V
– Supply current	120 mA
– Fly back time	0.8 ms
– IC power dissipation	1.95 W
– Maximum scanning current (peak to peak)	1.0 A
– For safe working up to a heatsink of $R_{th} = 18°$ C/W is required	$T_{amb} = 60°C$

FIGURE 5 – TYPICAL APPLICATION CIRCUIT FOR LARGE SCREEN B/W TV SET

($R_Y = 10\ \Omega$; $L_Y = 20$ mH ; $I_Y = 1$ Ap.p)



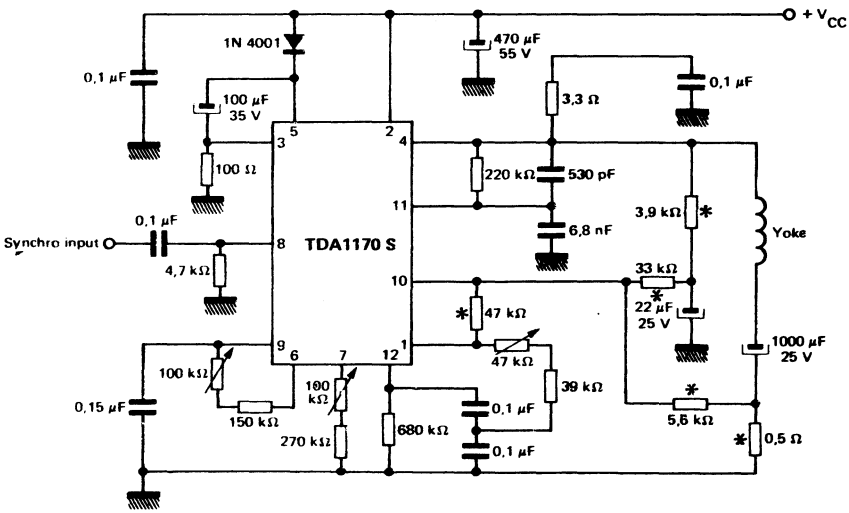
*Tolerance 5 %

TYPICAL PERFORMANCES

– Operating supply voltage	22 V
– Supply current	145 mA
– Fly back time	0.7 ms
– IC power dissipation	2.3 W
– Maximum scanning current (peak to peak)	1.2 V
– For safe working up to a heatsink of $R_{th} = 14$ °C/W is required	$T_{amb} = 60$°C

FIGURE 6 – TYPICAL APPLICATION CIRCUIT FOR LARGE SCREEN 110° PIL TVC SET

(R_Y = 1.0 Ω ; L_Y = 25 mH ; I_Y = 1.25 Ap.p)



*Tolerance 5 %

TYPICAL PERFORMANCES

– Operating supply voltage	25 V
– Supply current	175 mA
– Fly back time	1 ms
– IC power dissipation	3.25 W
– Maximum scanning current (peak to peak)	1.4 Ap.p
– For safe working up to a heatsink of R_{th} = 8.5° C/W is required	T_{amb} = 60°C

THERMAL CHARACTERISTICS OF TDA1170 S

FIGURE 7 – EXAMPLE OF TDA1170 S WITH EXTERNAL HEATSINK

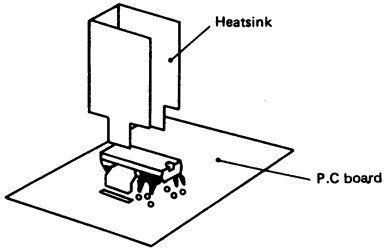
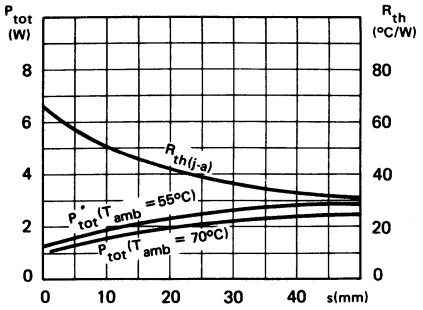
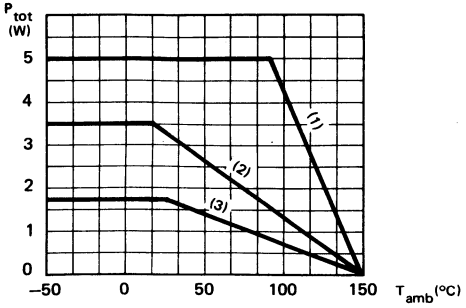


FIGURE 8 – MAXIMUM POWER DISSIPATION AND JUNCTION-AMBIENT THERMAL RESISTANCE VS. "s"



(See fig. 12)

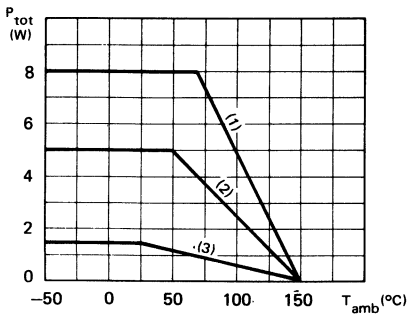
FIGURE 9 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



(1) With infinite heat sink
(2) With heat sink 25°C/W
(3) Free air

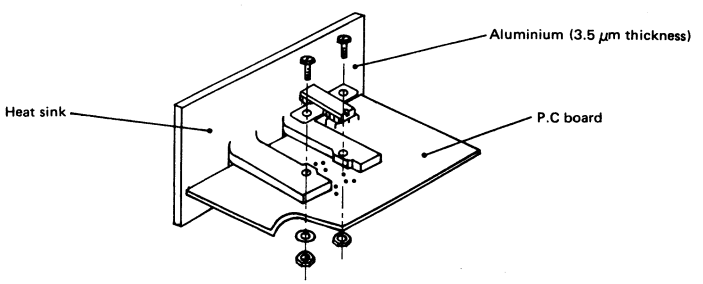
THERMAL CHARACTERISTICS OF TDA1170 SH

FIGURE 10 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



(1) With infinite heat sink
(2) With heat sink 25° C/W
(3) Free air

FIGURE 11 – MOUNTING EXAMPLE



MOUNTING INSTRUCTIONS

During soldering the tab temperature must not exceed 260° C and the soldering time must not be longer than 12 seconds.

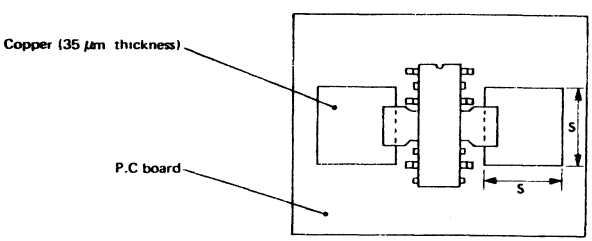
The external heatsink or printed circuit copper area must be connected to electrical ground.

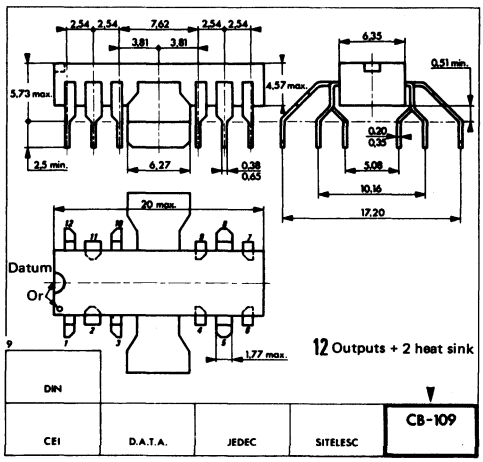
TDA1170 S

The junction to ambient thermal resistance of the TDA1170 S can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 12) or to an external heatsink (fig. 7).

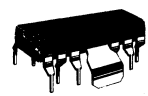
The diagram of fig. 8 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "S" of two equal square copper areas having a thickness of 35 μ (1.4 mil).

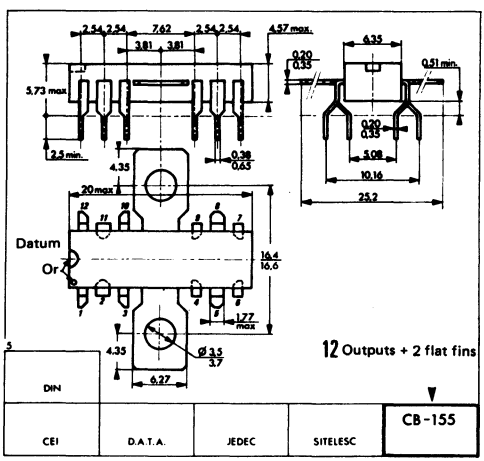
FIGURE 12 – EXAMPLE OF P.C BOARD COPPER AREA USED AS HEATSINK



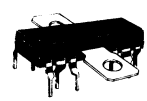


CASE / CB- 109





CASE / CB- 155



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TDA2540
TDA2541

IF AMPLIFIER WITH DEMODULATOR AND AFC
AMPLI FI TELEVISION AVEC DEMODULATEUR ET CAF

The TDA2540 and 2541 are IF amplifier and A.M. demodulator circuits for colour and black and white television receivers using PNP or NPN tuners. They are intended for reception of negative or positive modulation CCIR standard.

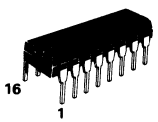
Les TDA2540 et 2541 sont des amplificateurs FI et démodulateurs AM pour les récepteurs TV équipés de tuner PNP ou NPN. Ils sont prévus pour la réception des standards CCIR à modulation négative ou positive.

They incorporate the following functions / Ils comprennent les fonctions suivantes :

- **Gain controlled amplifier** / Ampli à gain commandé
- **Synchronous demodulator** / Démodulateur synchrone
- **White spot inverter** / Inverseur de parasites
- **Video preamplifier with noise protection** / Préampli vidéo avec protection contre le bruit
- **Switchable AFC** / Circuit CAF déconnectable
- **AGC with noise gating** / CAG avec porte de bruit
- **Tuner AGC output (NPN tuner for 2540)-(PNP tuner for 2541)** / Sortie CAG pour la partie HF. (tuner NPN pour 2540)-(tuner PNP pour 2541)
- **Provision for video output inhibition (VCR play back)** / Inhibition possible de la sortie vidéo (reproduction VCR)
- **Supply voltage** / Tension d'alimentation **12 V typ.**
- **Supply current** / Courant d'alimentation **50 mA typ.**
- **I.F. input voltage at** / Tension d'entrée FI à : **f = 38.9 MHz ; 100 μ V_{eff} typ.**
- **Video output voltage** / Tension de sortie vidéo **3 Vpp typ.**
- **I.F. voltage gain control range** / Plage de contrôle du gain en tension FI **64 dB typ.**
- **Signal to noise ratio at** / Rapport signal/bruit à : **V_I = 10 mV ; 58 dB typ.**
- **A.F.C. output voltage swing for** / Excursion de la tension de c.a.f. en sortie pour : **Δf = 100 kHz ; 10 V min.**

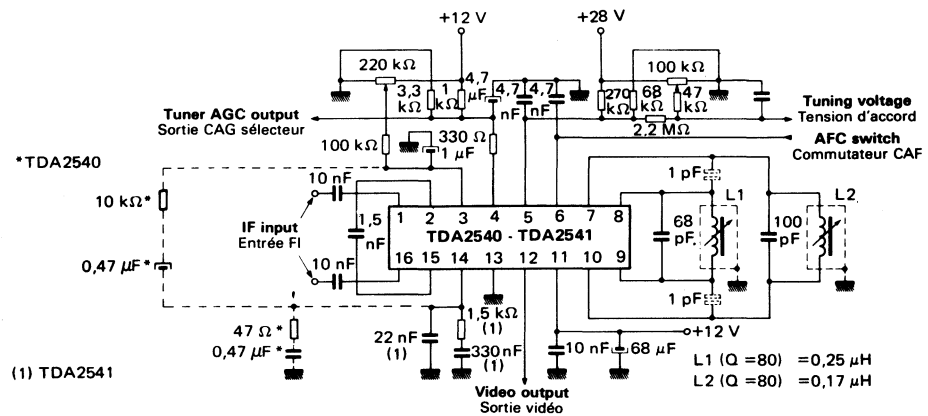
IF AMPLIFIER WITH DEMODULATOR AND AFC
AMPLI FI TELEVISION AVEC DEMODULATEUR ET CAF

CASE / BOITIER **CB-79**



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE

APPLICATION CIRCUIT
SCHEMA D'APPLICATION



NT8148

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

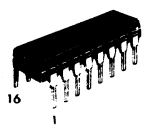
VALEURS LIMITES ABSOLUES
ABSOLUTE MAXIMUM RATINGS

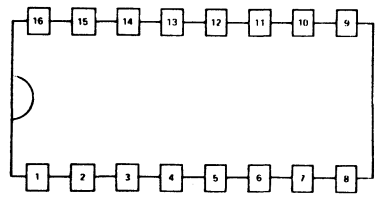
(limites absolues selon publication CEI 134)
(According to IEC 134 regulation)

Tension d'alimentation Supply voltage	max.	V(11-13)	13,8	V
Tension de c.a.g. du sélecteur Tuner a.g.c voltage	max.	V(4-13)	12	V
Puissance dissipée Power dissipation	max.	P_{tot}	900	mW
Température de stockage Storage temperature	min. max.	T_{stg}	−55 +125	°C °C
Température ambiante de fonctionnement Operating ambient temperature	min. max.	T_{amb}	−25 +60	°C °C

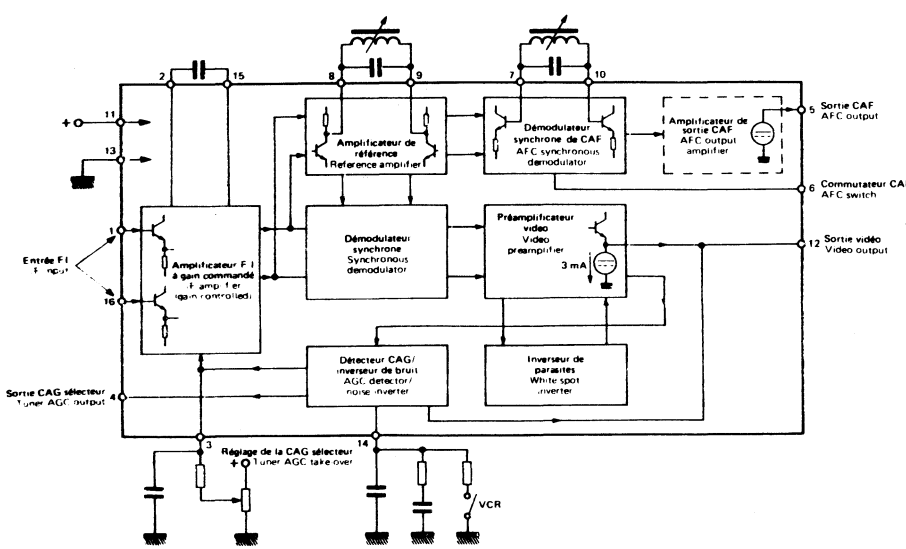
BROCHAGE (Vue de dessus)
PIN CONFIGURATION (Top view)

BOITIER **CB-79**
Case





SCHEMA BLOC
BLOCK DIAGRAM



CARACTERISTIQUES ELECTRIQUES
ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C ; V(11-13) = 12 V ; f = 38,9 MHz

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITIONS	MIN	TYP	MAX.	UNITES UNITS
Gamme de tension d'alimentation Supply voltage range	V(11-13)		10,2	12	13,8	V
Courant d'alimentation Supply current	I_{11}		42	50	60	mA
Tension d'entrée FI au début de c.a.g IF input voltage for onset of a.g.c	$V(1\text{-}16)_{eff}$	f = 38,9 MHz	60	85	180	µV
Tension d'entrée maximum Max input voltage				140		mV
Tension de sortie vidéo Video output voltage	V(12-13)			3		Vpp
Impédance d'entrée différentielle Differential input impedance	Z(1-16)			2 kΩ en parallèle avec 2 pF 2 kΩ in parallel with 2 pF		
Niveau de sortie en l'absence du signal Zero signal output level	V(12-13)		5,7	6	6,3	V
Niveau du fond de synchro en sortie Top synchro output level	V(12-13)		2,9	3,07	3,2	V
Variation de la tension de sortie de CAF AFC output voltage swing	V(5-13)	Δf = 100 kHz	10	11		V
Plage de commande de la CAG - FI IF voltage gain control range	ΔG_v		52	64		dB
Rapport signal/bruit (1) Signal to noise ratio	S_N	V_I = 10 mV	50	58		dB
Bande passante de l'amplificateur vidéo (à – 3 dB) Bandwidth of video amplifier (–3 dB)	B			6		MHz
Gain différentiel Differential gain	G			4	10	%
Phase différentielle Differential phase	ϕ			2	10	%
Résidu de porteuse à la sortie vidéo Carrier signal at video output	V(12-13)RMS	V_I = 10 mV		4	10	mV
Résidu d'harmonique 2 à la sortie vidéo 2nd harmonic of carrier at video output	V(12-13)RMS	V_I = 10 mV		20	40	mV
Variation de la fréquence déterminant une excursion de la tension de sortie CAF de 10 V Change of frequency at AFC output voltage swing of 10 V	Δf			100	200	kHz
Intermodulation à 1,1 MHz (bleu) (2) Intermodulation at 1,1 MHz (blue)			46	60		dB
Intermodulation à 1,1 MHz (jaune) (2) Intermodulation at 1,1 MHz (yellow)			46	50		dB
Intermodulation à 3,3 MHz (3) Intermodulation at 3,3 MHz			46	54		dB
Niveau de coupure du CAF (CAF hors service = niveau bas) AFC switches off (AFC = low level)	V(6-13)				2,5	V

CARACTERISTIQUES ELECTRIQUES (suite)
ELECTRICAL CHARACTERISTICS (continued)

Note 1 : Voir figure 1
See waveform 1

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITIONS	MIN.	TYP.	MAX.	UNITES UNITS
Niveau de coupure de la sortie vidéo (VCR = niveau bas) VCR switches off (VCR = low level)	V(14-13)				1,1	V
Seuil d'action de l'inverseur de parasites blancs White spot inverter threshold level (note 1)				6,6		V
Niveau d'insertion de l'inverseur de parasites White spot insertion level (note 1)				4,7		V
Seuil d'action de l'inverseur de bruit Noise inverter threshold level (note 1)				1,8		V
Niveau d'insertion de l'inverseur de bruit (note 1) Noise insertion level				3,8		V
Gamme du courant de sortie CAG sélecteur Tuner AGC output current range	I(4)			0 → 10		mA
Tension de sortie CAG sélecteur Tuner AGC output voltage	V(4-13)	I(4) = 10 mA			0,3	V
Courant de fuite à la sortie CAG sélecteur Tuner AGC output leakage current	I(4)	TDA 2541 V(14-13) = 11V V(4-13) = 12V TDA 2540 V(14-13) = 3V V(4-13) = 12V			15	µA

(1) $S/N = \dfrac{V_O \text{ (noir à blanc) (black to white)}}{V_n \text{ typ. eff. à r.m.s at } B = 5 \text{ MHz}}$ dB

(2) $20 \log. \left(\dfrac{V_O \text{ à at } 4,4 \text{ MHz}}{V_O \text{ à at } 1,1 \text{ MHz}}\right) + 3,6$ dB

(3) $20 \log. \dfrac{V_O \text{ à at } 4,4 \text{ MHz}}{V_O \text{ à at } 3,3 \text{ MHz}}$

Fig. 1 – SIGNAL DE SORTIE VIDEO AVEC LES SEUILS D'ACTION DES INVERSEURS DE PARASITES ET DE BRUIT
VIDEO OUTPUT WAVEFORM SHOWING WHITE SPOT AND NOISE INVERTER THRESHOLD LEVELS

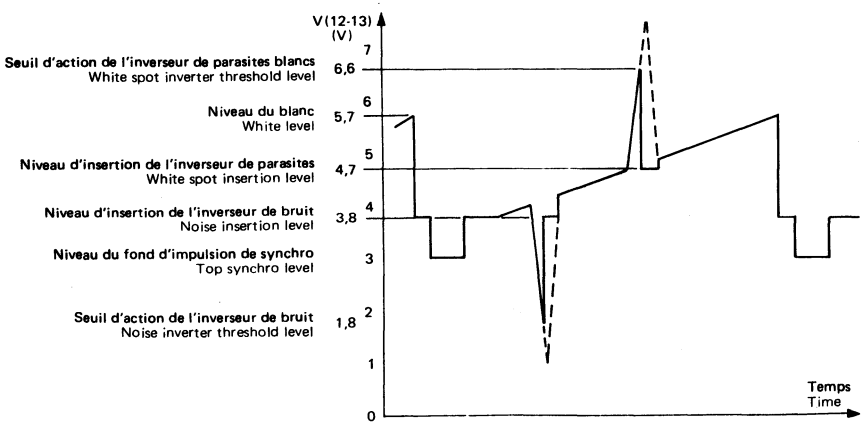
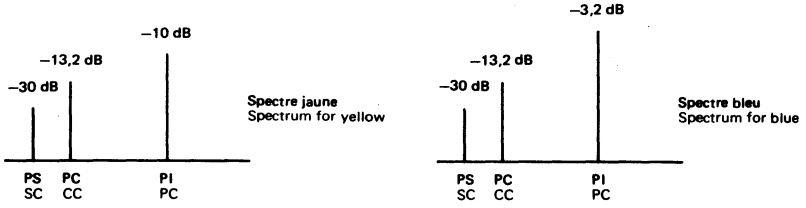


Fig. 2 – CONDITIONS D'ENTREE POUR LES MESURES D'INTERMODULATION
INPUT CONDITIONS FOR INTERMODULATION MEASUREMENTS

Barres couleurs standard (75 % contraste - standard CCIR - système PAL)
Standard colour bar with 75 % contrast



PS : Niveau de la porteuse son (FM)
SC : Sound carrier level

PC : Niveau de la porteuse chrominance
CC : Chrominance carrier level

PI : Niveau de la porteuse image
PC : Picture carrier level

Par rapport au niveau du fond de synchronisation
With respect to top synchro level

Fig. 3 – CIRCUIT DE MESURE D'INTERMODULATION
TEST SET-UP FOR INTERMODULATION

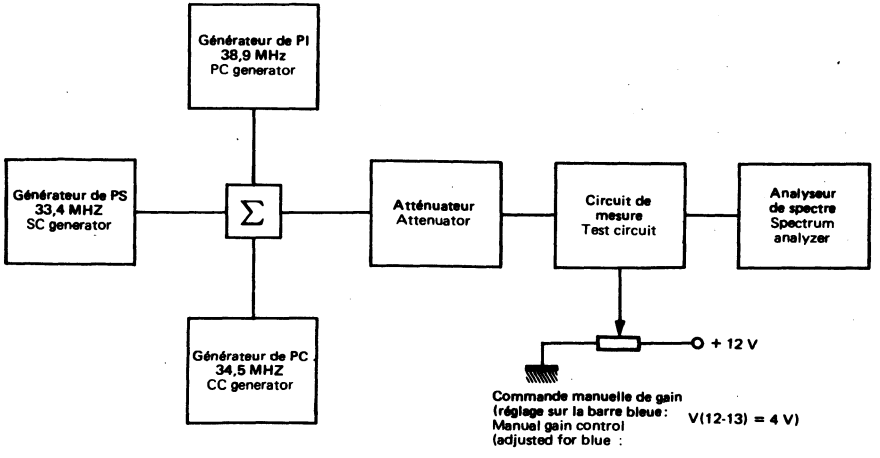


Fig. 4 – TENSION DE SORTIE CAF V(5-13) EN FONCTION DE LA FREQUENCE
AFC VOLTAGE VERSUS FREQUENCY V(5-13)

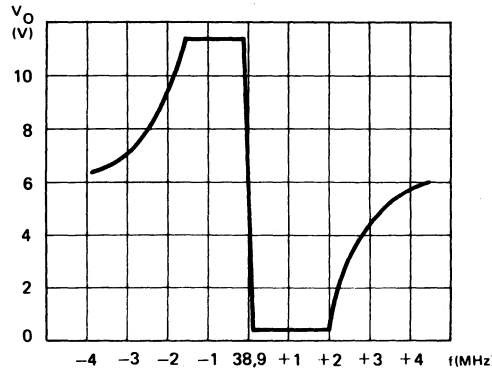


Fig. 5 – TENSION DE SORTIE CAF V(5-13) EN FONCTION DE LA FREQUENCE
AFC VOLTAGE VERSUS FREQUENCY V(5-13)

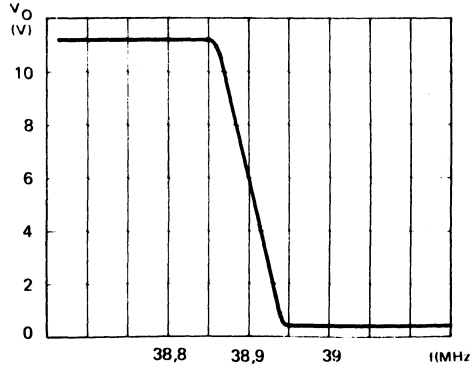
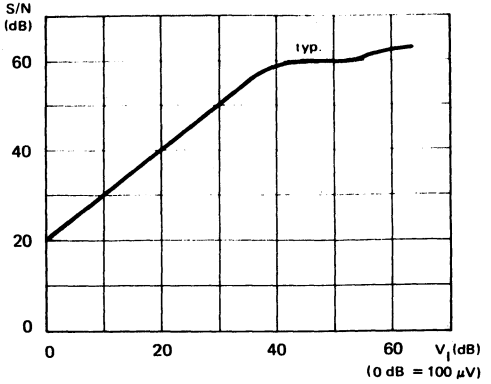
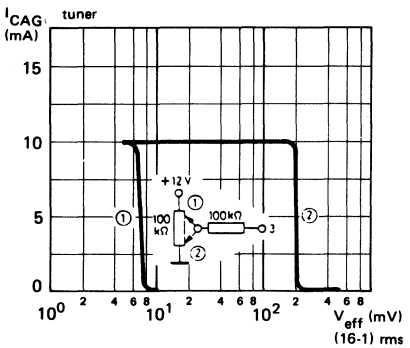


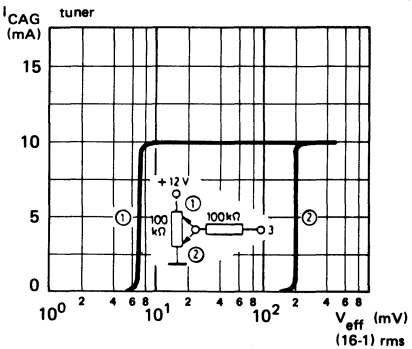
Fig. 6 – RAPPORT SIGNAL/BRUIT EN FONCTION DE LA TENSION D'ENTREE V(1-16)
SIGNAL/NOISE RATIO VERSUS INPUT VOLTAGE V(1-16)



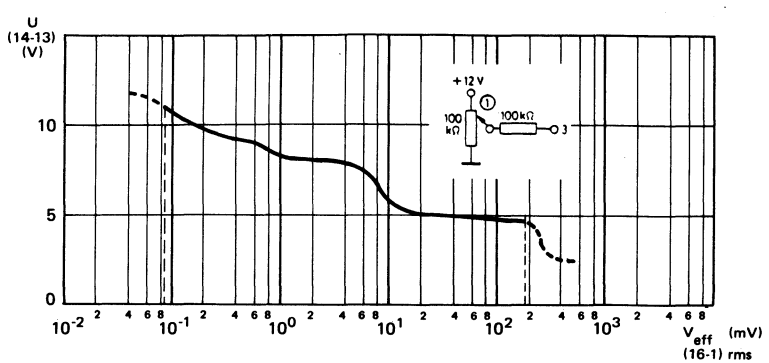
TDA 2540



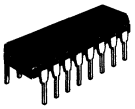
TDA 2541



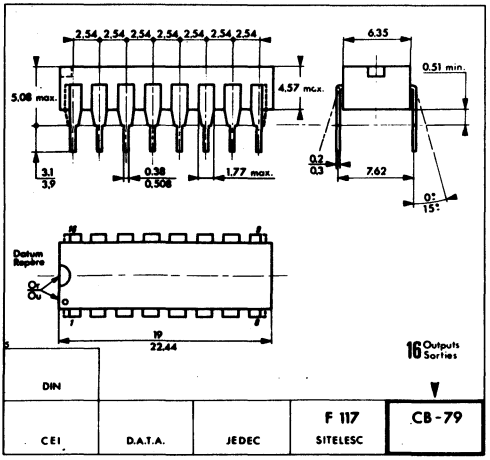
TDA 2540 – TDA 2541



CASE / BOITIER CB-79



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TDA2542

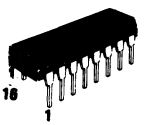
IF AMPLIFER WITH DEMODULATOR AND AFC

The TDA 2542 is an IF amplifier and AM demodulator circuit for colour and black and white television receivers using PNP tuners. It is intended to reception positive modulation for french standard.
It incorporates the following functions

- Gain controlled amplifier
- Synchronous demodulator
- Video preamplifier
- Switchable AFC
- AGC
- Tuner AGC output (PNP tuner)
- Supply voltage 12 V typ.
- Supply current 50 mA typ.
- IF input voltage at f = 32.7 MHz ; 100 μV_{eff} typ.
- Video output voltage 3 Vpp typ.
- IF voltage gain control range 64 dB typ.
- Signal to noise ratio at V_I = 10 mV ; 58 dB typ.
- A.F.C. output voltage swing for Δf = 100 kHz 10 V min.

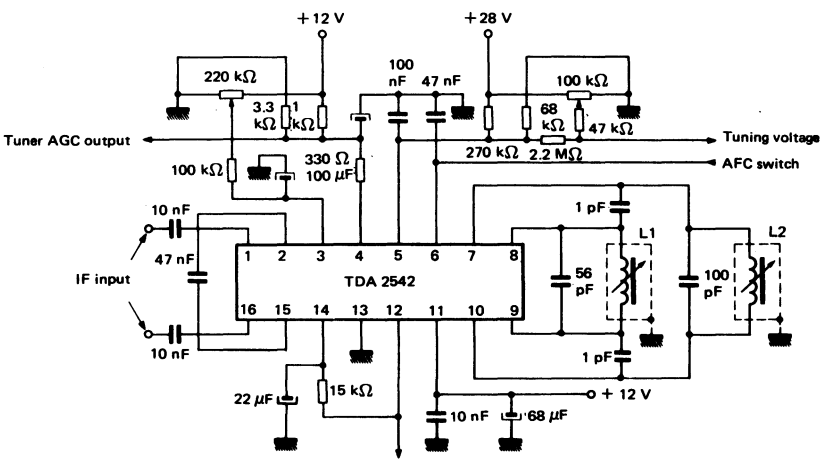
IF AMPLIFIER WITH DEMODULATOR AND AFC

CASE CB-79



DP SUFFIX
PLASTIC PACKAGE

APPLICATION CIRCUIT

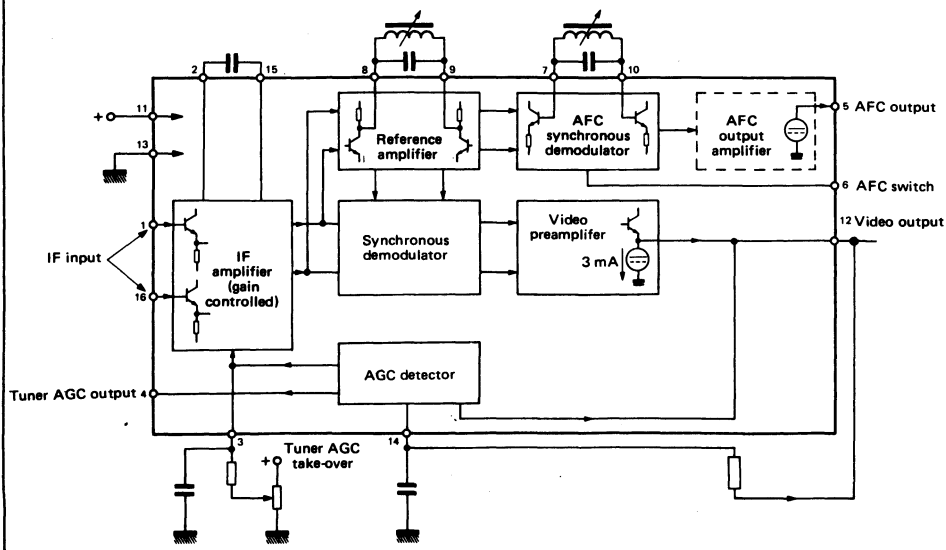


NT8148-A

MAXIMUM RATINGS (According to IEC regulation)

Rating	Symbol	Value	Unit
Supply voltage	V(11-13)	13.8	V
Tuner a.g.c. voltage	V(4-13)	12	V
Power dissipation	P_{tot}	900	mW
Storage temperature	T_{stg}	- 55 to + 125	°C
Operating ambient temperature	T_{oper}	- 25 to + 60	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

$T_{amb} = 25°C$; V(11-13) = 12 V ; f = 32.7 MHz

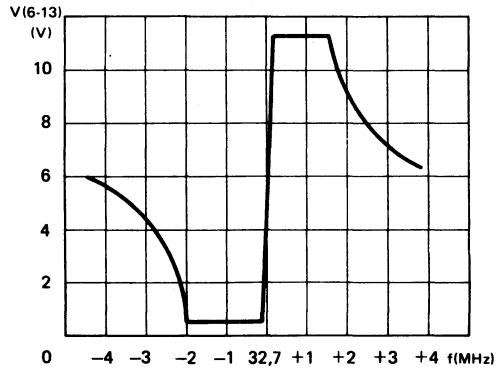
characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage range	V(11-13)	10.2	12	13.8	V
Supply current	I(11)	40	50	58	mA
IF input voltage for onset of a.g.c. (f = 32.7 MHz)	$V(1.16)_{eff}$	–	85	160	μV
Max input voltage	–	–	140	–	mV
Video output voltage	V(12-13)	–	3	–	V_{pp}
Differential input impedance (2kΩ in parallel with 2pF)	Z (1-16)	–	2	–	kΩ
Zero signal output level	V(12-13)	–	2.9	–	V
AFC output voltage swing (Δf = 100 KHz)	V(5-13)	10	11	–	V
IF voltage gain control range	ΔG_V	58	64	–	dB
Signal to noise ratio (1) (V_I = 10 mV)	S_N	50	58	–	dB
Bandwidth of video amplifier (-3 dB)	B	5	6	–	MHz
Differential gain	G	–	4	10	%
Differential phase	Ø	–	2	10	%
Carrier signal at video output (2) (V_I = 10 mV)	R_p	–	58	–	dB
2nd harmonic of carrier at video output (3) (V_I = 10 mV)	R_2	–	44	–	dB
Change of frequency at AFC output voltage swing of 10 V	Δ_f	–	100	200	KHz
Reference voltage of AGC detector	V(14)	–	3.9	–	V
Tuner AGC output current range	I(4)		0 → 10		mA
Tuner AGC output voltage (I(4) = 10 mA)	V(4-13)	–	–	0.3	V
Tuner AGC output leakage current (V(14-13) = 11 V ; V(4-13) = 12 V)	I(4)	–	–	15	μA

(1) $S/_N = \dfrac{V_S \text{ (black to white)}}{V_n \text{ typ. r.m.s at B = 5 MHz}}$ dB

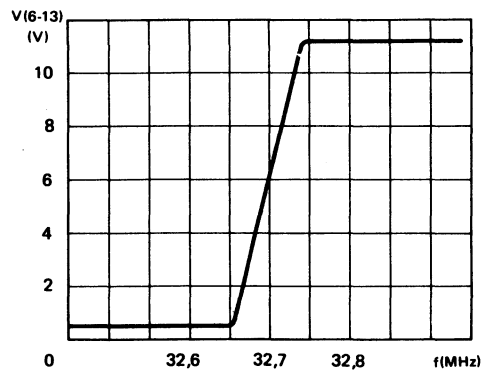
(2) $R_p = 20 \log. \dfrac{V_{S\,CC}}{V_S \text{ (32.7 MHz)}}$

(3) $R2 = 20 \log. \dfrac{V_{S\,CC}}{V_S \text{ (65.4 MHz)}}$

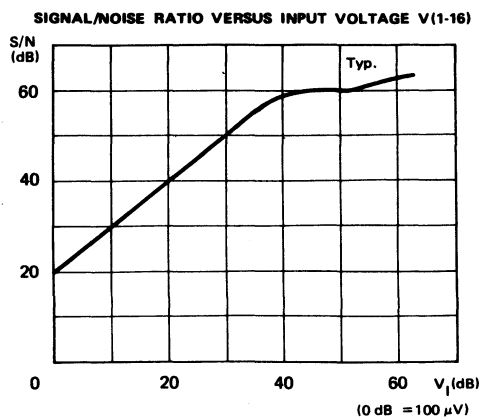
AFC VOLTAGE VERSUS FREQUENCY V(5-13)

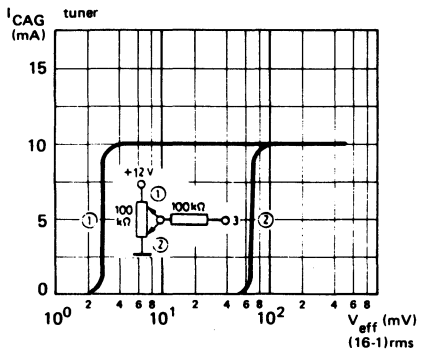


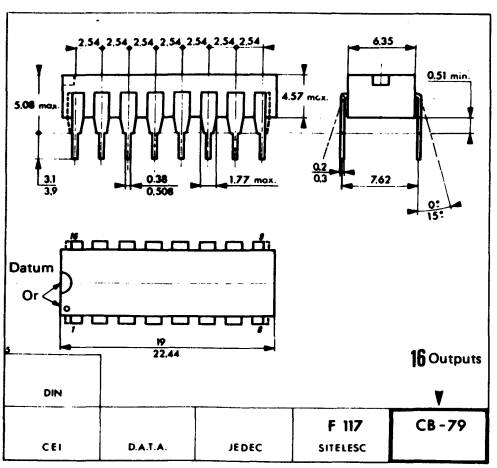
AFC VOLTAGE VERSUS FREQUENCY V(5-13)



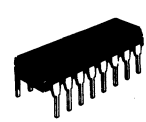
SIGNAL/NOISE RATIO VERSUS INPUT VOLTAGE V(1-16)







CASE CB-79



DP SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TDA2593

SYNCHRO AND HORIZONTAL DEFLECTION CONTROL FOR COLOR TV SET
SYNCHRONISATION ET BALAYAGE LIGNE POUR TV COULEUR

The TDA2593 is a circuit intended for the horizontal deflection of solid-state color TV sets, supplied with transistors or SCR'S.

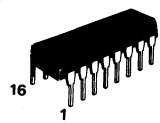
It performs the following functions :
- **Line oscillator (two levels switching)**
- **Phase comparison between synchro-pulse and oscillator voltage $\phi 1$, enabled by an internal pulse, (better parasitic immunity)**
- **Phase comparison between the flyback pulses and the oscillator voltage $\phi 2$**
- **Coïncidence detector providing a large hold-in-range**
- **Filter characteristics and gate switching for video recorder application**
- **Noise gated synchro separator**
- **Frame pulse separator**
- **Blanking and sand castle pulses generators compatibles with new decoder circuits**
- **Horizontal power stage phase lagging circuit**
- **Switching of control output pulse width**
- **Separated supply voltage output stage allowing direct drive of SCR'S circuit**
- **Security circuit makes the output pulse suppressed when poor supply voltage.**

Le TDA2593 est un circuit permettant de réaliser la base de temps ligne pour les récepteurs de télévision couleur utilisant des étages de balayage équipés de transistors ou de thyristors.

Il remplit les fonctions suivantes :
- Oscillateur de ligne (commutation à deux niveaux)
- Comparateur de phase entre l'impulsion de synchro de lignes et la tension d'oscillation $\phi 1$ validé par une impulsion interne (meilleure immunité aux parasites)
- Comparateur de phase entre les impulsions de retour de lignes et la tension d'oscillation $\phi 2$
- Détecteur de coïncidence $\phi 3$ assurant l'élargissement de la plage de capture
- Commutation des caractéristiques de filtre et de porte lors de l'utilisation d'enregistreur vidéo
- Séparateur de signal synchro et circuit de suppression de parasites
- Séparateur des impulsions de synchro trame
- Elaboration d'impulsions d'effacement de retour de lignes et de sélection de salves de couleur, adaptée aux nouveaux circuits de décodage
- Circuit de décalage de phase de l'impulsion de sortie
- Circuit de commutation de la durée de l'impulsion de sortie
- Etage de sortie à alimentation séparée permettant l'attaque directe des circuits à thyristors
- Circuit de protection supprimant l'impulsion de sortie en cas de tension d'alimentation trop basse.

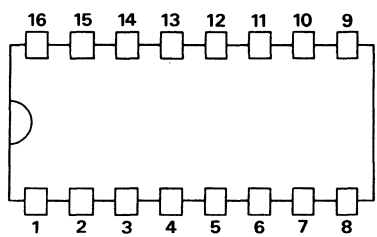
SYNCHRO AND HORIZONTAL DEFLECTION CONTROL FOR COLOR TV SET
SYNCHRONISATION ET BALAYAGE LIGNE POUR TV COULEUR

CASE/BOITIER CB-79



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE

PIN CONFIGURATION
BROCHAGE



1 **Supply voltage**
Tension d'alimentation
2 **Output stage supply voltage**
Alimentation de l'étage de sortie
3 **Output pulse**
Signal de sortie
4 **Selection of output pulse duration**
Sélection de la durée d'impulsion de sortie
5 **Decoupling**
Découplage
6 **Reference pulse (fly-back) for the 2nd phase comparator**
Impulsion de référence (retour lignes) pour le second comparateur de phase
7 **Sand castle pulse**
Sortie impulsion effacement lignes et sélection de salve
8 **Vertical synchro output**
Sortie de l'impulsion de synchro verticale

9 **Synchro separator output**
Entrée du séparateur de synchro
10 **Noise separator input**
Entrée du séparateur de bruit
11 **V.C.R. switching**
Commutation magnétoscope
12 **Time constant switching (third phase comparator)**
Commutation de constante de temps du 3ème comparateur de phase
13 **First phase comparator output**
Sortie du premier comparateur de phase
14 **Ramp oscillator capacitance**
Capacité d'intégration de rampe d'oscillateur
15 **Adjustment of the charge current**
Réglage du courant de charge de la capacité d'intégration
16 **Ground**
Masse.

NT8035

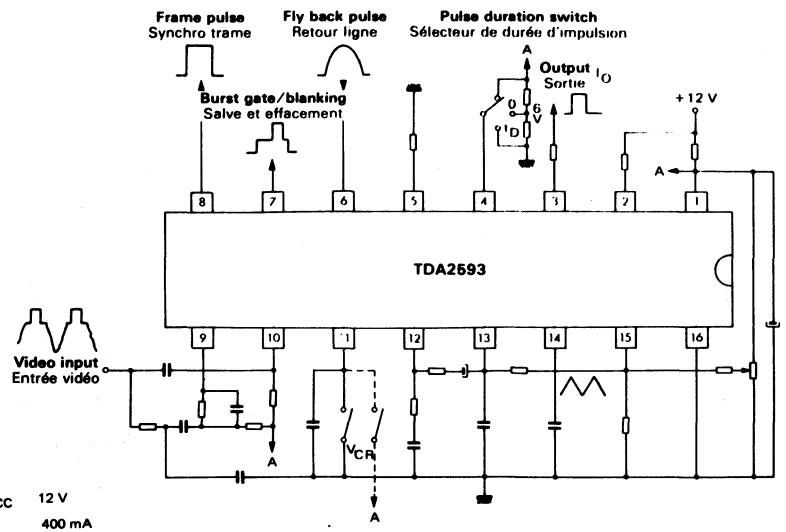
THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

CARACTERISTIQUES PRINCIPALES
MAIN CHARACTERISTICS

Tension d'alimentation Supply voltage	V(1-16)	12 typ.	V
Courant d'alimentation Supply current	I(1)	30 typ.	mA
SIGNAUX D'ENTREE INPUT SIGNALS			
Tension d'entrée du séparateur de synchronisation Synchro separator input voltage	V(9-16) (pp)	3 à 4	V
Tension d'entrée des séparateurs de bruit Noise separators input voltage	V(10-16) (pp)	3 à 4	V
Tension de commande du commutateur de durée d'impulsion de sortie : Control voltage of the output pulse switching circuit : t = 7 µS (thyristor)	V(4-16)	9,4 à V(1-16)	V
t = 14 µS + t_d (transistor)	V(4-16)	0 à 3,5	V
t = 0 (V3-16 = 0)	V(4-16)	5,4 à 6,6	V
SIGNAUX DE SORTIE OUTPUT SIGNALS			
Impulsion de synchronisation verticale Frame synchro pulse	V(8-16) (pp)	11 typ.	V
Impulsion de sélection de salve Sandcastle pulse	V(7-16) (pp)	11 typ.	V
Impulsion de commande ligne Horizontale driver stage control pulse	V(3-16) (pp)	10,5 typ.	V

SCHEMA DE PRINCIPE
BLOCK DIAGRAM

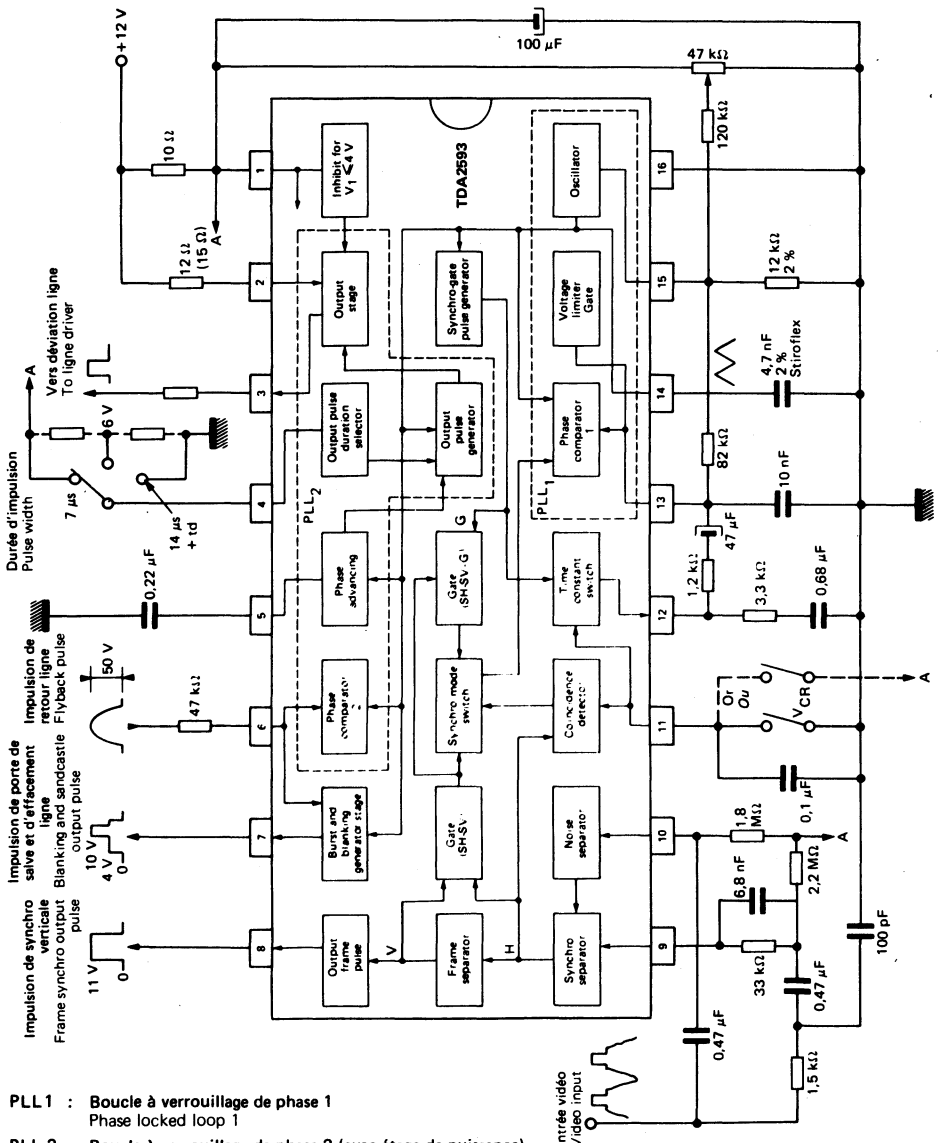


VALEURS LIMITES ABSOLUES
ABSOLUTE MAXIMUM RATINGS

Limites absolues selon la publication CEI 134
Absolute maximum ratings according to CEI 134 data sheet

Tension d'alimentation à la borne 1 Supply voltage to pin 1	V(1-16)	13,2	V
Tension d'alimentation à la borne 2 Supply voltage to pin 2	V(2-16)	18	V
Tension à la borne 4 Voltage to pin 4	V(4-16)	13,2	V
Tension à la borne 9 Voltage to pin 9	V(9-16)	± 6	V
Tension à la borne 10 Voltage to pin 10	V(10-16)	± 6	V
Tension à la borne 11 Voltage to pin 11	V(11-16)	13,2	V
Courant aux bornes 2 et 3 (avec thyristor) Current at pins 2 and 3 (with thyristor)	$I_{2M} = -I_{3M}$	650	mA
Courant aux bornes 2 et 3 (avec transistor) Current at pins 2 and 3 (with transistor)	$I_{2M} = -I_{3M}$	400	mA
Courant à la borne 4 Current to pin 4	I(4)	1	mA
Courant à la borne 6 Current to pin 6	I(6)	± 10	mA
Courant à la borne 7 Current to pin 7	I(7)	−10	mA
Courant à la borne 11 Current to pin 11	I(11)	2	mA
Puissance totale dissipée Power dissipation	P_{tot}	800	mW
Température ambiante de fonctionnement Operating ambient temperature	T_{amb}	$-20_{to}^{à} +70$	°C
Température de stockage Storage temperature	T_{stg}	$-25_{to}^{à} +125$	°C

SCHÈMA D'APPLICATION
APPLICATION SCHEMA



PLL 1 : **Boucle à verrouillage de phase 1**
Phase locked loop 1

PLL 2 : **Boucle à verrouillage de phase 2 (avec étage de puissance)**
Phase locked loop 2 (with power stage)

CARACTERISTIQUES ELECTRIQUES
ELECTRICAL CHARACTERISTICS

Spécifications applicables pour : V1-16 = 12 V
These specifications apply for: T_{amb} = 25°C

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITION	MIN.	TYP.	MAX.	UNITES UNITS
SIGNAUX D'ENTREES INPUT SIGNALS						
Séparateur de synchronisation (borne 9) Synchro separator (pin 9)						
Tension de seuil à l'entrée Input threshold voltage	V(9-16)			0,8		V
Courant de seuil à l'entrée Input threshold current	I(9)				5	µA
Courant d'entrée à l'état conducteur On-state input current	I(9)			5 à to 100		µA
Courant de déconnexion d'entrée Disconnect input current	I(9)		100	150		µA
Courant d'entrée à l'état bloqué Off-state input current	I(9)	V9-16 = –5 V			–1	µA
Signal d'entrée vidéo (impulsions de synchro positives) Video input signal (positive synchro pulses)	V(9)	Crête à crête (note 1) peak to peak		3 à to 4		V
Séparateur de bruit (borne 10) Noise separator (pin 10)						
Tension de seuil à l'entrée Input threshold voltage	V(10-16)			1,4		V
Courant de seuil à l'entrée Input threshold current	I(10)		100	150		µA
Courant d'entrée Input current	I(10)			5 à to 100		µA
Courant d'entrée à l'état bloqué Off-state input current	I(10)	V10-16 = –5 V			–1	µA

CARACTERISTIQUES ELECTRIQUES (suite)
ELECTRICAL CHARACTERISTICS (continued)

Spécifications applicables pour : V1-16 = 12 V
These specifications apply for : T_{amb} = 25°C

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITION	MIN.	TYP.	MAX.	UNITES UNITS
Signal d'entrée vidéo (impulsions de synchro positives) Video input signal (positive synchro pulses)	V(10)	**Crête à crête** (note 1) peak to peak		3 à 4		V
Signal parasite superposé admissible Allowed superimposed parasitic signal	V(10)				7	V
Impulsion de retour de ligne (borne 6) Flyback pulse (pin 6)						
Tension de seuil à l'entrée Input threshold voltage	V(6-16)			1,4		V
Niveau de la limitation à l'entrée Input limitation level	V(6)			–0,7 et +1,4		V
Courant d'entrée Input current	I(6)		0,01	1	2	mA
Commutateur de durée d'impulsion de sortie (borne 4) Output pulse width control switch (pin 4)						
Tension d'entrée Input voltage	V(4-16)	t = 7 µS (thyristor)		9,4 à V(1-16)		V
	V(4-16)	t = 14 µS + t_d (transistor)		0 à 3,5		V
	V(4-16)	t = 0 (V3-16 = 0) (note 2)		5,4 à 6,6		V
Courant d'entrée Input current	I(4)	t = 7 µS (thyristor)	200			µA
	I(4)	t = 14 µS + t_d (transistor)	200			µA
	I(4)	t = 0 (V3-16 = 0)		0		

CARACTERISTIQUES ELECTRIQUES (suite)
ELECTRICAL CHARACTERISTICS (continued)

Spécifications applicables pour : V1-16 = 12 V
These specifications apply for : T_{amb} = 25°C

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITION	MIN.	TYP.	MAX.	UNITES UNITS
Commutateur pour lecture d'enregistrement vidéo (borne 11) Video recorder switch (pin 11)						
Tension d'entrée Input voltage	V(11-16)	V.C.R en/on service (Borne 11 niveau bas) (Pin 11 low level)		0 à/to 2,5		V
	V(11-16)	V.C.R en/on service (Borne 11 au +V_{CC}) (Pin 11 to +V_{CC})		9 à/to V(1-16)		V
Courant d'entrée Input current	I(11)	V.C.R en/on service (Borne 11 au niveau bas) (Pin 11 low level)			200	µA
	I(11)	V.C.R on/on service (Borne 11 au +V_{CC}) (Pin 11 to +V_{CC})			2	mA
SIGNAUX DE SORTIE OUTPUT SIGNALS						
Impulsions de synchro trames (posit.) (borne 8) Frame synchro pulses (positive) (pin 8)						
Tension de sortie Output voltage	V(8-16)	Valeur crête Peak value	10	11		V
Résistance de sortie Output impedance	R(8)			2		kΩ
Retard entre les fronts avant du signal d'entrée et du signal de sortie Delay between leading edge of input signal and leading edge of output signal	t_{on}			15		µS
Retard entre les fronts arrière du signal d'entrée et du signal de sortie Delay between trailing edge of input signal and trailing edge of output signal	t_{off}			15		µS

CARACTERISTIQUES ELECTRIQUES (suite)
ELECTRICAL CHARACTERISTICS (continued)

Spécifications applicables pour : V1-16 = 12 V
These specifications apply for : T_{amb} = 25°C

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITION	MIN.	TYP.	MAX.	UNITES UNITS
Impulsions de sélection de salves (posit) (borne 7) Sandcastle pulse (positive) (pin 7)						
Tension de sortie Output voltage	V(7-16)	**Valeur crête** Peak value	10	11		V
Résistance de sortie Output impedance	R(7)			70		Ω
Courant de sortie durant le front descendant Output current during trailing edge	I(7)			2		mA
Durée des impulsions de sélection de salves Sandcastle pulse width	t_7 t7	V7 = 7 V	3,7		4,3	µS
Relation de phase entre le milieu des impulsions de synchro sur l'entrée et le front montant des impulsions de sélection de salves Phase between middle input synchro pulse and leading edge of sandcastle pulse	Δt	V7 = 7 V	2,15		3,15	µS
Impulsion d'effacement de retour de ligne (borne 7) Flyback blanking pulse (pin 7)						
Tension de sortie Output voltage	V(7-16)	**Valeur crête** Peak value	4		5	V
Résistance de sortie Output impedance	R(7)			70		Ω
Courant de sortie durant le front descendant Output current during trailing edge	I(7)			2		mA
Impulsion de commande de lignes (posit) (borne 3) Control pulse for horizontal driver (positive) (pin 3)						
Tension de sortie Output voltage	V(3-16)	**Valeur crête** Peak value		10,5		V

CARACTERISTIQUES ELECTRIQUES (suite)
ELECTRICAL CHARACTERISTICS (continued)

Spécifications applicables pour : V1-16 = 12 V
These specifications apply for : T_{amb} = 25°C

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITION	MIN.	TYP.	MAX.	UNITES UNITS
Résistance de sortie Output impedance	R(3)	Front montant Leading edge		2,5		Ω
	R(3)	Front descendant Trailing edge		20		Ω
Durée des impulsions de commande Control pulse width	t3	(Thyristor) V4 = 9,4 à to V(1-16)	5,5		8,5	µS
	t3	(Transistor) V4 = 0 à to 4 V (note 3)		$14 + t_d$		µS
Mise hors circuit de l'impulsion de commande Control pulse is disabled for	V(1-16)			4		V
Relation de phase totale Overall phase relationship						
Relation de phase entre le milieu de l'impulsion de synchro et le milieu de l'impulsion de retour ligne Phase between middle synchro pulse and middle flyback pulse	t_z	Avec With t_r = 12 µS (note 4)	1,9		3,3	µS
Sensibilité au réglage de courant Sensitivity to current adjust	ΔI/Δt			30		µA/µS
Oscillateur (bornes 14 et 15) Oscillator (pins 14 and 15)						
Tension de seuil Threshold voltage	V(14-16)	Niveau bas Low level		4,4		V
	V(14-16)	Niveau haut High level		7,6		V
Courant de charge et de décharge Current generator	I(14)			± 0,47		mA
Fréquence libre d'oscillation Free running frequency	f	C_{osc} = 4700 pF R_{osc} = 12 kΩ		15625		Hz

CARACTERISTIQUES ELECTRIQUES
ELECTRICAL CHARACTERISTICS

Spécifications applicables pour : V1-16 = 12 V
These specifications apply for : T_{amb} = 25°C

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITION	MIN.	TYP.	MAX.	UNITES UNITS
Tolérance de la fréquence Tolerance on frequency	Δf	(note 5)			± 5	%
Sensibilité de la commande de fréquence Frequence control sensitivity	$\Delta f/I15$			31		Hz/µA
Plage de réglage Spread of frequency	Δf	Avec le schéma d'application proposé With application schematic proposed		± 10		%
Influence de la tension d'alimentation sur la fréquence Influence of supply voltage on frequency	$\frac{\Delta f/f}{\Delta V/Vnom.}$	(note 5)			± 0,05	%
Variation de la fréquence quand V1-16 chute à 5 V Frequency change when decreasing the supply down to 5 V	Δf	V(1-16) = 5 V (note 5)			± 10	%
Coefficient de température de la fréquence Frequency temperature coefficient	T	(note 5)			$\pm 10^{-4}$	/°K
Comparateur de phase ϕ1 (borne 13) Phase comparator ϕ1 (pin 13)						
Plage de tension de commande Control voltage range	V(13-16)			3,8 à to 8,2		V
Courant de commande Control current	I(13)	Valeur crête Peak value		± 1,9 à to ± 2,3		mA
Courant de sortie à l'état bloqué Off-state output current	I(13)	V(13-16) = 4 à to 8 V			−1	µA
Résistance de sortie Output impedance	R(13)	V(13-16) = 4 à to 8 V (note 6)		Forte High		
	R(13)	V(13-16) < 3,8 V ou or > 8,2 V (note 7)		Faible Low		
Sensibilité de la commande Control sensibility				2		KHz/µS

CARACTERISTIQUES ELECTRIQUES
ELECTRICAL CHARACTERISTICS

Spécifications applicables pour : V1-16 = 12 V
These specifications apply for : T_{amb} = 25°C

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITION	MIN.	TYP.	MAX	UNITES UNITS
Plage de capture et de maintien Catching and holding range	Δf			± 780		Hz
Tolérance de la plage de capture et de maintien Catching and holding range tolerance	$\Delta f/f$	(note 5)		± 10		%
Comparateur de phase $\phi 2$ et déphaseur (borne 5) Phase comparator $\phi 2$ and phase-shift (pin 5)						
Plage de tension de commande Control voltage range	V(5-16)			5,4 à / to 7,6		V
Courant de commande Control current	I(5)	Valeur crête Peak value		± 1		mA
Courant de sortie à l'état bloqué Off-state output current	I(5)	V(5-16) = 5,4 à / to 7,6 V			–5	µA
Résistance de sortie Output impedance	R(5)	V(5-16) = 5,4 à / to 7,6 V (note 6)		Forte High		
	R(5)	V(5-16) < 5,4 V ou / or > 7,6 V		8		kΩ
Retard maximum entre le front montant de l'impulsion de sortie et le front descendant de l'impulsion de retour Max. delay between output pulse leading edge and flyback pulse trailing edge	t_d	t_r = 12 µS			15	µS
Erreur de commande statique Static control error	$\Delta t/\Delta t_d$				0,2	%
Détecteur de coïncidence $\phi 3$ (borne 11) Coïncidence detector $\phi 3$ (pin 11)						
Tension de sortie Output voltage	V(11-16)		0,5	à / to 6		V

CARACTERISTIQUES ELECTRIQUES
ELECTRICAL CHARACTERISTICS

Spécifications applicables pour : V1-16 = 12 V
These specifications apply for : T_{amb} = 25°C

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITION	MIN.	TYP.	MAX.	UNITES UNITS
Courant de sortie Output current	I(11)	Sans coïncidence Without coïncidence		0,1		mA
	I(11)	Avec coïncidence With coïncidence		−0,5		mA
Commutateur de constante de temps (borne 12) Time constant switch (pin 12)						
Tension de sortie Output voltage	V(12-16)			6		V
Courant de sortie Output current	I(12)			± 1		mA
Résistance de sortie Output impedance	R(12)	V(11-16) = 2,5 à 7 V		100		Ω
	R(12)	V(11-16) < 1,5 ou > 9 V		60		kΩ
Générateur d'impulsions (interne) Pulse generator (internal)						
Durée des impulsions Pulse width	t			7,5		µS

Note 1 : **Plage admissible 1 à 7 V.**
Allowed range 1 to 7 V.

Note 2 : **Ou borne 4 libre.**
Or pin 4 not connected.

Note 3 : **Avec t_r = 12 µS.**
With t_r = 12 µS.

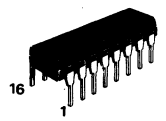
Note 4 : **Le réglage de la relation de phase totale et donc du front montant de l'impulsion de sortie est effectué automatiquement par le comparateur de phase φ 2. Si un réglage supplémentaire est souhaité, on peut imposer un courant à la borne 5.**
The adjustment of overall phase relation (and output pulse leading edge position) is automatically performed by phase comparator φ 2. If additional adjustment is needed, a current have to be imposed at pin 5.

Note 5 : **Sans tenir compte de la tolérance des composants extérieurs.**
Tolerance of peripheral components not included.

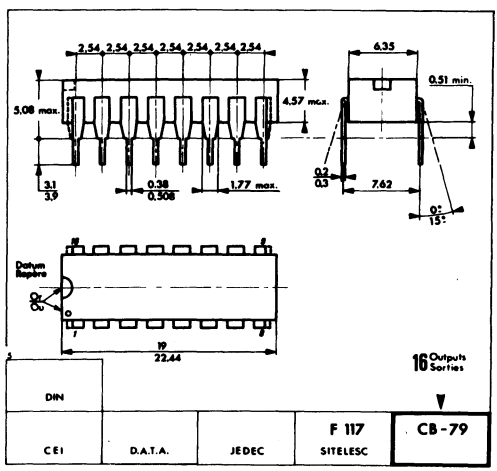
Note 6 : **Générateur de courant.**
Current generator.

Note 7 : **Emetteur-suiveur.**
Emitter-follower.

CASE/BOITIER CB-79



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE



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Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TDA3300 B

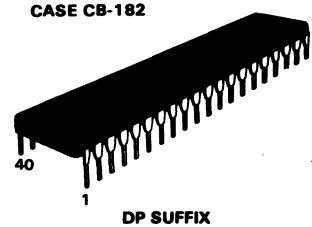
TV COLOUR PROCESSING SYSTEM

The TDA 3300 B is a new generation colour processing system. The device will accept a PAL or NTSC composite video signal. At outputs the three colour signals need only a simple driver amplifier to interface to the picture tube. There are also four inputs for On-Screen Display and the complementary fast blanking for use with Teletext, TV games, cameras, etc...

- **Full multistandard capability**
- **On-Screen Display inputs + fast blanking**
- **Three DC, high impedance user controls**
- **Automatic black level set-up**
- **Beam current limiting**
- **Inexpensive 4.43/3.58 MHz reference generation**
- **Single 12 V supply**
- **Low dissipation - typically 600 mW**

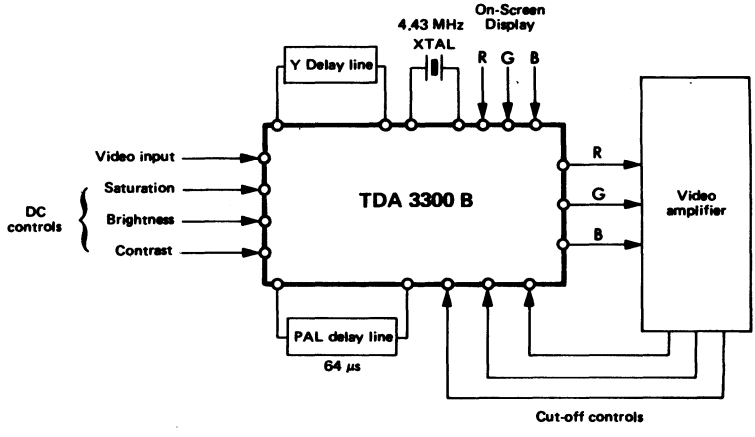
TV COLOUR PROCESSING SYSTEM

CASE CB-182



DP SUFFIX
PLASTIC PACKAGE

SIMPLIFIED APPLICATION DIAGRAM



NT8104-A

THOMSON SEMICONDUCTORS
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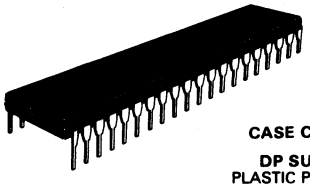
THOMSON COMPONENTS

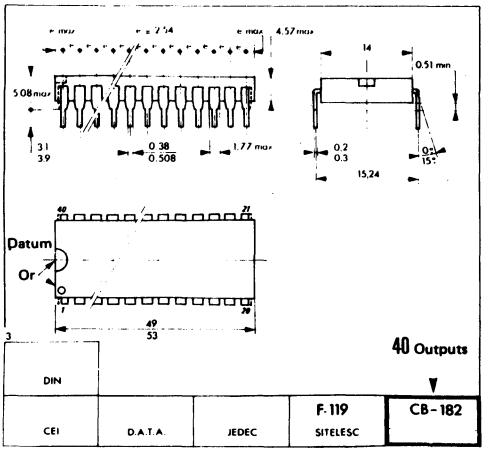
TDA3300 B – PIN CONFIGURATION



CASE CB-182

DP SUFFIX
PLASTIC PACKAGE

Chroma input	1	40	+9 V internal reference
ACC capacitor	2	39	+12 V
Chroma DL driver, emitter	3	38	Ground
Chroma DL driver, collector	4	37	1 V composite video input
Saturation control	5	36	Delayed luma input
Ident capacitor	6	35	Luma DL drive & 3 V inverted o/p
V input	7	34	Luma emitter trap
U input	8	33	Luma collector trap
90° loop capacitor	9	32	Contrast control
Oscillator loop filter	10	31	Black level clamp
Xtal drive	11	30	Britghtness control
Xtal feedback	12	29	Peak beam limit adjust
Ground	13	28	Frame pulse i/p
Blue output	14	27	Sandcastle pulse i/p
Blue o/p clamp capacitor	15	26	OSD input green
Blue o/p feedback	16	25	OSD input red
Green output	17	24	OSD input blue
Green o/p clamp capacitor	18	23	OSD input fast blanking
Green o/p feedback	19	22	Red o/p feedback
Red output	20	21	Red o/p clamp capacitor



MAXIMUM RATINGS $T_{amb} = +25°C$ (Unless otherwise stated)

RATINGS	PINS	VALUES	UNITS
Supply voltage	39	16	V
Operating temperature range		0°C, +70°C	°C
Storage temperature range		-65°C, +150°C	°C

ELECTRICAL CHARACTERISTICS $T_{amb} = +25°C$ (Unless otherwise stated)

PARAMETERS	SYMBOLS	PINS	MIN.	TYP.	MAX.	UNITS
Supply voltage		39	10,8	12	13,2	V
Supply current		39		55		mA
Composite video input voltage		37		1		Vp.p
CHROMA INPUT VOLTAGE						
(Burst p.p ACC controlled)		1	10		200	mV
Max chroma input voltage (Burst p.p)					400	mV
ACC range				25		dB
RGB ON-SCREEN DISPLAY INPUT						
(Black and white)		24		1		V
OSD required drive impedance		25		75		Ω
OSD frequency response		26				
(Flat to)				5		MHz
Positive fast blanking input threshold				0,5		V
SANDCASTLE PULSE INPUT THRESHOLD		27				
Line				2,0		V
Burst gate				8,0		V
Frame pulse		28	4,0		12	V
Beam current reference threshold				2,0		V
RGB output level (black and white)		14	4,0			V
		17				
		20				
Inverted composite video output		35		3,0		V
Active range of user controls		5	0,5		4,5	V
Source impedance of user controls		30			1	MΩ
(Mid range gain at 2,5 V)				-10 (relative to max)		dB
Control range – contrast & saturation				40		dB
Brightness (at video output)				±1		V
U and V reference phase errors					5	°
Peak beam current limit		29		2 x I(29)		

FIGURE 1 – EXTERNAL COMPONENTS

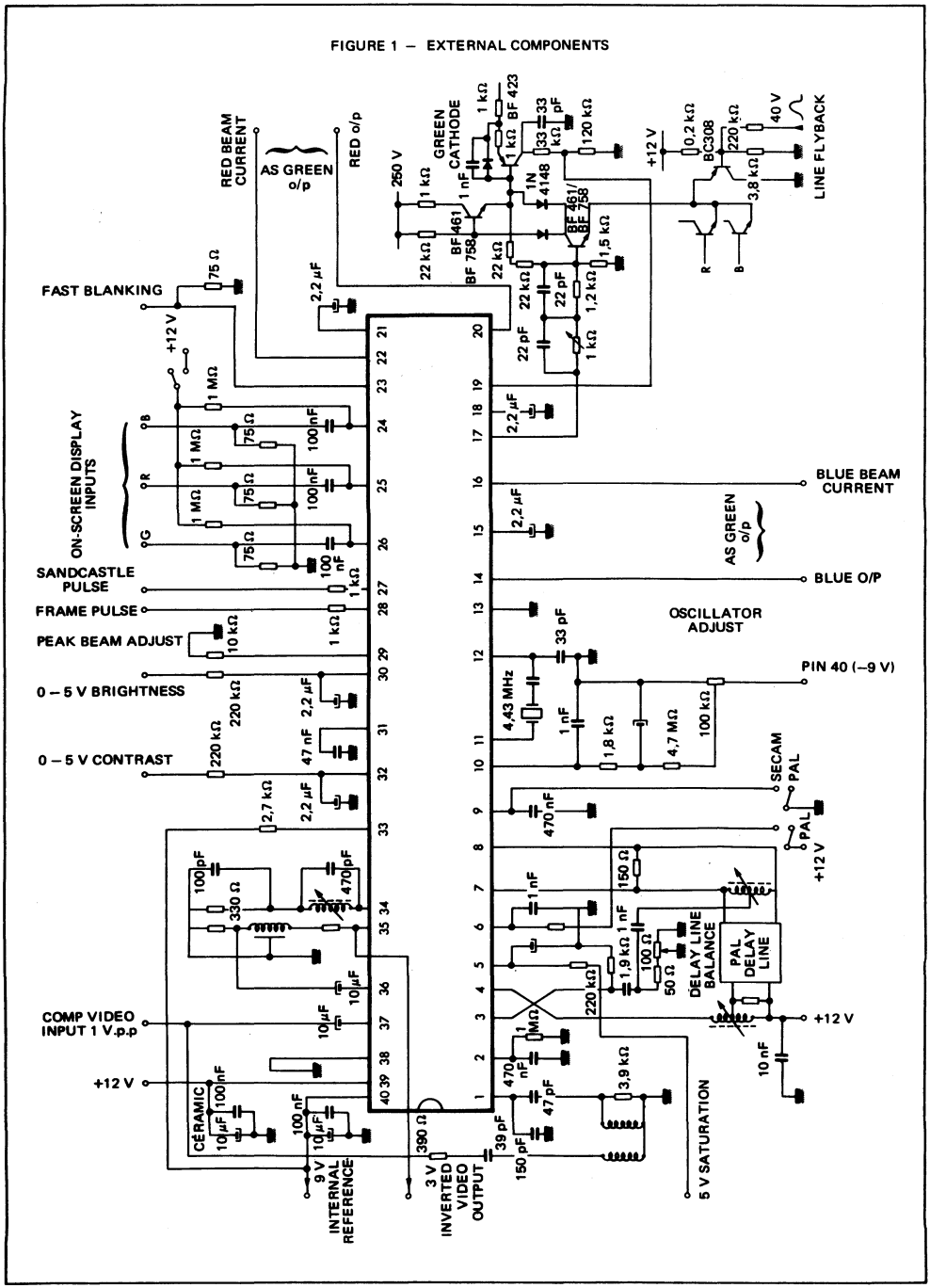
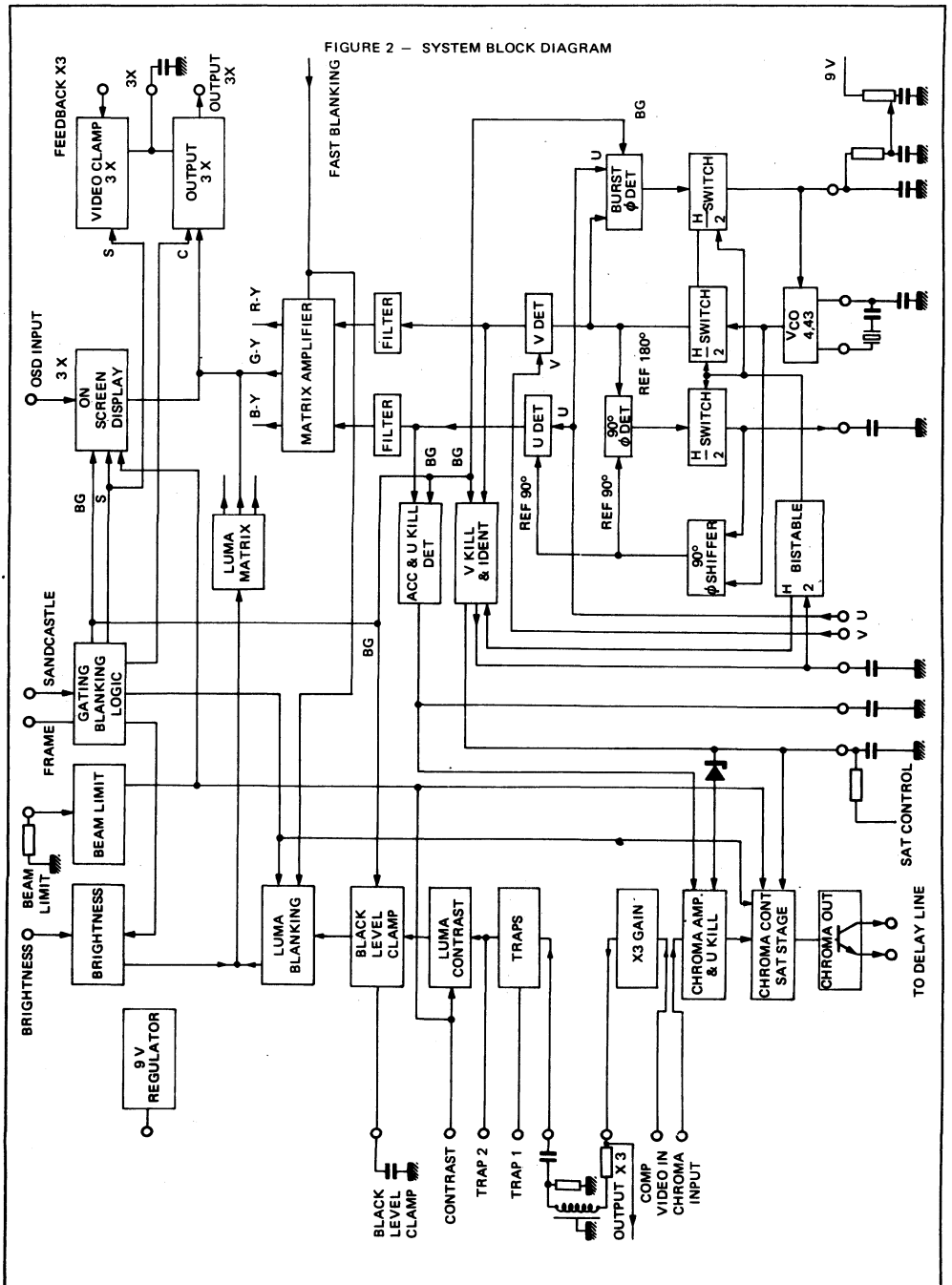


FIGURE 2 – SYSTEM BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The circuit operation can be followed by referring to the block diagram, figure 2.

The Luma Channel

In order to ensure compatability with standard video transmission systems the luma input channel is high impedance, AC coupled, designed to accept a 1 V composite video signal. After a X3 gain voltage amplifier, the inverted luma signal is brought out to the luma delay time. This output is low impedance to match the delay line accurately, and as the signal is inverted it is highly suitable for driving a sync. separator such as the TDA2593 or TBA920.

Following the luma delay line the signal is fed to the chroma trap stage where external emitter and collector loads ensure accurate definition of the stage gain.

The contrast control is an electronic "gain" control of the current sharing type with a feedback clamp on the output to set the black level at the black level clamp.

The action of the black level clamp has been designed for minimum interference on the video signal. This is achieved by comparing the output of the contrast control with an internal 5 V reference. The output from the comparator which features a push-pull output for good carrier or burst rejection, is then integrated by the external black level clamp capacitor.

The final interface between the luma channel and the luma matrix is the brightness control.

During the line and frame blanking periods a switching circuit effectively blanks the luma signal and inserts a nominal black level of an internally derived 5 V reference level. However, the voltage source is modified by a current source ; the latter based on the "gain" control circuit described below - thus it becomes a controllable current source. This applies a variable offset between ± 1 V, to the nominal black level, all of which is held during the frame blanking period, thus making a brightness control.

The "gain" control circuit used for the three user controls is of the form shown in figure 3.

This configuration gives well defined characteristics, depending on the current ratios. However, the circuit response of the contrast and saturation controls has been shaped to appear linear to the user.

All the controls have an active range of 0,5 to 4,5 V making them compatible with D/A convertor derived control signals, such as those from remote control systems.

The Chroma Channel

The chroma signal is fed to three controlled stages ; for automatic colour control (ACC), contrast (to track the luma signal) and saturation. The two latter controls are designed along the same lines as the luma contrast control with the same law. One of these two stages is returned to full gain and the other to nominal (10 dB down from max.) during the burst gate period to provide a standard burst level for the ACC.

The saturation stage also provides the chroma kill function, which operates under two eventualities. Firstly the signal is shut down in the event of prolonged misidentification (the time being determined by the external capacitor on pin 2) or lack of identification and secondly, the saturation is reduced as the ACC voltage nears its zero level.

The chroma delay line drive is supplied by a transistor whose emitter and collector are brought out, the collector drives the delay line while the emitter supplies the direct signal for matrixing at the delay line output.

In the burst phase detector the system compares the constant phase burst of the U channel, at the delay line output, with the alternating reference drive to the V detector. The burst phase detector cancels out any resulting output alternation. At the same time any DC offsets are converted to alternating components, which are integrated to zero in the loop filter. Any resulting error voltage is applied to the 4,43 MHz voltage controlled reference oscillator.

CIRCUIT DESCRIPTION (continued)

A similar arrangement, the 90° phase detector, compares the phase of the reference drive to the U detector with that of the reference drive to the V detector. The U detector drive comes from the reference oscillator via a voltage controlled 90° phase shifter which is, itself, controlled by the 90° phase detector, when the input is separated by exactly 90° there is zero output.

During burst time the V detector compares two signals of alternating phase. Thus the output is dependant on the phase relationship between these signals, that is the identification. With a correctly identified signal the output of the V kill and identification circuitry, which is integrated by the ident capacitor on pin 6, is low. However, when the signal is misidentified this will cause the voltage on the ident capacitor to increase. At a certain, predetermined threshold a trigger circuit fires to add extra current to the capacitor. After a further delay a pulse is added to the H/2 bistable, effectively reversing its phase.

By use of a simple switch, see the application circuit, figure 1, a current can be fed on to the ident capacitor. This forces the trigger circuits on and locks the H/2 bistable in the V state, in this condition the system is able to decode NTSC signals, without the delay line.

An ACC voltage, independant of the identification phase, is derived from the output of the U detector by the ACC and U kill detector - which is a similar circuit to the V kill and ident circuit.

The outputs of the U and V detectors are filtered and fed to a balanced resistive matrix to generate the three colour difference signals, R–Y, G–Y and B–Y. A non-saturating circuit returns the inputs to zero for fast blanking.

It is in the final matrix that the luma signal, the colour difference signals, plus any On-Screen Display signals, as current sources, are brought together and summed. The three resultant signals are fed to the virtual earth inputs of the on-chip output stages.

Inputs for On-Screen Display are fed into the system as a voltage between the black-white limits of 1 V. All three inputs are voltage to current converted and fed to "gain" control stages which are controlled by the luma contrast control. Each input is AC coupled and black level clamped using the coupling capacitor as the storage element for the clamp voltage.

The three on-chip output stages are high gain, class AB amplifiers with the gain set by parallel feedback resistors. This makes for a well defined gain and stable output voltage level.

One of the major features of the chroma III system is its beam current feedback and beam current limiting. This is a peak detecting system specially designed to enhance the system's normal video or digital signal handling compatability.

The beam current in each cathode of the picture tube is monitored by a high-voltage PNP transistor, see the application circuit figure 1. A sample of this current is feedback to the TDA3300. During a scan this beam current sample is compared, as a voltage across an internal resistor, with a reference voltage developed across a second internal resistor whose current is determined by the resistor value on pin 29.

If the beam current exceeds this reference the circuit reduces the contrast.

It will be remembered that in the luma channel a reference black level is inserted into the luma signal during the line and frame blanking periods. While this reference level is present, and after the frame flyback, the output stage feedback input goes high impedance and an internal comparator is activated. This circuit compares an internal reference voltage with the voltage developed across the same external resistor by picture tube beam current. External capacitive integration of the comparator's output sets up a current which is injected into the input of the output amplifier to keep the reference level at a nominal black.

The internal, line blanking and burst gate pulses are derived from a standard "sandcastle" pulse, as shown in figure 4, fed to pin 27. Frame blanking is derived from a frame flyback pulse applied to pin 28. A simple counter counts the first two lines after the frame flyback and clamps the next, and subsequent lines to the nominal black reference level.

APPLICATION NOTE

The resistance values shown in figure 1 will result in nominal values, for peak beam limiting and beam current feedback, of 2 mA and 17 μA per gun.

As for any given picture tube the colour phosphors vary in efficiency, with blue, generally, being the most efficient, it is possible to scale the beam current feedback resistors (in figure 1, 120 kΩ in the collector of the BF 493) accordingly. The average needs for a typical tube to give illuminant D (6550° k) are as follows :

- Red 34 %
- Blue 28 %
- Green 38 %

Setting up the reference oscillator

a) Connect a colour bar test signal to the circuit ; switch off the burst
b) Connect pin 5, saturation control, to + 12 V – this will un-kill the system
c) Adjust the oscillator, with the 100 kΩ potentiometer on pin 10, for zero beat

Setting up the delay line

In general terms, the balance is adjusted by use of the delay line gain balance potentiometer and the phase by use of the delay line matching coils.

On-screen display

In a receiver not designed to be equiped with the on-screen display facility it is strongly recommended that the three on-screen display and fast blanking inputs are tied to ground.

FIGURE 3 – GAIN CONTROL

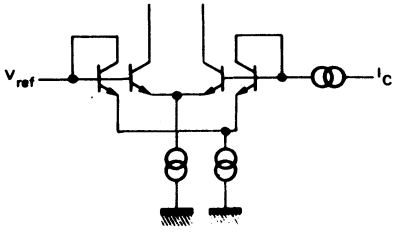
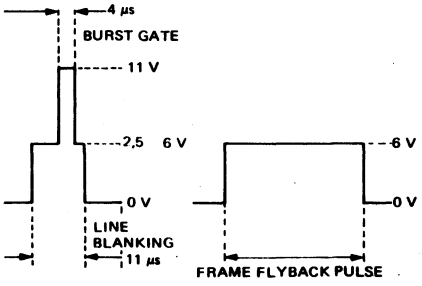


FIGURE 4 – SANDCASTLE & FRAME PULSES



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Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TEA1014

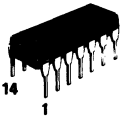
VIDEO AND AUDIO SIGNALS SWITCHING FOR THE PERI-TELEVISION PLUG

This integrated circuit provides all video and sound switching allowing connections between the peri-TV plug and video, sound sections in the TV set.
Input and output signal characteristics follow the norms of the SCART specification n° 108 of November 1978.
The TEA1014 is supplied in a DIP TO-116, 14 lead package.

- Video crosstalk ⩾ 60 dB
- Low impedance video output 75 Ω
- Short-circuit protection of inputs and outputs
- Internal horizontal PLL time constant switching in case of video recorder reception.

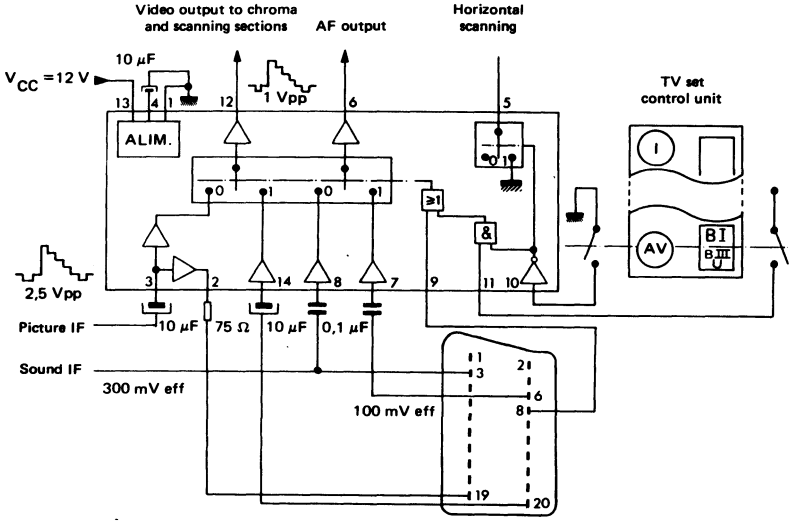
VIDEO AND AUDIO SIGNALS SWITCHING FOR THE PERI-TELEVISION PLUG

CASE CB-2 (TO-116)



DP SUFFIX
PLASTIC PACKAGE

APPLICATION CIRCUIT



NT8044-A

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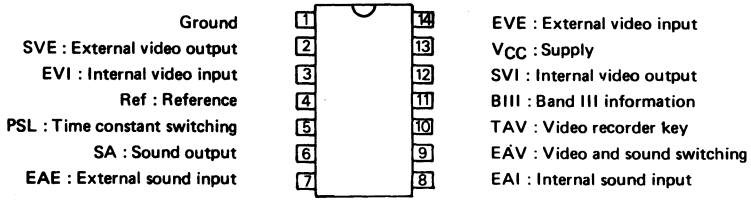
THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	18	V
Storage temperature range	T_{stg}	- 40, + 150	°C
Junction temperature	T_j	+ 150	°C
Operating temperature	T_{oper}	- 10, + 100	°C

PIN CONFIGURATION



The main functions of the I.C. are following :

VIDEO SWITCHING

2 electronically switched inputs :

- one 2 Vpp input for signal coming from the picture IF
- one 1 Vpp input for signal coming from the peri-TV plug.

2 outputs :

- 1 Vpp output (low impedance 75 Ω) for peri-TV plug
- 1 Vpp output low impedance for video section of the TV set.

Each input and output is protected from ground short-circuit. The 75 Ω output is protected through a 75 Ω resistor.

AUDIO SWITCHING

Two electronically switched inputs :

- 300 mV rms input coming from Audio IF
- 100 mV rms input coming from the peri-TV plug

one low impedance output 300 mV rms.

Inputs and outputs are also protected against ground short-circuit.

SWITCHING LOGIC

The logic takes into account the informations on 3 pins.

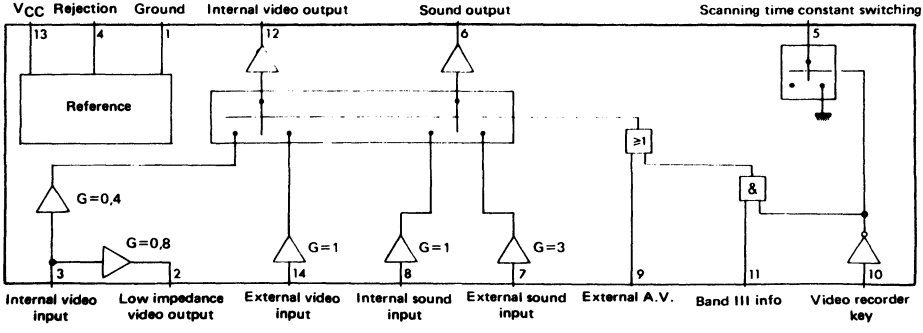
- Internal or external video and sound (pin 8 peri TV plug)
- Band III informations
- Video recorder key.

External Video and Audio signals are selected in two cases.

When there is a voltage information coming from peri-TV plug.
When the video recorder key is selected (on TV front panel) and programmed on band III.

This I.C. includes an internal switch (open collector transistor) which commutes the time constant of the horizontal PLL circuit in case of video recorder reception.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

$11\ V \leqslant V_{CC} \leqslant 14\ V$; $T_{amb} = +25°C$ (Unless otherwise specified).

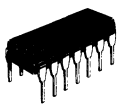
Characteristic	Symbol	Min	Typ	Max	Unit
Total power dissipation (V_{CC} = 12 V)		–	350	450	mW
Internal video input (coming from picture FI) (Pin 3)					
Video signal amplitude (Positive video)		–	2.5	6.8	V_{PP}
Input voltage range (refered to D.C. input voltage)		- 2.9	–	+ 3.9	V
Input impedance		5	–	–	kΩ
Input capacitance		–	–	5	pF
External video input (Coming from peri-TV plug) (Pin 14)					
Video signal amplitude (Positive video)		–	1	2.8	V_{PP}
Input voltage range (Refered to D.C. input voltage)		- 1.2	–	+ 1.6	V
Input impedance		5	–	–	kΩ
Input capacitance		–	–	5	pF
TV video output (Pin 12)					
Signal amplitude		–	1	2.8	V_{PP}
Output voltage swing (Refered to D.C. output voltage)		- 1.2	–	+ 1.6	V
Output dynamic impedance		–	–	10	Ω
D.C. output voltage (Without input signal)		–	3.5	–	V
Loading resistance		300	–	–	Ω
Video bandwidth (± 0.5 dB)		6	–	–	MHz
Gain/internal video		–	- 8	–	dB
Gain/external video		–	0	–	dB
External video output (low impedance) (Pin 2)					
Signal amplitude (on 150 Ω grounded)		–	2	5.5	V_{PP}
Output voltage swing		- 2.4	–	+ 3.1	V
Dynamic output impedance		–	10	–	Ω
D.C. output voltage (without input signal)		–	3.5	–	V
Minimum loading resistance (Electrical working non specified)		75	–	–	Ω
Gain/internal video		–	- 2	–	dB
Output video signals characteristics					
Video rejection between two inputs (0 to 6 MHz)		- 55	–	–	dB
Differential group delay		–	–	20	ns
Linearity distortion					
Luma (Test line 17)		–	2	–	%
Chroma (Test line 331)		–	2	–	%
Intermodulation luma-chroma (Test line 331)		–	5	–	%
Supply voltage rejection		50	–	–	dB

ELECTRICAL CHARACTERISTICS

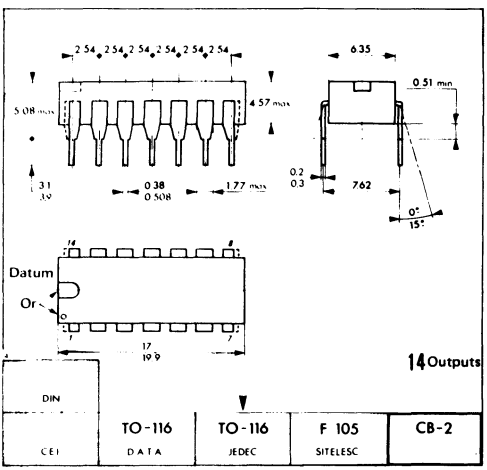
$11\ V \leq V_{CC} \leq 14\ V$; $T_{amb} = +25°C$ (Unless otherwise specified).

Characteristic	Symbol	Min	Typ	Max	Unit
Internal sound input (Pin 8)					
Input signal		–	0.3	2	V_{eff}
Input impedance		–	20	–	kΩ
External sound input (Pin 7)					
Input signal		–	0.1	0.7	V_{eff}
Input impedance		–	20	–	kΩ
Sound output (Pin 6)					
Output signal amplitude		–	0.3	–	V_{eff}
Output voltage swing		–	2	–	V_{eff}
Distortion (V_O = 0.6 V_{eff})		–	–	0.5	%
Bandwidth		16	–	–	KHz
Output impedance		–	40	–	Ω
Load impedance		2	–	–	kΩ
Gain/internal input		–	0	–	dB
Gain/external input		–	10	–	dB
Supply voltage rejection		60	–	–	dB
Crosstalk		- 60	–	–	dB
Video/sound crosstalk		- 60	–	–	dB
LOGIC					
External A.V. input (peri-TV plug) (Pin 9)					
Unactive low level or unconnected pin (logic state 0) - (TV receiving)		0	–	3	V
Active high level (logic state 1) (Ext. receiving)		9	–	V_{CC}	
Input impedance		–	10	–	kΩ
"Band III" input (Pin 11)					
Unactive low level or unconnected pin (logic state 0)		- 8	–	+ 3	V
Active high level (logic state 1)		9	–	V_{CC}	V
Input impedance high level		–	10	–	kΩ
Input current low level		–	–	1	μA
Video-recorder key input (Pin 10)					
Unactive high level or unconnected pin (logic state 1)		9	–	V_{CC}	V
Active low level (logic state 0)		0	–	3	V
Input impedance		–	10	–	kΩ
Open collector output (time - constant switching) (Pin 5)					
Leakage current (open collector)		–	–	1	μA
Maximum low level voltage (I(5) = 10 mA V_{CC})		–	–	1.5	V

CASE CB-2 (TO-116)



DP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

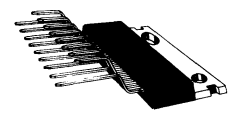
TEA1020

VERTICAL SWEEP FOR LARGE SCREEN COLOR T.V SETS

The TEA1020 is a complete vertical sweep system designed for TV sets. It includes a fly-back generator, a triggerable ramp generator, a power amplifier, a blanking-pulse generator and safety systems.
Its large output transistors and special "Power-in-line" case make it able to work without any external power stage and give it a good reliability.

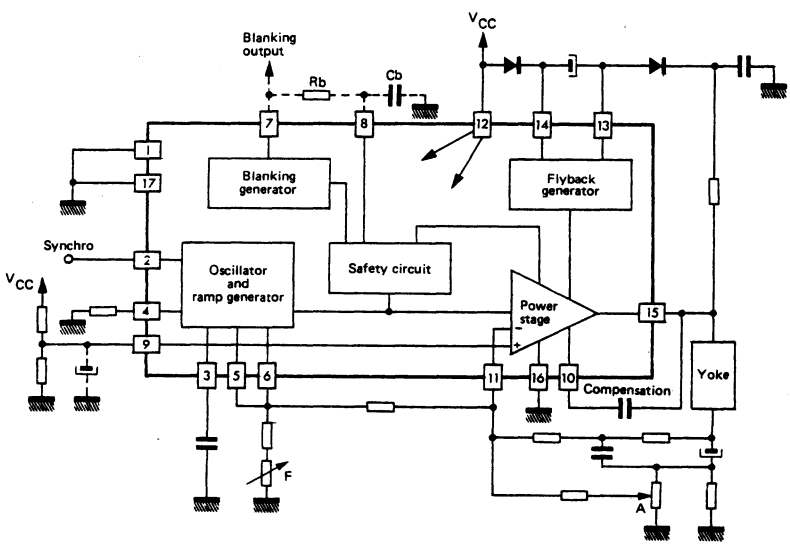
VERTICAL SWEEP FOR LARGE SCREEN COLOR T.V SETS

CASE CB-215



SP SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



NT8041-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

ABSOLUTE MAXIMUM RATINGS

Direct supply voltage	V_{CC}	35	V
Flyback peak voltage	V_{FB}	65	V
Output current (repetitive)	I_O	± 2,5	A
Output current (non repetitive)	I_O	± 3,5	A
Storage and junction temperature	T_j - T_{stg}	−40 → +150	°C
Current at pin 13			
non repetitive	I_{FB}	± 3	A
repetitive *	I_{FB}	± 2	A

*$t \leq 1$ ms for $t_o = 20$ ms

FUNCTIONAL DESCRIPTION

This integrated circuit, specially intended for large screen color T.V. sets, includes the following built in units :

Oscillator

It provides a linear positive going ramp voltage. The amplitude keeps proportional to V_{CC}. The free running frequency is fixed by external components : one capacitor and one resistor. The frequency drift versus V_{CC} or temperature is very low.

Synchronization

The synchro stage is gated in order to allow input pulse action only during the last fourth of free running period.

Blanking

During normal operation the circuit provides a positive blanking pulse of 12.6 Volts amplitude. The duration is slightly adjustable around 1.3 ms, depending on the value of an external resistor (pin 4). The blanking output provides two extra functions :

- When connecting pin 3 to ground there is no sweep and a permanent 12.6 V voltage is provided at blanking output (pin 7), allowing cut-off adjustment of picture tube.
- When there is no fly-back pulse, due to an external circuit failure, the permanent 12.6 V voltage is also present at pin 7, to prevent picture tube damage.

Power amplifier

The output stage is a complete power amplifier with high current capability, allowing direct driving of deflection coils. It includes thermal protection.

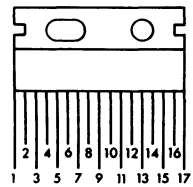
Fly-back generator

During the retrace time the output voltage is permitted to reach 2 x V_{CC}, due to a built in system (fly-back generator) and few external components.

But, the circuit can be used without fly-back generator.

PIN CONFIGURATION

Case : CB-215

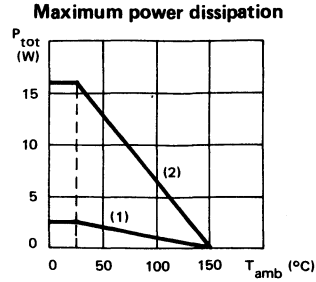


1, 17	Substrat	9	Power amplifier + input
2	Synchronization	10	Compensation
3	Oscillator capacitor	11	Power amplifier – input
4	Reference current	12	$+V_{CC}$
5	Oscillator output	13	Fly-back
6	Frequency adjustment	14	Power stage supply voltage
7	Blanking output	15	Output
8	Safety blanking input	16	Power ground

THERMAL CHARACTERISTICS

Junction-ambient thermal resistance	$R_{th(j-a)}$	35	°C/W
Junction-case thermal resistance	$R_{th(j-c)}$	3	°C/W

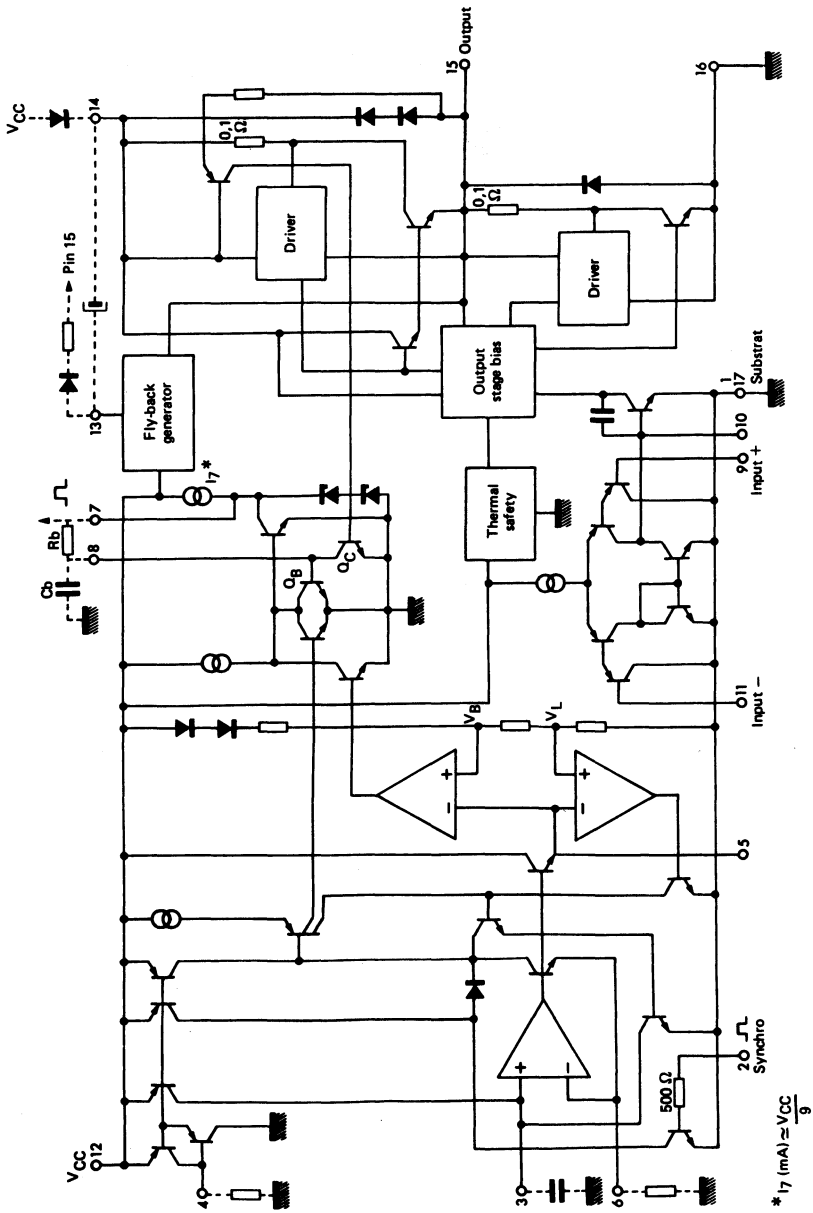
Maximum power dissipation



(1) Without heatsink

(2) With heatsink 5°C/W

SCHEMATIC DIAGRAM

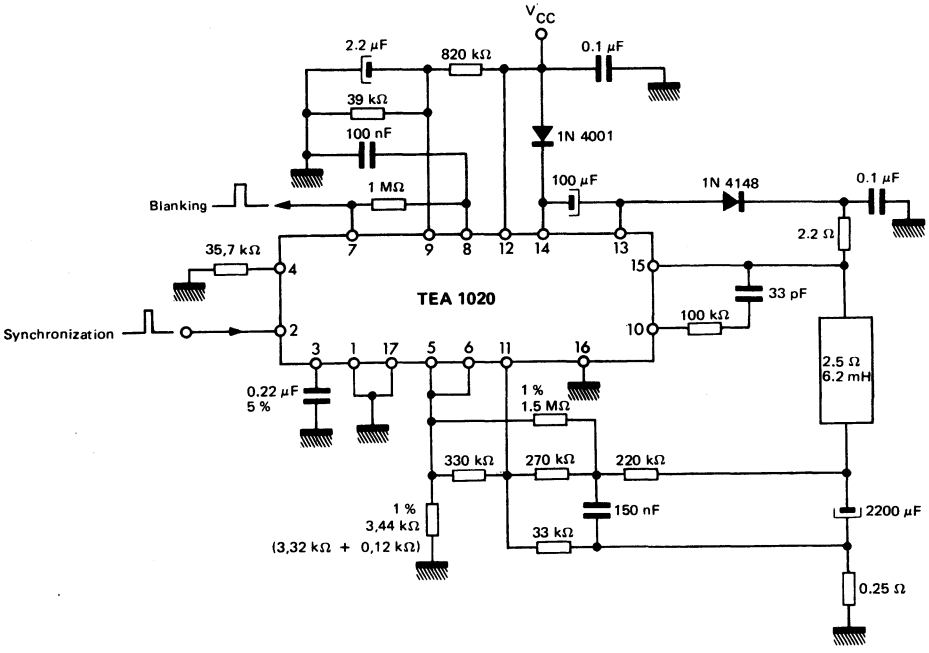


GENERAL ELECTRICAL CHARACTERISTICS (refer to the test circuit) V_{CC} = 18 V, T_{amb} = 25°C

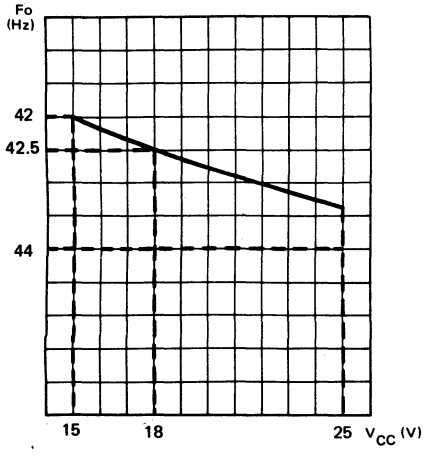
PARAMETERS	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply current without load (P12 and P14)	I12 + I14			25	50	mA
Triggering time (pull-in range)	t_o = 23.5 ms			5.8		ms
Free period time	Co = 0.22 µF R4 = 35.7 kΩ 1 % R5-6 = 3.5 kΩ			23.5		ms
Pin 5 peak to peak oscillator saw-tooth voltage	Co = 0.22 µF R4 = 35.7 kΩ V_{CC} = 20 V			$V_{CC}/3$		V
Blanking pulse time	Co = 0.22 µF R4 = 35.7 kΩ		1.4	1.5	1.6	ms
Pin 7 blanking pulse amplitude				12.6		V
Blanking available Pin 7 current *				150		µA
Blanking time drift versus temperature $\frac{dt}{dT_j}$				1		µs/°C
Pin 5 maximum output current				10		mA
Amplifier input bias current	I9 − I11			100		nA
Synchronization						
Pin 2 input current				1		µA
input impedance				0.5		kΩ
maximum voltage					1.5	V
Oscillator frequency drift versus supply voltage $\frac{dF}{dV_{CC}}$	V_{CC} = 15 → 25 V			0.1		Hz/V
Oscillator frequency drift versus temperature $\frac{dF}{dT_{case}}$				0.003		Hz/°C
Thermal protection				140		°C

* : To get an upper blanking current, put an external resistor from 7 to V_{CC}
The pin 7 capability of switching an external current to ground is 4 mA

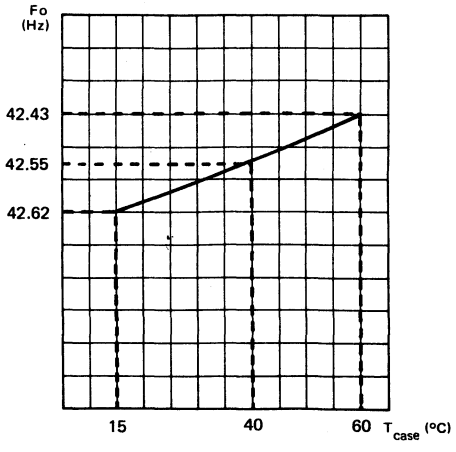
DYNAMIC TEST CIRCUIT



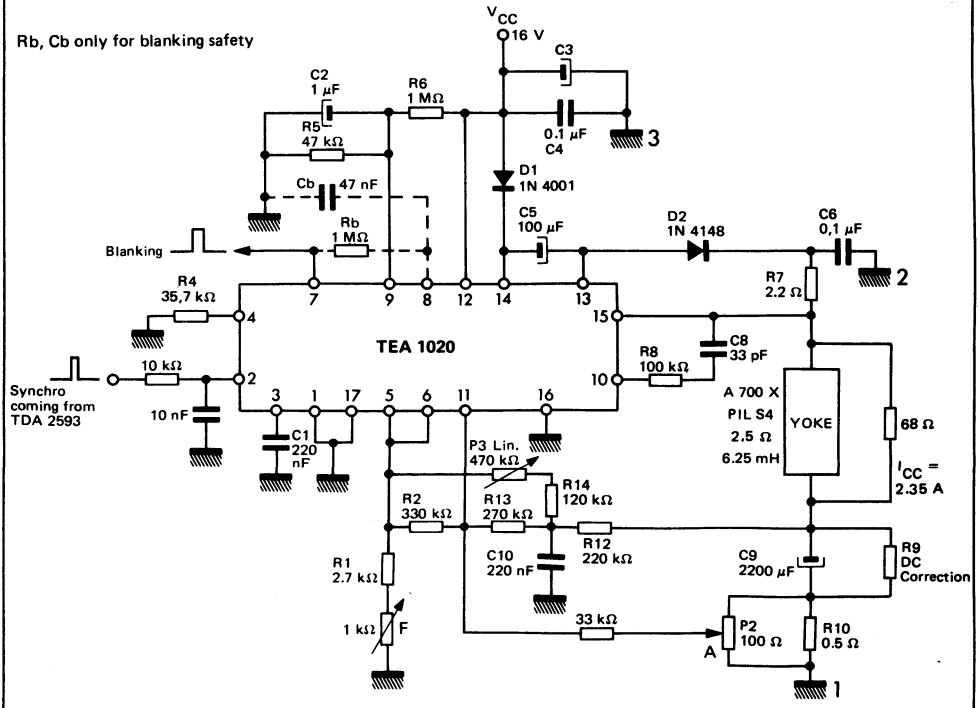
FREQUENCY VARIATION OF UNSYNCHRONIZED OSCILLATOR VERSUS SUPPLY VOLTAGE



FREQUENCY VARIATION OF UNSYNCHRONIZED OSCILLATOR VERSUS TEMPERATURE

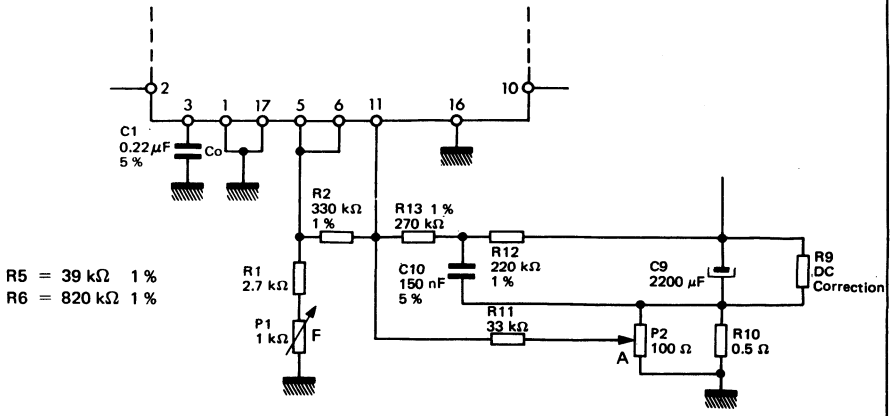


TYPICAL APPLICATION CIRCUIT FOR 110° COLOR TV SETS USING 110° PIL S4 TUBE



If necessary connect a capacitor 1000 pF between pins 9 and 11 to reject line influence.

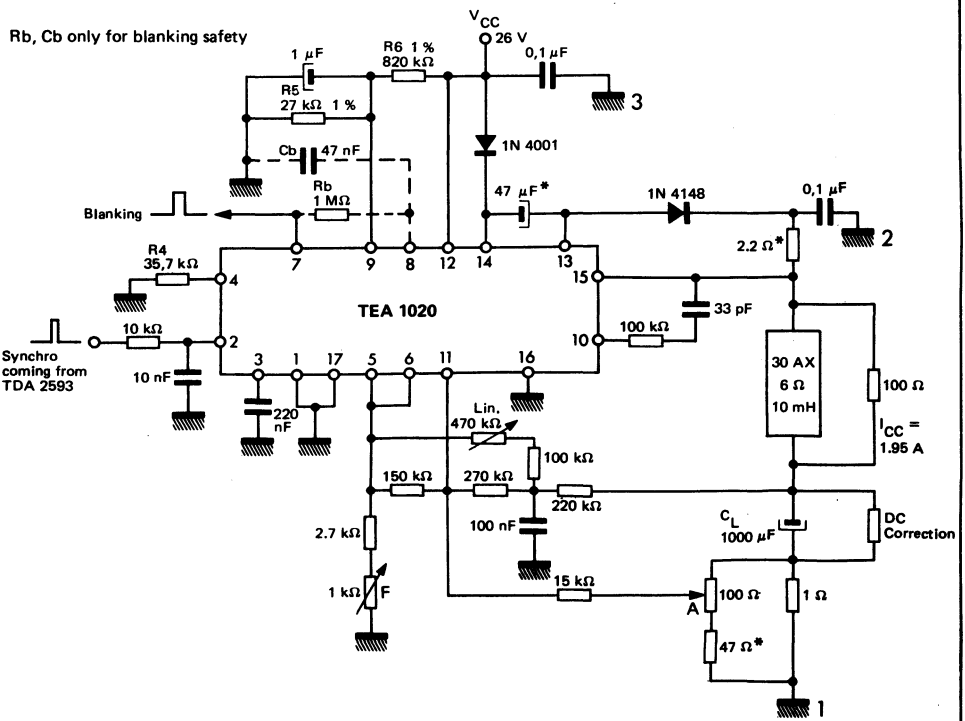
With no linearity adjustment



ELECTRICAL CHARACTERISTICS FOR DEFLECTION CIRCUIT WITH VIDEOCOLOR PIL S4 TUBE

PARAMETERS	SYMBOLS	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
YOKE FEATURES PIL S4							
Resistance	Rd				2.5	3.1	Ω
Inductance	Ld				6.25		mH
Peak to peak yoke current	I_{CC}				2.35	2.6	A
Supply voltage	V_{CC}			15	16	20	V
Fly-back time		V_{CC} = 15 V			1.2		ms
Power dissipation in the IC	P_D	V_{CC} = 15 V			3.6		W
	P_D	V_{CC} = 20 V			5.5		W
Pin 13 operating peak current in fly-back generator					±1.3		A
Non repetitive (accidental) maximum peak current in fly-back		t = 1 ms t_o = 20 ms				±2.2	A
Pin 15 non repetitive (accidental) maximum peak output current						±3	A
Fly-back voltage					32	40	V
Pins 5 and 6 oscillator saw-tooth amplitude		V_{CC} = 15 V			5		V
Pin 7 blanking time		V_{CC} = 15 V			1.25		ms
Junction temperature with heatsink of R_{th} = 10°C/W	T_j	V_{CC} = 15 V T_{amb} = 30°C			80		°C

TYPICAL APPLICATION CIRCUIT FOR 110° COLOR TV SETS USING 110° 30 AX TUBE



For safe working it is important to respect the marked value *

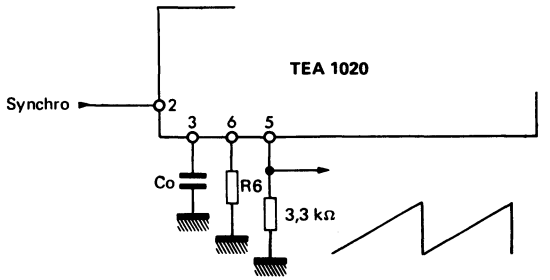
If necessary connect a capacitor 1000 pF between pins 9 and 11 to reject line influence.

ELECTRICAL CHARACTERISTICS FOR DEFLECTION CIRCUIT WITH 30 AX TUBE

PARAMETERS	SYMBOLS	TEST CONDITIONS		MIN.	MAX.	TYP.	UNITS
YOKE FEATURES 30 AX							
Resistance	Rd				6	7.6	Ω
Inductance	Ld				10		mH
Peak to peak yoke current	I_{CC}				2	2.2	A
Supply voltage	V_{CC}			25	26	29	V
Fly-back time		V_{CC} = 26 V				1	ms
Power dissipation in the IC	P_D	V_{CC} = 26 V			5		W
	P_D	V_{CC} = 29 V			6		W
Pin 13 operating peak current in fly-back generator					±1.1		A
Non repetitive (accidental) maximum peak current in fly-back		t = 1 ms t_o = 20 ms				2	A
Pin 15 non repetitive (accidental) maximum peak output current						2	A
Fly-back voltage					52	60	V
Pins 5 and 6 oscillator saw-tooth amplitude		V_{CC} = 26 V			8		V
Pin 7 blanking time		V_{CC} = 26 V			1.25		ms
Junction temperature with heatsink of R_{th} = 10°C/W	T_j	V_{CC} = 26 V T_{amb} = 30 °C			95		°C

APPLICATION INFORMATION

Low impedance oscillator saw-tooth output **Pin 5**



No effect of the load on the free frequency

The values of R6 becomes then twice the value of R5-6 in the normal application

$Co = 0.22\ \mu F$ $R6 = 7\ k\Omega$ $t_o = 23.5$ ms

(R6 can be in series with a potentiometer to adjust the frequency)

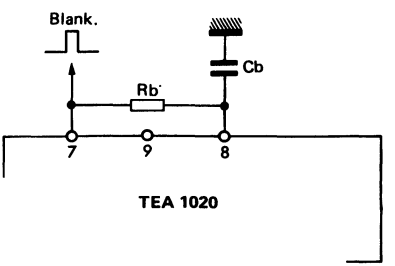
Blanking time

Can be adjusted by the value of R4.

$R4 = 30.1\ k\Omega$ $Co = 0.22\ \mu F$ $t_{blank.} = 1.25$ ms

Blanking safety

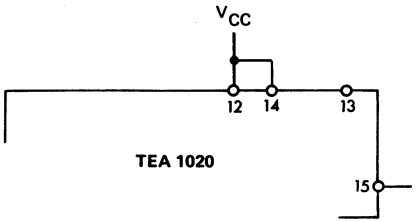
When there is no sweep, blanking is switched "ON" automatically if Rb and Cb are connected.



Rb = 1 MΩ
Cb = 47 nF

Application without fly-back generator

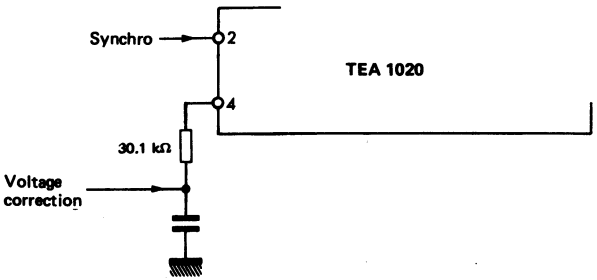
For example : 20 AX yoke



Automatic format correction

The saw-tooth amplitude is proportional to V_{CC} so that the format is made automatically when the supply voltage is given by the horizontal transformer. In an other case two other possibilities.

a – When the voltage correction comming from the beam current increase and the amplitude must decrease.

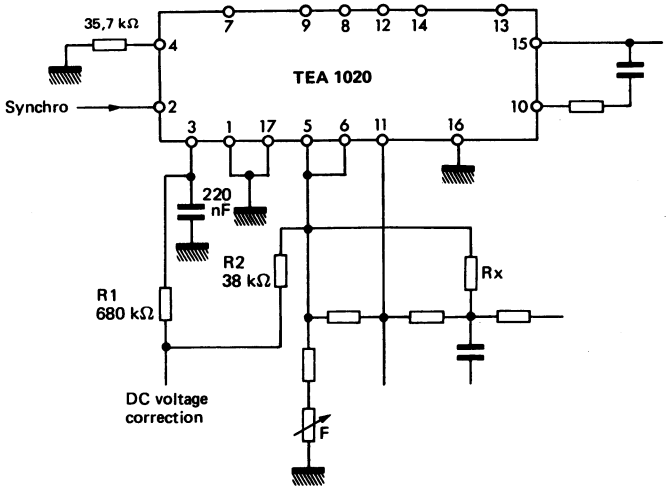


Format correction	5 %
V_{CC}	20 V
Voltage correction	0 - 1 V

No effect on the free frequency

In this case if the amplitude decreases of 5% the blanking time increases of 5%.

b – When the voltage correction decreases and the amplitude must decrease

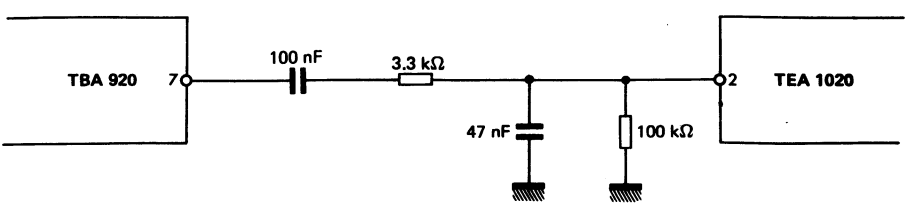


Rx must be adjusted to compensate the parabolic effect of R1 if there is no linearity adjustment.

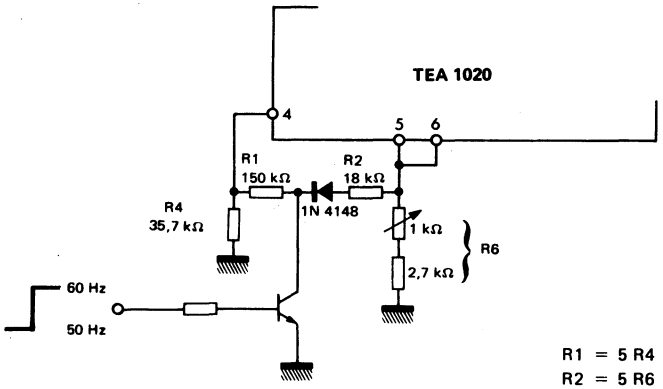
Format correction	5 %
DC voltage correction	2 V – 0
V_{CC}	20 V

– no effect on free frequency
– Blanking time variation ⩽ 3 %

Synchronization network for synchro coming from TBA 920 Pin 7



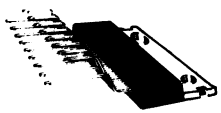
Automatic standard switching with constant amplitude (50 Hz · 60 Hz)



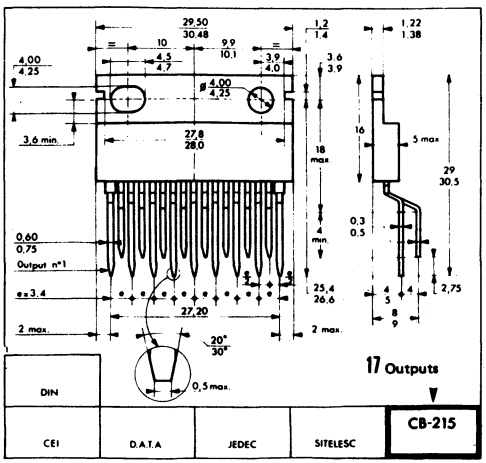
R1 = 5 R4
R2 = 5 R6

Printed circuit board layout information refered to the application diagram 110° S4 tube

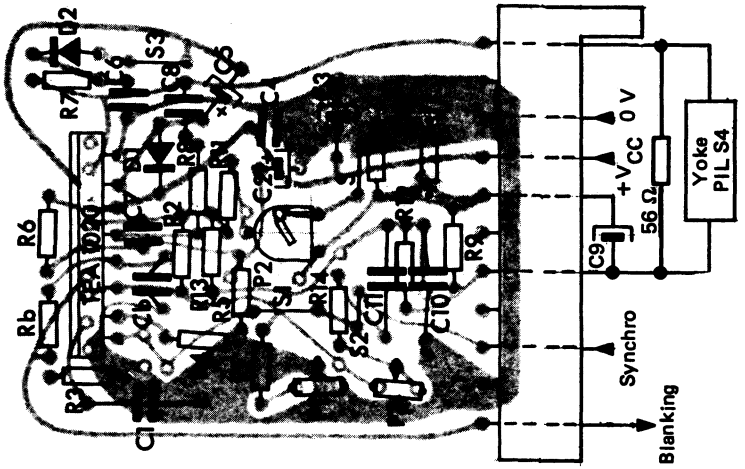
CASE CB-215



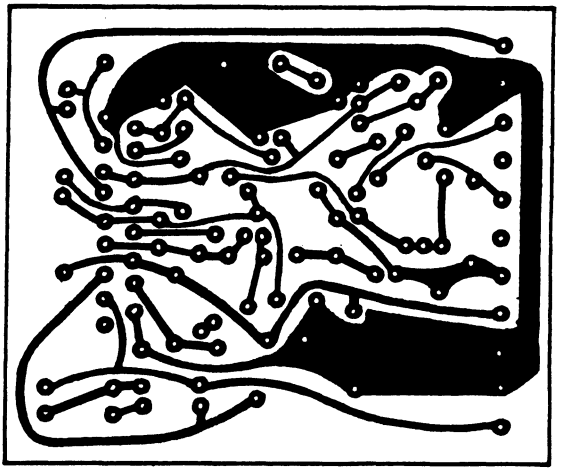
SP SUFFIX
PLASTIC PACKAGE



Component side



Copper side



– Each power ground 1, 2, 3 (refer to the application diagram 110° S4 tube) must be connected to the –supply (pin 16) with a minimum copper resistance.
Other grounds (oscillator and outputs) must be well decoupled from the power ground and connected to the –supply.

– Copper connections to pins 11 and 9 as short as possible to reject the line influence

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TEA1030B

TV VIDEO PROCESSING I.C FOR COLOR TV SET

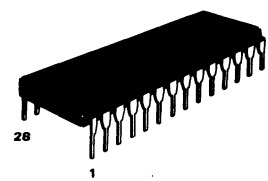
The TEA1030B is a new video processor I.C compatible with all standards PAL/SECAM/NTSC and new needs such as teletex, antiope, TV games, remote control etc...

PRINCIPAL FEATURES

- Matrixing of R, G, B signal from (R-Y) and (B-Y)
- Electronic control of contrast, brightness and saturation
- Three channels video switch, for selection of internal signal (broadcast) or external R, G, B information
- Automatic cut-off adjustment.

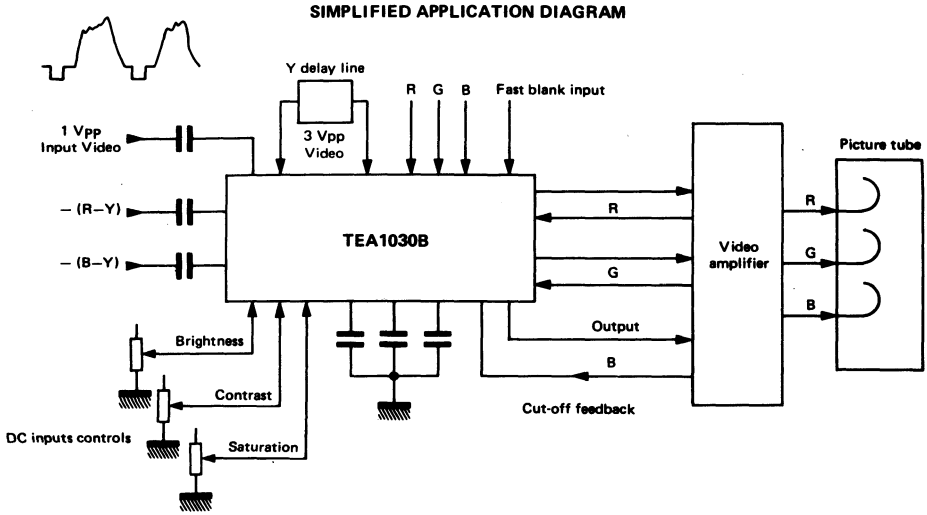
TV VIDEO PROCESSING I.C FOR COLOR TV SET

CASE CB-132



DP SUFFIX
PLASTIC PACKAGE

SIMPLIFIED APPLICATION DIAGRAM



NT8243-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

In order to ensure compatibility with standard video transmission systems the luma input is a high impedance, AC coupled, designed to accept a 1 V video signal. After a X3 gain voltage amplifier the inverted luma signal is brought out to the luma delay line. This output is low impedance to match the delay line accurately, and as the signal is inverted, it is highly suitable for driving a synchronization separator such as the TDA2593 or TBA920.

Following the luma delay line the video is controlled by an electronic gain control with a range of 40 dB.

The DC luma level is locked on the black level (cut-off current) with a range of ± 1 V depending of brightness. The DC voltage level is clamped during each line retrace and an external capacitor holds this voltage during the line trace.

After brightness and contrast controls the luminance is fed to the matrix with R-Y and B-Y signals.

The voltage gain of R-Y and B-Y is controlled by saturation. The saturation is in tracking with contrast and then the R-Y and B-Y signals are fed to the matrix and summed with on-screen display signals which are controlled in gain by the luma contrast control. Each input is AC coupled and black level clamped using the coupling capacitor as the storage element for the clamp voltage.

All the controls have an active range of 0.5 to 4.5 V making them compatible with D/A convertor derived control signals, such as those from remote control systems. The three on-chip output stages are high gain class B amplifiers with the gain set by parallel feedback resistor. This gives a well defined gain and stable output voltage level. The beam current in each cathode of the picture tube is monitored by a high-voltage PNP transistor. A sample of this current is fed back to the IC.

In the luma signal a reference black level is inserted during the line and frame blanking periods. While this reference level is present, and after the frame flyback, the output stage feedback input goes high impedance and an internal comparator is actived.

This circuit compares an internal reference voltage to the voltage developed across an external resistor by the picture tube beam current, and the output voltage is trimmed to get the desired cathode current value.

An internal logic delivers blanking and clampling pulses from the normalized sand castle and frame retrace signals.

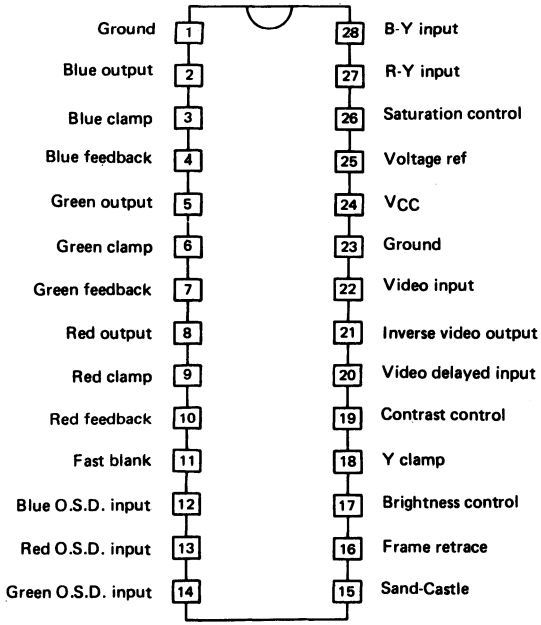
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	16	V
Operating temperature range	T_{oper}	0, + 70	°C
Storage temperature range	T_{stg}	−65, + 150	°C

THERMAL CHARACTERISTICS

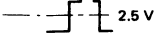
Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	55	°C/W

PIN CONFIGURATION

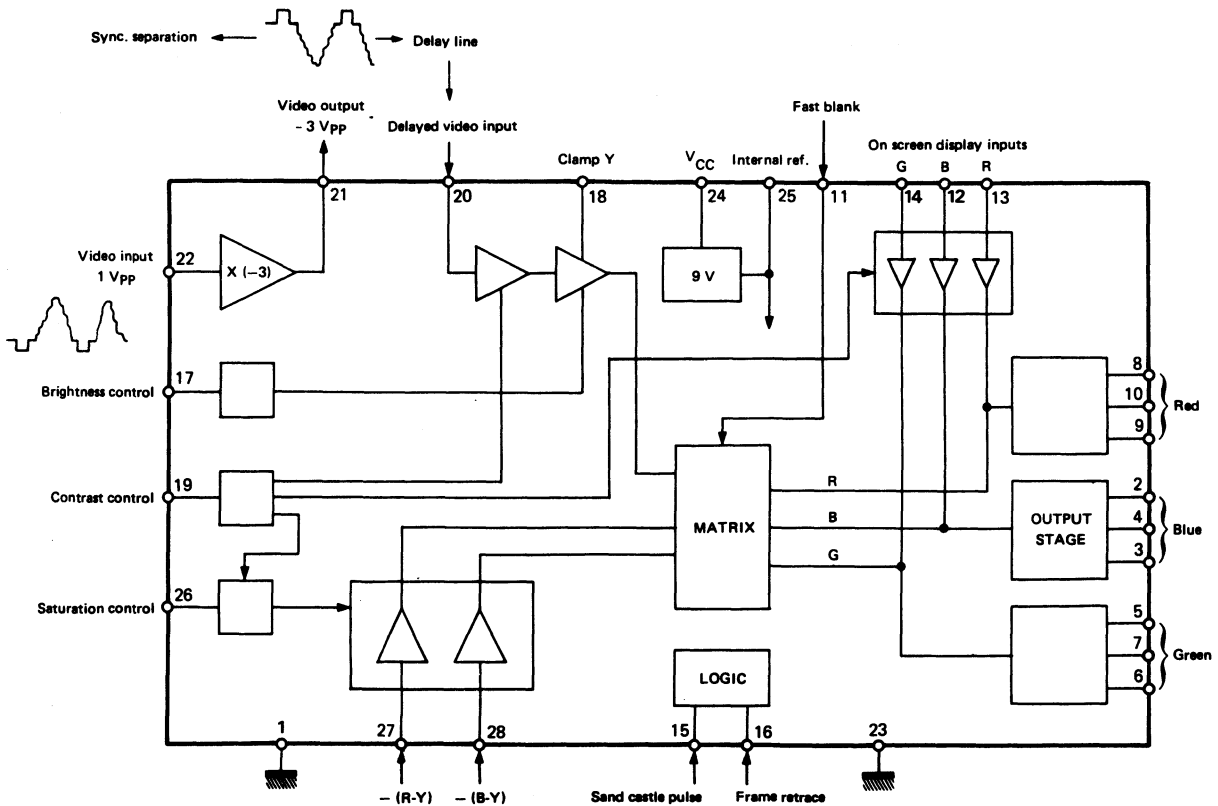


ELECTRICAL CHARACTERISTICS

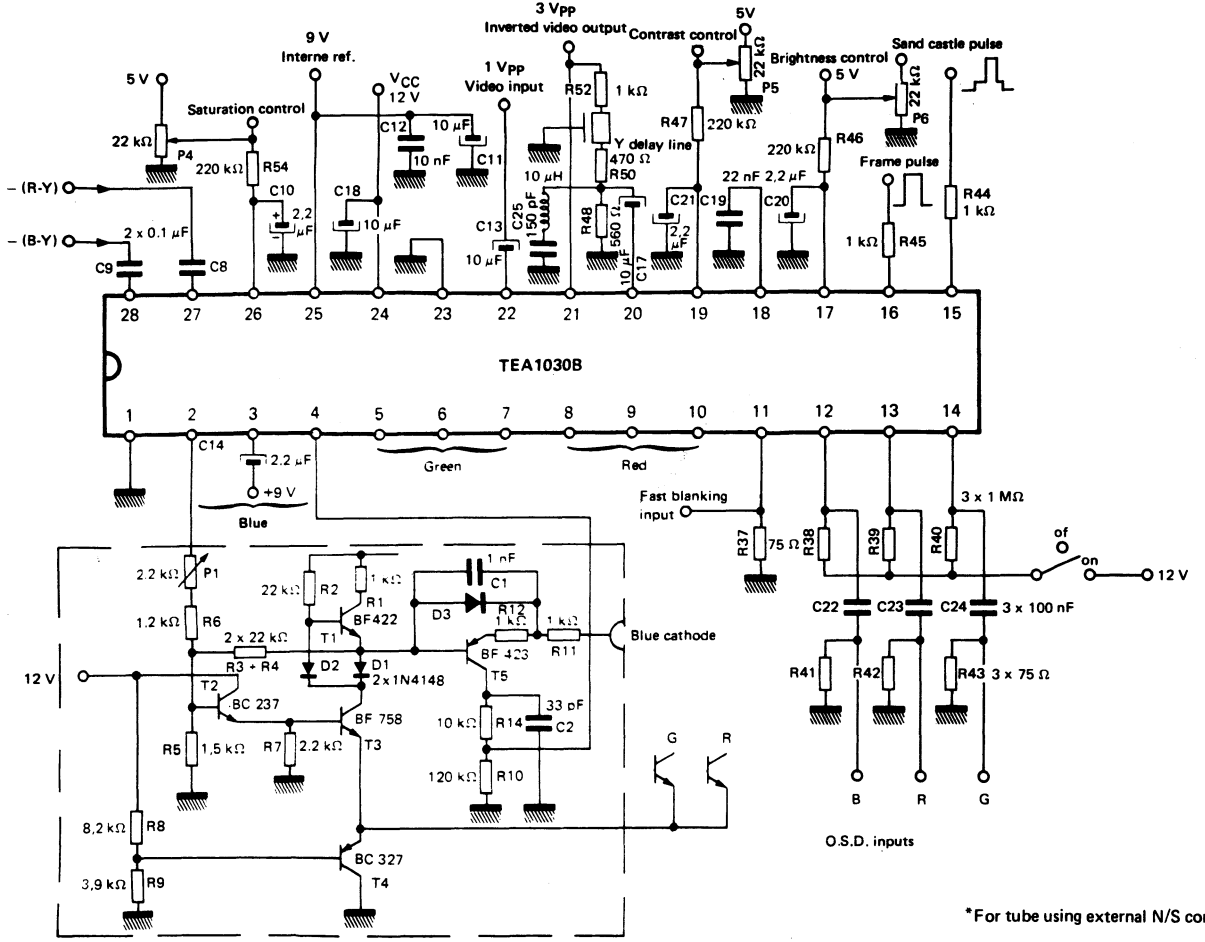
$T_{amb} = +25°C$; $V_{CC} = 12$ V (unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage	Pin 24	V_{CC}	10.8	12	13.2	V
Supply current	Pin 24	I_{CC}	–	55	–	mA
Internal voltage ref.	Pin 25	V_Z	–	9	–	V
Video input	Pin 22	–	–	1	–	V_{PP}
Output voltage inv. video (V22 = 1 V_{PP})	Pin 21	–	–	3	–	V_{PP}
Max output voltage swing	Pin 21	–	–	7	–	V_{PP}
–3 dB bandwidth	Pins 2-5-8	–	4.5	5	–	MHz
(R–Y) input voltage (100 % modulation)	Pin 27	–	–	1.4	2	V_{PP}
(B–Y) input voltage (100 % modulation)	Pin 28	–	–	1.0	2	V_{PP}
– 3 dB bandwidth		–	1.5		–	MHz
Luma gain						
G21/22	Pin 21	–	8.5	10	11.5	dB
G2/20 ; G5/20 ; G8/20 at max adjustement	Pins 2-5-8	–	15.5	17	18.5	dB
Differential gain fault : Luma channel		–	–	–	0.5	dB
Chroma gain						
G8/27 at max adjustment		–	11.5	13	14.5	dB
G2/28 at max adjustment		–	11.5	13	14.5	dB
Chroma gain ratio at max adjustment		–	–	–	0.5	dB
Voltage control for electronic potentiometers						
Contrast (Pin 19) - Saturation (Pin 26)						
Range of adjustment						
V19 = 5 V ; V26 = 5 V		–	–	G_{max}	–	dB
V19 = 0 V ; V26 = 0 V Attenuation		–	40	46	–	dB
Brightness (Pin 17)						
V_{out} adjustment (V17 varying from 0 to 5 V)		–	–	± 1	–	V
On screen display inputs	Pins 12-13-14					
OSD input voltage (Black to white level)		–	–	1	2	V
OSD gain (V2/12 ; V8/13 ; V5/14)		–	13.5	15	17	dB
OSD generator max impedance		–	–	–	75	Ω
- 3 dB bandwidth		–	5	–	–	MHz
Fast blanking threshold		–	–	0.5	–	V
Max output voltage swing	Pins 2-5-8	–	7	8	–	V_{PP}
Feed-back threshold	Pins 4-7-10	–	1.7	2	2.4	V
Sand-Castle input	Pin 15					
Clamp Y  8 V			–	8	–	V
Line blanking  2.5 V			–	2.5	–	V
Frame return input voltage	Pin 16	–	–	2.5	–	V
Control current (V15 = V16 = 4 V)			–	0.5	–	mA
Matrix coefficient						
Red output (V5/V8 with V27 = 1 V ; V28 = 0 ; V20 = 0)				0.51	–	–
Blue output (V5/V2 with V27 = 0 ; V28 = 1 ; V20 = 0)		–	–	0.19	–	–

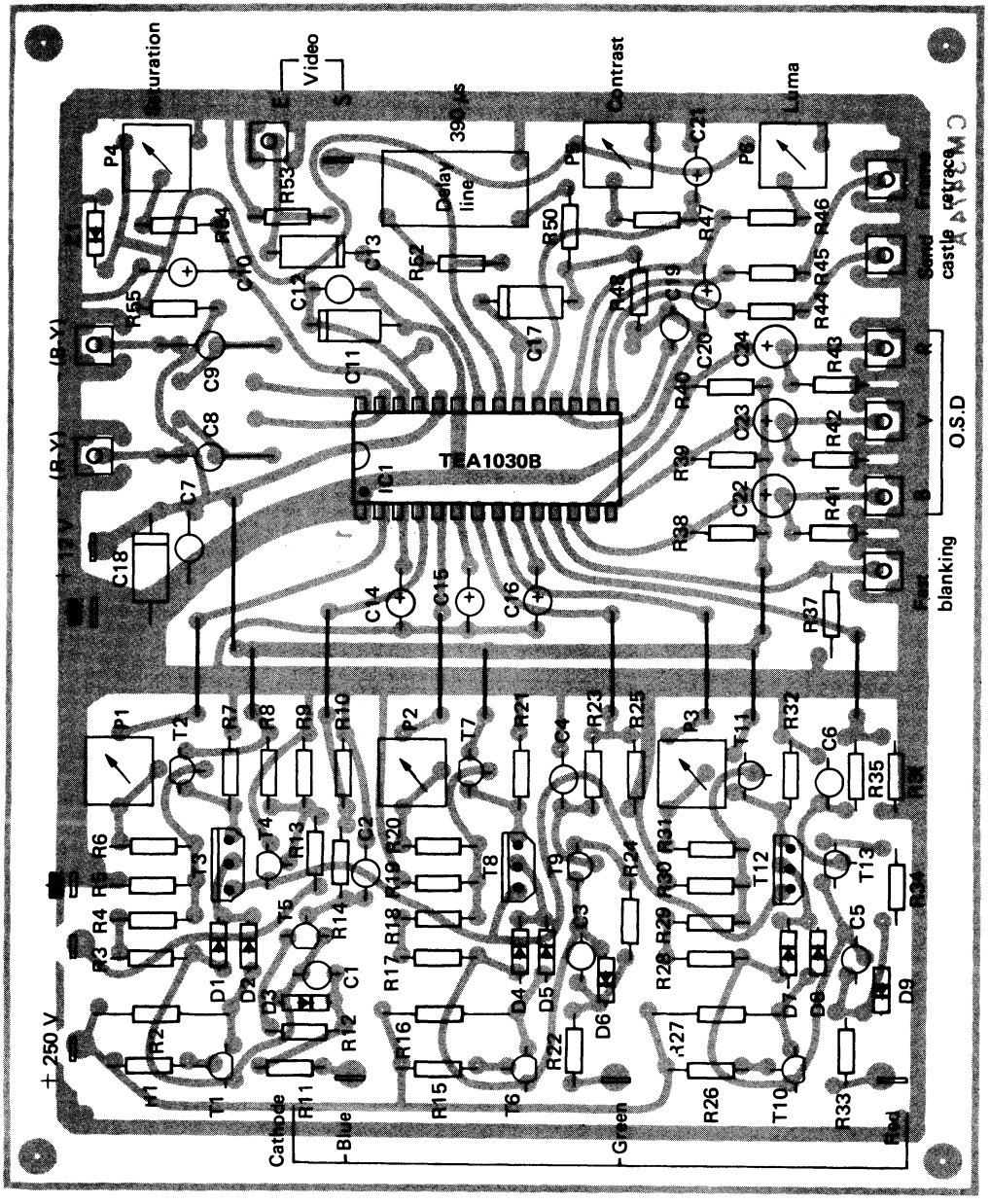
BLOCK DIAGRAM



APPLICATION CIRCUIT



COMPONENT SIDE



N°	Value	P
R1	1 kΩ	1/4 W
R2	22 kΩ	1 W
R3	22 kΩ	1/4 W
R4	22 kΩ	"
R5	1.5 kΩ	"
R6	1.2 kΩ	"
R7	2.2 kΩ	"
R8	8.2 kΩ	"
R9	3.9 kΩ	"
R10	120 kΩ	"
R11	1 kΩ	"
R12	1 kΩ	"
R13	220 kΩ	"
R14	10 kΩ	"
R15	1 kΩ	"
R16	22 kΩ	1 W
R17	22 kΩ	1/4 W
R18	22 kΩ	"
R19	1.5 kΩ	"
R20	1.2 kΩ	"
R21	2.2 kΩ	"
R22	1 kΩ	"
R23	10 kΩ	"
R24	1 kΩ	"
R25	120 kΩ	1/4 W
R26	1 kΩ	"
R27	22 kΩ	1 W

N°	Value	P
R28	22 kΩ	1/4 W
R29	22 kΩ	"
R30	1.5 kΩ	"
R31	1.2 kΩ	"
R32	2.2 kΩ	"
R33	1 kΩ	"
R34	1 kΩ	"
R35	10 kΩ	"
R36	120 kΩ	"
R37	75 Ω	"
R38	1 MΩ	"
R39	1 MΩ	"
R40	1 MΩ	"
R41	75 Ω	"
R42	75 Ω	"
R43	75 Ω	"
R44	1 kΩ	"
R45	1 kΩ	"
R46	220 kΩ	"
R47	220 kΩ	"
R48	560 Ω	"
R50	470 Ω	1/4 W
R52	1 kΩ	"
R53	1 kΩ	"
R54	220 kΩ	"
R55	1 kΩ	"

N°	Value	U
C1	1 nF	
C2	33 pF	
C3	1 nF	
C4	33 pF	
C5	1 nF	
C6	33 pF	
C7	10 nF	63 V
C8	100 nF	63 V
C9	100 nF	63 V
C10	2.2 µF	35 V
C11	10 µF	63 V
C12	10 nF	63 V
C13	10 µF	63 V
C14	2.2 µF	35 V
C15	2.2 µF	35 V
C16	2.2 µF	35 V
C17	10 µF	63 V
C18	10 µF	63 V
C19	22 nF	
C20	2.2 µF	35 V
C21	2.2 µF	35 V
C22	4.7 µF	63 V
C23	4.7 µF	63 V
C24	4.7 µF	63 V
C25	150 pF	

N°	Typ
T1	BF 422
T2	BC 237
T3	BF 758
T4	BC 327
T5	BF 423
T6	BF 422
T7	BC 237
T8	BF 758
T9	BF 423
T10	BF 422
T11	BC 237
T12	BF 758
T13	BF 423

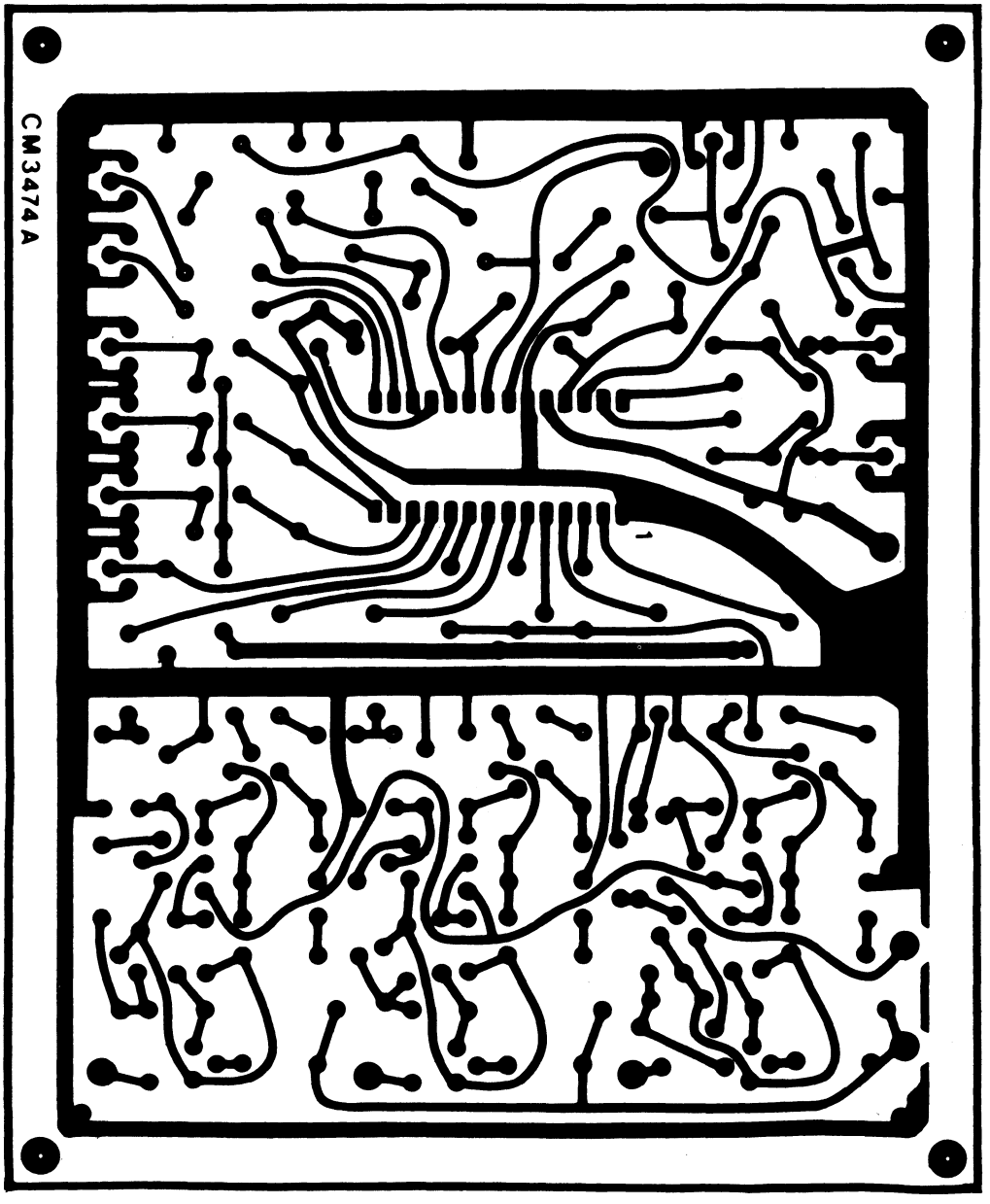
N°	Typ
IC1	TEA1030B

N°	Value
P1	2.2 kΩ
P2	2.2 kΩ
P3	2.2 kΩ
P4	22 kΩ
P5	22 kΩ
P6	22 kΩ

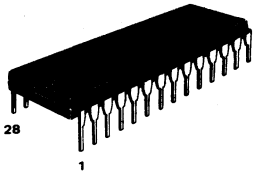
N°	Typ
DL	TDK

N°	Typ
D1	1N4148
D2	"
D3	"
D4	"
D5	"
D6	"
D7	"
D8	"
D9	"
Z1	5 V

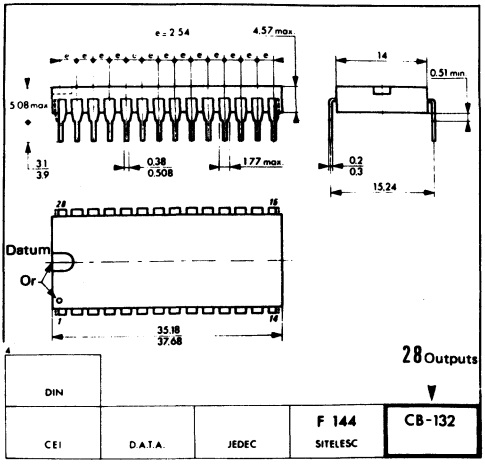
COPPER SIDE



CASE CB-132



DP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

MULTI CHANNELS AF STEREOPHONIC SWITCH WITH PRIORITY

COMMUTATEUR BF STEREO A PLUSIEURS VOIES A PRIORITE

This integrated circuit allows to select one of:

- **five stereophonic channels with the J-TEA1035, TEA1035 DP-24 version**
- **four stereophonic channels with the TEA1035 DP-18 version**
- **three stereophonic channels with the TEA1035 DP-14 version**

Using several circuits allows to select one of N channels.
Control process with priority and negative logic
Principal characteristics:

- **Non selected channel separation** — **80 dB typ.**
- **Distortion** — **< 0.01 % typ.**
- **Circuit protected against short-circuit on the outputs and on the bias voltage pin.**

Ce circuit permet de sélectionner une voie stéréo parmi:

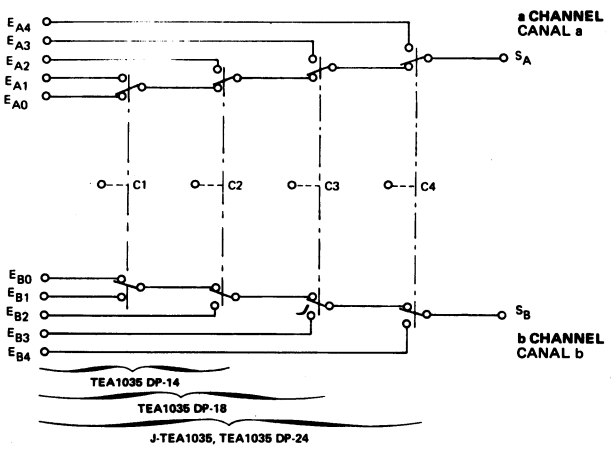
- 5 voies stéréo avec les versions J-TEA 1035, TEA 1035 DP-24
- 4 voies stéréo avec la version TEA 1035 DP-18
- 3 voies stéréo avec la version TEA 1035 DP-14

L'association de plusieurs circuits permet de sélectionner une voie parmi N.
Le système de commande est à priorité et à logique négative.
Caractéristiques principales:

- Isolation d'une voie non sélectionnée — 80 dB typ.
- Distorsion — <0,01 % typ.
- Circuit protégé contre les courts-circuits sur les sorties et la polarisation.

FUNCTIONNAL DIAGRAM

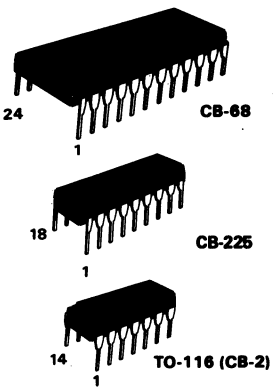
SCHEMA DE PRINCIPE



MULTI CHANNELS AF STEREOPHONIC SWITCH WITH PRIORITY

COMMUTATEUR BF STEREO A PLUSIEURS VOIES A PRIORITE

CASES / BOITIERS



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE

TRUTH TABLE
TABLE DE VERITE

C1	C2	C3	C4	Switch channel *Canal commuté*
V_H	V_H	V_H	V_H	0
V_L	V_H	V_H	V_H	1
X	V_L	V_H	V_H	2
X	X	V_L	V_H	3
	X	X	V_L	4

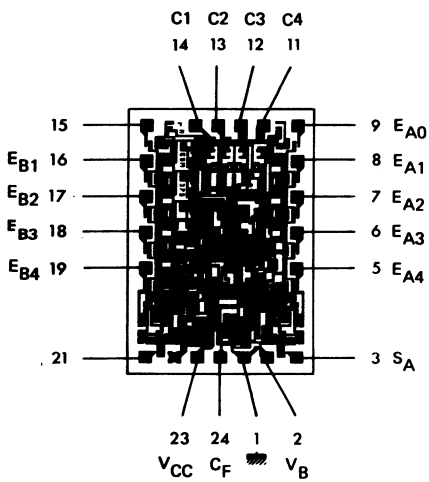
TEA1035 DP-14
TEA1035 DP-18
J-TEA1035, TEA1035 DP-24

NT8012

PIN CONFIGURATIONS
BROCHAGES

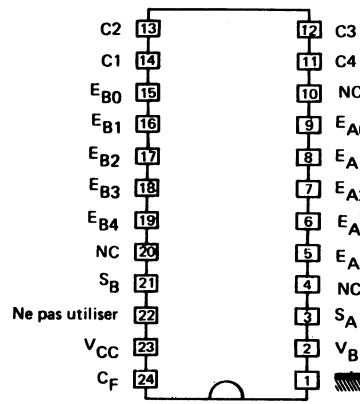
J-TEA1035

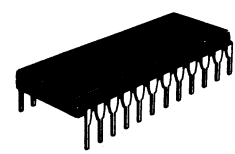
In chip (Dimension : 1720 x 2520 µm)
En pastille



TEA1035 DP-24

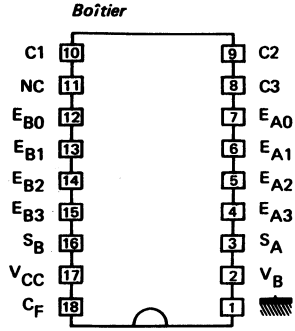
Case : CB-68
Boîtier

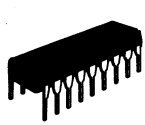




TEA1035 DP-18

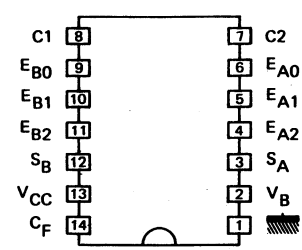
Case : CB-225
Boîtier

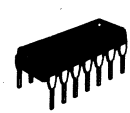




TEA1035 DP-14

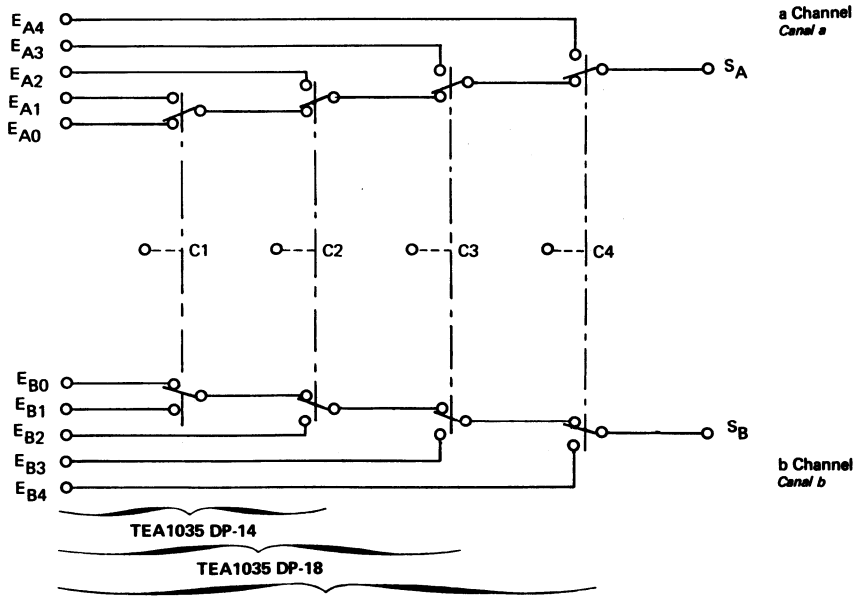
Case : TO-116 (CB-2)
Boîtier





FUNCTIONAL DIAGRAM
SCHEMA DE PRINCIPE

See application diagram : J-TEA1035, TEA1035 DP-24 (page 6/9)
Voir schéma d'application : TEA1035 DP-18 (page 7/9)
TEA1035 DP-14 (page 8/9)



TRUTH TABLE
TABLE DE VERITE

C1	C2	C3	C4	Switch channel *Canal commuté*
V_H	V_H	V_H	V_H	0
V_L	V_H	V_H	V_H	1
	V_L	V_H	V_H	2
X	X	V_L	V_H	3
X		X	V_L	4

TEA1035 DP-14
TEA1035 DP-18
J-TEA1035, TEA1035 DP-24

ABSOLUTE RATINGS (LIMITING VALUES)
VALEURS LIMITES ABSOLUES D'UTILISATION

PARAMETERS *PARAMETRES*		SYMBOLS *SYMBOLES*	PINS *BROCHES*	VALUES *VALEURS* MIN.	TYP.	MAX.	UNITS *UNITES*
Supply voltage *Tension d'alimentation*	J-TEA1035, TEA1035 DP-24 TEA1035 DP-18 TEA1035 DP-14	V_{CC}	23 17 13	8		18	V
Junction temperature *Température de jonction*		T_j				150	°C
Storage temperature *Température de stockage*		T_{stg}		− 25		+150	°C

ELECTRICAL CHARACTERISTICS *
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C V_{CC} = 8 → 18 V

PARAMETERS *PARAMETRES*		SYMBOLS *SYMBOLES*	PINS *BROCHES*	VALUES *VALEURS* MIN.	TYP.	MAX.	UNITS *UNITES*
Supply current *Courant d'alimentation*	J-TEA1035, TEA1035 DP-24 TEA1035 DP-18 TEA1035 DP-14	I_{CC}	23 17 13		10	20	mA
Supply voltage rejection ratio *Taux de réjection des alimentations*	J-TEA1035, TEA1035 DP-24 TEA1035 DP-18 TEA1035 DP-14	SVR	3, 21 3, 16 3, 12	48			dB
$C_F = 1\ \mu F$ $C_F = 0\ \mu F$					40		dB
DC bias voltage *Tension continue de polarisation*		V_B	2	$\frac{V_{CC}-2}{2}$		$\frac{V_{CC}-0,5}{2}$	V
Input current *Courant d'entrée*	J-TEA1035, TEA1035 DP-24	I_I	5-15, 6-16, 7-17, 8-18, 9-10	−1		+1	µA
	TEA1035 DP-18		4, 5, 6, 7, 12, 13, 14, 15				
	TEA1035 DP-14		4, 5, 6, 9, 10, 11				
Input current dispersion between the two way of a same channel *Dispersion des courants d'entrée des voies d'un même canal*						100	nA
Input impedance *Impédance d'entrée*		Z_I		47			kΩ
Input capacitance *Capacité d'entrée*		C_I				10	pF

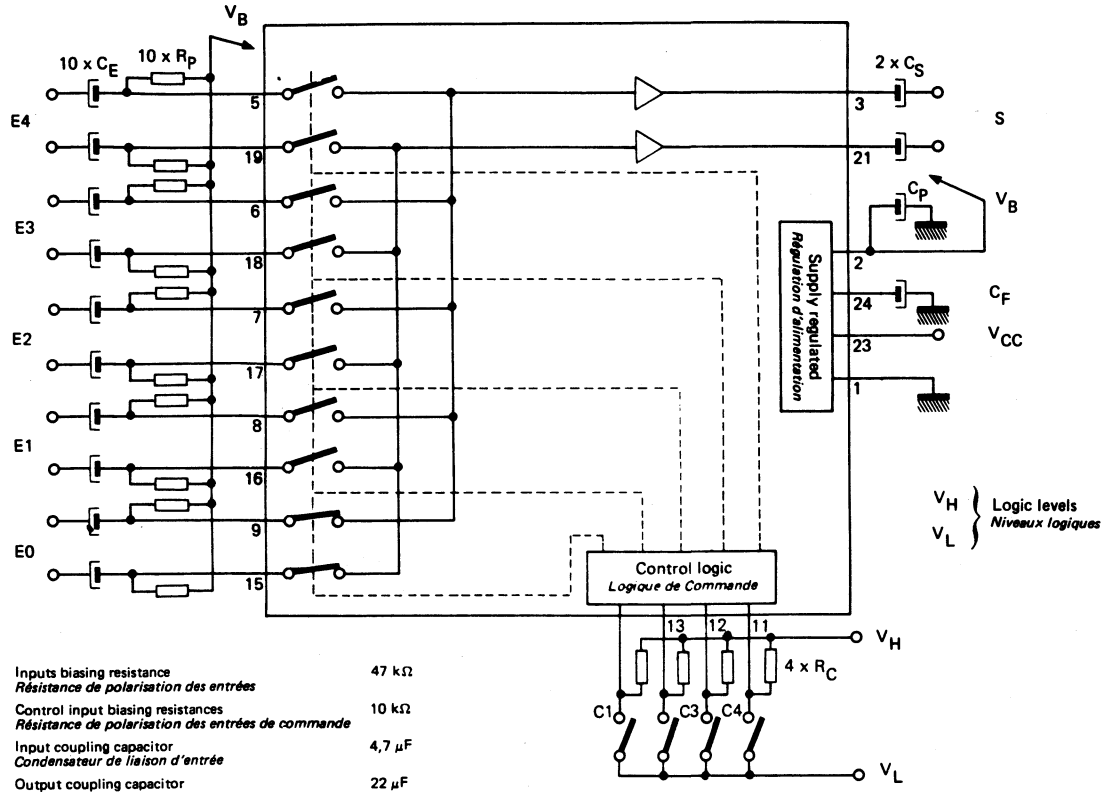
* Characteristics measured with external component schown in application circuits
Caractéristiques mesurées avec les composants extérieurs indiqués dans les schémas d'application

ELECTRICAL CHARACTERISTICS (continued)
CARACTERISTIQUES ELECTRIQUES (suite)

PARAMETERS *PARAMETRES*	SYMBOLS *SYMBOLES*	PINS *BROCHES*	VALUES *VALEURS* MIN.	TYP.	MAX.	UNITS *UNITES*
Capacitance between two nearest inputs *Capacité entre deux entrées voisines*				3		pF
Switching threshold *Seuil de commutation sur les entrées de commande* J-TEA1035, TEA1035 DP-24	V_H	11, 12, 13, 14	4,5			V
TEA1035 DP-18		8, 9, 10				
TEA1035 DP-14	V_L	7, 8			1,5	V
Separation between 20 Hz and 15 kHz *Isolation de 20 Hz à 15 kHz*						
Generator impedance $< 2{,}2\ k\Omega$ *Impédance du générateur*						
Input signal level $1\ V_{eff}$ *Niveau du signal d'entrée*						
Between a non selected way and corresponding channel output *Entre une voie non commutée et la sortie du canal correspondant*			70	80		dB
Between a selected way and the other channel output *Entre une voie commutée et la sortie de l'autre canal*			70	80		dB
Control inputs impedance *Impédance des entrées de commande*			0,1	3		MΩ
Output impedance *Impédance de sortie* J-TEA1035, TEA1035 DP-24	Z_O	3, 21			2,2	kΩ
TEA1035 DP-18		3, 16				
TEA1035 DP-14		3, 12				
Gain *Gain*	G		−0,5	0	+0,5	dB
Bandwidth *Bande passante* at *à* ±0,1 dB	B		20		15000	Hz
Distortion *Distorsion* $V_{CC} = 14\ V$ $V_I = 0{,}2\ V_{eff}$	d			0,004	0,1	%
$V_I = 0{,}5\ V_{eff}$				0,003	0,2	%
$V_I = 1\ V_{eff}$				0,005	0,5	%
Noise voltage *Tension de bruit* $R_G \leq 2{,}2\ k\Omega$	V_n				10	μV

APPLICATION DIAGRAM
SCHEMA D'APPLICATION

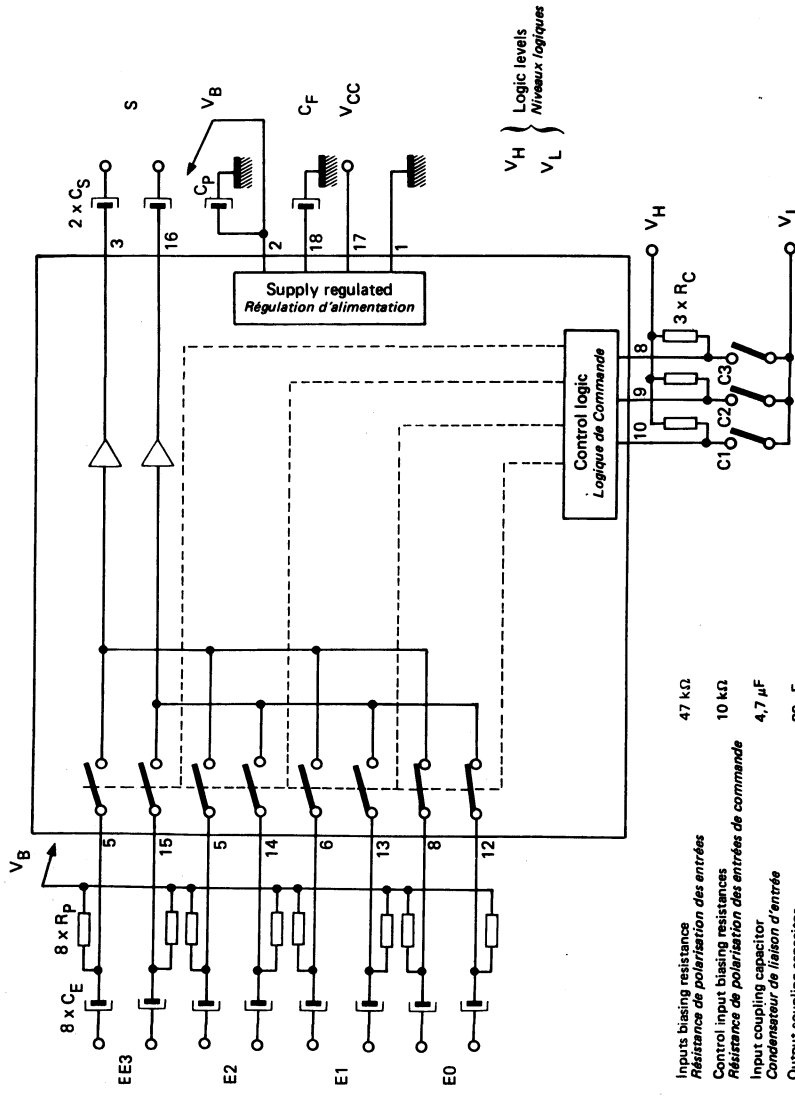
J-TEA1035, TEA1035 DP-24



R_P	Inputs biasing resistance *Résistance de polarisation des entrées*	47 kΩ
R_C	Control input biasing resistances *Résistance de polarisation des entrées de commande*	10 kΩ
C_E	Input coupling capacitor *Condensateur de liaison d'entrée*	4,7 µF
C_S	Output coupling capacitor *Condensateur de liaison de sortie*	22 µF
C_P	Bias filter capacitor *Condensateur de filtrage de la polarisation*	100 µF
C_F	Supply voltage filter capacitor *Condensateur de filtrage de l'alimentation*	0 µF *or/ou* 1 µF

APPLICATION DIAGRAM
SCHEMA D'APPLICATION

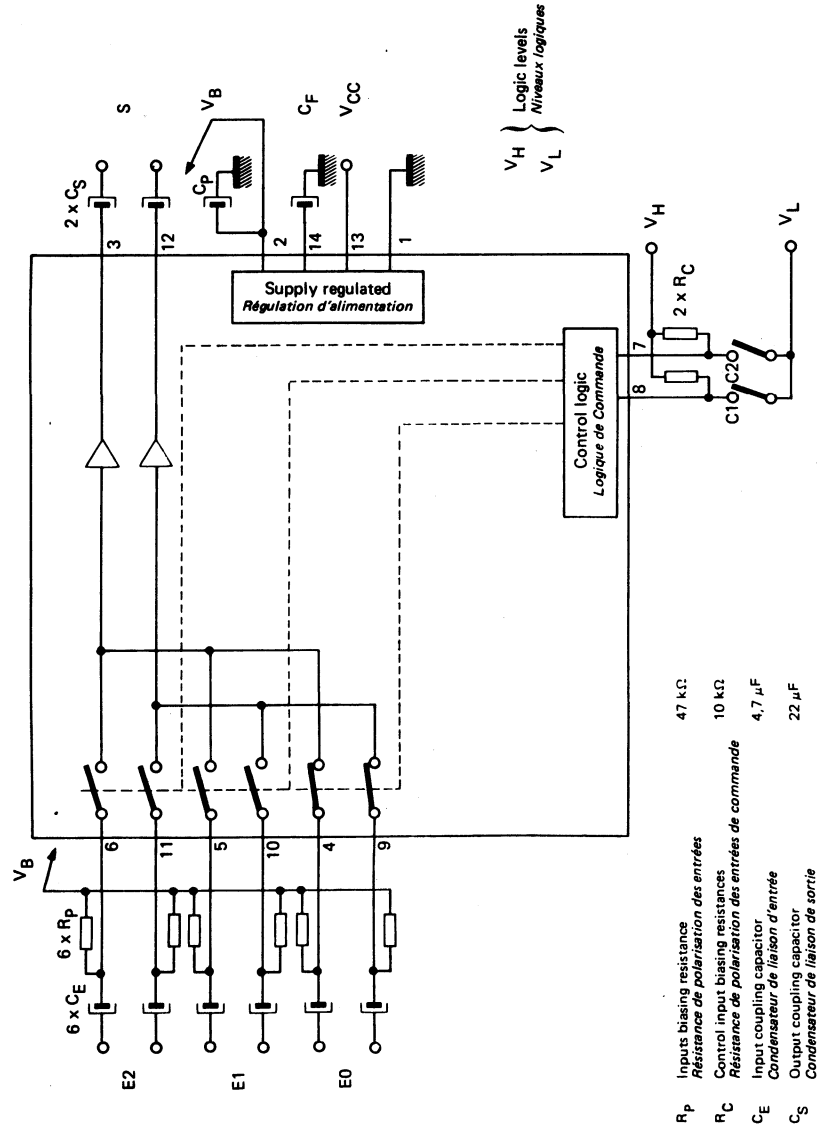
TEA1035 DP-18



R_P	Inputs biasing resistance *Résistance de polarisation des entrées*	47 kΩ
R_C	Control input biasing resistances *Résistance de polarisation des entrées de commande*	10 kΩ
C_E	Input coupling capacitor *Condensateur de liaison d'entrée*	4,7 µF
C_S	Output coupling capacitor *Condensateur de liaison de sortie*	22 µF
C_P	Bias filter capacitor *Condensateur de filtrage de la polarisation*	100 µF
C_F	Supply voltage filter capacitor *Condensateur de filtrage de l'alimentation*	0 µF *or/ou* 1 µF

APPLICATION DIAGRAM
SCHEMA D'APPLICATION

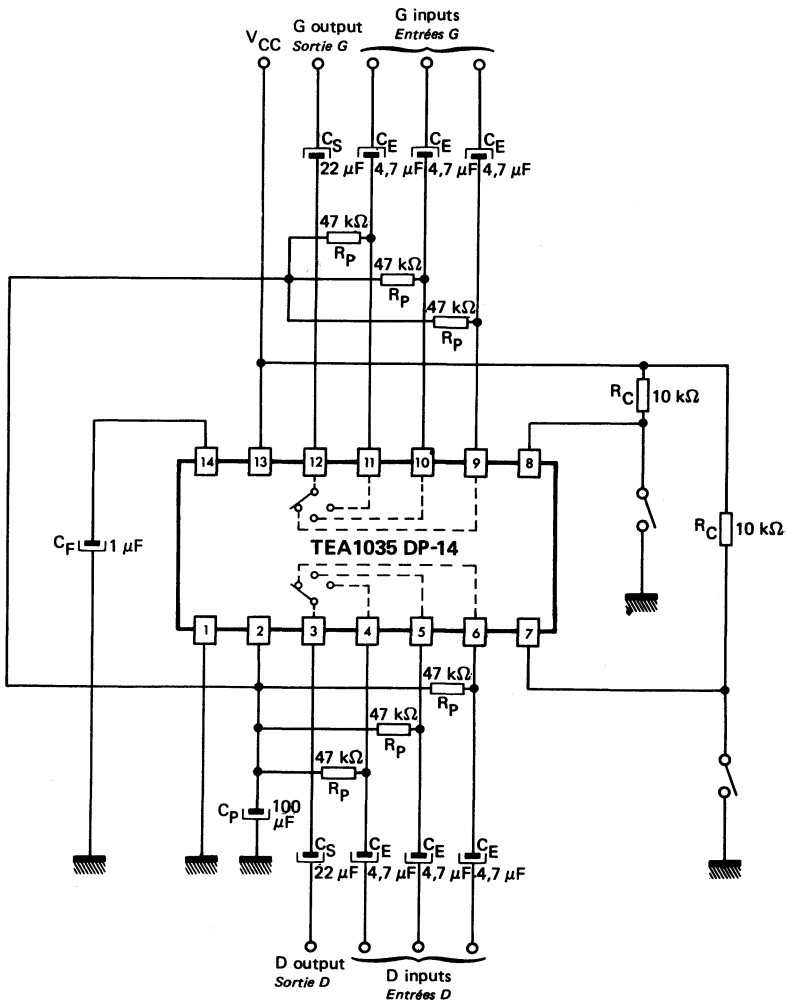
TEA1035 DP-14



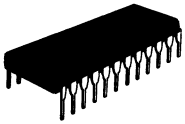
R_P	Inputs biasing resistance *Résistance de polarisation des entrées*	47 kΩ
R_C	Control input biasing resistances *Résistance de polarisation des entrées de commande*	10 kΩ
C_E	Input coupling capacitor *Condensateur de liaison d'entrée*	4,7 µF
C_S	Output coupling capacitor *Condensateur de liaison de sortie*	22 µF
C_P	Bias filter capacitor *Condensateur de filtrage de la polarisation*	100 µF
C_F	Supply voltage filter capacitor *Condensateur de filtrage de l'alimentation*	0 µF *or/ou* 1 µF

APPLICATION EXAMPLE
EXEMPLE D'APPLICATION

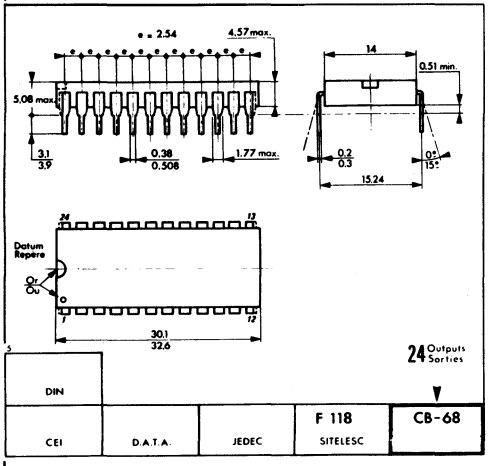
TEA1035 DP-14



CASE / BOITIER CB-68

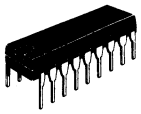


DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE

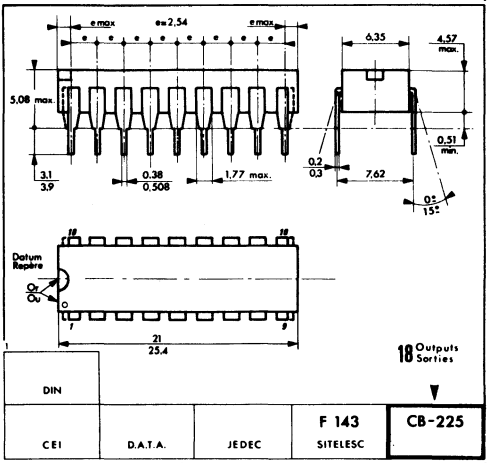


DIN				
CEI	D.A.T.A.	JEDEC	F 118 SITELESC	CB-68

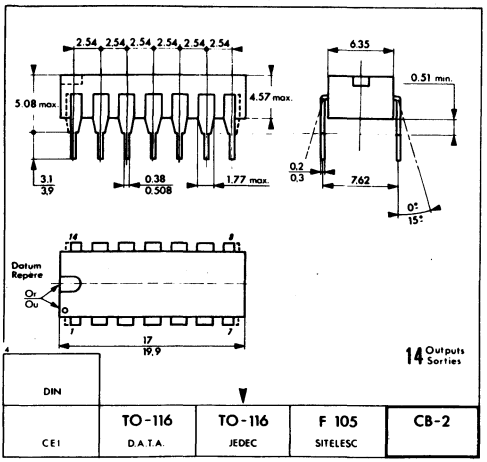
CASE / BOITIER CB-225



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE

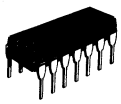


DIN				
CEI	D.A.T.A.	JEDEC	F 143 SITELESC	CB-225



DIN				
CEI	TO-116 D.A.T.A.	TO-116 JEDEC	F 105 SITELESC	CB-2

TO-116 (CB-2)



DP SUFFIX
PLASTIC PACKAGE
SUFFIXE DP
BOITIER PLASTIQUE

These specifications are subject tc change without notice.
Please inquire with our sales offices about the availability of the different packages.

10/10

THOMSON SEMICONDUCTORS

TEA 2014

ADVANCE INFORMATION

VIDEO SWITCHING CIRCUIT FOR TV

This integrated circuit provides all video switching allowing connections between the peri TV plug and video sections in the TV set. The TEA 2014 is supplied in a 8 leads case CB-98.

Main features

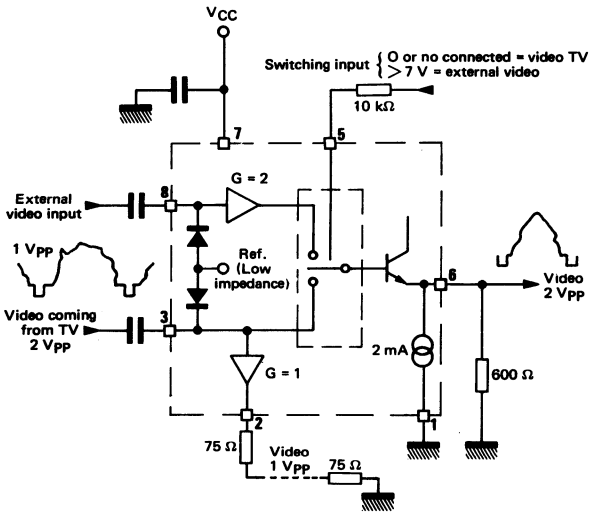
- 1 video output 75 Ω - 1 Vpp no switched
- 1 switched video output 2 Vpp
- Video cross talk : 50 db typical
- Short circuit protection of inputs and outputs
- Clamped video inputs.

VIDEO SWITCHING

CASE CB-98

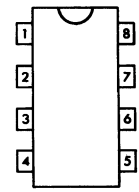
DP SUFFIX
PLASTIC PACKAGE

TYPICAL APPLICATION AND TEST CIRCUIT



We advice to protect the 75 Ω output through a 75 Ω resistor for supply voltage upper than 9 V.

PIN ASSIGNMENT



1 - Ground
2 - 75 Ω video output
3 - Internal video input
4 - Not to be used
5 - Switching input
6 - Switched video output
7 - Supply voltage
8 - External video input

SP8213-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	18	V
Operating temperature with load > 150 Ω with load = 75 Ω	T_{oper}	 −10,+ 100 −10,+ 70	°C
Junction temperature	T_j	−40,+ 150	°C
Storage temperature	T_{stg}	−40,+ 150	°C
Minimum DC load resistor P6		600	Ω
Minimum DC load resistor P2		75	Ω

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	90 typ.	°C/W

ELECTRICAL CHARACTERISTICS

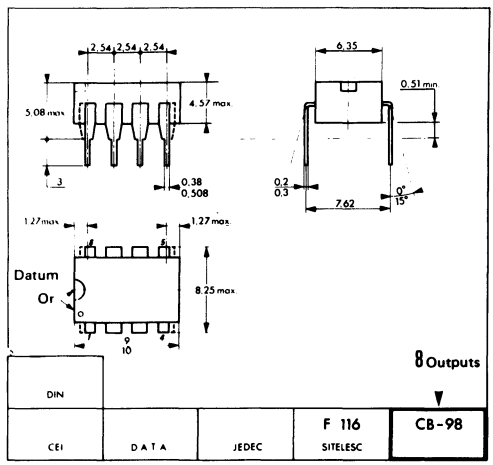
T_{amb} =+ 25°C, V_{CC} = 9 V (unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage range	V_{CC}	8	–	14	V
Supply current (no load on pin 2 and pin 6)	I_{CC}	–	–	20	mA
Supply current (with 75 Ω between pin 2-1, with 600 Ω between pin 6-1)	I_{CC}	–	75	–	mA
Total power dissipation with load	P_{tot}	–	450	–	mW
Internal video input swing from picture FI (Positive video)	–	–	–	4.5	V_{PP}
Internal video input impedance (Positive video)	–	50	–	–	KΩ
Internal video input bias current (Positive video)	–	10	25	40	μA
External video input swing (Positive video)	–	–	–	2	V_{PP}
External video input impedance (positive video)	–	50	–	–	KΩ
Switched video output swing	–	–	–	4.5	V_{PP}
Switched video output dynamic impedance	–	–	–	20	Ω
Switched video DC output voltage (Sync. pulse level, note 1) (600 Ω)	–	1,7	2	2,4	V
Switched video band width (−1 dB)	–	6	–	–	MHz
Switched video output gain Pin 6 - pin 8 (gain with 600 Ω load) Pin 6 - pin 3 (gain with 600 Ω load)	 –	 + 4 −1	 + 5 −0.5	 + 6 0	dB
External video output swing (with 75 Ω load)	–	–	2	2.2	V
External video dynamic output impedance	–	–	10	–	Ω
External video DC output voltage (Sync. pulse level, note 1) (75 Ω)	–	1,7	2	2,4	V
External video output gain (Pin 2 - pin 3 gain with 75 Ω load)	–	−1.8	−1	−0.4	dB
Switching input unactive low level or unconnected pin (TV receiving)	–	0	–	3	V
Switching input active level (ext. receiving)	–	7	–	V_{CC}	V
Switching input impedance	–	10	–	–	KΩ
Video rejection between two inputs 0 to 5 MHz 1 KHz	 – –	 – −50	 −50 –	 – –	dB
Differential group delay	–	–	15	–	ns
Linearity distortion Luma (test line 17) Chroma (test line 331) Intermodulation Luma - Chroma (test line 331)		 – – –	 2 2 5	 – – –	%
Supply voltage rejection (1 KHz)	–	40	50	–	dB

Note 1 : Use a video signal with a synchro pulse in order to make the clamp work in a correct way (75 Ω to the ground and 10 μF in serie).

CASE CB-98

DP SUFFIX
PLASTIC PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TEA2015 A

VERTICAL SWEEP FOR BLACK AND WHITE AND 90° COLOR T.V SETS

The TEA2015 A is a complete vertical sweep system designed for TV sets. It includes a fly-back generator a triggerable ramp generator, a power amplifier, a blanking-pulse generator and safety systems.

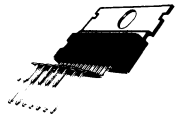
Its large output transistors and special "single in-line" case make it able to work without any external power stage and give it a good reliability, it is protected against thermal over load and short-circuit.

MAIN FEATURES

- V_{CC} max. 30 V
  60 V (Flyback)
- $I_{OUT} = \pm 1$ A
- No frequency adjustment
- Linearity adjustment possible to suppress
- Frequency and linearity adjustments may be suppressed for standard operation.

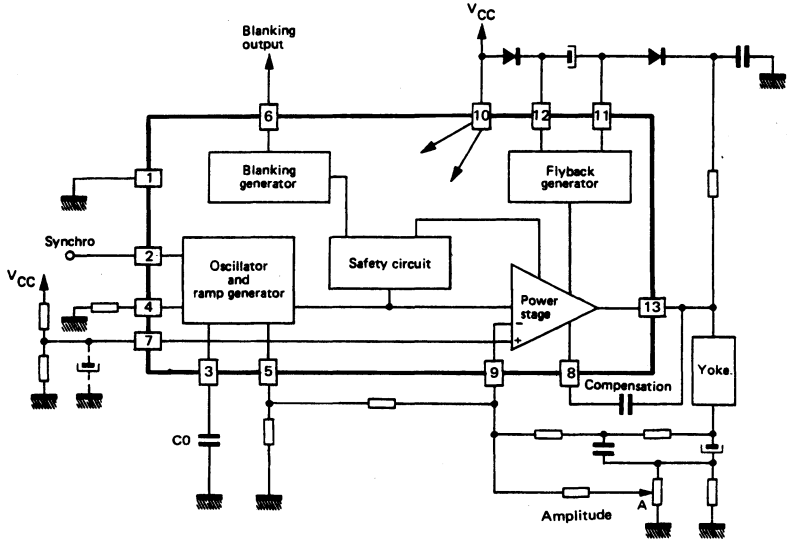
VERTICAL SWEEP FOR BLACK AND WHITE AND 90° COLOR TV SETS

CASE CB-230



SP SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



NT4118-A

FUNCTIONAL DESCRIPTION

This integrated circuit, specially intended for 90° color TV sets, includes the following built in units :

Oscillator

It provides a linear positive going ramp voltage. The amplitude keeps proportional to V_{CC}. The free running frequency is fixed by external components : one capacitor and one resistor. The frequency drift versus V_{CC} or temperature is very low.

Synchronization

The synchro stage is gated in order to allow input pulse action only during the last fourth of free running period.

Blanking

During normal operation the circuit provides a positive blanking pulse of 12.6 Volts amplitude. The duration is slightly adjustable around 1.3 ms, depending on the value of an external resistor (pin 4).

Power amplifier

The output stage is a complete power amplifier with high current capability, allowing direct driving of deflection coils. It includes thermal and short circuit protection.

Fly-back generator

During the retrace time the output voltage is permitted to reach 2 x V_{CC}, due to a built in system (fly-back generator) and few external components.

But, the circuit can be used without fly-back generator.

ABSOLUTE MAXIMUM RATINGS

Direct supply voltage	V_{CC}	35	V
Flyback peak voltage	V_{FB}	65	V
Output current (repetitive)	I_O	± 2	A
Output current (non repetitive)	I_O	± 2,5	A
Storage and junction temperature	T_j - T_{stg}	−40 → +150	°C
Current at pin 13			
non repetitive	I_{FB}	± 2,5	A
repetitive *	I_{FB}	± 2	A

*$t \leq 1$ ms for $t_o = 20$ ms

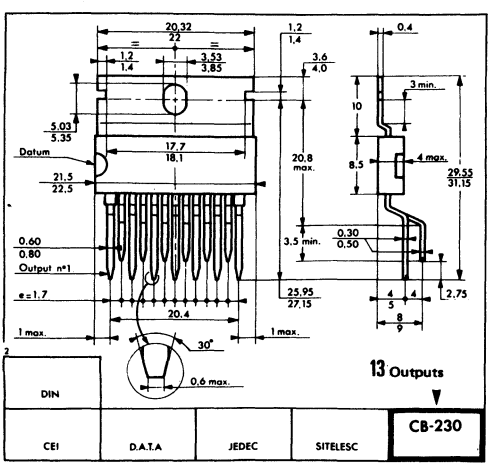
PIN CONFIGURATION

CASE CB-230

1	Substrate	7	Power amplifier + input
2	Synchronization	8	Compensation
3	Oscillator capacitor	9	Power amplifier − input
4	Reference current	10	$+V_{CC}$
5	Oscillator output and F. adjustment	11	Flyback generator
6	Blanking output	12	V_{CC} power stage
		13	Output

THERMAL CHARACTERISTICS

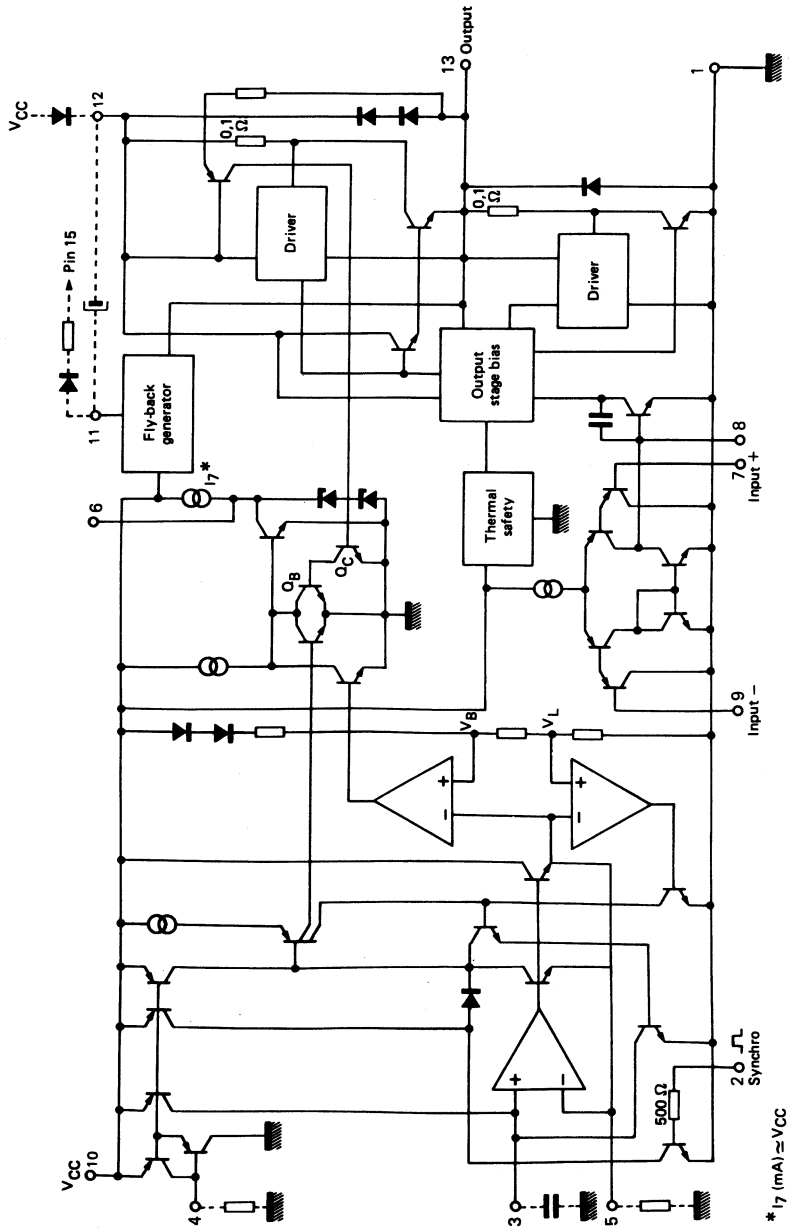
Junction-ambient thermal resistance	$R_{th(j-a)}$	50	°C/W
Junction-case thermal resistance	$R_{th(j-c)}$	7	°C/W



CASE CB-230

SP SUFFIX
PLASTIC PACKAGE

SCHEMATIC DIAGRAM

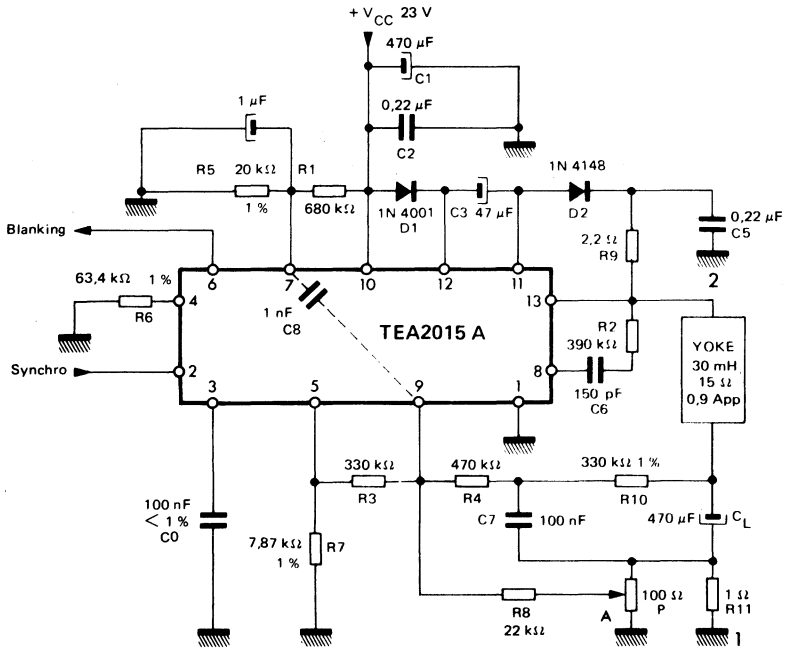


GENERAL ELECTRICAL CHARACTERISTICS (refer to the test circuit) V_{CC} = 23 V , T_{amb} = 25°C

PARAMETERS	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply current without load (P10 and P12)	I(10) + I(12)			25	50	mA
Triggering time (pull-in-range)	t_o = 23.5 ms			5.8		ms
Free period time	Co = 0.1 µF R4 = 63,4 kΩ R5 = 7,87 kΩ		21,6	23.5	25,4	ms
Pin 5 peak to peak oscillator saw-tooth voltage	Co = 0.1 µF R4 = 63,4 kΩ V_{CC} = 22 V			$V_{CC}/3$		V
Blanking pulse time	Co = 0.1 µF R4 = 63,4 kΩ		1,15	1.3	1,45	ms
Pin 6 blanking pulse amplitude				12.6		V
Blanking available pin 6* current				150		µA
Blanking time drift versus temperature $\frac{dt}{dTj}$				1		µs/°C
Amplifier input bias current	I(9) − I(7)			100		nA
Synchronisation						
Pin 2 input current				1		µA
Input impedance				0.5		kΩ
Maximum voltage					1.5	V
Oscillator frequency drift versus supply voltage $\frac{dF}{dV_{CC}}$	V_{CC} = 15 ÷ 25 V			0.1		Hz/V
Oscillator frequency drift versus temperature $\frac{dF}{dT_{case}}$				0.003		Hz/°C
Thermal protection				140		°C

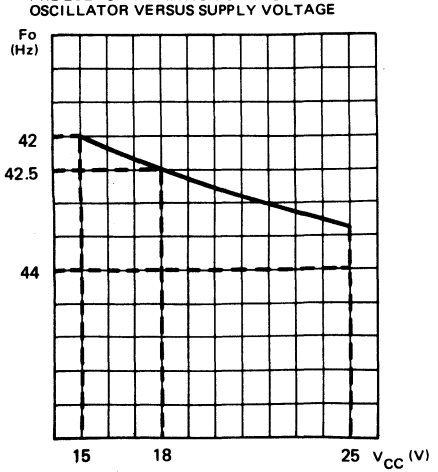
* To get an upper blanking current, put an external resistor from 6 to V_{CC}
The pin 6 capability to switching an external current to ground is 4 mA

DYNAMIC TEST CIRCUIT

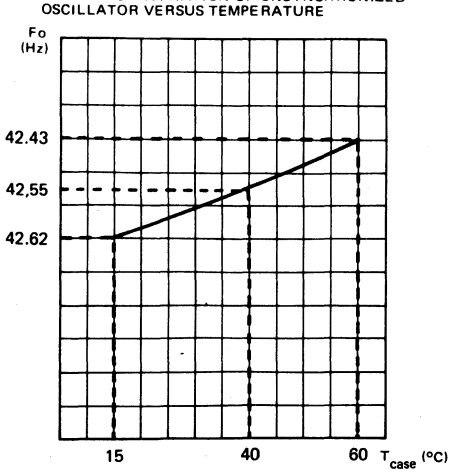


If necessary connect a capacitor 1 nF between pins 9 and 7 to reject line influence.

FREQUENCY VARIATION OF UNSYNCHRONIZED OSCILLATOR VERSUS SUPPLY VOLTAGE



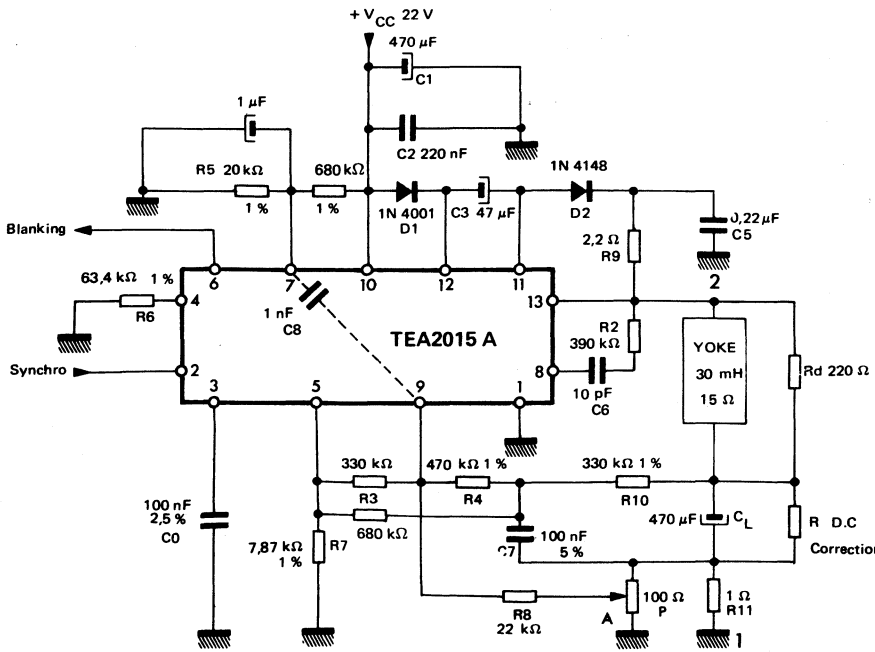
FREQUENCY VARIATION OF UNSYNCHRONIZED OSCILLATOR VERSUS TEMPERATURE



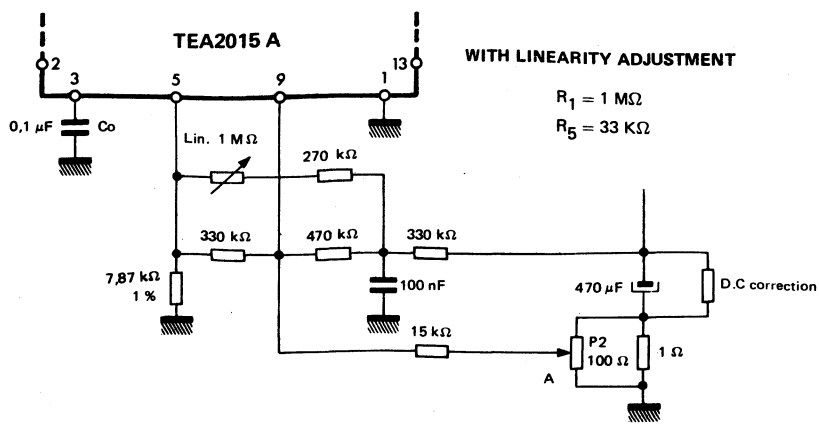
ELECTRICAL CHARACTERISTICS FOR DEFLECTION CIRCUIT WITH VIDEOCOLOR PIL A 421 X SERIES COILS

PARAMETERS	SYMBOLS	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
YOKE FEATURES PIL S4							
Resistance	Rd					15	Ω
Inductance	Ld					30	mH
Peak to peak yoke current	I_{CC}					0,9	A
Supply voltage	V_{CC}			20		22	V
Supply current		V_{CC} = 22 V				155	mA
Fly-back time		V_{CC} = 22 V				1	ms
IC power dissipation	P_D	V_{CC} = 22 V				2,3	W
Pin 12 operating peak current in fly-back generator	I_{FB}					± 0,45	A
Non repetitive (accidental) maximum peak current in fly-back		t = 1 ms t_o = 20 ms				±2	A
Pin 13 non repetitive (accidental) maximum peak output current						±2,5	A
Fly-back voltage						44	V
Pin 5 oscillator saw-tooth amplitude		C_3 = 100 nF V_{CC} = 22 V R_4 = 63,4 kΩ				9	V
Pin 6 blanking time		C_3 = 100 nF V_{CC} = 22 V R_4 = 63,4 kΩ				1,3	ms
Junction temperature with heatsink of R_{th} = 10°C/W	T_j	V_{CC} = 22 V T_{amb} = 30°C				70	°C

TYPICAL APPLICATION CIRCUIT FOR 90° COLOR TV SETS USING A 421 X TUBE WITH NO LINEARITY ADJUSTMENT



If necessary connect a capacitor 1 nF between pins 9 and 7 to reject line influence.



WITH LINEARITY ADJUSTMENT

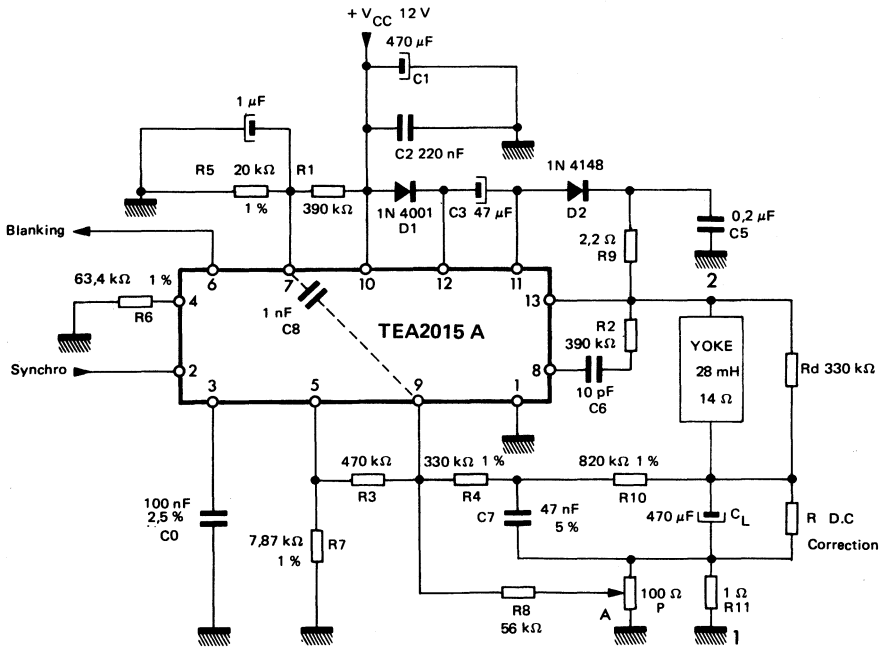
$R_1 = 1\ M\Omega$

$R_5 = 33\ K\Omega$

ELECTRICAL CHARACTERISTICS FOR SMALL SCREEN B/W DEFLECTION CIRCUIT WITH SERIES COILS

PARAMETERS	SYMBOLS	TEST CONDITIONS		MIN. TYP. MAX.	UNITS
YOKE FEATURES SERIES COILS					
Resistance	Rd			14	Ω
Inductance	Ld			28	mH
Peak to peak yoke current	I_{CC}			0,6	A
Supply voltage	V_{CC}			12	V
Fly-back time		V_{CC} = 12 V		1,2	ms
Power dissipation in the IC	P_D	V_{CC} = 12 V		0,9	W
Pin 11 operating peak current in fly-back generator				± 0,3	A
Non repetitive (accidental) maximum peak current in fly-back		t = 1 ms t_o = 20 ms		± 2	A
Pin 13 non repetitive (accidental) maximum peak output current				±2,5	A
Fly-back voltage				24	V
Pin 5 oscillator saw-tooth amplitude		V_{CC} = 12 V		4,7	V
Pin 6 blanking time		V_{CC} = 12 V		1,3	ms
Junction temperature without heatsink	T_j	V_{CC} = 12 V T_{amb} = 30 °C		75	°C

TYPICAL APPLICATION CIRCUIT FOR SMALL SCREEN B/W TV SET SERIES COILS

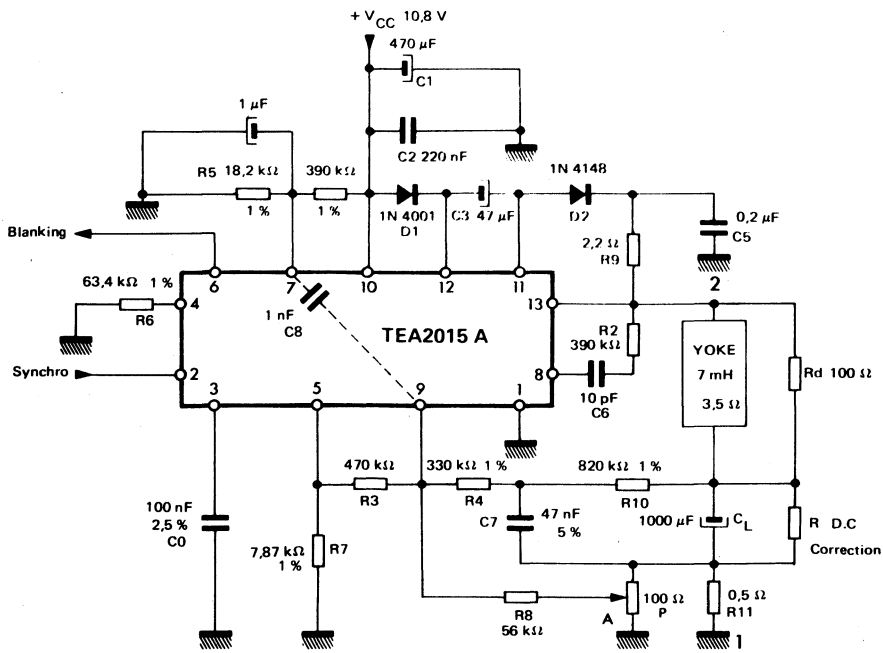


If necessary connect a capacitor 1 nF between pins 9 and 7 to reject line influence.

ELECTRICAL CHARACTERISTICS FOR SMALL SCREEN B/W DEFLECTION CIRCUIT WITH PARALLEL COILS

PARAMETERS	SYMBOLS	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
YOKE FEATURES PARALLEL COILS							
Resistance	Rd				3,5		Ω
Inductance	Ld				7		mH
Peak to peak yoke current	I_{CC}				1,2		A
Supply voltage	V_{CC}			8,8		10,8	V
Fly-back time		V_{CC} = 10,8 V			0,8		ms
Power dissipation in the IC	P_D	V_{CC} = 10,8 V			1,5		W
Pin 11 operating peak current in fly-back generator					± 0,6		A
Non repetitive (accidental) maximum peak current in fly-back		t = 1 ms t_o = 20 ms				± 2	A
Pin 13 non repetitive (accidental) maximum peak output current						±2,5	A
Fly-back voltage					21		V
Pin 5 oscillator saw-tooth amplitude		V_{CC} = 10,8 V			4		V
Pin 6 blanking time		V_{CC} = 10,8 V			1,3		ms
Junction temperature with heatsink of R_{th} = 30°C/W	T_j	V_{CC} = 10,8 V T_{amb} = 30°C			85		°C

TYPICAL APPLICATION CIRCUIT FOR SMALL SCREEN B/W SET PARALLEL COILS



If necessary connect a capacitor 1 nF between pins 9 and 7 to reject line influence.

APPLICATION INFORMATION

Blanking time

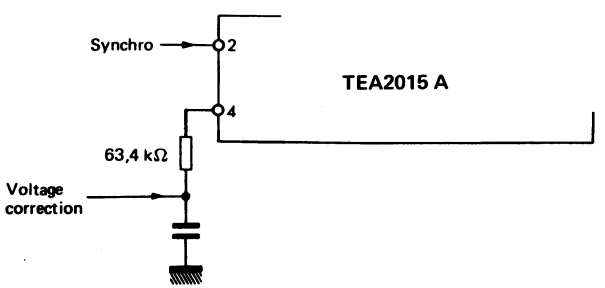
Can be adjusted by the value of R4

R4 = 63,4 kΩ Co = 0,1 μF t_{blank} = 1,3 ms

Automatic format correction

The saw-tooth amplitude is proportional to V_{CC} so that the format is made automatically when the supply voltage is given by the horizontal transformer. In an other case two other possibilities.

a – When the voltage correction comming from the beam current increase and the amplitude must decrease.

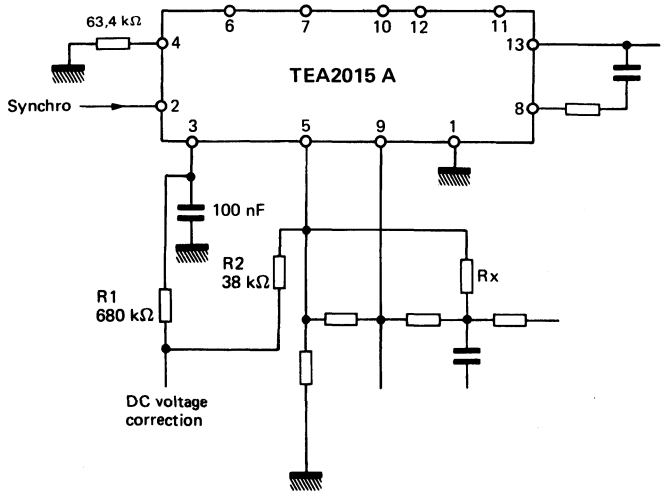


Format correction	5 %
V_{CC}	20 V
Voltage correction	0 - 1 V

No effect on the free frequency

In this case if the amplitude decreases of 5% the blanking time increases of 5%.

b – When the voltage correction decreases and the amplitude must decrease

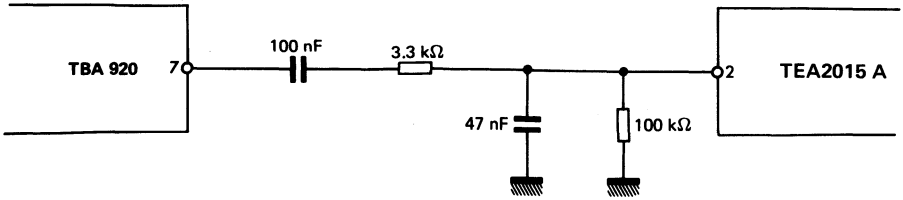


Rx must be adjusted to compensate the parabolic effect of R1 if there is no linearity adjustment.

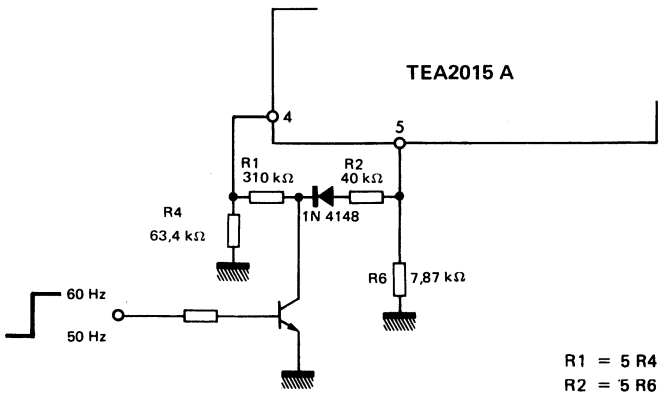
Format correction	5 %
DC voltage correction	2 V – 0
V_{CC}	20 V

– no effect on free frequency
– Blanking time variation ⩽ 3 %

Synchronization network for synchro coming from TBA 920 Pin 7

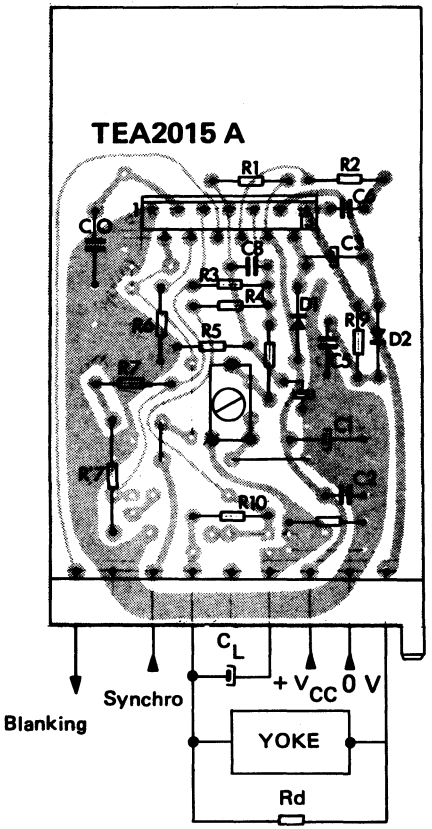


Automatic standard switching with constant amplitude (50 Hz - 60 Hz)

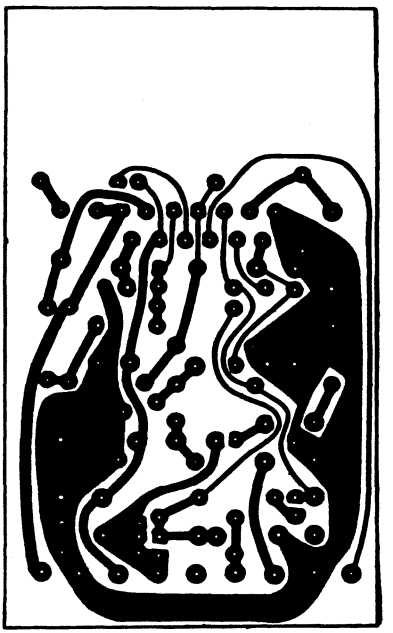


Printed circuit board layout information refered to the application diagram 90° COLOR TV SET

COMPONENT SIDE



COPPER SIDE



Each power ground 1, 2, 3 (refer to the application diagram 90° COLOR TV SET) must be connected to the –supply (pin 1) with a minimum copper resistance.
Other grounds (oscillator and outputs) must be well decoupled from the power ground and connected to the –supply.

Copper connections to pins 7 and 9 as short as possible to reject the line influence.

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TEA5030

ADVANCE INFORMATION

TV VIDEO PROCESSING I.C FOR COLOR TV SET

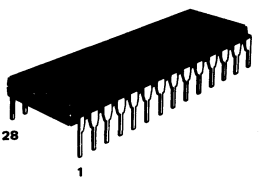
The TEA5030 is a new video processor I.C compatible with all standards PAL/SECAM/NTSC and new needs such as teletex, antiope, TV games, remote control etc...

PRINCIPAL FEATURES

- Matrixing of R, G, B signal from (R-Y) and (B-Y)
- Electronic control of contrast, brightness and saturation
- Three channels video switch, for selection of internal signal (broadcast) or external R, G, B information
- Automatic cut-off adjustment.

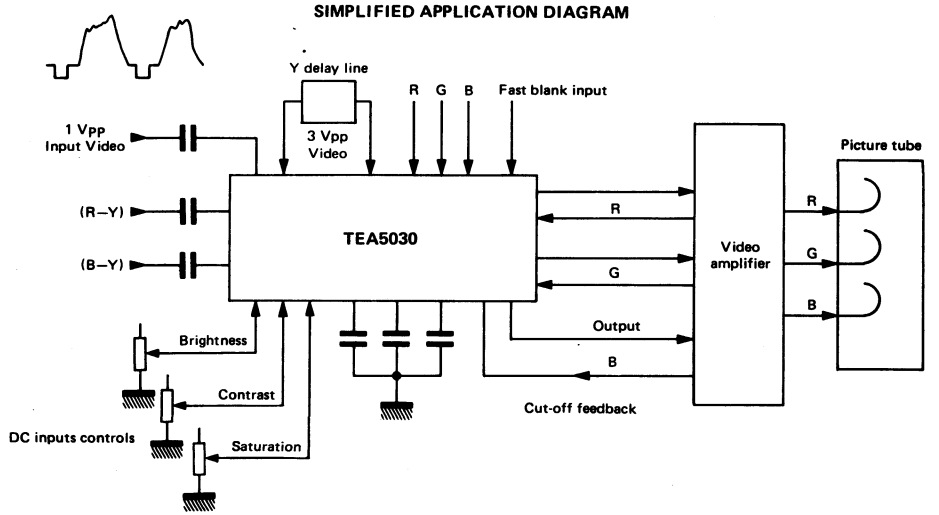
TV VIDEO PROCESSING I.C FOR COLOR TV SET

CASE CB-132



DP SUFFIX
PLASTIC PACKAGE

SIMPLIFIED APPLICATION DIAGRAM



SP8232-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

In order to ensure compatibility with standard video transmission systems the luma input is a high impedance, AC coupled, designed to accept a 1 V video signal. After a X3 gain voltage amplifier the inverted luma signal is brought out to the luma delay line. This output is low impedance to match the delay line accurately, and as the signal is inverted, it is highly suitable for driving a synchronization separator such as the TDA2593 or TBA920.

Following the luma delay line the video is controlled by an electronic gain control with a range of 40 dB.

The DC luma level is locked on the black level (cut-off current) with a range of ± 1 V depending of brightness. The DC voltage level is clamped during each line retrace and an external capacitor holds this voltage during the line trace.

After brightness and contrast controls the luminance is fed to the matrix with R-Y and B-Y signals.

The R-Y and B-Y inputs are high impedance with AC coupling, compatible with decoder I'Cs such TEA5630 for SECAM and TEA5620 for PAL.

The voltage gain of R-Y and B-Y is controlled by saturation. The saturation is in tracking with contrast and then the R-Y and B-Y signals are fed to the matrix and summed with on-screen display signals which are controlled in gain by the luma contrast control. Each input is AC coupled and black level clamped using the coupling capacitor as the storage element for the clamp voltage.

All the controls have an active range of 0.5 to 4.5 V making them compatible with D/A convertor derived control signals, such as those from remote control systems. The three on-chip output stages are high gain class B amplifiers with the gain set by parallel feedback resistor. This gives a well defined gain and stable output voltage level. The beam current in each cathode of the picture tube is monitored by a high-voltage PNP transistor. A sample of this current is fed back to the IC.

In the luma signal a reference black level is inserted during the line and frame blanking periods. While this reference level is present, and after the frame flyback, the output stage feedback input goes high impedance and an internal comparator is actived.

This circuit compares an internal reference voltage to the voltage developed across an external resistor by the picture tube beam current, and the output voltage is trimmed to get the desired cathode current value.

An internal logic delivers blanking and clampling pulses from the normalized sand castle and frame retrace signals.

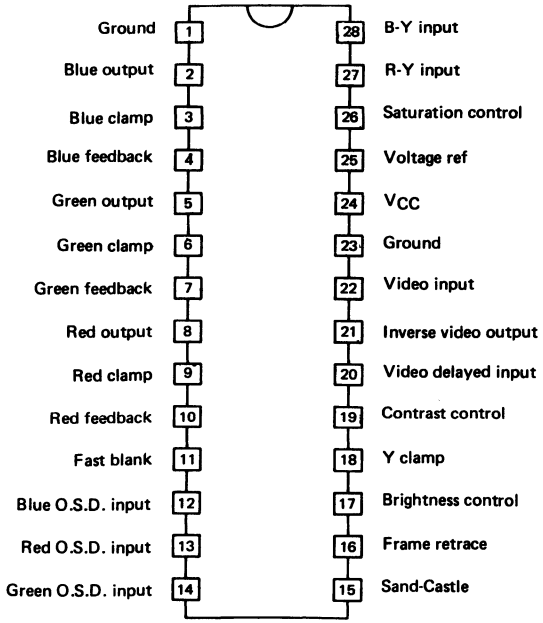
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	16	V
Operating temperature range	T_{oper}	0, + 70	°C
Storage temperature range	T_{stg}	–65, + 150	°C

THERMAL CHARACTERISTICS

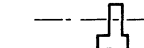
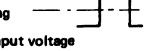
Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	55	°C/W

PIN CONFIGURATION

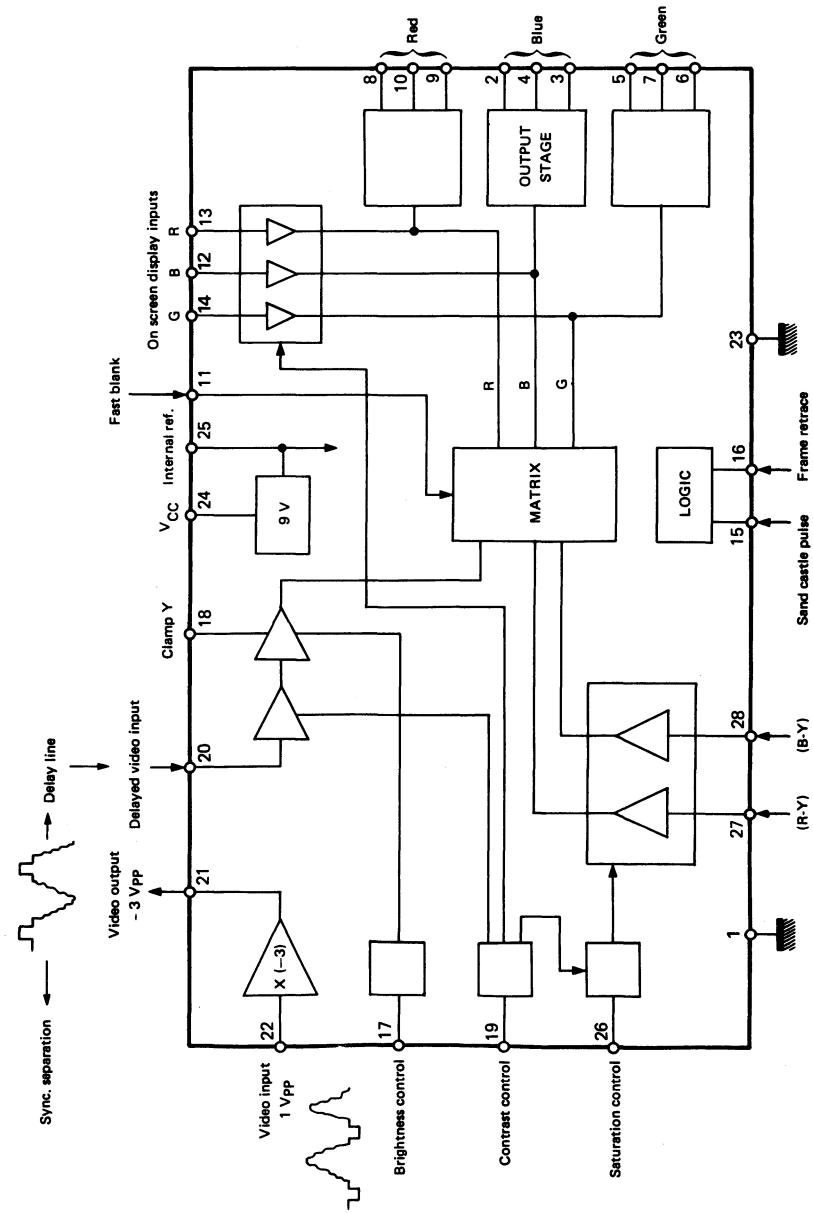


ELECTRICAL CHARACTERISTICS

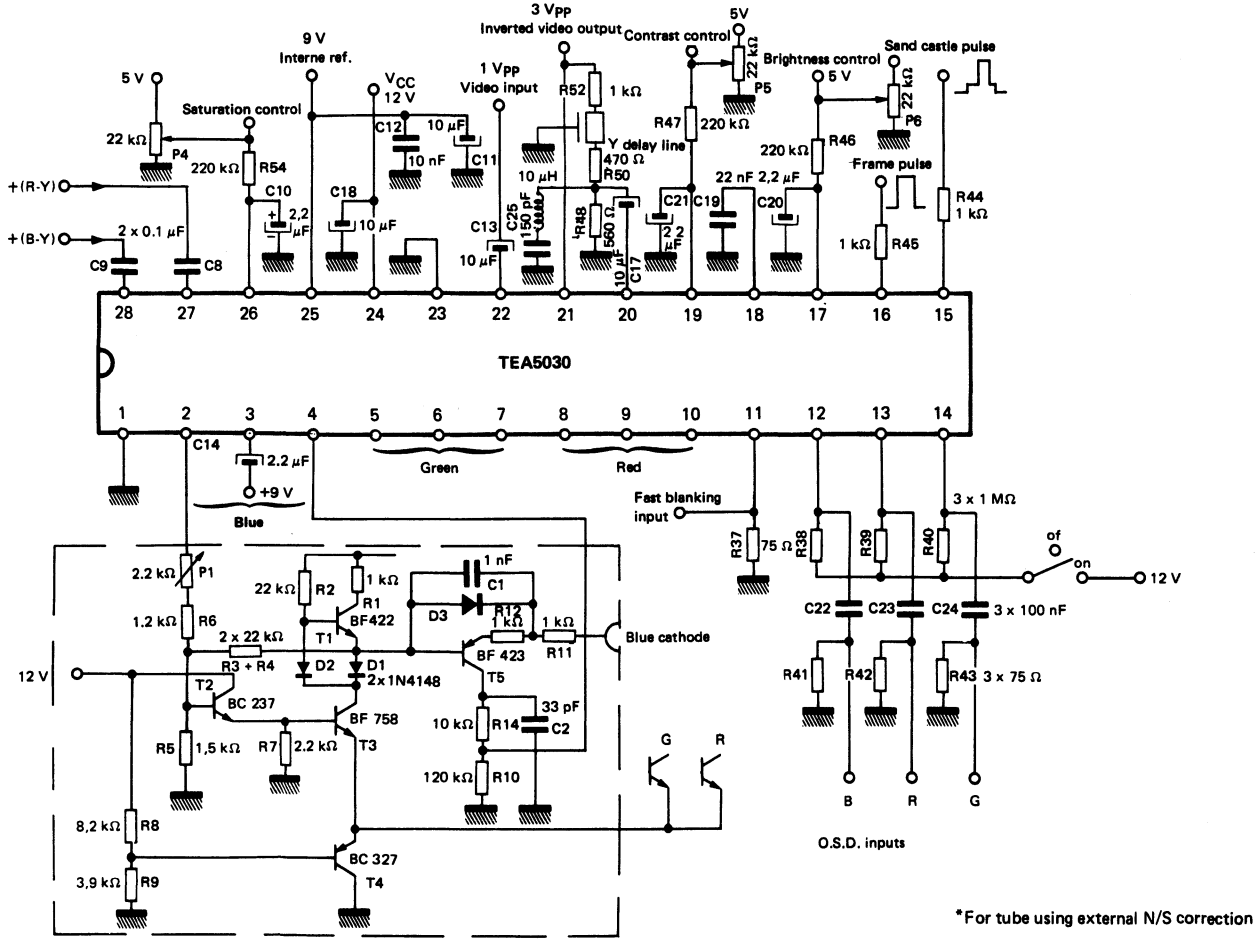
T_{amb} = + 25°C ; V_{CC} = 12 V (unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage	Pin 24	V_{CC}	10.8	12	13.2	V
Supply current	Pin 24	I_{CC}	–	55	–	mA
Internal voltage ref.	Pin 25	V_Z	–	9	–	V
Video input	Pin 22	–	–	1	–	Vpp
Output voltage inv. video (V22 = 1 Vpp)	Pin 21	–	–	3	–	Vpp
Max output voltage swing	Pin 21	–	–	7	–	Vpp
– 3 dB bandwidth	Pins 2-5-8	–	4.5	5	–	MHz
(R–Y) input voltage (100 % modulation)	Pin 27	–	–	1.4	2	Vpp
(B–Y) input voltage (100 % modulation)	Pin 28	–	–	1.0	2	Vpp
– 3 dB bandwidth		–	1.5	–	–	MHz
Luma gain						
G21/22	Pin 21	–	8.5	10	11.5	dB
G2/20 ; G5/20 ; G8/20 at max adjustement	Pins 2-5-8	–	14.5	16	18.5	dB
Differential gain fault : Luma channel		–	–	–	0.5	dB
Chroma gain						
G8/27 at max adjustment		–	12.5	14	15.5	dB
G2/28 at max adjustment		–	16.5	18	19.5	dB
Chroma gain ratio at max adjustment		–	1.45	1.55	1.70	
Voltage control for electronic potentiometers						
Contrast (Pin 19) - Saturation (Pin 26)						
Range of adjustment						
V19 = 5 V ; V26 = 5 V		–	–	G_{max}	–	dB
V19 = 0 V ; V26 = 0 V Attenuation		–	40	46	–	dB
Brightness (Pin 17)						
V_{out} adjustment (V17 varying from 0 to 5 V)		–	–	± 1	–	V
On screen display inputs	Pins 12-13-14					
OSD input voltage (Black to white level)		–	–	1	2	V
OSD gain (V2/12 ; V8/13 ; V5/14)		–	13.5	15	17	dB
OSD generator max impedance		–	–	–	75	Ω
– 3 dB bandwidth		–	5	–	–	MHz
Fast blanking threshold		–	–	0.5	–	V
Max output voltage swing	Pins 2-5-8	–	7	8	–	Vpp
Feed-back threshold	Pins 4-7-10	–	1.7	2	2.4	V
Sand-Castle input	Pin 15					
Clamp Y  8 V			–	8	–	V
Line blanking  2.5 V			–	2.5	–	V
Frame return input voltage	Pin 16	–	–	2.5	–	V
Control current (V15 = V16 = 4 V)			–	0.5	–	mA
Matrix coefficient						
Red output (V5/V8 with V27 = 1 V ; V28 = 0 ; V20 = 0)		–	–	0.51	–	–
Blue output (V5/V2 with V27 = 0 ; V28 = 1 ; V20 = 0)		–	–	0.19	–	–

BLOCK DIAGRAM

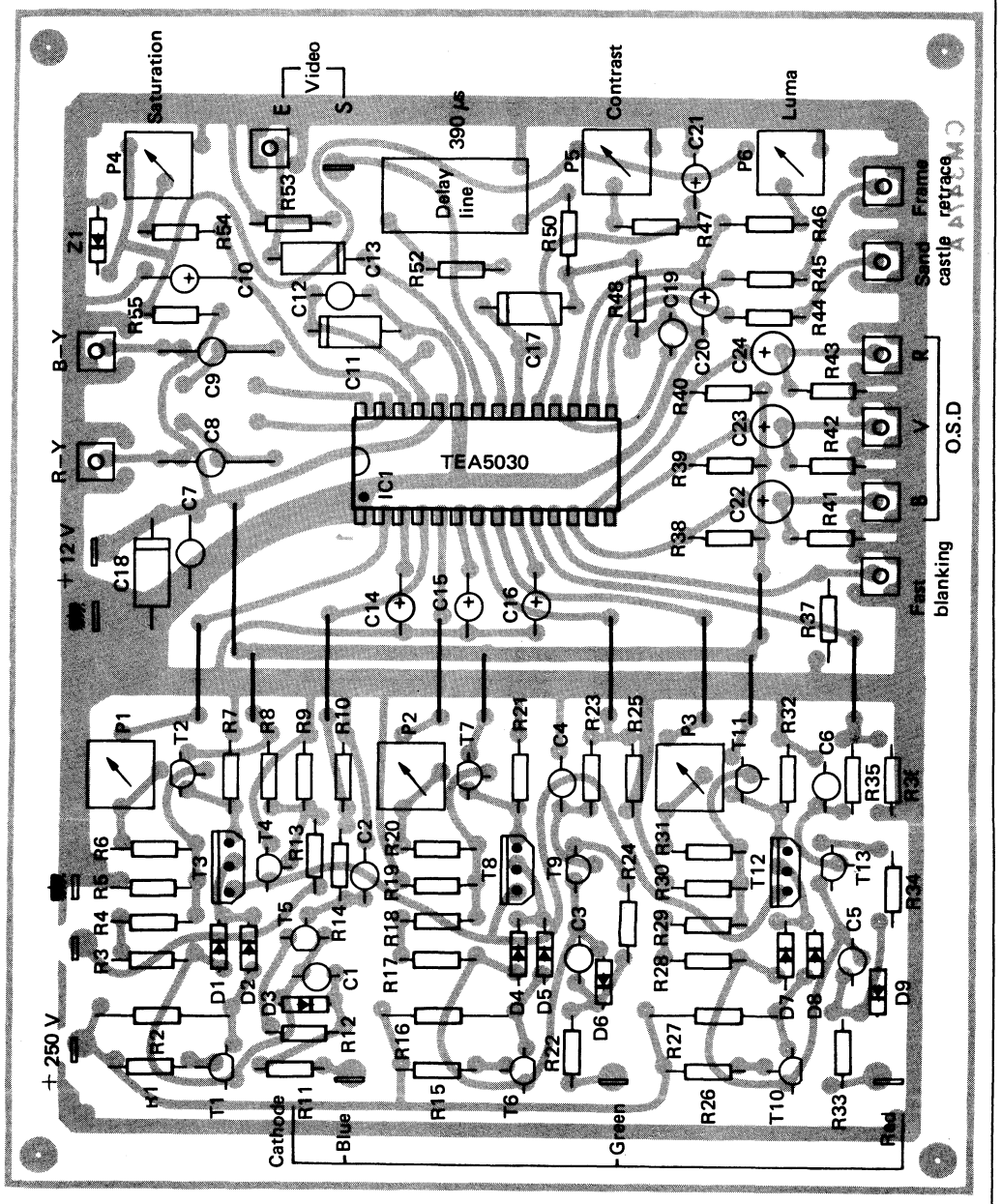


APPLICATION CIRCUIT



*For tube using external N/S correction

COMPONENT SIDE



N°	Value	P
R1	1 kΩ	1/4 W
R2	22 kΩ	1 W
R3	22 kΩ	1/4 W
R4	22 kΩ	"
R5	1.5 kΩ	"
R6	1.2 kΩ	"
R7	2.2 kΩ	"
R8	8.2 kΩ	"
R9	3.9 kΩ	"
R10	120 kΩ	"
R11	1 kΩ	"
R12	1 kΩ	"
R13	220 kΩ	"
R14	10 kΩ	"
R15	1 kΩ	"
R16	22 kΩ	1 W
R17	22 kΩ	1/4 W
R18	22 kΩ	"
R19	1.5 kΩ	"
R20	1.2 kΩ	"
R21	2.2 kΩ	"
R22	1 kΩ	"
R23	10 kΩ	"
R24	1 kΩ	"
R25	120 kΩ	1/4 W
R26	1 kΩ	"
R27	22 kΩ	1 W

N°	Value	P
R28	22 kΩ	1/4 W
R29	22 kΩ	"
R30	1.5 kΩ	"
R31	1.2 kΩ	"
R32	2.2 kΩ	"
R33	1 kΩ	"
R34	1 kΩ	"
R35	10 kΩ	"
R36	120 kΩ	"
R37	75 Ω	"
R38	1 MΩ	"
R39	1 MΩ	"
R40	1 MΩ	"
R41	75 Ω	"
R42	75 Ω	"
R43	75 Ω	"
R44	1 kΩ	"
R45	1 kΩ	"
R46	220 kΩ	"
R47	220 kΩ	"
R48	560 Ω	"
R50	470 Ω	1/4 W
R52	1 kΩ	"
R53	1 kΩ	"
R54	220 kΩ	"
R55	1 kΩ	"

N°	Value	U
C1	1 nF	
C2	33 pF	
C3	1 nF	
C4	33 pF	
C5	1 nF	
C6	33 pF	
C7	10 nF	63 V
C8	100 nF	63 V
C9	100 nF	63 V
C10	2.2 µF	35 V
C11	10 µF	63 V
C12	10 nF	63 V
C13	10 µF	63 V
C14	2.2 µF	35 V
C15	2.2 µF	35 V
C16	2.2 µF	35 V
C17	10 µF	63 V
C18	10 µF	63 V
C19	22 nF	
C20	2.2 µF	35 V
C21	2.2 µF	35 V
C22	4.7 µF	63 V
C23	4.7 µF	63 V
C24	4.7 µF	63 V
C25	150 pF	

N°	Typ
T1	BF 422
T2	BC 237
T3	BF 758
T4	BC 327
T5	BF 423
T6	BF 422
T7	BC 237
T8	BF 758
T9	BF 423
T10	BF 422
T11	BC 237
T12	BF 758
T13	BF 423

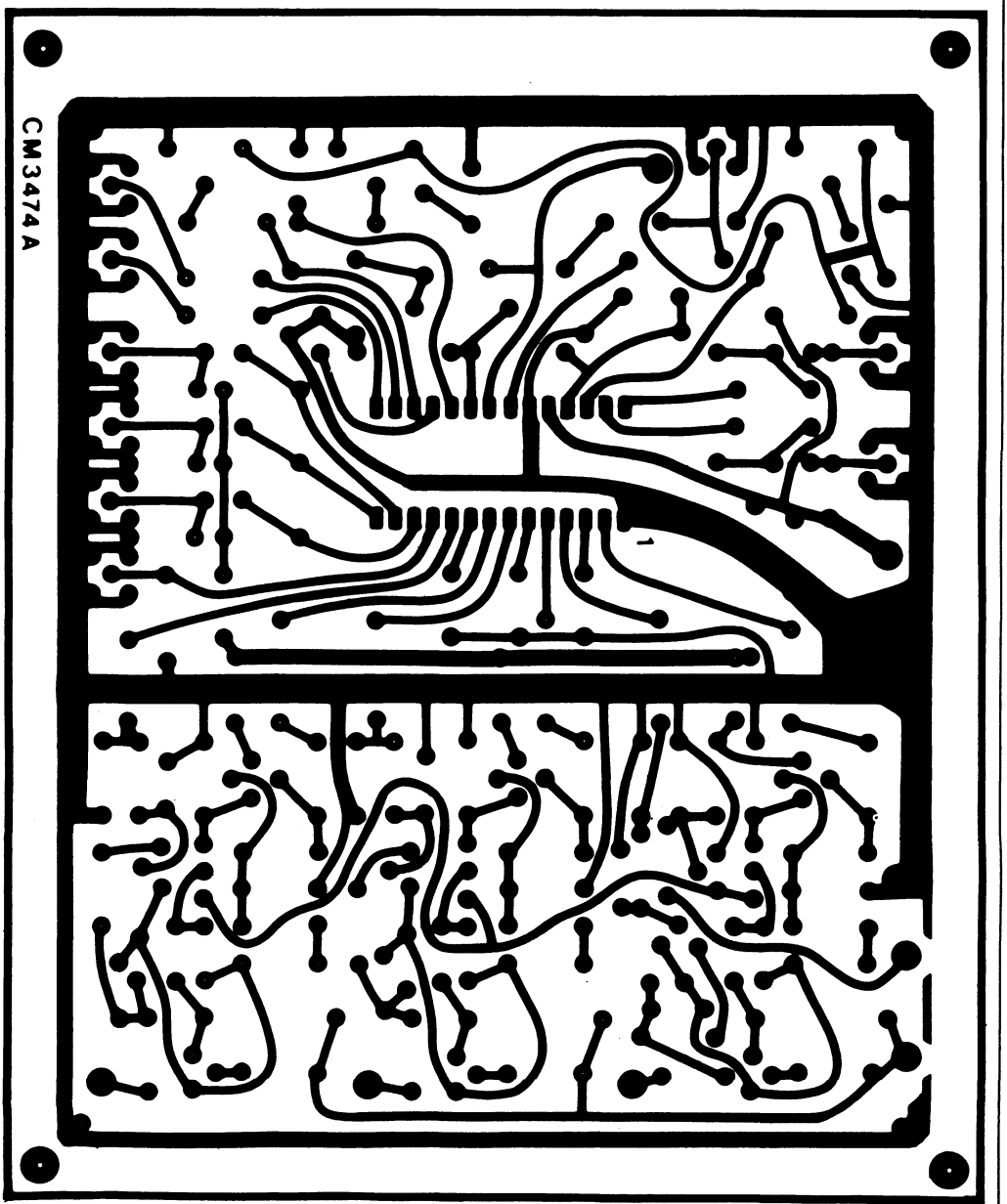
N°	Typ
IC1	TEA 5030

N°	Value
P1	2.2 kΩ
P2	2.2 kΩ
P3	2.2 kΩ
P4	22 kΩ
P5	22 kΩ
P6	22 kΩ

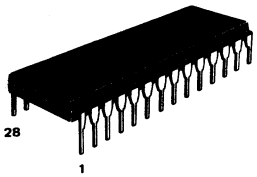
N°	Typ
DL	TDK

N°	Typ
D1	1N4148
D2	"
D3	"
D4	"
D5	"
D6	"
D7	"
D8	"
D9	"
Z1	5 V

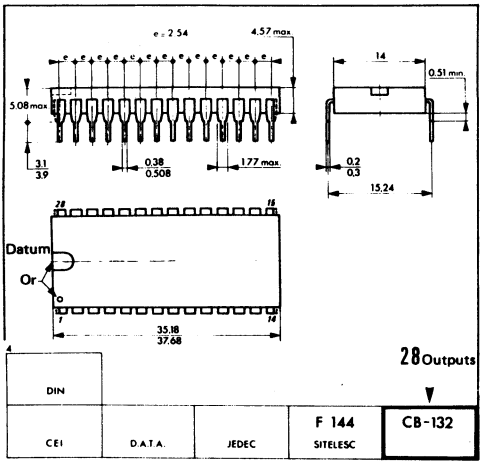
COPPER SIDE



CASE CB-132



DP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TEA5620

ADVANCE INFORMATION

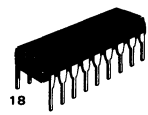
COLOR TV PAL DECODER

MAIN FEATURES

- Phase locked reference oscillator
- U and V axis decoders
- ACC and identification detectors
- Killer
- Use of a standard 4.43 MHz Xtal
- Compatibility with the SECAM decoder TEA 5630 for PAL-SECAM application.

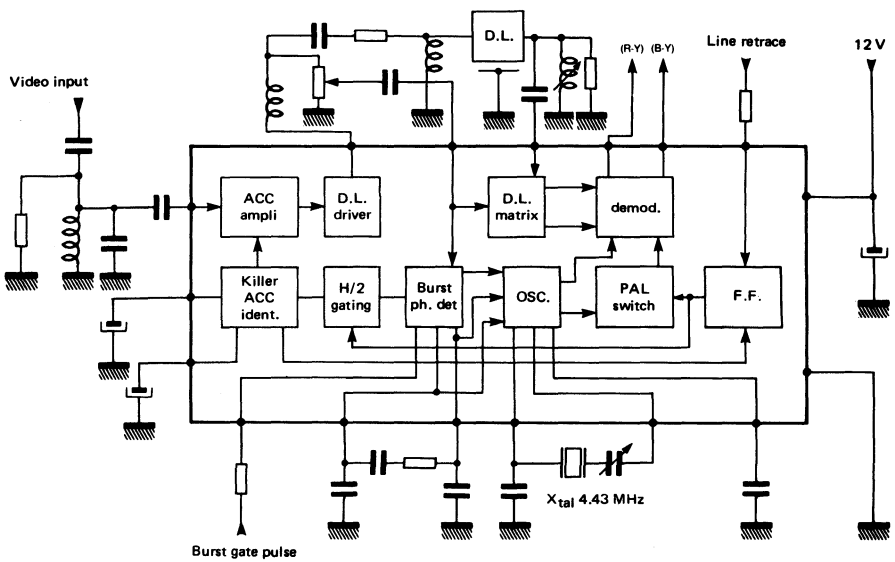
COLOR TV PAL DECODER

CASE CB-225



DP SUFFIX
PLASTIC PACKAGE

SIMPLIFIED APPLICATION



SP8227-A

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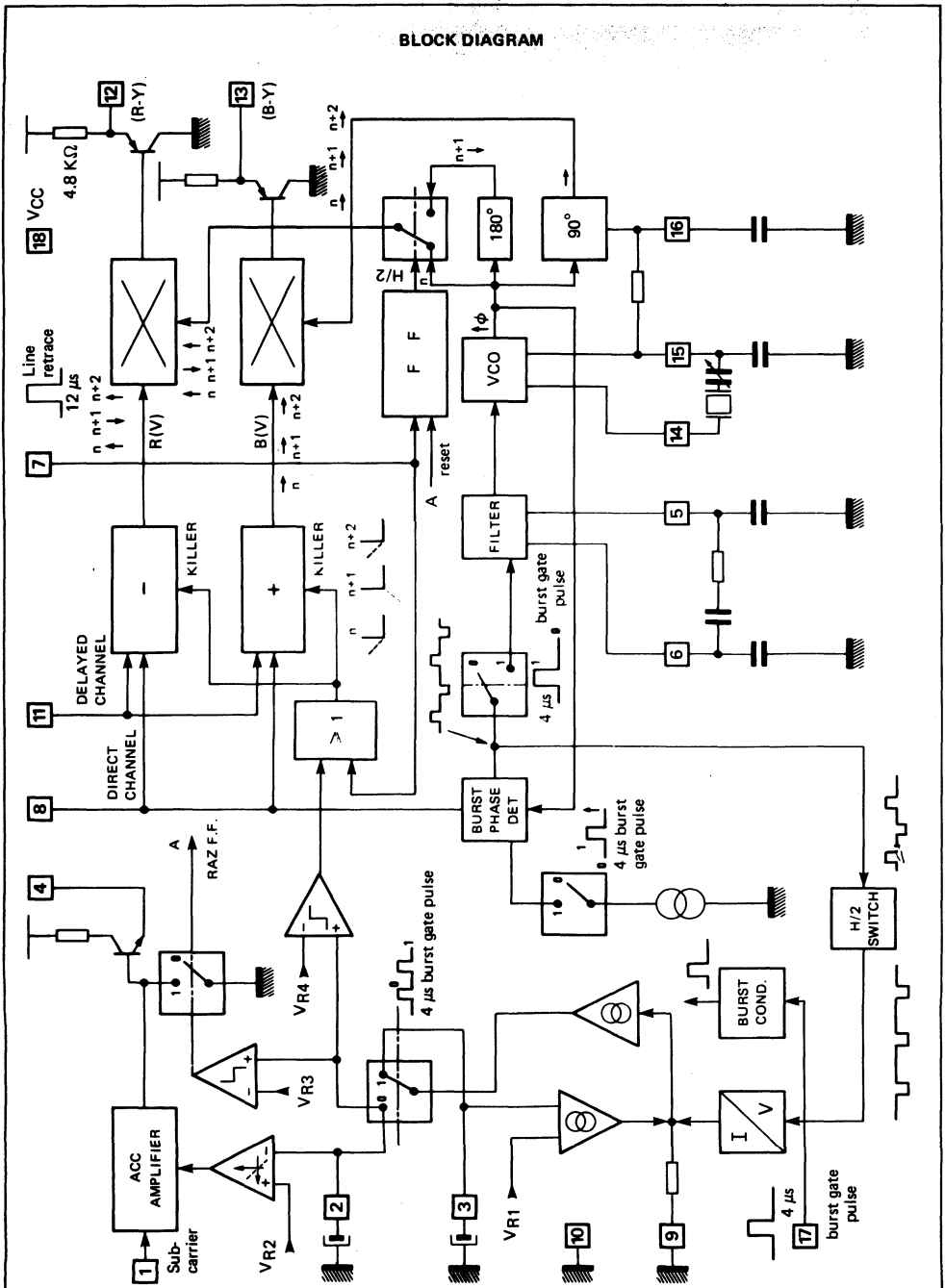
THOMSON COMPONENTS

BLOCK DIAGRAM



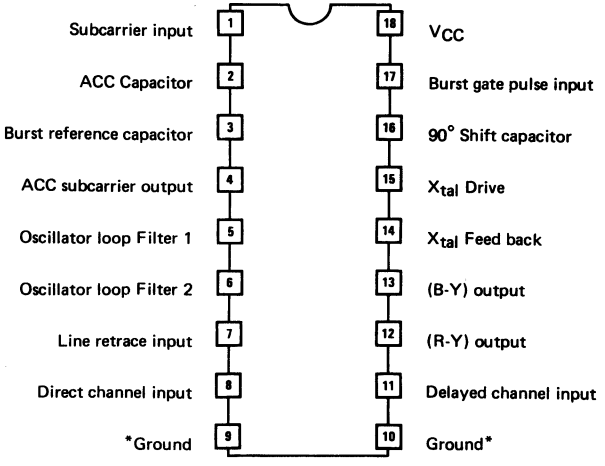
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	14.4	V
Power dissipation	P_D	800	mW
Operating ambient temperature	T_{amb}	−20 + 70	°C
Storage temperature	T_{stg}	−55 + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal resistance Junction-ambient	$R_{th\ amb}$	60	°C/W

PIN CONFIGURATION



*Pins 9 and 10 have to be both grounded.

ELECTRICAL CHARACTERISTICS

V_{CC} = + 12 V ; T_{amb} = + 25°C (unless otherwise noted).

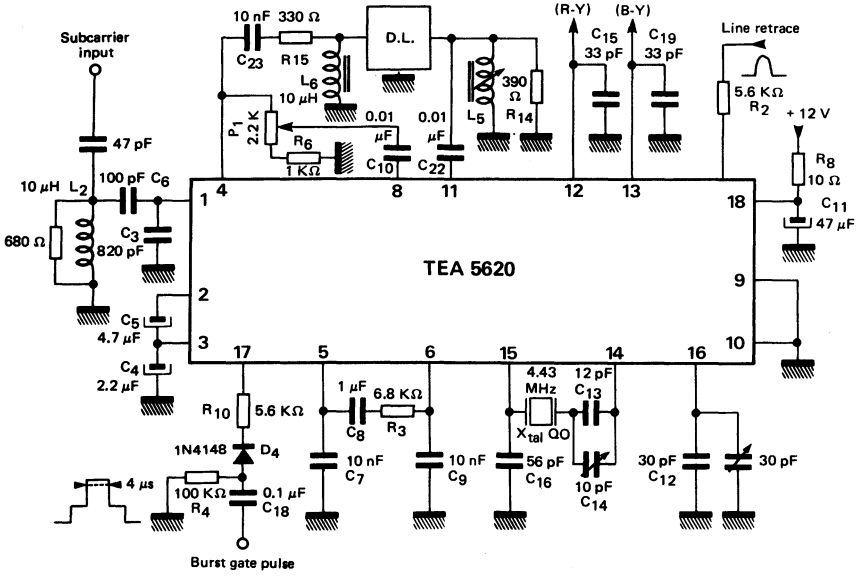
Parameter		Symbol	Min	Typ	Max	Unit
Operating supply voltage	Pin 18	V_{CC}	10	12	14.4	V
Supply current	Pin 18	I_{CC}	–	40	47	mA
DC voltage at pin 12 (V_{CC} = 12 V)		$V_{12\text{-}10}$	–	10	–	V
DC voltage at pin 13 (V_{CC} = 12 V)		$V_{13\text{-}10}$	–	10	–	V
DC voltage at pin 2 (Without burst signal)		$V_{2\text{-}10}$	–	5	–	V
DC voltage at pin 3		$V_{3\text{-}10}$	–	5	–	V
Burst output signal (Burst input 0.1 Vpp)	Pin 4	V_{eb}	0.45	0.6	0.75	Vpp
Chroma input voltage (burst pp ACC controlled)	Pin 1	V_{ci}	5	100	200	mVpp
ACC range	Pin 4	ACC_1	27	30	33	dB
(R-Y) output voltage Standard color bar burst input 0.1 Vpp	Pin 12	V_o (R-Y)	1.2	1.8	2.4	Vpp
(B-Y) output voltage Standard color bar burst input 0.1 Vpp	Pin 13	V_o (B-Y)	1.2	1.8	2.4	Vpp
(B-Y) / (R-Y) output ratio (Standard color bar)		B-Y / R-Y	0.8	1	1.2	Times
Crosstalk between (R-Y) and (B-Y) channel (Burst input 0.1 Vpp)		CdB	–	-30	–	dB
Residual subcarrier (120 pF connected to pins 12 - 13)		V_r	–	–	50	mVpp
Color killer level at killer operation against burst 0.1 Vpp	Pins 12 - 13	E_k	-40	-35	-30	dB
V_{CO} control sensivity (Burst input 0.7 Vpp to the pin 8) (Variation of oscillator frequency versus Pin 5 to 6 voltage.)	Pins 5 - 6	β	1	1.8	2.6	Hz/mV

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = + 12 V ; T_{amb} = + 25°C (unless otherwise noted).

Parameter	Symbol	Min	Typ	Max	Unit
Pull-in frequency range (Burst input 0.7 V_{PP} to the pin 8) (Variation of burst frequency.) Pin 15	F_p	± 500	± 800	–	Hz
Phase hold characteristics (Phase deviation for 100 Hz ΔF burst)	ϕ	–	0.03	0.05	°/Hz
Line retrace threshold Pin 7	VdLr	–	2.5	–	V
Sampling pulse threshold Pin 17	VdL	0.65	0.8	0.9	V
Color killer leak Standard color bar signal component, when killer is on. Pins 12 - 13	ELK	–	–	10	mV_{PP}
Input impedance Pin 1 F = 4.43 MHz V_i = 100 mV_{PP}	Z_e	–	2.8	–	KΩ
		–	10	–	pF
Oscillation start supply voltage Pin 14 V_{CC} rising from lowside.	V_{IS}	–	–	8	V
Thermal resistance Junction-ambient	$R_{th(j-a)}$	–	60	–	°C/W

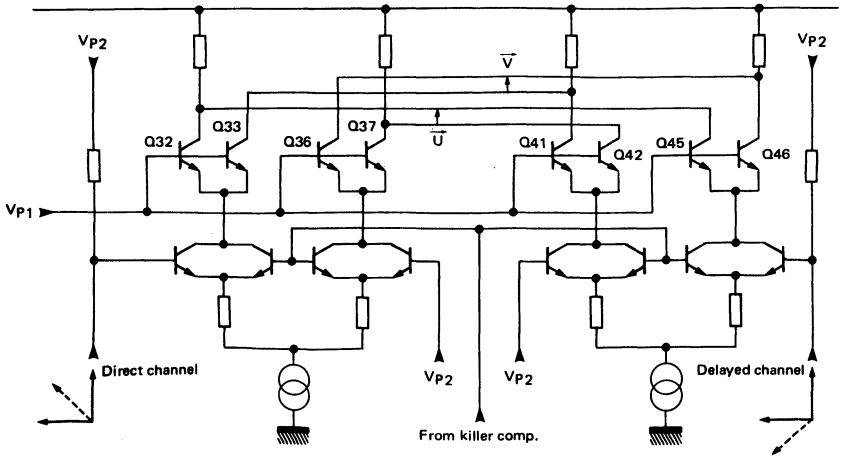
TYPICAL APPLICATION AND TEST CIRCUIT



GENERAL DESCRIPTION

DL MATRIX

The adding and substraction function for the direct signal and the delayed signal are also performed by the IC with the under circuit. The U matrix is made with Q32 - Q45 - Q37 - Q42 ; the V matrix is made with Q33 - Q41 - Q46 - Q36. The integration of the DL matrix only requires one delay line for the PAL/SECAM application with the TEA 5630. It also allows lower cost for external components.



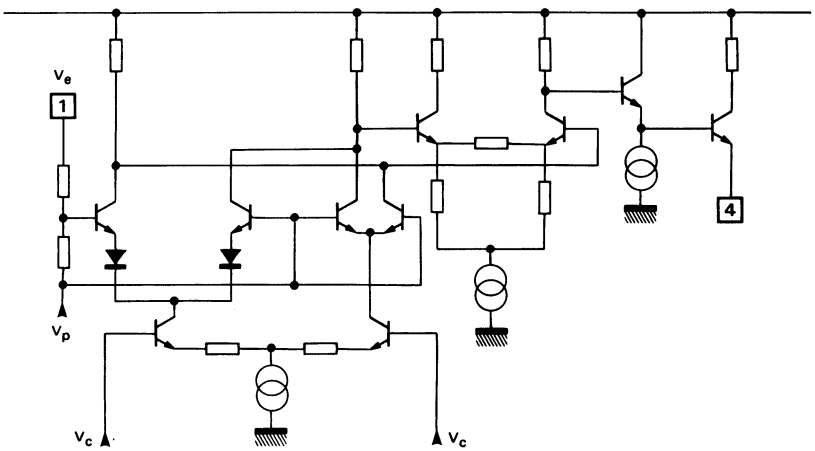
ACC AMPLIFIER

This ACC amplifier is performed with a double differential stage. The subcarrier is sent to the input of the first pair, while the second is connected to a reference voltage. The gain of the amplifier is controlled by the ACC voltage, by switching the bias current through a third differential pair.
The dynamic range obtained by this device is 32 dB. The bias voltage on the pin 1 is 5.6 V. The burst signal delivered by the pin 4 is about 0.6 Vpp for an input signal on pin 1 variable from 5 to 200 mV.

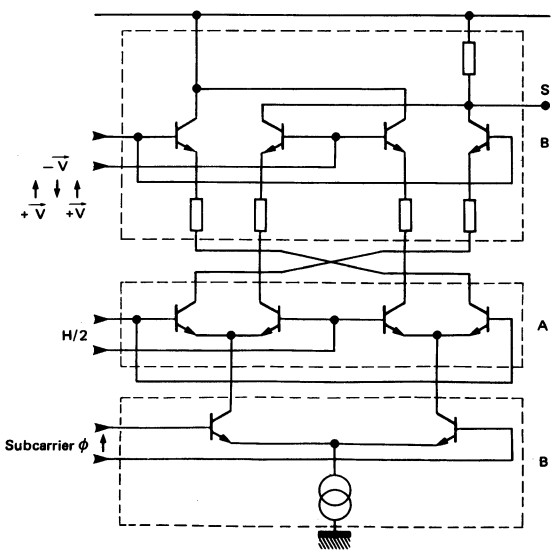
U AND V AXIS DECODERS

They consist on two phase detector stages (B). They provide output signals proportionnal to the magnitude of the chroma signal phased with the regenerated subcarrier feeding the stage.
The subcarrier is fed to the Vaxis decoder through an H/2 switch (A). This switch is required to make the phase of this signal the same than the burst.

ACC AMPLIFIER



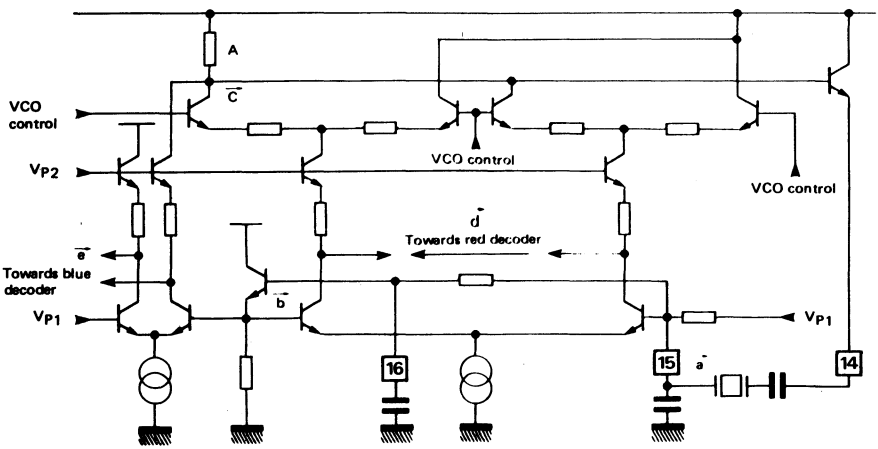
U AND V AXIS DECODERS

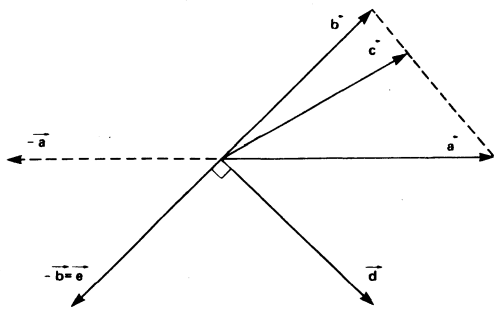


VOLTAGE CONTROL OSCILLATOR

The frequency of the VCO is depending on the vector adding performed at point A between $\vec{b}$ and $\vec{d}$ (see graphe). This adding is controlled by the voltage coming from the burst phase detector. This VCO is attractive because it uses a standard low cost Xtal. The 90° phase shift is made by vector addition and by a 45° phase shifter connected to the pin 16.

VOLTAGE CONTROL OSCILLATOR

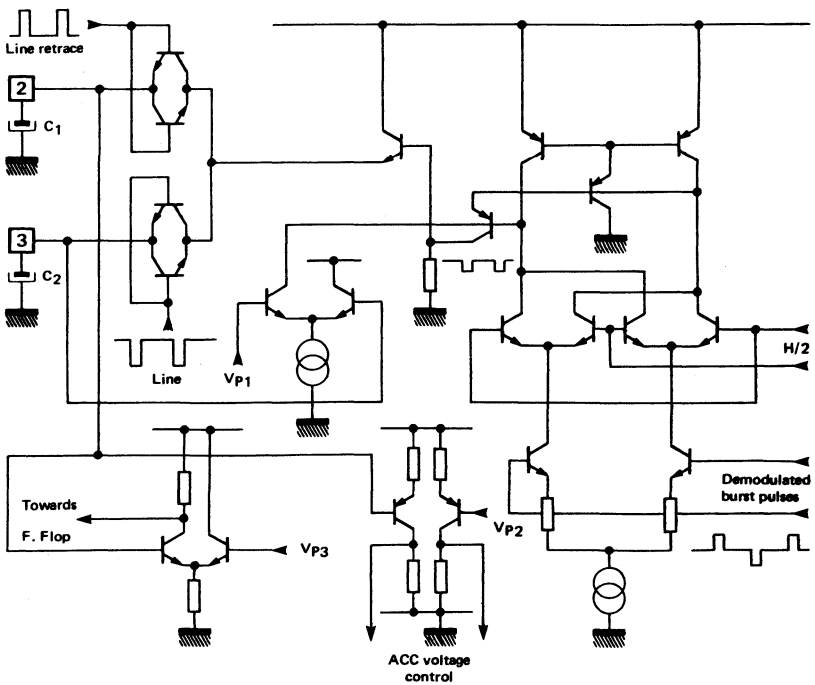




SAMPLING AND HOLD STAGE

This stage performs the identification and provides the ACC control voltage. A bias voltage is stored in C_2 capacitor during the line trace. The C_1 capacitor stores this bias voltage decreased by the demodulated burst peak value. So the differential voltage between C_1 and C_2 is not depending of a bias voltage, out of any drift, and therefore suitable to control the ACC amplifier.

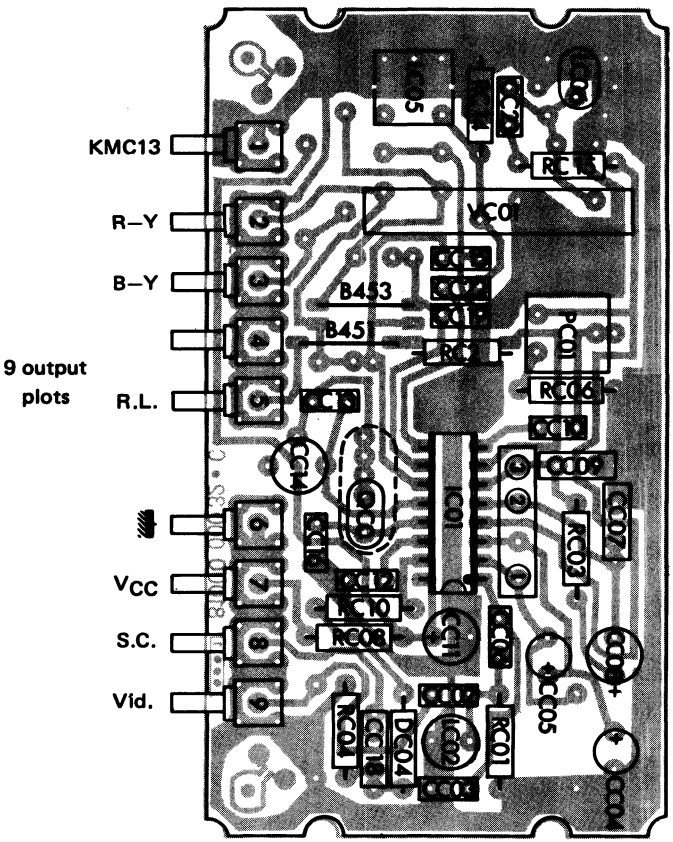
SAMPLING AND HOLD STAGE



TYPICAL APPLICATION

See electric diagram page 6

COMPONENT SIDE



N°	Capa.	U	%
CC02	47 pF		
CC03	820 pF		
CC04	2.2 µF	63	
CC05	4.7 µF	35	
CC06	100 pF		
CC07	0.01 µF	250	
CC08	1 µF	63	
CC09	0.01 µF	250	
CC10	10 nF		
CC11	47 µF	16	
CC12	56 pF		
CC13	12 pF		
CC14	10-30 pF		
CC15	33 pF		
CC16	56 pF		
CC18	0.1 µF	100	
CC19	33 pF		
CC22	10 nF		
CC23	10 nF		

N°	Value	P	%
RC01	820 Ω		5
RC02	5.6 k		5
RC03	6.8 kΩ		5
RC04	100 kΩ		5
RC06	1 kΩ		5
RC08	27 Ω		
RC10	5.6 kΩ		5
			5
			5
RC14	390 Ω		5
RC15	330 Ω		5

N°	Value
LC02	10 µH
LC05	7 - 13 µH
LC06	10 µH

N°	Value
VC01	DL710

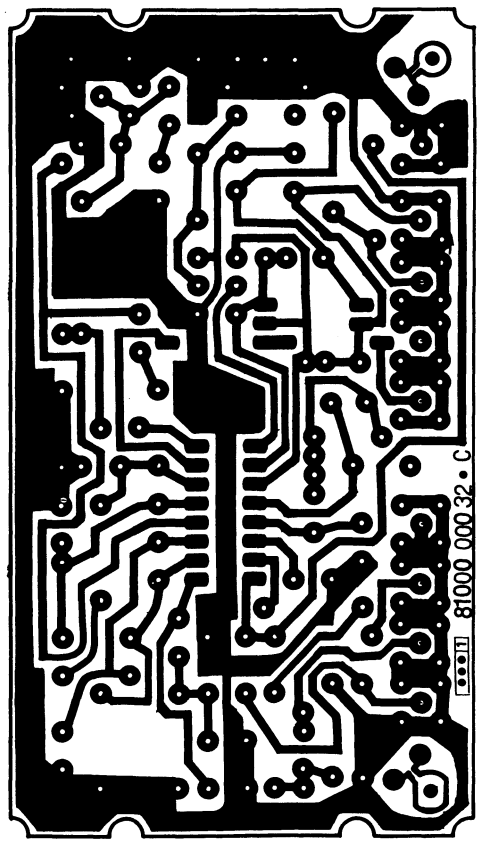
N°	Value
PC01	2.2 kΩ

N°	Value
QC0	4433.619 KHz

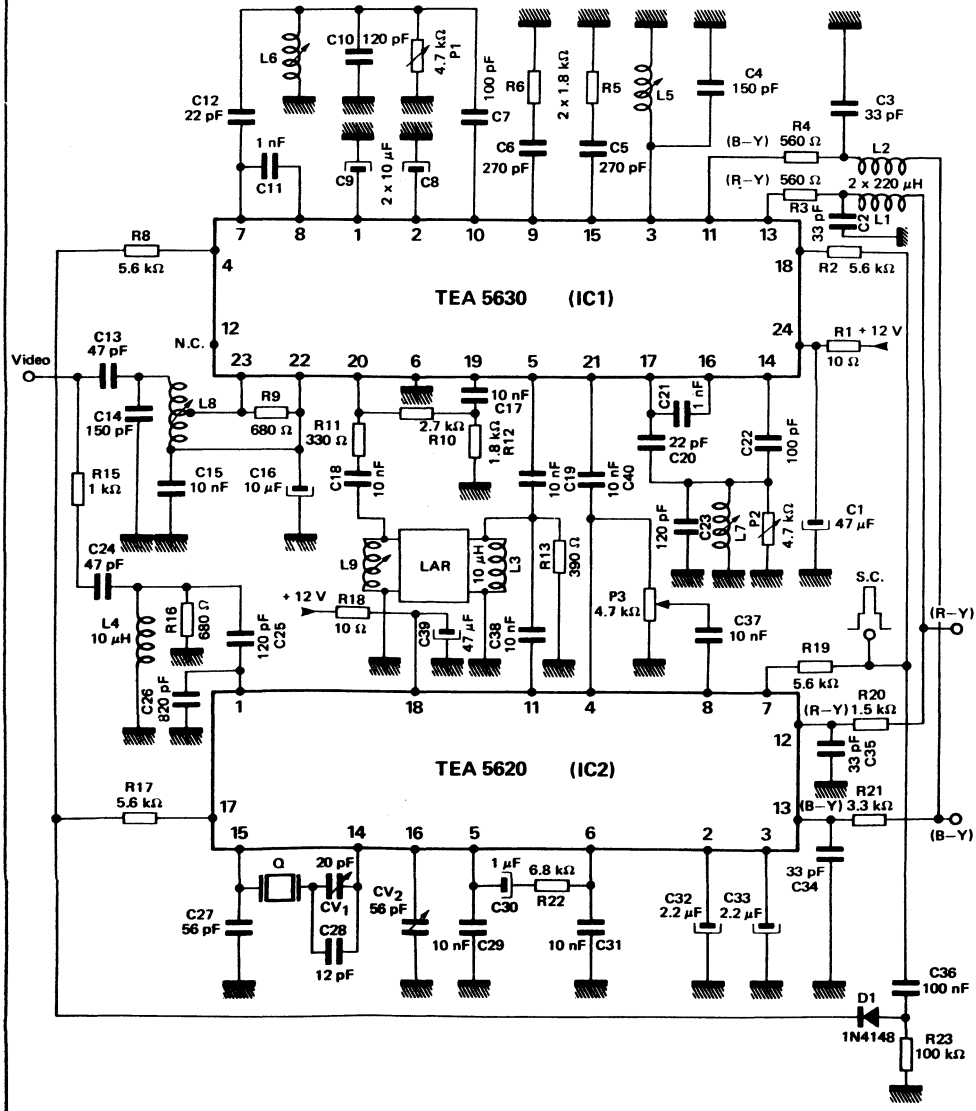
N°	Type
DC04	1N4148

N°	Type
IC01	TEA 5620

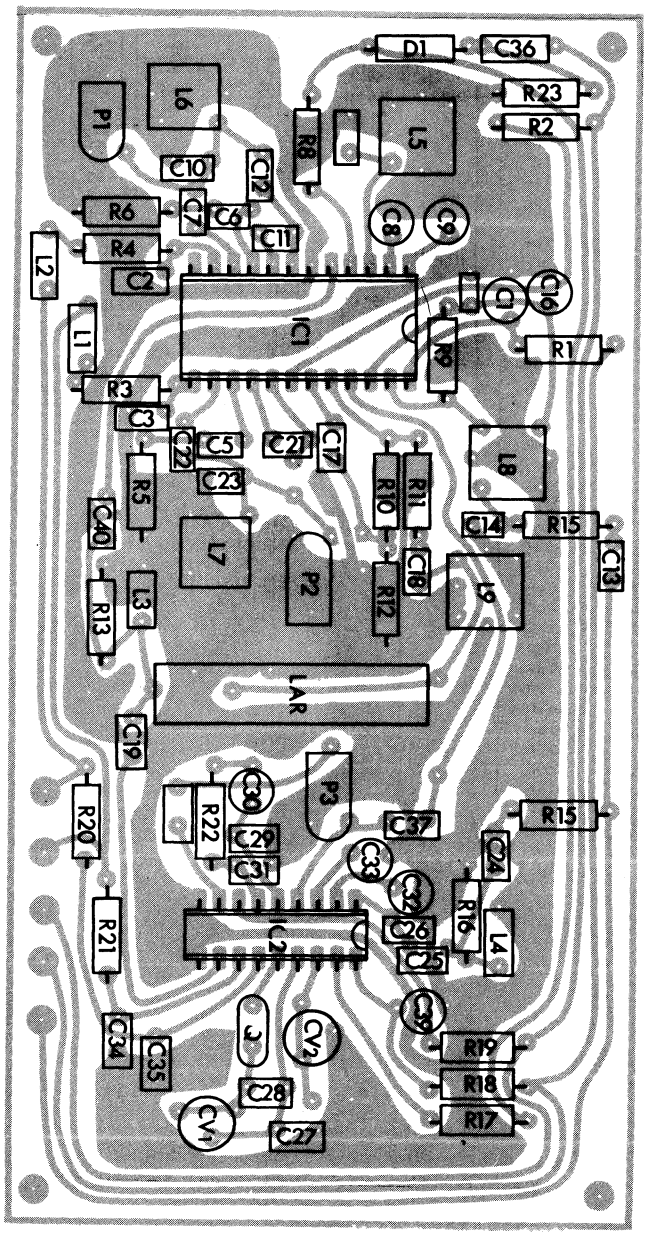
COPPER SIDE



PAL-SECAM APPLICATION
TEA5620-TEA5630



COMPONENT SIDE



N°	Value
C1	47 µF
C2	33 pF
C3	33 pF
C4	150 pF
C5	270 pF
C6	270 pF
C7	100 pF
C8-C9	10 µF/16 V
C10	120 pF
C11	1 nF
C12	22 pF
C13	47 pF
C14	150 pF
C15	10 nF
C16	10 µF/16 V
C17	10 nF
C18	10 nF
C19	10 nF
C20	22 pF
C21	1 nF
C22	100 pF
C23	120 pF
C24	47 pF
C25	120 pF
C26	820 pF
C27	56 pF
C28	12 pF
C29	10 nF
C30	1 µF/16 V
C31	10 nF
C32	2.2 µF/16 V
C33	2.2 µF/16 V
C34	33 pF
C35	33 pF
C36	100 nF
C37	10 nF
C38	10 nF
C39	47 µF/25 V
C40	10 nF

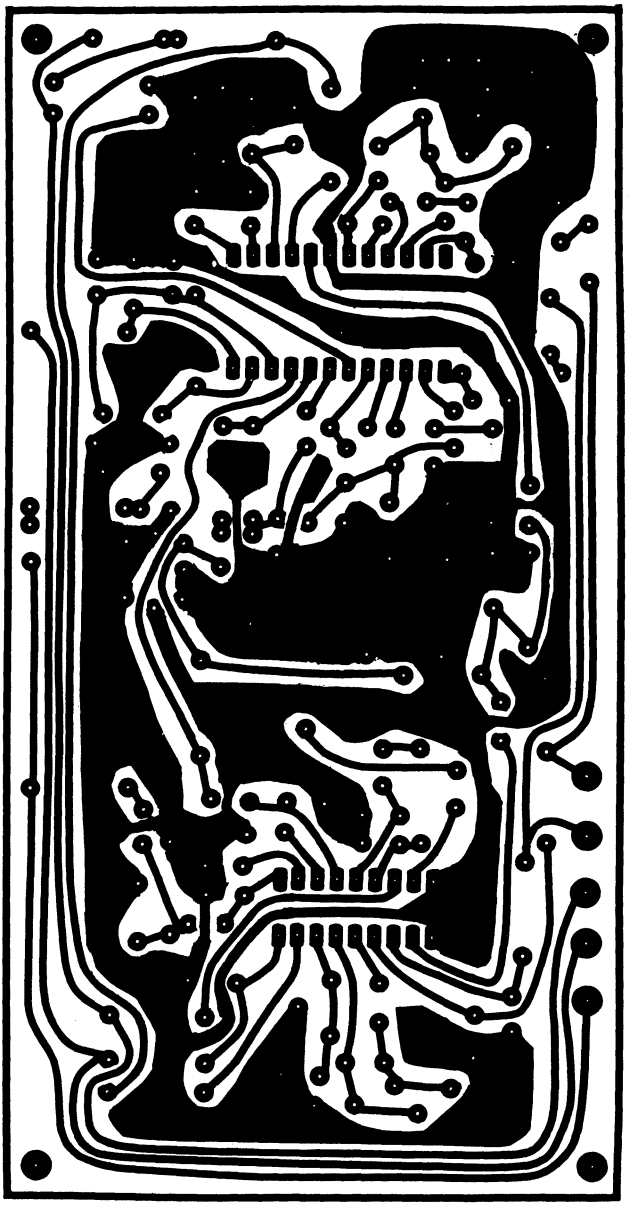
N°	Value
R1	10 Ω
R2	5.6 kΩ
R3	560 Ω
R4	560 Ω
R5	1.8 kΩ
R6	1.8 kΩ
R8	5.6 kΩ
R9	680 Ω
R10	2.7 kΩ
R11	330 Ω
R12	1.8 kΩ
R13	390 Ω
R15	1 kΩ
R16	680 Ω
R17	5.6 kΩ
R18	10 Ω
R19	5.6 kΩ
R20	1.5 kΩ
R21	3.3 kΩ
R22	6.8 kΩ
R23	100 kΩ

N°	Value
P1	4.7 kΩ
P2	4.7 kΩ
P3	4.7 kΩ
Q quartz	4.433 MHz
CV_1	3 - 30 pF
CV_2	6 - 60 pF

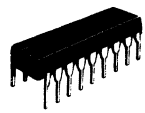
N°	Type or value
D1	1N4148
LAR:	LAA64 µs
IC_1	TEA 5630
IC_2	TEA 5620
L1	220 µH
L2	220 µH
L3	10 µH
L4	10 µH
L8	0.7 - 1.3 µH

N°	Type	Value
L5	TOKO RCL 36270 - 14	10-15 µH
L6	TOKO RCL 36270 - 13	7 µH
L7	TOKO RCL 36270 - 13	7 µH
L9	TOKO RCL 36270 - 09	10 µH

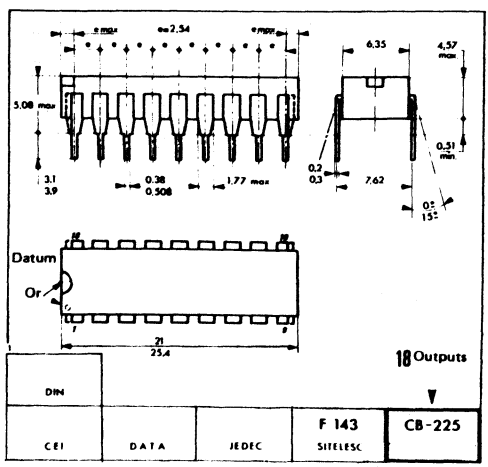
COPPER SIDE



CASE CB-225



DP SUFFIX
PLASTIC PACKAGE



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THOMSON SEMICONDUCTORS

TEA5630

ADVANCE INFORMATION

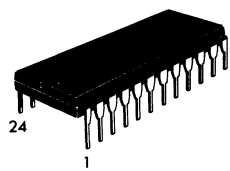
COLOR TV SECAM CHROMA SIGNAL PROCESSING CIRCUIT

MAIN FEATURES

- Subcarrier limiter
- R–Y, B–Y demodulators
- Identification and killer
- PAL-SECAM switches for multistandard application.

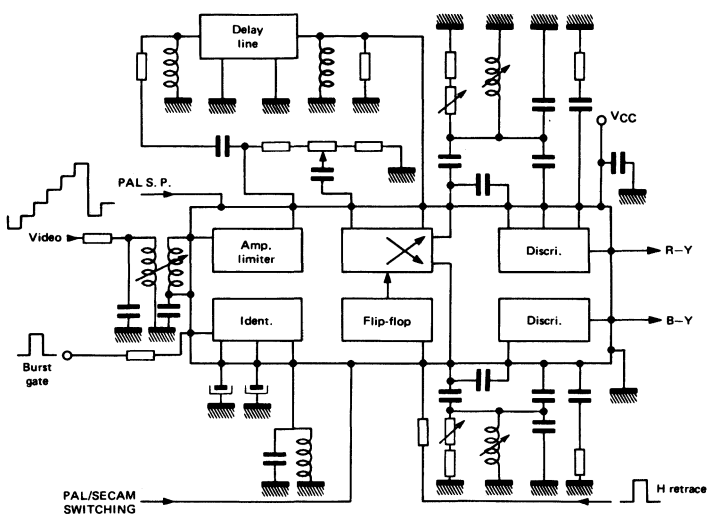
COLOR TV SECAM DECODER

CASE CB-68



DP SUFFIX
PLASTIC PACKAGE

SIMPLIFIED APPLICATION



SP8203-A

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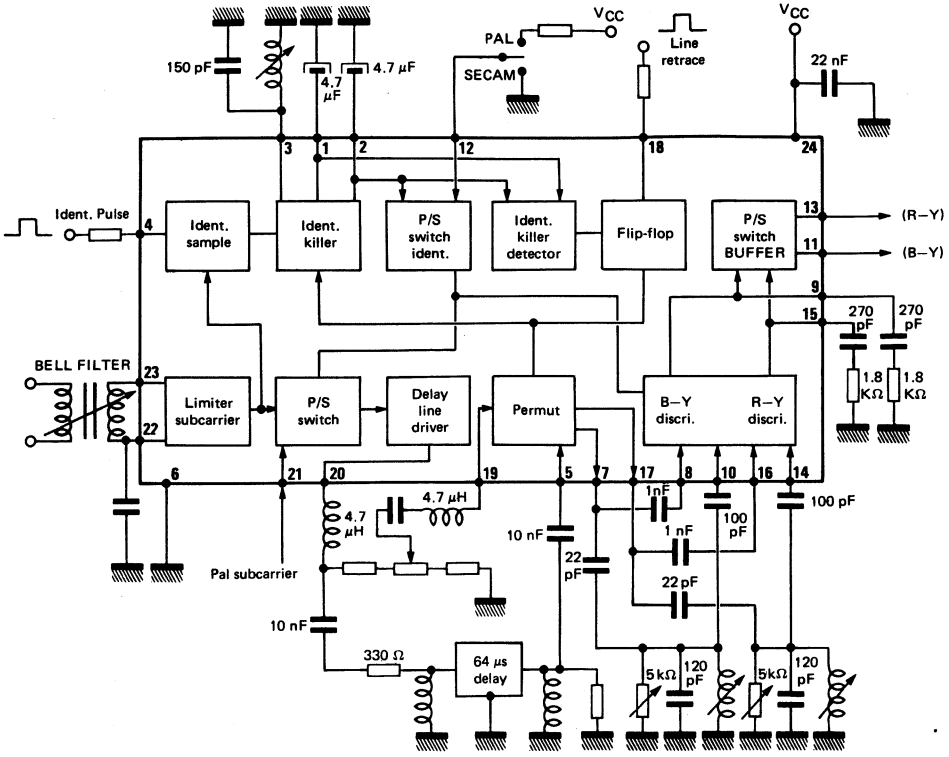
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

BLOCK DIAGRAM



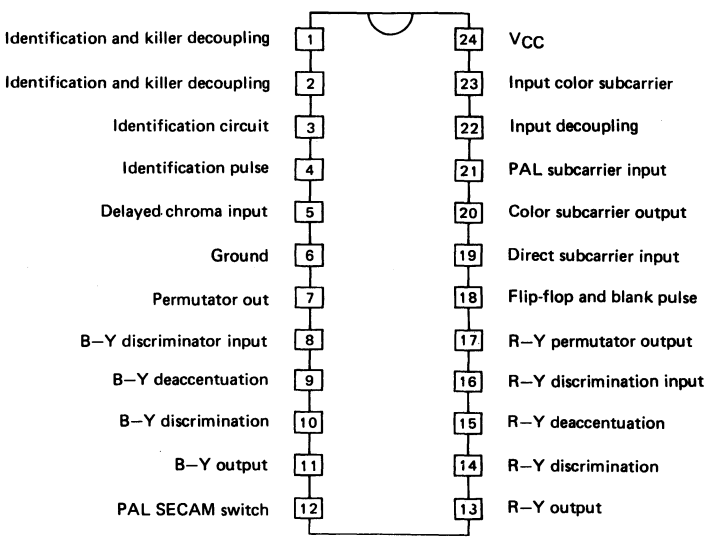
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	14.4	V
Power dissipation	P_{tot}	760	mW
Operating ambient temperature	T_{oper}	- 20 + 70	°C
Storage temperature	T_{stg}	- 55 + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal resistance Junction-ambient	$R_{th(j-a)}$	60	°C/W

PIN CONFIGURATION

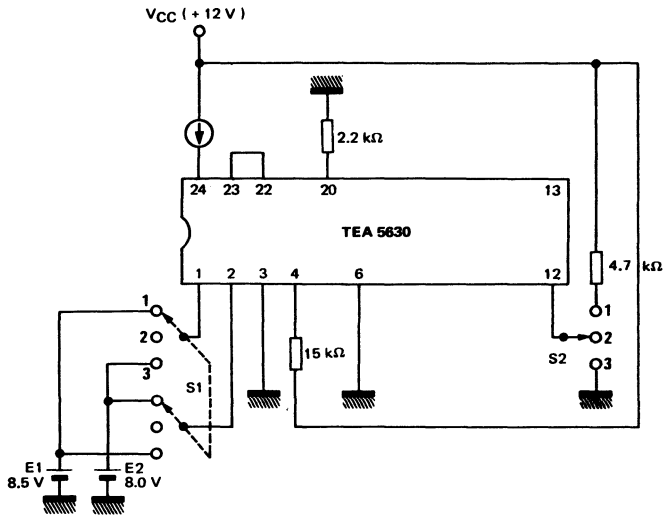


ELECTRICAL CHARACTERISTICS

$T_{amb} = +25°C$, $V_{CC} = 12$ V (unless otherwise noted).

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage	V_{CC}	9	12	13	V
Supply current (Test circuit 1, S1= 2 ; S2= 2)	I_{CC}	20	30	37	mA
Limiter amplifier output voltage pin 20 (V_e= 100 mV_{pp}, Test circuit 2)	V_O (1)	1.7	2.2	–	V_{pp}
Limiter amplifier output voltage pin 20 , V_e= –30 dB V_e= 3.2 mV_{pp}, Test circuit 2	V_O (2)	0.6	1.4	–	V_{pp}
PAL amplifier gain (V_e= 300 mV_{pp}, Test circuit 2) V_s pin 20 / V_e pin 21	A_V	0.95	–	1.3	–
Permutator output pin 7 - 17 (Vpin 19 – 5= 400 mV_{pp}, Test circuit 2)	–	–	1.4	–	V_{pp}
Permutator input impedance pin 19 - 5 (Test circuit 1, S1= 2 ; S2= 2)	–	–	2.5	–	KΩ
B–Y output pin 11 (colourbar signal generator 75 %, Test circuit 2)	e_o	0.6	1	1.3	V_{pp}
R–Y output pin 13 (colourbar signal generator 75 %, Test circuit 2)	e_o	0.7	1.2	1.6	V_{pp}
Color killer level (V_{in}= 100 mV_{pp}, Test circuit 2)	e_k	–34	–27	–20	dB
Permutator crosstalk (Test circuit 2, S7= 2)	C_{T1}	–	–60	–50	dB
PAL/SECAM Switching crosstalk (Test circuit 2)	C_{T2}	–	–33	–30	dB
H Pin 18 threshold	–	0.85	1	–	V
Identification sampling pulse threshold pin 4	–	0.65	0.8	0.9	V
Identification voltage pin 3	–	6	–	–	V_{pp}

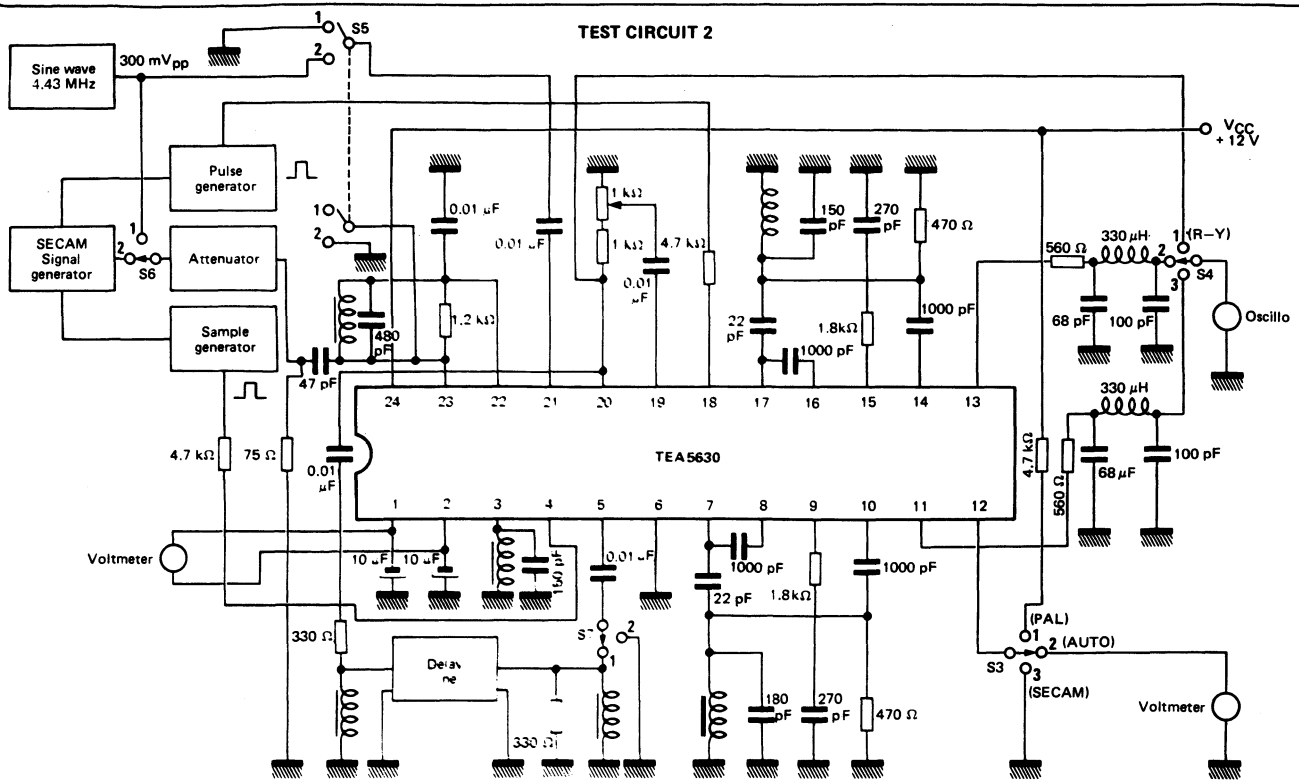
TEST CIRCUIT 1



DC ELECTRICAL CHARACTERISTICS

Pin voltage / Referred to ground	S1	S2	Min	Typ	Max	Unit
Pin 1 - 2	2	3	4.8	5.7	6.4	V
Pin 5 - 19	2	3	1.8	2.4	3	V
Pin 7 - 17	2	3	10.6	11.2	11.8	V
Pin 8 - 16	2	3	4.7	5.4	6.1	V
Pin 9 - 15	2	3	6.3	7.2	8	V
Pin 10 - 14	2	3	2.5	3.3	4	V
Pin 11 - 13	2	3	6.8	8	9	V
Pin 20	2	3	6.8	7.9	9	V
Pin 21	2	3	2.6	3.3	4	V
Pin 22	2	3	2.3	3	3.7	V
Pin 9 - 15	2	1	–	11.9	–	V
Pin 11 - 13	2	1	–	11.9	–	V

TEST CIRCUIT 2



	V_O (1)	V_O (2)	A_V	e_o (1) B–Y	e_o (1) R–Y	e_k	C_{T1}	C_{T2}
S_3	2	3	1	2	2	3	2	3
S_4	1	1	1	3	3	3	3	1
S_5	1	1	2	1	1	1	1	2
S_6	2	2	2	2	2	2	2	2

GENERAL DESCRIPTION

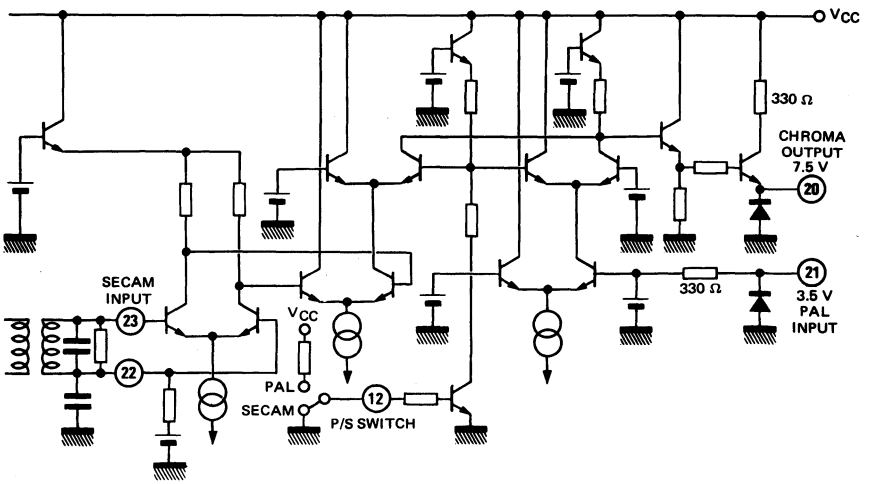
LIMITER AND CHROMA PAL/SECAM SWITCHING

The chroma signal is applied to the input of a limiter stage. After limitation the output signal is sent to an electronical switch which selects the signal coming from the limiter (for SECAM) or from the PAL input (Pin 21). The high output voltage of chrominance signal, 2.2 V_{pp} in SECAM operation, permits to obtain a minimum of crosstalk in the permutation and discrimination. The DC output voltage of the PAL IC connected in parallel for PAL/SECAM must be higher than $V_{CC} - 5$ V.

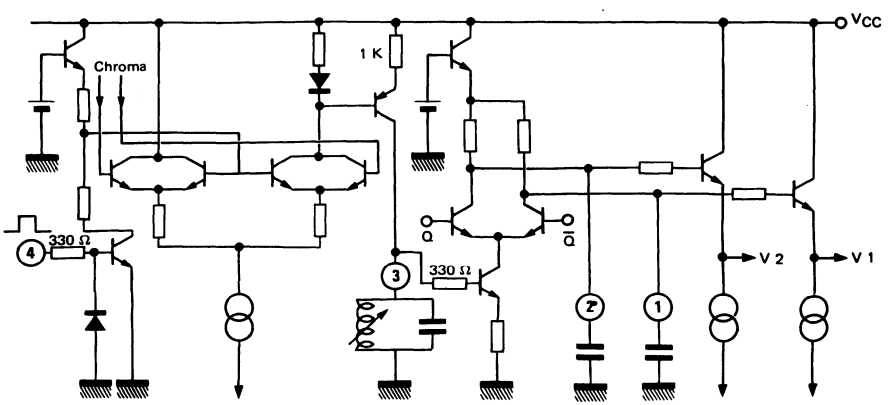
IDENTIFICATION AND KILLER

The identification information is sampled during the identification pulse (PIN 4). The burst differential amplitude voltage on the according circuit pin 3 is amplified and held by capacitors pin 2 and pin 1 to give the right flip-flop phase and killer information.
The circuit is able to identify line by line or line and frame. The choice of identification mode is programmable by the user depending on the identification pulse pin 4.

LIMITER AND CHROMA PAL/SECAM SWITCH



IDENTIFICATION AND KILLER



PERMUTATOR

Two inputs on the permutator :

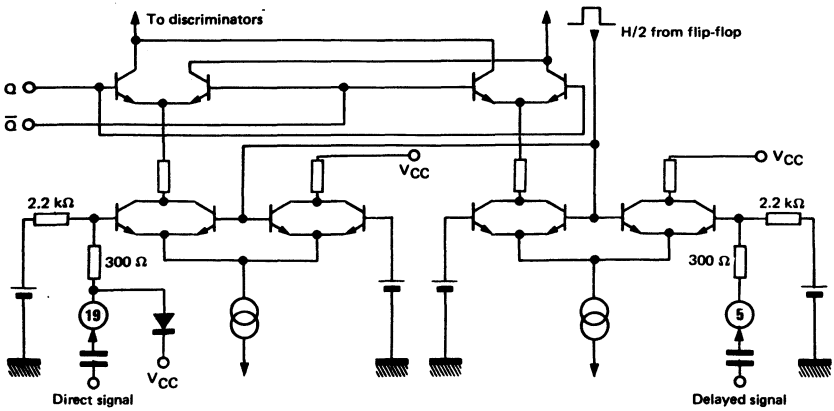
- the direct signal is sent on pin 19,
- the delayed signal is sent on pin 5.

The permutator is controled by a flip-flop at H/2 frequency in order to have (R−Y) signal on pin 17 and (B−Y) signal on pin 7. The output chroma signal typical value is 1.4 V.

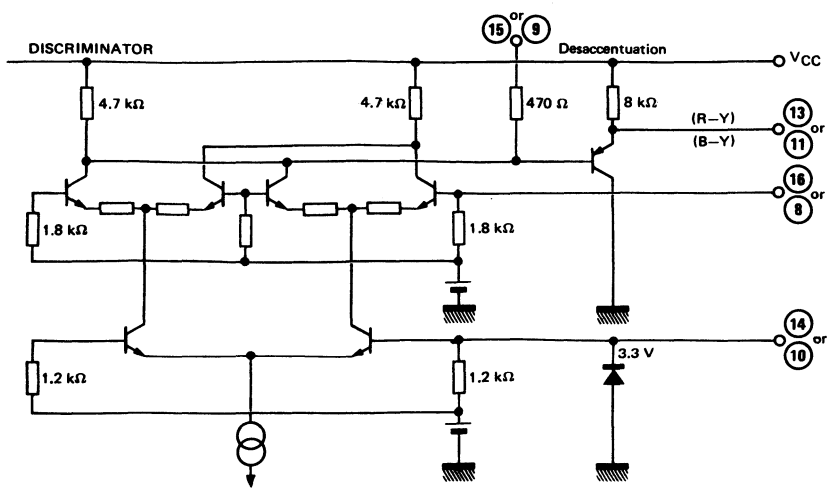
DISCRIMINATORS

They use coïncidence detectors with external according circuit L-C. The (R−Y) and (B−Y) demodulated signal amplitude and linearity can be adjusted by the choice of the damping resistor value in parallel with the L-C circuit. The desaccentuation circuit is connected on the load of the coïncidence detection.
Two PNP emitter followers provide the (R−Y) and (B−Y) signals at low impedance output.
In PAL operating the output impedance is equivalent to a 8 KΩ resistance between output and V_{CC}.

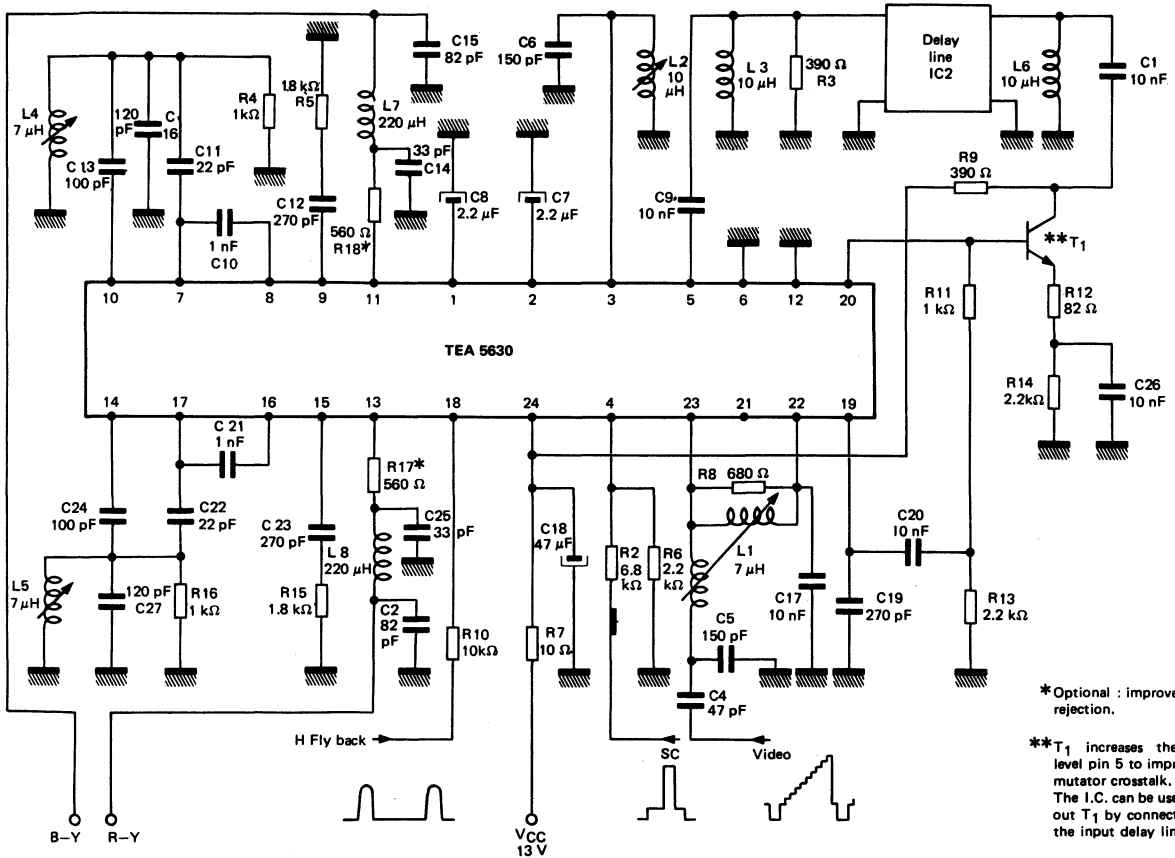
PERMUTATOR



DISCRIMINATORS



TYPICAL APPLICATION

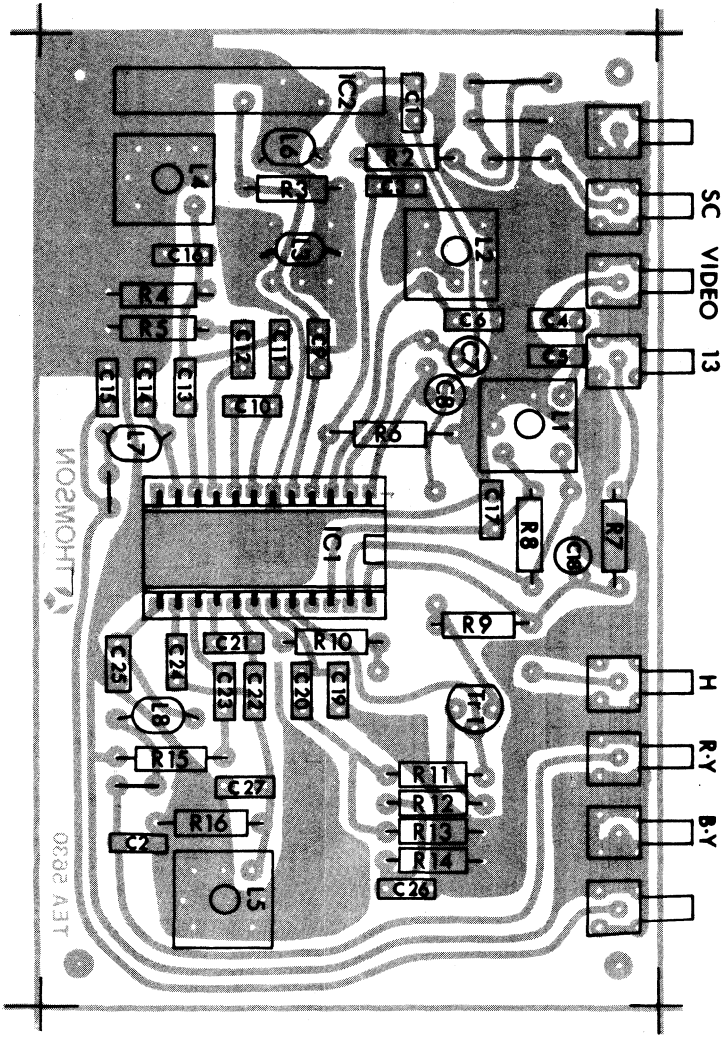


*Optional : improves subcarrier rejection.

**T_1 increases the subcarrier level pin 5 to improve the permutator crosstalk.
The I.C. can be used also without T_1 by connecting directly the input delay line at pin 20.

P.C BOARD AND COMPONENT LAYOUT (FOR SECAM DECODER)

COMPONENT SIDE



N°	Type
Tr1	BC548 B

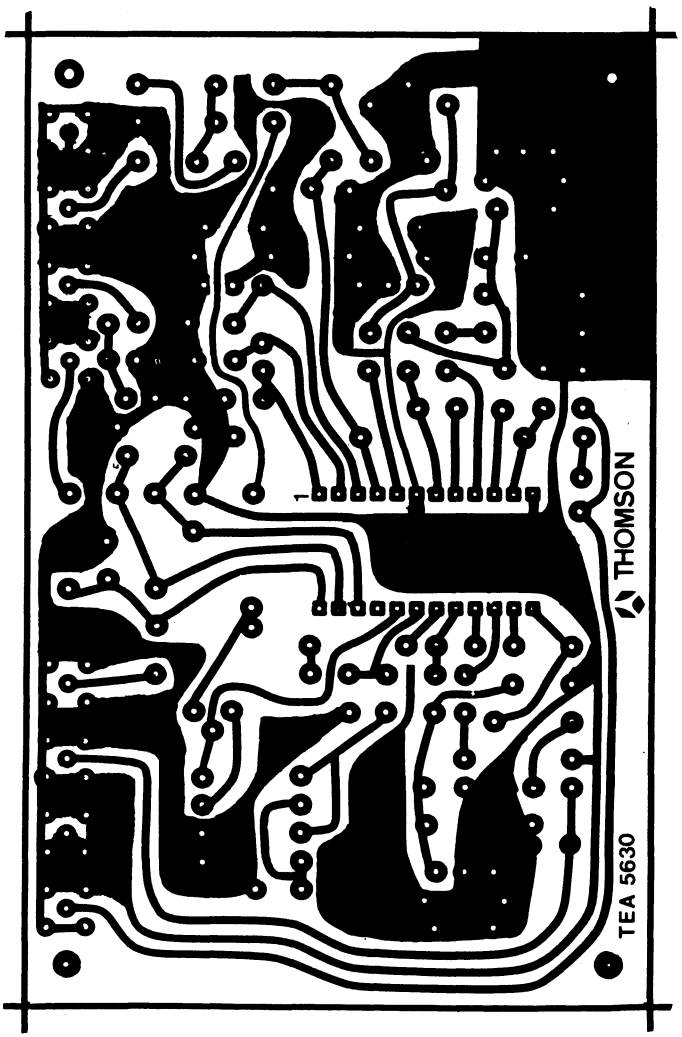
N°	Value
R2	6.8 kΩ
R3	390 Ω
R4	1 kΩ
R5	1.8 kΩ
R6	2.2 kΩ
R7	10 Ω
R8	680 Ω
R9	390 Ω
R10	10 kΩ
R11	1 kΩ
R12	82 Ω
R13	2.2 kΩ
R14	2.2 kΩ
R15	1.8 kΩ
R16	1 kΩ
R17*	560 Ω
R18*	560 Ω

N°	Capa.
C1	10 nF
C2	82 pF
C3	100 pF
C4	47 pF
C5	150 pF
C6	150 pF
C7	2.2 µF
C8	2.2 µF
C9	10 nF
C10	1 nF
C11	22 pF
C12	270 pF
C13	100 pF
C14	33 pF
C15	82 pF
C16	120 pF
C17	10 nF
C18	47 µF
C19	270 pF
C20	10 nF
C21	1 nF
C22	22 pF
C23	270 pF
C24	100 pF
C25	33 pF
C26	10 nF
C27	120 pF

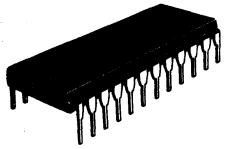
N°	Type	Val.
L1	Toko RCL 3627010	~7 µH
L2	" " 3627014	10-15 µH
L3		10 µH
L4	" " 3627013	~7 µH
L5	" " 3627013	~7 µH
L6		10 µH
L7		220 µH
L8		220 µH

*Optional : improves subcarrier rejection.

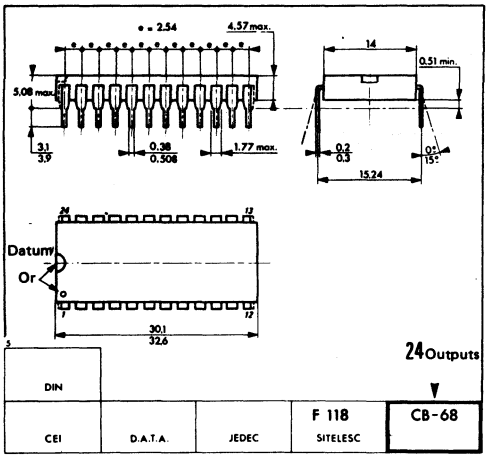
COPPER SIDE



CASE CB-68



DP SUFFIX
PLASTIC PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

UAA4000

REMOTE CONTROL TRANSMITTER

The UAA4000 is an easily expandable, 32 command, pulse position modulation transmitter drawing zero standby current.

- Ultrasonic or infra-red transmission
- Direct drive for ultrasonic transducer
- Direct drive of visible LED when using infra-red
- Very low power requirements
- Pulse position modulation gives excellent immunity from noise and multipath reflections
- Single pole key matrix
- Switch resistance up to 1 kΩ tolerated
- Few external components
- Anti-bounce circuitry on chip.

Quick reference data

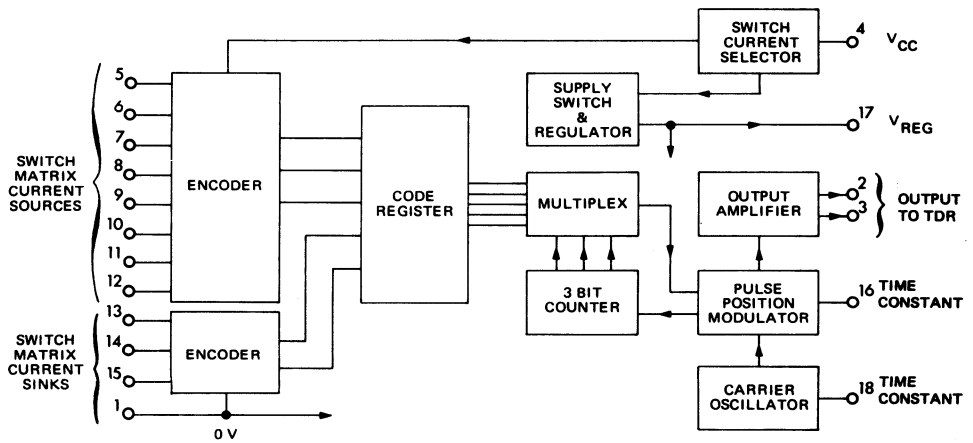
- Power supply : 9 V, standby 6 μA, operating 8 mA
- Modulation : pulse position with or without carrier
- Coding : 5 bits word giving a primary command set of 32 commands
- Key entry : 8 x 4 single pole key matrix
- Date rate : selectable 1 bit/sec to 10 k bit/sec
- Carrier frequency : selectable 0 Hz (no carrier) to 200 Hz.

REMOTE CONTROL TRANSMITTER

CASE CB-225

DP SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



NT8050R1-A

THOMSON SEMICONDUCTORS
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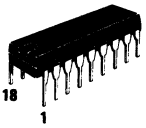
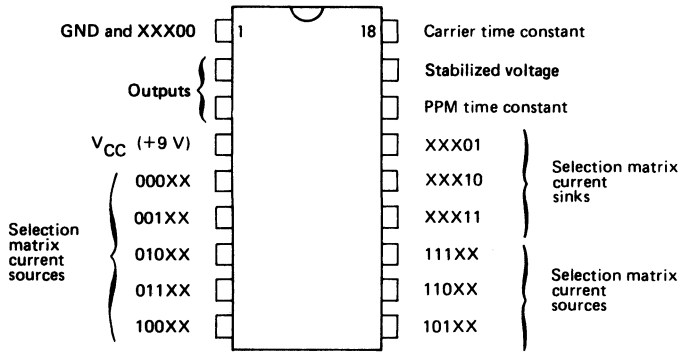
THOMSON COMPONENTS

PIN CONFIGURATION

CASE CB-225

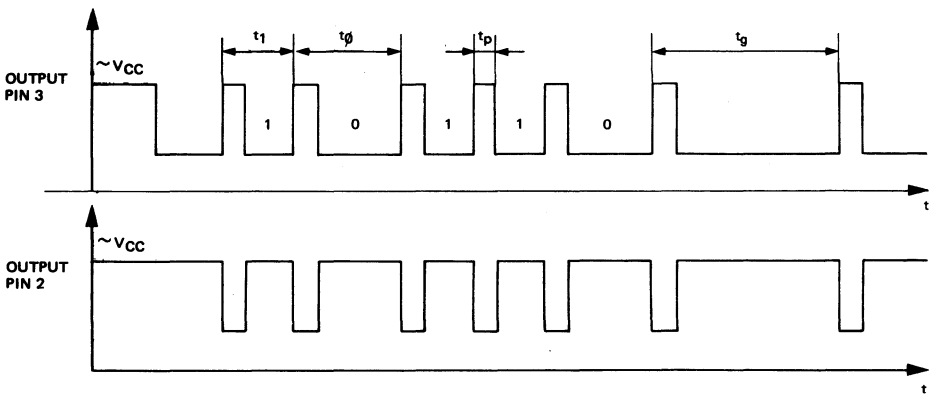




MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating voltage range, V4	V_{CC}	7 to 11	V
Maximum power dissipation	P_{tot}	600	mW
Maximum output current (Pin 3)	I_C	5	mA
Operating temperature range	t_{oper}	−10 to+ 65	°C
Storage temperature range	t_{stg}	−55 to+ 125	°C

OUTPUT WAVEFORMS (PPM WORD NOTATION)

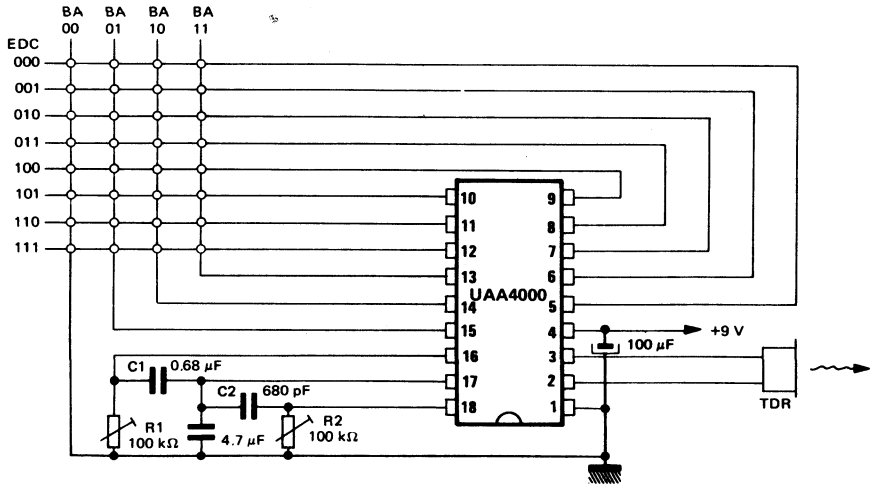


ELECTRICAL CHARACTERISTICS (See test circuit next page)
T_{amb}= 25°C, V_{CC} = 9 V, f_o = 40 KHz, t_1 = 18 ms
4.7 µF capacitor on pin 17 (Unless otherwise noted).

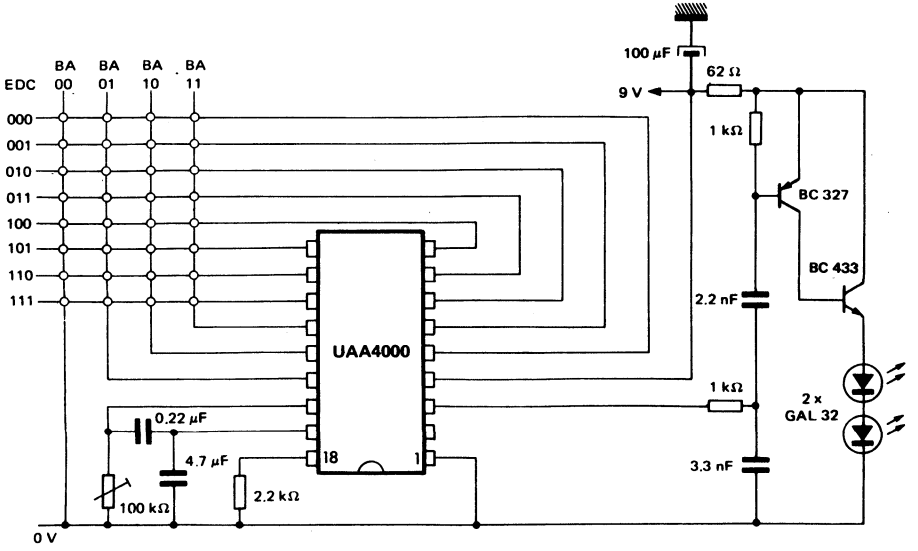
Characteristic		Symbol	Min	Typ	Max	Unit
Operating supply current	Pin 4		–	8	16	mA
Standby supply current	Pin 4		–	–	30	µA
Stabilized voltage	Pin 17		3.9	4.2	4.5	V
Output current available	Pin 17		–	–	1	mA
Output voltage swing (Unloaded)	Pins 2, 3		–	8	V_{CC}	V
Output current (Peak value)	Pins 2, 3		–	–	5	mA
External switch resistance			–	–	1	kΩ
External switch closing time			6	–	–	ms
External carrier oscillator (R2 required, C_2 = 680 pF)	Pin 18		20	40	80	kΩ
External PPM resistor (R1 required, C_1 = 0.68 µF)	Pin 16		15	30	60	kΩ
Ratio t0/t1	Pins 2, 3		1.4	1.5	1.6	
Pulse width	Pins 2, 3	t_p	2	3	4	ms
Inter-word gap	Pins 2, 3	t_g	50	54	58	ms

APPLICATION CIRCUITS

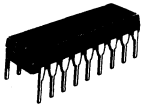
TEST AND ULTRASONIC APPLICATION CIRCUIT



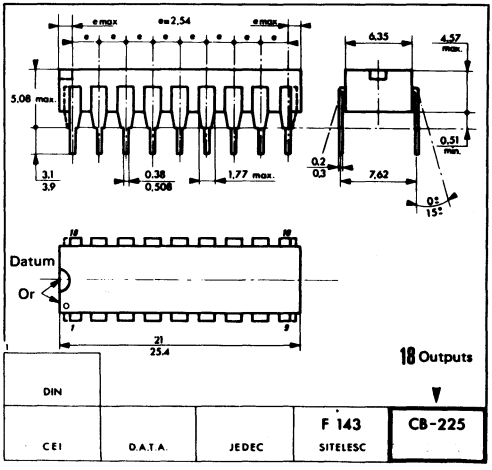
INFRA-RED APPLICATION CIRCUIT



CASE CB-225



DP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

UAA4000S

ADVANCE INFORMATION

REMOTE CONTROL TRANSMITTER

The UAA4000S is an easily expandable, 32 command, pulse position modulation transmitter drawing zero standby current.

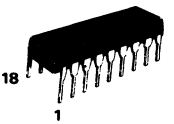
- Ultrasonic or infra-red transmission
- Direct drive for ultrasonic transducer
- Direct drive of visible LED when using infra-red
- Very low power requirements
- Pulse position modulation gives excellent immunity from noise and multipath reflections
- Single pole key matrix
- Switch resistance up to 1 kΩ tolerated
- Few external components
- Anti-bounce circuitry on chip.

Quick reference data

- Power supply : 9 V, standby 6 μA, operating 8 mA
- Modulation : pulse position with or without carrier
- Coding : 5 bits word giving a primary command set of 32 commands
- Key entry : 8 x 4 single pole key matrix
- Date rate : selectable 1 bit/sec to 10 k bit/sec
- Carrier frequency : selectable 0 Hz (no carrier) to 200 Hz.

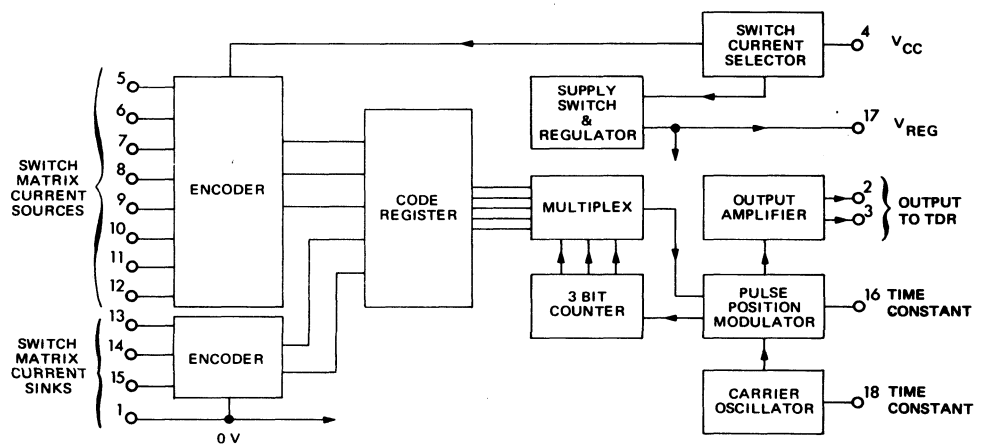
REMOTE CONTROL TRANSMITTER

CASE CB-225



DP SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



SP8244-A

THOMSON SEMICONDUCTORS
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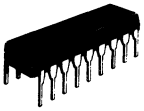
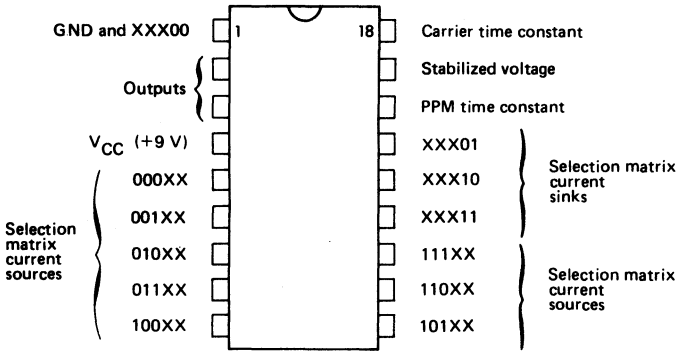
THOMSON COMPONENTS

PIN CONFIGURATION

CASE CB-225

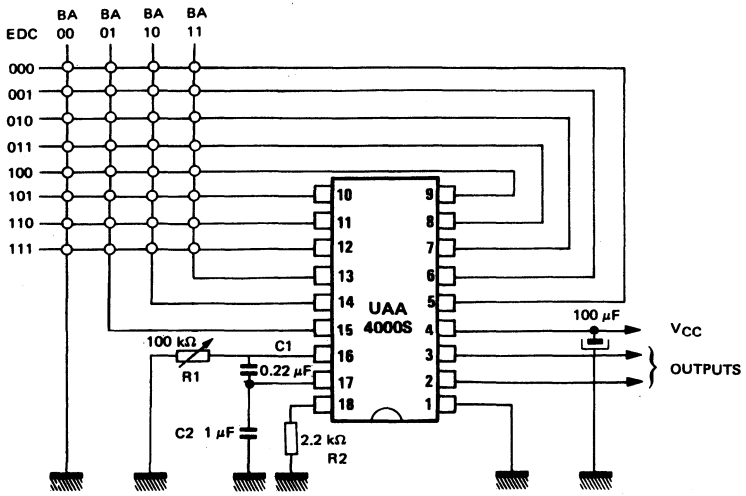




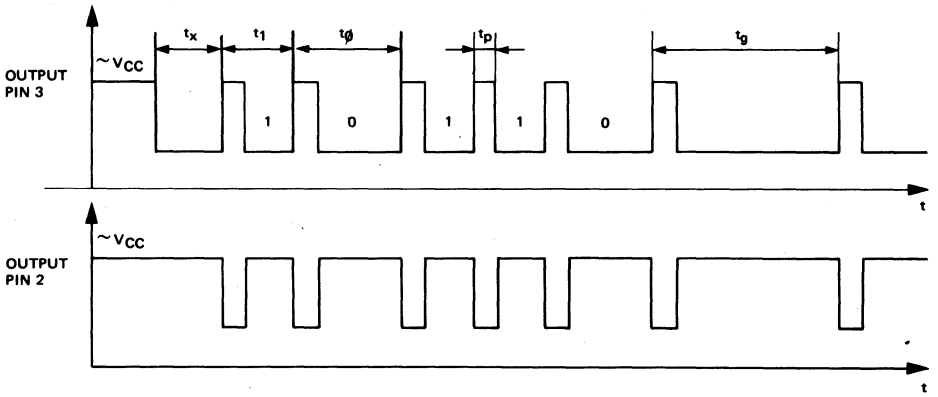
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating voltage range, V4	V_{CC}	6.5 to 11	V
Maximum power dissipation	P_{tot}	600	mW
Maximum output current (Pin 3)	I_C	10	mA
Operating temperature range	t_{oper}	−10 to+ 65	°C
Storage temperature range	t_{stg}	−55 to+ 125	°C

TEST AND INFRA-RED APPLICATION CIRCUIT



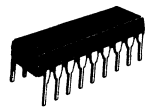
OUTPUT WAVEFORMS (PPM WORD NOTATION)



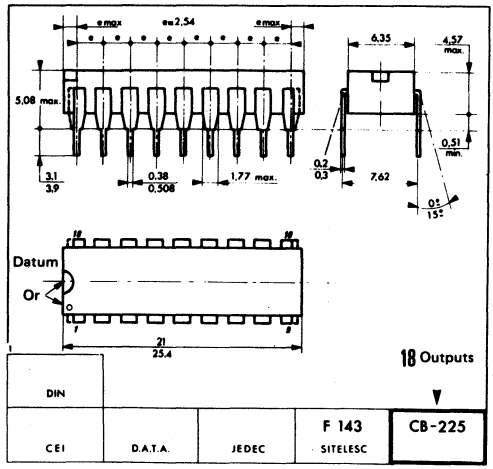
ELECTRICAL CHARACTERISTICS (See test circuit previous page)
T_{amb} = 25°C, V_{CC} = 6.5 to 11 V
1 µF capacitor on pin 17 (Unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
Operating supply current (V_{CC} = 9 V)	Pin 4		–	8	16	mA
Standby supply current (V_{CC} = 9 V)	Pin 4		–	–	10	µA
Stabilized voltage	Pin 17		3.9	4.2	4.5	V
Output voltage swing (unloaded)	Pin 3		–	–	V_{CC}–0.1	V
Output current available	Pin 17		–	–	1	mA
Output current (V_{CEsat} = 1 V)	Pin 2		–	–	10	mA
	Pin 3		–	–	5	mA
External switch resistance	Pins 5 to 15					
ON			–	–	5	kΩ
OFF			–	–	2	MΩ
External switch closing time			6	–	–	ms
External PPM resistor (R_1 required, C_1 = 0.22 µF)	Pin 16		15	30	60	kΩ
Ratio t0/t1	Pins 2, 3		1.4	1.5	1.6	
Pulse width	Pins 2, 3	t_p	2	3	4	ms
Pre-pulse width	Pin 3	t_x	–	(2.15 to 2.33) x t_1	–	ms
Timing tolerance t_1			–	± 5	–	%
Jitter time of t_1		Δt_1	–	± 1	–	%
Inter-word gap		t_g	–	$3t_1 + \Delta t_1$	–	ms
Pre-pulse fall time			–	200	–	µs

CASE CB-225



DP SUFFIX
PLASTIC PACKAGE



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THOMSON SEMICONDUCTORS

UAA4009

ADVANCE INFORMATION

REMOTE CONTROL RECEIVER

UAA4009 is an I2L/BIPOLAR circuit for use as a receiver of remote control signals for television control applications.

This device :

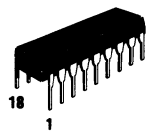
- receives 15 of the 32 codes transmitted by the UAA4000 (PPM),
- commutes tuning voltage for 12 TV channels,
- provides 0 to 6 V voltage (16 steps) for one electronic potentiometer,
- gives "stand-by" information.

MAIN FEATURES

- On-chip oscillator,
- Used with IR or ultrasonic transmission system,
- 5 bits PPM modulation, first transmitted must be zero,
- 2 successive codewords comparison,
- 12 channels set either by remote control or output pin grounding,
- Muting during channel change,
- Priority channel set by external capacitor,
- $V^+ = 12$ V
- $I^+ = 15$ mA
- PPM pulses : ----- 12 V typ. / ___ 0 V
- Channel output : open NPN collector with feed-back information.
- Stand-by output : open NPN collector
- V_{max} output : 35 V.

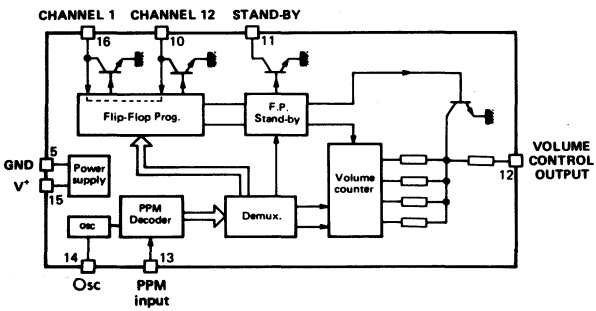
REMOTE CONTROL RECEIVER

CASE CB-225

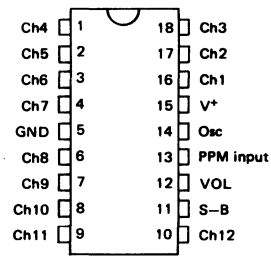


DP SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



SP8209-A 1/6

THOMSON SEMICONDUCTORS
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THOMSON COMPONENTS

GENERAL DESCRIPTION

PPM DEMODULATION

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. Frequency is linked with transmission rate.
Following numerical values are given at f = 5.1 KHz.
For example, 5.1 KHz ensures potentiometer up or down travelling to be completed in about 5.5 s and channel 1 is set in 120 ms.

Each pulse that is received starts a counter. Input is masked for first 3.5 ms. Windows from 3.5 to 7 ms and from 7 to 13 ms determine whether a 1 or a 0 is present. Periods between pulses of 13 to 25.5 ms are recognised as word intervals.

Checks are made to ensure 5 bits are received for a word to be valid ; two consecutive and identical words allow corresponding function activation, 13 ms after receiving last pulse of the 2nd word (max 109 ms after first pulse of the first word).

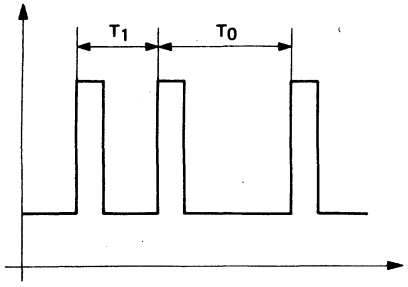
CODES

00001	Channel 1
00010	Channel 2
00011	Channel 3
00100	Channel 4
00101	Channel 5
00110	Channel 6
00111	Channel 7
01000	Channel 8
01001	Channel 9
01010	Channel 10
01011	Channel 11
01100	Channel 12
01101	Stand-by ON
01110	Volume UP
01111	Volume DOWN

NOTES : • 00001
1st last to be transmitted.

• Other codes are ignored.

PPM INPUT PULSES



CHANNELS

Channel activation is achieved either by remote control, or directly by momentary grounding corresponding pin of the circuit. This allows local push-switch control without external components.

Outputs : an open collector transistor grounds desired pin while others are high impedance (V_{max} = 35 V). The typical current grounded is 10 mA.

STAND-BY

S – B is activated (S – B ON) only by remote control ; it is disabled by activation of any channel either by remote control or front-panel switches.

S – B ON activates muting.

Output : Open collector S – B ON : high impedance
S – B OFF : grounded.

MUTING

During channel change or while S – B is on, volume is reduced to minimum by grounding external capacitor. When muting is released, volume goes back to previous value by charging capacitor with RC constant to be adjusted at desired value (R is 2 kΩ typ.).

VOLUME

A four bits binary counter drives a resistors array. It provides 0 to 6 V variation in 16 steps. Output impedance is 2 kΩ (50 Ω if muting is on).
Increment is inhibited when S – B is ON.

BEHAVIOUR AT START

When power is switched on :

- volume is preset at 0111 digital state, that is 2.8 V on volume output.
- channel with greatest capacity to the ground is activated.
  Ex. : on "typ. app. fig.", 2.2 nF have been connected to channel N.

OSCILLATOR

The minimum resistor value on pin 14 is 30 kΩ.

$T = C\,(160\,R + 1660)$ for V_{CC} = 12 V.

T = oscillator period (μs)
C = capacitance (μF)
R = resistance (KΩ).

NB :

- When S – B is ON, 33 V tuning voltage must keep present. Otherwise all outputs are going to ground and consequently S – B is disabled.
- V^+ 12 V must be present to ensure output can accept 33 V.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	10 → 15	V
Voltage on "channel off" pins	V_{CHoff}	35	V
Current on "channel on" pins	I_{CHon}	20	mA
PPM input high voltage	V_{in}	20	V
Stand-by on voltage	V_{SBon}	15	V
Stand-by off current	I_{SBoff}	2	mA
Volume output current (available)	I_{VOL}	2	mA
Operating ambient temperature	T_{oper}	0+ 70	°C
Max power dissipation	P_{tot}	500	mW

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	70	°C/W

ELECTRICAL CHARACTERISTICS V_{CC} = 12 V ; T_{amb} = + 25°C (unless otherwise noted)

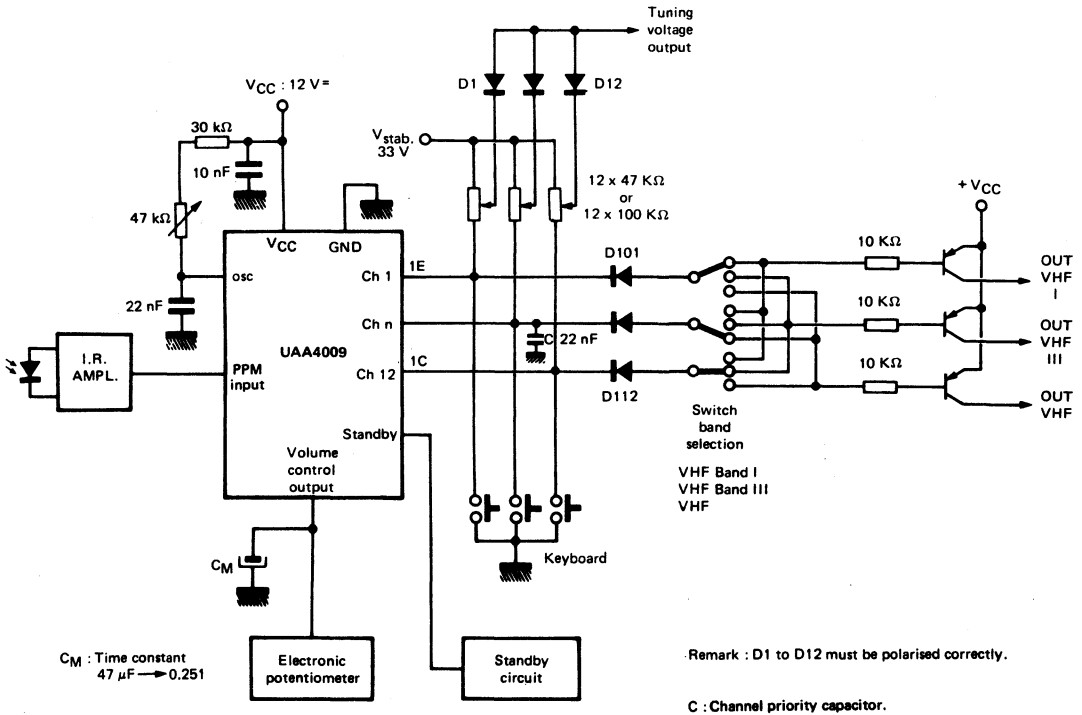
Characteristic	Symbol	Min	Typ	Max	Unit
Supply current	I_{CC}	10	15	30	mA
Voltage on "channel off" pins	V_{CHoff}	–	33	35	V
Current on "channel off" pins (V_{CHoff} = 33 V)	I_{CHoff}	–	–	1	µA
Voltage on "channel on" pins (I_{CHon} = 10 mA)	V_{CHon}	–	50	80	mV
Current on "channel on" pins	I_{CHon}	–	10	20	mA
Temperature coefficient	$\frac{\Delta V_{CHon}}{\Delta \theta}$	–	150	300	µV/°C
PPM input low voltage	V_{in}	–	0 to 3	–	V
PPM input low current (V_{in} = 0 V)	I_{in}	–	–30	–	µA
PPM input high voltage	V_{in}	–	5	20	V
PPM input high current (V_{in} = V_{CC} = 12 V)	I_{in}	–	2	–	µA
Stand-by on voltage	V_{SBon}	–	V_{CC}	15	V
Stand-by on current (V_{SBon} = 12 V)	I_{SBon}	–	–	1	µA
Stand-by off voltage (at I_{SBoff} = 1 mA)	V_{SBoff}	–	–	0.15	V
Stand-by off current	I_{SBoff}	–	1	2	mA
Volume voltage swing (unloaded)	ΔV_{VOL}	4.9	6	7	V
Volume voltage (step zero)	V_{VOL}	–	50	100	mV
Starting volume voltage	V_{VOLst}	–	2.8	–	V
Volume output impedance (S - B off)	R_{OUTvol}	1.4	2	2.6	kΩ
(S - B on)	R_{OUTVOL}	35	50	65	Ω
Volume output current (available)	I_{VOL}	–	–	2	mA
Temp. coefficient volume-voltage (Load= 20 kΩ)	$\frac{\Delta V_{VOL}}{\Delta \theta}$	–	2	–	mV/°C
V_{CC} ripple rejection (50→100 Hz)	–	30	40	–	dB
Oscillator frequency	F_{osc}	0.5	5.1	10	KHz
Optimum oscillator adjustment with UAA4000 transmitter	T*	–	1/29	–	t"1" transmitted
Input pulse width	–	10	–	–	µs
PPM window for "1"	t"1"	19.5	–	34.5	T*
for "0"	t"0"	35.5	–	66.5	T*
for "synchro"	t"s"	67.5	–	130.5	T*
Oscillator max allowable dispersion (transmitter f_{osc}= cst)	f_{osc}	–	–	± 20	%
Channel change delay	T_{ch}	–	2 words+ 67 T*	–	–
Volume swing average delay	T_{VOL}	2.8	2.8 x 10^4 T*	–	s

EXTERNAL FORCED SWITCHING

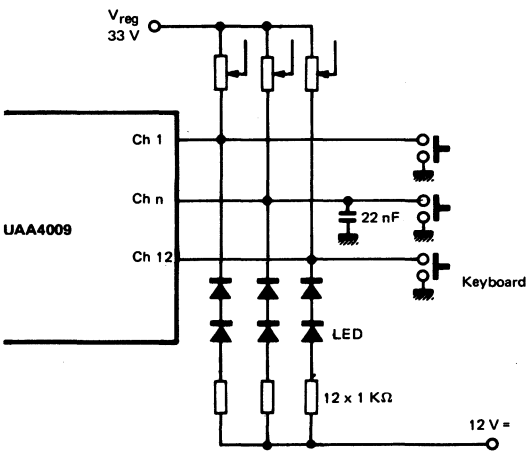
External channel activating level	–	–	–	3.5	V
Minimum switching time	–	–	20	–	µs

T* : Receiver oscillator period at optimal frequency matching between transmitter and receiver.

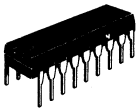
TYPICAL APPLICATION



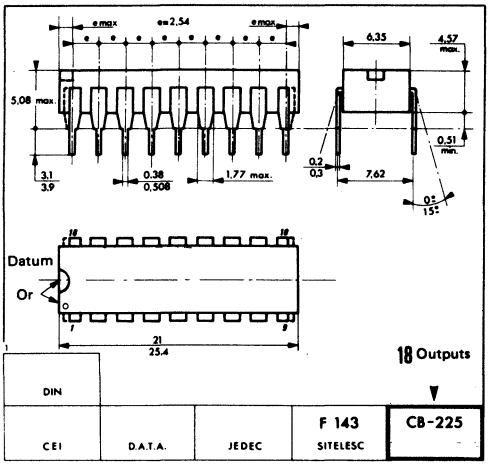
APPLICATION WITH LED DISPLAY



CASE CB-225



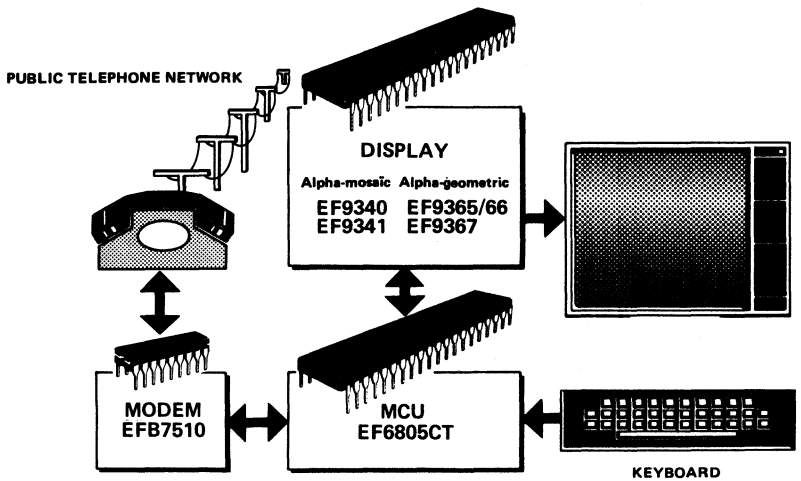
DP SUFFIX
PLASTIC PACKAGE



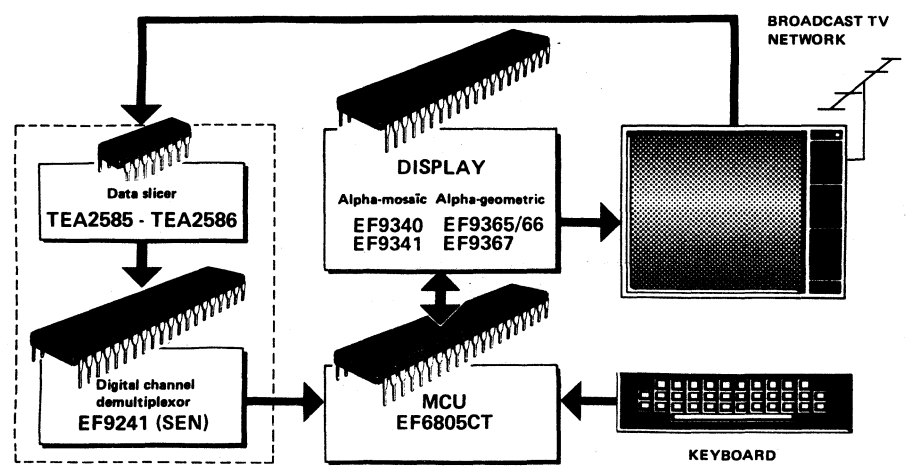
This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

3

TELEMATICS



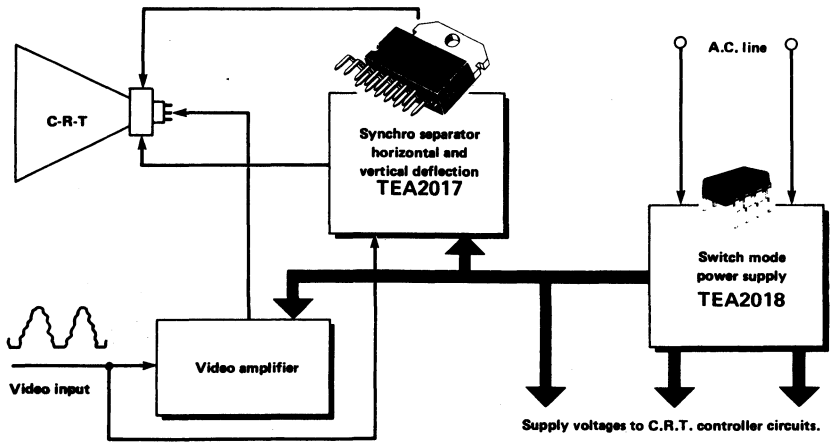
VIDEOTEX



TELETEXT

Function	Features	Part number	Package	Page
DATA SLICER	• Extraction of digital data broadcasted on a TV channel. • Generation of the clock in phase with the data, generation of a validation signal for the framing code recognition.	TEA2585 + TEA2586	DIL16 (CB-79) DIL16 (CB-79)	371 379
DIGITAL CHANNEL DEMULT.	Associated with a FIFO RAM, this circuit receives the data from the data slicer and performs digital channel demultiplexing.	EF9241	DIL40 (CB-182)	259
CRT CONTROL	CRT controller Character generator These two circuits, associated with a 1K x 16 RAM constitute a complete alpha-mosaïc display unit. Easy extension up to 2 additional sets of 96 characters each which can be dynamically down-loaded (Dynamically Redefinable Character Set : DRCS).	EF9340 EF9341	DIL40 (CB-182) DIL40 (CB-182)	261 261
	Graphic display processor. 50 Hz/625 lines. Interlaced up to 512x512.	EF9365	DIL40 (CB-182)	289
	Graphic display processor. 50 Hz/625 lines. Non interlaced 256 x512.	EF9366	DIL40 (CB-182)	289
	Graphic display processor. 50 Hz/625 lines or 60 Hz/525 lines. Interlaced or non interlaced up to 512 x 1024.	EF9367	DIL40 (CB-182)	317
INTELLIGENT TERMINAL CONTROLLER	6805 family 8-bit microcomputer. This circuit is an intelligent controller for interconnected systems and is especially designed to optimize all applications of terminals linked to a telephone line. • Internal asynchronous universal receiver/transmitter with two independent baud rate generators. • Up to 4 K bytes of internal user ROM and 16 K byte external addresing space. • 240 bytes of RAM (64 bytes of maintainable RAM) • Internal 8-bit programmable timer with 7-bit reloadable prescaler. • 8 operating modes (6 expanded addressing modes). • Up to 29 bidirectional I/O lines and 2 control lines. • 4 internal vectored interrupts. • Internal digital clock generator.	EF6805 CT	DIL40 (CB-182)	217
MODEM	Asynchronous FSK MODEM - 75/1200 bauds. CCITT - V23 and BELL-202 compatible.	EFB7510	DIL18(CB-225)	349
COMPLETE DEFLECTION	Complete horizontal and vertical deflection circuit. Direct drive of frame yoke (maximum output current : ± 1.5 A), direct drive of line Darlington, muting output.	TEA2017	SIL15 (CB-501)	361
SWITCH MODE POWER SUPPLY	Power supply control circuit for fixed frequency fly-back power supplies up to 80 W. Direct drive of the switching transistor. Output current $I_B = KI_C$. Total protection from overload, short-circuit and temperature. Low rest current. Additional sync. capability with internal PLL.	TEA2018 TEA2019	DIL8 (CB-98) DIL14 (CB-2)	577 581

3



COLOR AND BLACK AND WHITE DISPLAYS

Function	Features	Part number	Package	Page
COMPLETE DEFLECTION	Complete horizontal and vertical deflection circuit. Direct drive of frame yoke (maximum output current : ± 1.5 A), direct drive of line Darlington, muting output.	TEA2017	SIL15 (CB-501)	361
SWITCH MODE POWER SUPPLY	Power supply control circuit for fixed frequency fly-back power supplies up to 80 W. Direct drive of the switching transistor. Output current $I_B = KI_C$. Total protection from overload, short-circuit and temperature. Low rest current.	TEA2018	DIL8 (CB-98)	577
	Additional sync. capability with internal PLL.	TEA2019	DIL14 (CB-2)	581

THOMSON SEMICONDUCTORS

EF6805 CT

HMOS

8-BIT MICROCOMPUTER

8-BIT MICROCOMPUTER

The EF6805CT MCU is a member of the EF6805 family which is pin to pin 6801 compatible.
This MCU can function as a monolithic microcomputer or can be expanded up to a 16 K bytes addressing space, according to 8 enhanced operating modes. On chip ressources include a Universal Asynchronous Communication Controller (UACC), a flexible programmable timer, 240 bytes of RAM and up to 4 K bytes of user ROM.

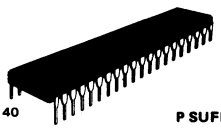
HARDWARE FEATURES : improved 6801 features.

- 8 bit architecture
- 240 bytes of RAM with 80 retainable bytes (V_{CC} standby)
- Memory mapped I/O
- 4096 bytes of user ROM
- Internal Universal Asynchronous full duplex receiver transmitter, with two independent baud rate generators, Communication Controller (UACC)
- Internal 8 bit programmable timer with 8 bit reloadable prescaler
- Four internal vectored interrupts (timer, transmitter, receiver, software interrupt)
- Three external vectored interrupts ($\overline{NMI}$, $\overline{IRQ}$, SC1)
- Master RESET
- 29 bidirectional I/O lines and 2 control lines
- 8 enhanced programmable operating modes
- Internal crystal clock generator
- 5 V single supply.

SOFTWARE FEATURES of the 6805 family :

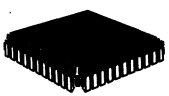
- Similar to EF6800
- Byte efficient instruction set
- Easy to program
- True bit manipulation
- Bit test and branch instructions
- Versatile interrupt handling
- Powerful indexed addressing for tables
- Full set of conditional branches
- Memory usable as register/flags
- Single instruction memory examine/change
- 10 powerful addressing modes

CASE CB-182



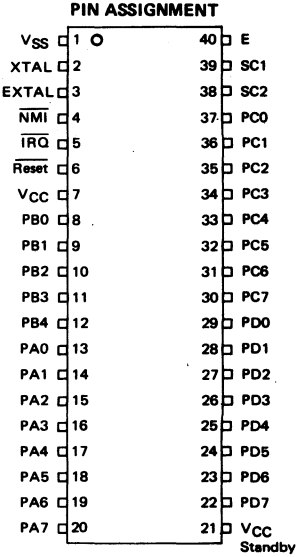
P SUFFIX
PLASTIC PACKAGE

CASE CB-508



FN SUFFIX
SURPICOP
(PLASTIC CHIP-CARRIER)

PIN ASSIGNMENT



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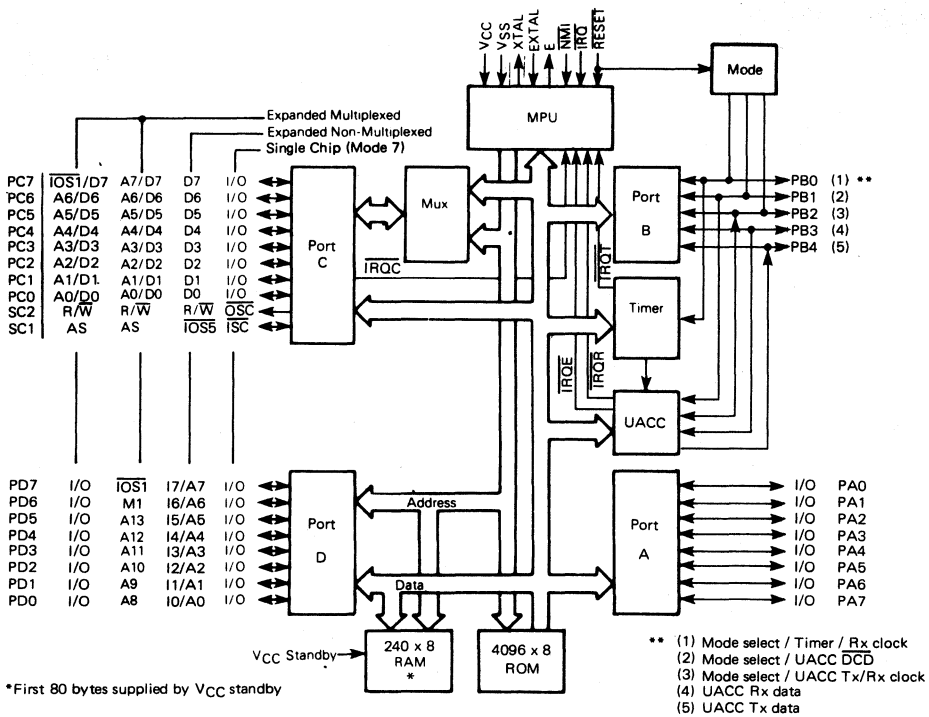
THOMSON COMPONENTS

FIGURE 1 – EF6805CT MICROCOMPUTER FAMILY BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
Thermal Resistance			
Plastic	θ_{JA}	50	°C/W
Ceramic		50	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Input protection is enhanced by connecting unused inputs to either V_{DD} or V_{SS}.

CONTROL TIMING (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of Operation	f_o	0.5	–	1.25	MHz
Crystal Frequency	f_{XTAL}	2	4.9152	5	MHz
External Oscillator Frequency	$4f_o$	2	–	5	MHz
Crystal Oscillator Start Up Time	t_{rc}	–	–	100	ms
Processor Control Setup Time	t_{PCS}	–	200	–	ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5% V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	$\overline{RESET}$	V_{IH}	V_{SS} + 4	–	V_{CC}	V
	Other inputs (Note 1)		V_{SS} + 2.0	–	V_{CC}	
Input Low Voltage	All inputs (Notes 1 & 2)	V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	V
Input load current (V_{in} = V_{IL})	Port D	I_{in}	–	–	0.5	mA
	SC1		–	–	0.8	
Input Current (V_{in} = 0 to 5.25 V)	$\overline{RESET}$	I_{in}	–	–	2.5	μA
	$\overline{NMI}$, $\overline{IRQ}$		–	12	25	
Three-State (Off State) Input Current (V_{in} = 0.5 to 2.4 V)	PA0-PA7, PC0-PC7	I_{TSI}	–	2.0	10	μA
	PB0, PB4		–	10.0	100	
Output High Voltage (I_{load} = – 100 μA, V_{CC} = min)	PC0-PC7	V_{OH}	V_{SS} + 2.4	–	–	V
(I_{load} = – 65 μA, V_{CC} = min)	PD0-PD7, SC1, SC2		V_{SS} + 2.4	–	–	
(I_{load} = – 100 μA, V_{CC} = min)	E, Other Outputs		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{load} = 2.0 mA, V_{CC} = min)	All Outputs	V_{OL}	–	–	V_{SS} + 0.5	V
Darlington Drive Current (V_O = 1.5 V)	PA0-PA7	I_{OH}	1.0	2.5	10.0	mA
Internal Power Dissipation (Measured at T_A = 0°C in Steady-State Operation)		P_{INT}	–	700	1200	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f_o = 1.0 MHz)	All Inputs	C_{in}	–	–	10.0	pF
V_{CC} Standby	Powerdown	V_{SBB}	4.0	–	5.25	V
	Powerup	V_{SB}	4.75	–	5.25	
Standby Current	Powerdown	I_{SBB}	–	–	6	mA

Notes :
1 - Except Mode Programming Levels ; See Figure 18.
2 - Except XTAL, EXTAL.

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts – Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts – User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

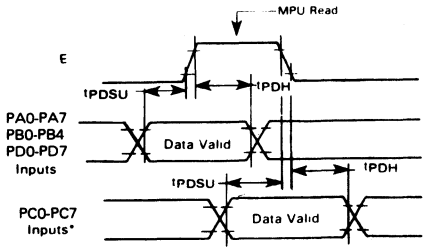
$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

PERIPHERAL PORT TIMING (Refer to Figures 2, 5)

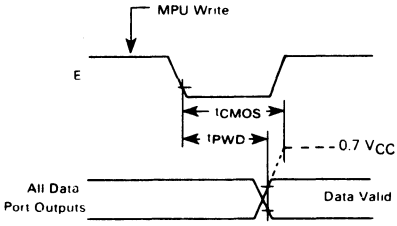
Characteristics	Symbol	Min	Typ	Max	Unit
Peripheral Data Setup Time	t_{PDSU}	200	–	–	ns
Peripheral Data Hold Time	t_{PDH}	200	–	–	ns
Delay Time, Enable Positive Transition to $\overline{OSC}$ Negative Transition	t_{OSD1}	–	–	350	ns
Delay Time, Enable Positive Transition to $\overline{OSC}$ Positive Transition	t_{OSD2}	–	–	350	ns
Delay Time, Enable Negative Transition to Peripheral Data Valid Port A, B, C, D	t_{PWD}	–	–	350	ns
Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid	t_{CMOS}	–	–	2.0	µs
Input Strobe Pulse Width	t_{PWIS}	200	–	–	ns
Input Data Hold Time	t_{IH}	80	–	–	ns
Input Data Setup Time	t_{IS}	20	–	–	ns
Delay time, ISC active edge to OSC rising edge (handshake mode)	t_{IOH}	300	–	–	ns

FIGURE 2 – DATA SETUP AND HOLD TIMES (MPU READ)



*Port C Non-Latched Operation (LATCH ENABLE = 0)

FIGURE 3 – DATA SETUP AND HOLD TIMES (MPU WRITE)



NOTES
1 10 k Pullup resistor required for Port B to reach 0.7 V_{CC}
2 Not applicable to PB1
3 Port D cannot be pulled above V_{CC}

FIGURE 4 – PORT C OUTPUT STROBE TIMING (EF6805CT SINGLE-CHIP MODE)

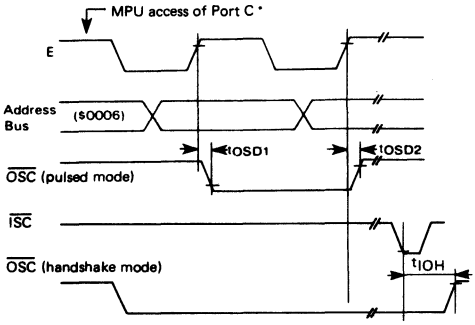
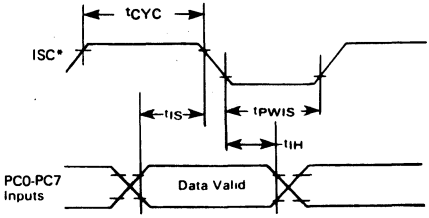


FIGURE 5 – PORT C LATCH TIMING (EF6805CT SINGLE-CHIP MODE)



* active on negative edge if CR2 (bit 2 of Port C control/status register) is reset.

NOTE : Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted.

BUS TIMING (See figures 6 and 7)

Characteristic	Symbol	Min	Typ	Max	Unit
Cycle time	t_{CYC}	0.8	–	2	µs
Address strobe pulse width high*	t_{PWASH}	150	–	–	ns
Address strobe rise time	t_{ASR}	5	–	30	ns
Address strobe fall time	t_{ASF}	5	–	30	ns
Address strobe delay time*	t_{ASD}	70**	–	–	ns
Enable rise time	t_{ER}	5	–	30	ns
Enable fall time	t_{EF}	5	–	30	ns
Enable pulse width high time*	t_{PWEH}	340	–	–	ns
Enable pulse width low time*	t_{PWEL}	350	–	–	ns
Address strobe to enable delay time	t_{ASED}	30	–	–	ns
Data delay write time	t_{DDW}	–	–	225	ns
Data set up time	t_{DSR}	70	–	–	ns
Data hold time Read Write	t_{DHR} t_{DHW}	10 20	– –	– –	ns
Muxed-address set up time for latch	t_{ASL}	20	–	–	ns
Non muxed address set up time for latch	t_{ASH}	20	–	–	ns
Muxed-address hold time for latch	t_{AHL}	20	–	–	ns
Address hold time	t_{AH}	20	–	–	ns
Address R/$\overline{W}$ set up time before E	t_{AS}	140	–	–	ns
A0-A7 set up time before E	t_{ASM}	130	–	–	ns
Peripheral access time	t_{ACC}	–	–	400	ns
Oscillator stabilization time	t_{RC}	100	–	–	ms

* At specified cycle time.

** t_{ASD} parameters listed assume external TTL clock drive with 50 % ± 5 % duty cycle. Devices driven by an external TTL clock with 50 % ±1 % duty cycle or which use a crystal have the following t_{ASD} specifications : 80 ns min. (1.25 MHz).

FIGURE 6 – BUS CHARACTERISTICS IN EXPANDED NON MULTIPLEXED MODES

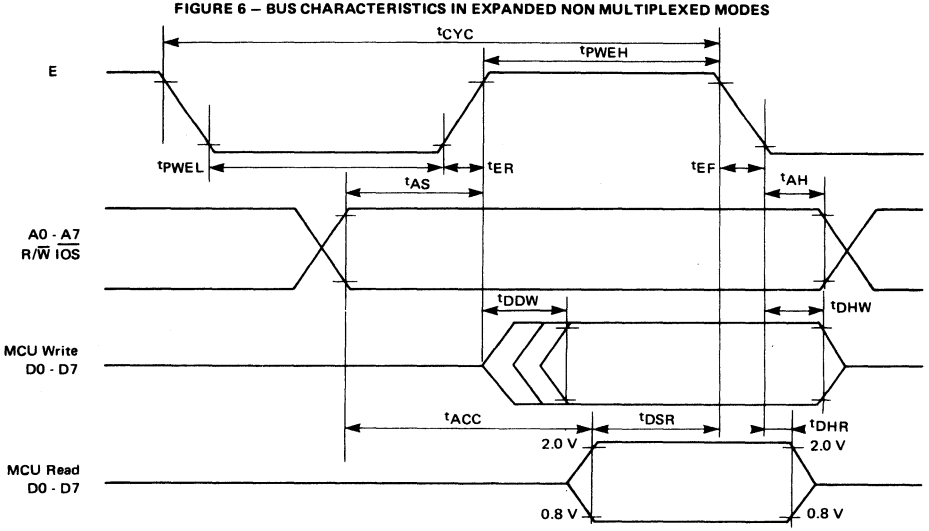
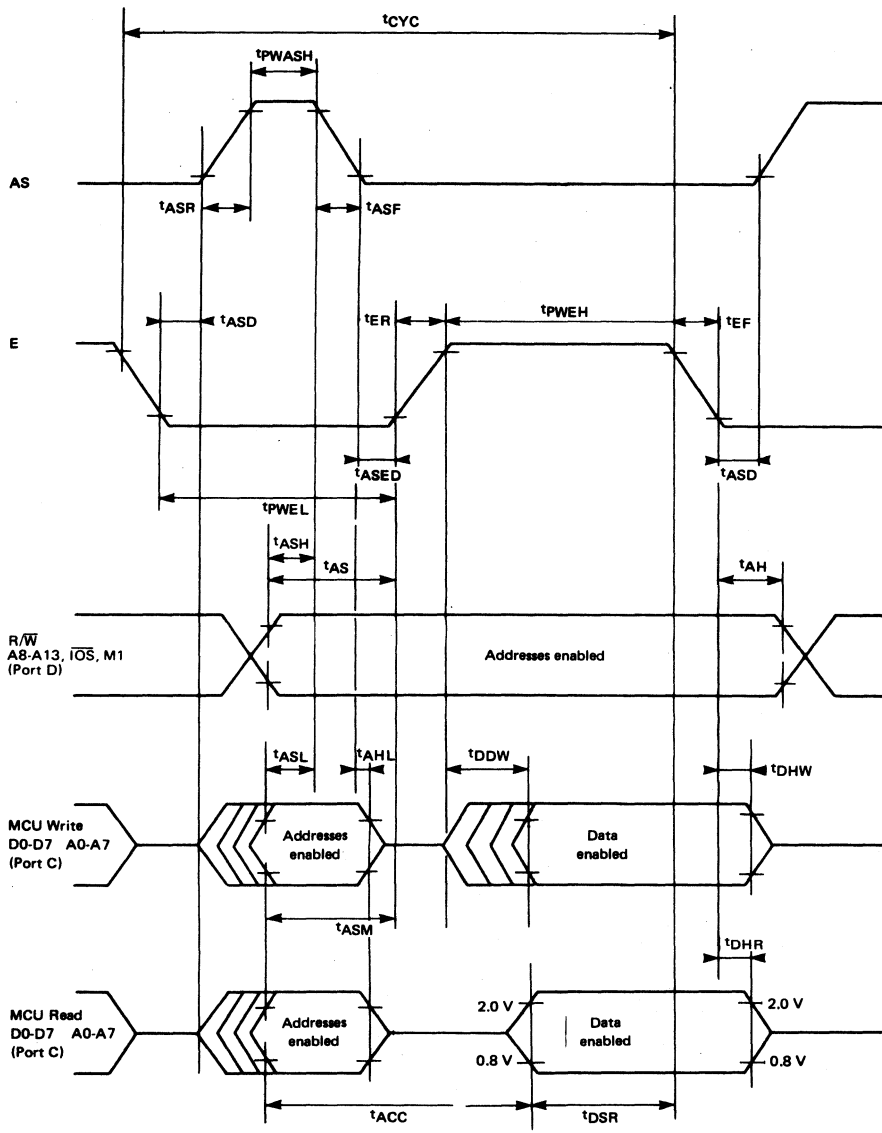


FIGURE 7 – BUS CHARACTERISTICS IN EXPANDED MULTIPLEXED MODES



NOTES :
- Voltage levels shown are $V_L \leqslant 0.5$ V, $V_H \geqslant 2.4$ V unless otherwise specified.
- *Measurement points* shown are 0.8 V and 2.0 V unless otherwise specified.
- Memory devices should be enabled only during E high to avoid Port C bus contention.

U A C C TIMING (See figures 8, 9, 10 and 11)

Characteristic	Symbol	Min	Typ	Max	Unit
MAIN EXTERNAL CLOCK					
Low level pulse width	t_{PWCL}	500	–	–	ns
High level pulse width	t_{PWCH}	500	–	–	ns
Rise time	t_{CR}	–	–	100	ns
Fall time	t_{CF}	–	–	100	ns
Frequency	CF*	–	–	307.2	KHz
RECEIVER DATA INPUT - SIGNAL DETECTION					
Rise time	t_{RRD}	–	–	100	ns
Fall time	t_{RFD}	–	–	100	ns
TRANSMITTER/RECEIVER CLOCK OUTPUT					
Frequency	ERCF*	–	–	307.2	KHz
Rise time	t_{ERR}	–	–	100	ns
Cycle ratio	ERCR	40	–	60	%
Fall time	t_{ERF}	–	–	100	ns
TRANSMITTER DATA OUTPUT					
Rise time	t_{ERD}	–	–	100	ns
Fall time	t_{EFD}	–	–	100	ns

* With a crystal frequency of 4.9152 MHz.

FIGURE 8 – MAIN EXTERNAL CLOCK

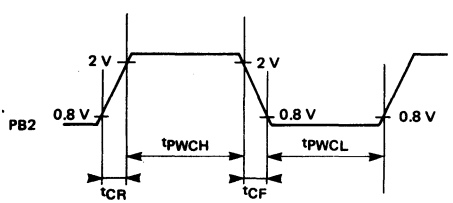


FIGURE 9 – RECEIVER DATA INPUT - SIGNAL DETECTION

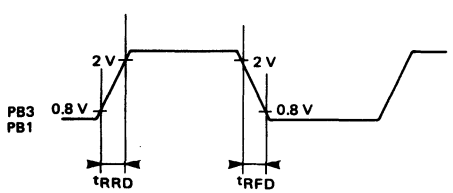


FIGURE 10 – TRANSMITTER/RECEIVER CLOCK OUTPUT

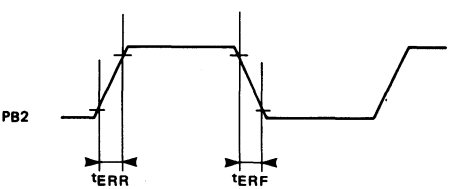


FIGURE 11 – TRANSMITTER DATA OUTPUT

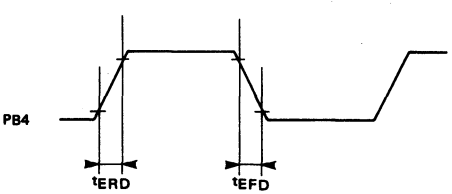


FIGURE 12 – CMOS LOAD

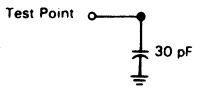
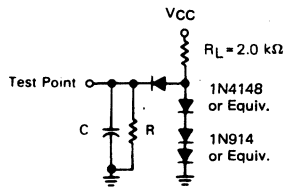


FIGURE 13 – TIMING TEST LOAD PORTS A, B, C, D



C = 90 pF for PC0-PC7, PD0-PD7, E, SC1, SC2
= 30 pF for PA0-PA7, PB0-PB4
R = 37 kΩ for PD0-PD7, E, SC1, SC2
= 24 kΩ for PA0-PA7, PB0-PB4, PC0-PC7

INTRODUCTION

The EF6805CT is an 8-bit monolithic microcomputer which can be configured to function in a wide variety of applications. The facility which provides this extraordinary flexibility is its ability to be hardware programmed into eight different operating modes. The operating mode controls the configuration of 18 of the 40 MCU pins, available on-chip resources, memory map, location (internal or external) of interrupt vectors, and type of external bus. The configuration of the remaining 22 pins is not dependent on the operating mode.

Twenty-nine pins are organized as three 8-bit ports and one 5-bit port. Each port consists of at least a Data Register and a write-only Data Direction Register. The Data Direction Register is used to define whether corresponding bits in the Data Register are configured as input (clear) or output (set).

The term "port", by itself, refers to all of the hardware associated with the port. When the port is used as a "data port" or "I/O port", it is controlled by the port Data Direction Register and the programmer has direct access to the port pins using the port Data Register. Port pins are labled as Pij where i identifies one of four ports and j indicates the particular bit.

EF6805CT is pin to pin compatible with 6801 family. The microprocessor unit (MPU) is software compatible with the EF6805 family. Furthermore, the EF6805CT has eight enhanced operating modes.

OPERATING MODES

EF6805CT provides 8 different operating modes (modes 0 to 7) which are hardware selectable. Two of these modes (0 and 4) are reserved to the manufacturer for testing. Except mode 1, all these modes are similar to the corresponding 6801 programming modes.

The six user selectable modes can be grouped in 3 fundamental modes which refer to the supported bus type.

SINGLE CHIP MODE (mode 7)

The four MCU ports are configured as parallel input/output ports as shown figure 14.

LIMITED NON MUX EXPANDED MODE (mode 5) (see figure 15)

A 232 address space is provided through port D as port C acts as a bidirectional data bus. Two control signals $\overline{IOS}$ and R/$\overline{W}$ are provided through SC1 and SC2 output pins.

This mode is an improved mode 5 of the 6801, fully compatible with the 6800 peripheral parts.

Port D is configured at RESET as an input data port. The port D data direction register can then be changed to provide any combination of the 8 least significant address bits (A0 to A7). The 6 most significant address bits (A8 to A13) are internally decoded and the $\overline{IOS5}$ output signals that an external address ($0018 to $007F or *$0180 to $01FF) is* issued.

MUX EXPANDED MODES (modes 1,2,3 and 6) (see figure 17)

Port C provides a least significant byte address/data multiplexed bus. Two control signals AS (Address Strobe) and R/$\overline{W}$ provided through SC1 and SC2 output pins. The addresses must be latched on the negative edge of AS strobe.

A plain 8 bit latch allows a complete demultiplexing when it is required.

In mode 1, the most significant bit of port C provides an $\overline{IOS1}$ signal : a low level at this pin on address time signals that an address belonging to the external address space ($0018 to $007F) is issued. Port D retains its general purpose I/O function. Mode 1 allows access up to 104 external addresses.

In modes 2 and 3, Port D provides the 6 most significant address bits. PD6 and PD7 provide respectively a M1 (opcode fetch) and a $\overline{IOS1}$ signal.

In mode 2 the internal RAM is enabled and the internal ROM is disabled. In mode 3, both internal ROM and RAM are disabled. Any disabled internal address space may be externally used.

In mode 6, port D is initially configured during RESET as an input data port. The port D data direction register can then be changed to provide any combination of the 6 most significant address lines (A8 to A13). Stated alternatively, any subset of A8 to A13 can be provided while retaining the remaining port D lines as data input. Table 1 gives an abstract of the operating mode characteristics.

FIGURE 14 – SINGLE-CHIP MODE (Mode 7)

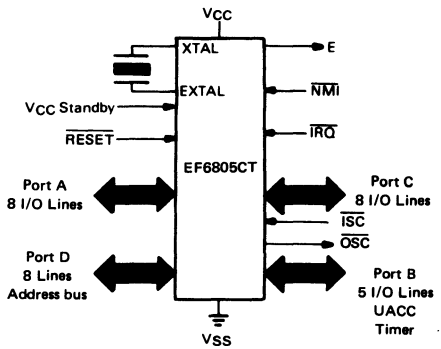
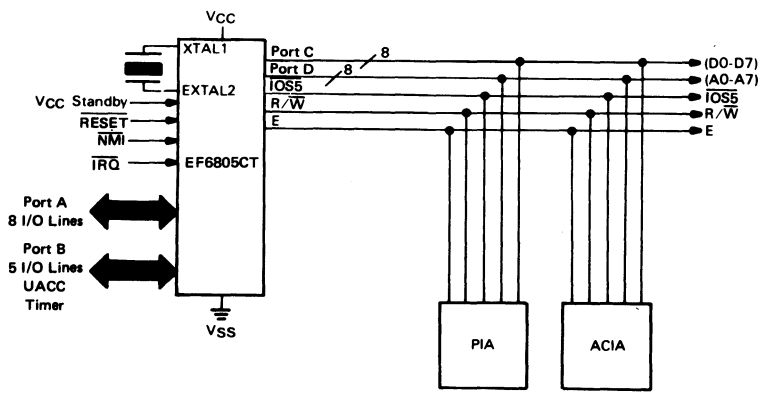


FIGURE 15 – EXPANDED NON-MULTIPLEXED CONFIGURATION (Mode 5)



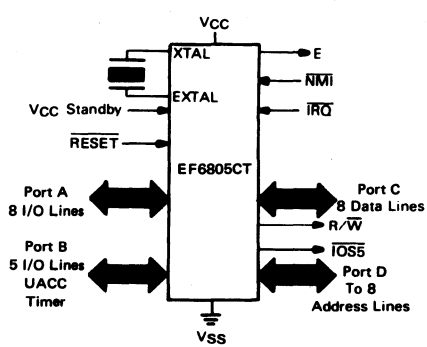


FIGURE 16 – TYPICAL LATCH ARRANGEMENT

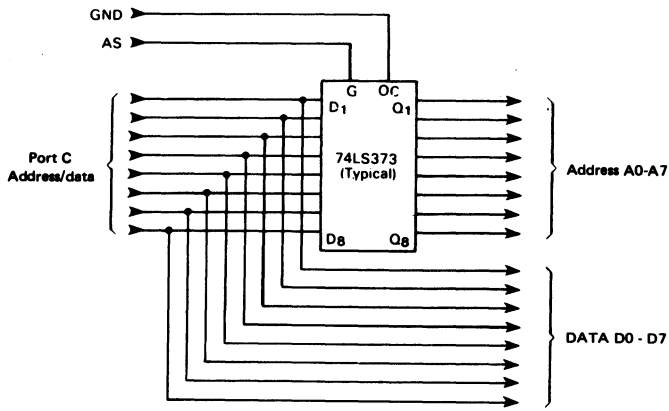
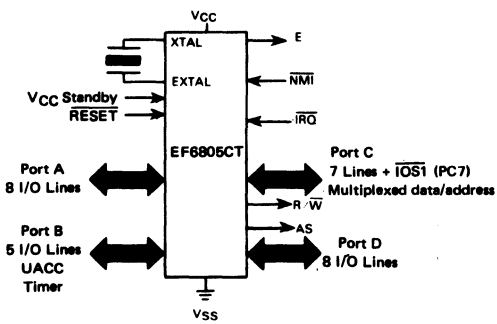


FIGURE 17 – EXPANDED MULTIPLEXED CONFIGURATION



MODE 1 : LIMITED MUX EXPANDED MODE

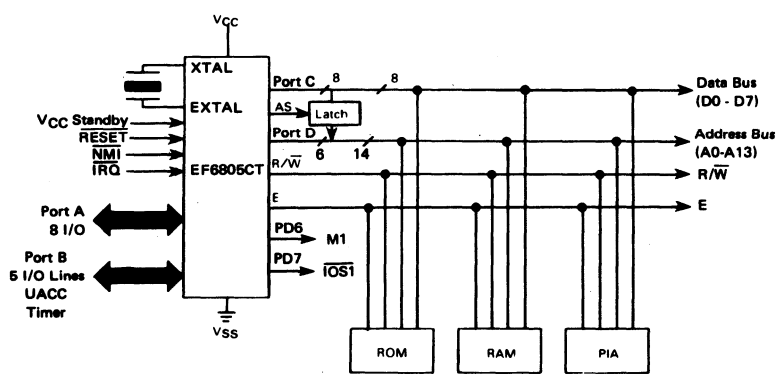


TABLE 1 – OPERATING MODE CHARACTERISTICS

Mode	Description	Port C	Port D	SC1 pin	SC2 pin	RAM	ROM (1)	External space
0	Reserved	–	–	–	–	–	–	–
1	Limited MUX expanded mode	Multiplexed Data/ LSB addresses (A0 to A6) and $\overline{IOS1}$	I/O	AS	R/$\overline{W}$	Enabled (from $0090 to $017F)	Enabled (from $3000 to $3FFF)	From $0018 to $007F ($\overline{IOS1}$ = 0 when external space is pointed)
2	Full MUX expanded mode (with external ROM)	Multiplexed Data/ LSB addresses	PD0-PD5 = A8-A13 PD6 = M1 PD7 = $\overline{IOS1}$ (3)	AS	R/$\overline{W}$	Enabled (from $0090 to $017F)	Disabled (2)	From $0018 to $007F and from $0180 to $3FFF (port C & D register addresses user selectable).
3	Full MUX expanded mode (with external ROM and RAM)	Multiplexed Data/ LSB addresses	PD0-PD5 = A8-A13 PD6 = M1 PD7 = $\overline{IOS1}$ (3)	AS	R/$\overline{W}$	Disabled (2)	Disabled (2)	From $0018 to $007F, from $0090 to $017F and, from $0180 to $3FFF (port C & D register addresses user selectable).
4	Reserved	–	–	–	–	–	–	–
5	Limited non MUX expanded mode (232 addresses)	Data (Bidirectional)	LSB addresses or inputs	$\overline{IOS5}$ (5) (external space selectable)	R/$\overline{W}$	Enabled (from $0090 to $017F)	Enabled (from $3000 to $3FFF)	From $0018 to $007F and from $0180 to $01FF ($\overline{IOS5}$ = 0 when external space is pointed).
6	Full MUX expanded mode	Multiplexed data/ LSB addresses	PD0-PD5 = A8-A13 or inputs PD6= input or M1 PD7= input or $\overline{IOS1}$ (4)	AS	R/$\overline{W}$	Enabled (from $0090 to $017F)	Enabled (from $3000 to $3FFF)	From $0018 to $007F and from $0180 to $2F7F (port C register addresses user selectable).
7	Monochip	I/O	I/O	ISC (port C input strobe)	$\overline{OSC}$ (port C output strobe)	Enabled (from $0090 to $017F	Enabled (from $3000 to $3FFF)	–

(1) Available in 4 Kbytes version.
(2) Corresponding memory space becomes external space.
(3) $\overline{IOS1}$ = output decoding the addressing space : $0018 to $007F (active low).
(4) $\overline{IOS1}$ is available on PD7 in mode 6 when this pin has been programmed as an output.
(5) $\overline{IOS5}$ = output decoding two external addressing spaces : $0018 to $007F and $0180 to $01FF.

PROGRAMMING THE MODE

The operating mode is programmed on port B (PB0, PB1 and PB2 pins) at the end of the reset procedure and on the positive edge of the RESET signal.
MCU reads the code of the operating mode on bits 5, 6 and 7 of the port B data register (located at the address $0003).
Port A, port B, UACC and timer are not modified by the operating mode.

Port B Data register

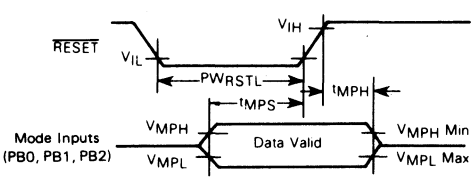
7	6	5	4	3	2	1	0	
MS2	MS1	MS0	DR4	DR3	DR2	DR1	DR0	$0003

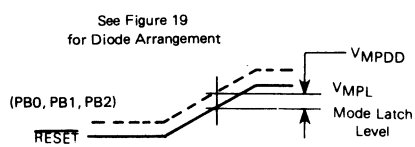
TABLE 2 – MODE SELECTION

MODE	PB2 MS2	PB1 MS1	PB0 MS0	BUS MODE	OPERATING MODE
7	H	H	H	I	Single chip mode
6	H	H	L	MUX	Full MUX expanded mode (int. ROM and RAM)
5	H	L	H	Non MUX	Limited non MUX expanded mode
4	H	L	L	–	Reserved
3	L	H	H	MUX	Full MUX expanded mode (ext. ROM and RAM)
2	L	H	L	MUX	Full MUX expanded mode (ext. ROM)
1	L	L	H	MUX	Limited MUX expanded mode
0	L	L	L	–	Reserved.

Legend : L : Logic "0" - H : Logic "1" - MUX : Multiplexed - I : Internal.

FIGURE 18 – MODE PROGRAMMING TIMING

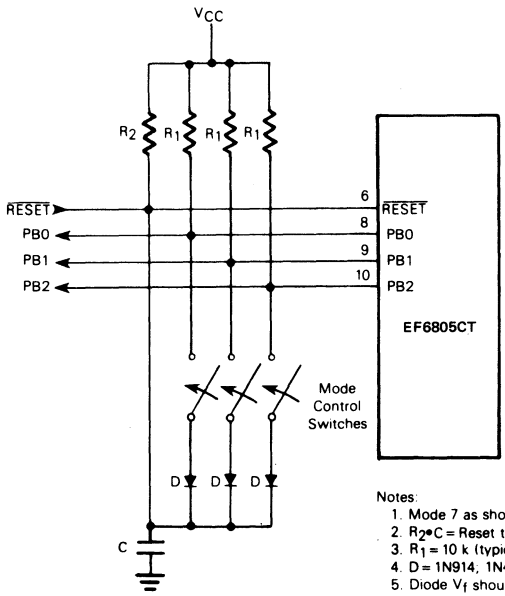




MODE PROGRAMMING (Refer to Figure 18)

Characteristic	Symbol	Min	Max	Unit
Mode Programming Input Voltage Low	V_{MPL}	–	1.8	V
Mode Programming Input Voltage High	V_{MPH}	4.0	–	V
Mode Programming Diode Differential (If Diodes are Used)	V_{MPDD}	0.6	–	V
$\overline{RESET}$ Low Pulse Width	PW_{RSTL}	3.0	–	E-Cycles
Mode Programming Setup Time	t_{MPS}	2.0	–	E-Cycles
Mode Programming Hold Time	t_{MPH}			ns
$\overline{RESET}$ Rise Time $\geqslant$ 1 µs		0	–	–
$\overline{RESET}$ Rise Time $<$ 1 µs		100	–	–

FIGURE 19 – TYPICAL MODE PROGRAMMING CIRCUIT



Notes:
1. Mode 7 as shown
2. $R_2 \bullet C$ = Reset time constant
3. R_1 = 10 k (typical)
4. D = 1N914; 1N4001 (typical)
5. Diode V_f should not exceed V_{MPDD} min.

FUNCTIONAL PIN DESCRIPTION

V_{CC} AND V_{SS}

V_{CC} and V_{SS} provide power to a large portion of the MCU. The power supply should provide + 5 volts (± 5 %) to V_{CC}, and V_{SS} should be tied to ground. Total power dissipation (including V_{CC} Standby), will not exceed P_D.

V_{CC} STANDBY

V_{CC} Standby provides power to the standby portion ($90 through $CF) of the RAM (See resident memory section).

XTAL AND EXTAL

These two pins interface either a crystal or TTL compatible clock to the MCU internal clock generator. Divide-by-four circuitry is included which allows use of inexpensive crystals. A 20 pF capacitor should be tied from each crystal pin to ground to ensure reliable startup and operation. Alternatively, XTAL may be driven by an external TTL compatible clock at $4f_o$ with a duty cycle of 50 % (± 5 %) with EXTAL connected to ground.

The internal oscillator is designed to interface with an AT-cut quartz crystal resonator operated in parallel resonance mode in the frequency range specified for f_{XTAL}. The crystal should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time. The MCU is compatible with most commercially available crystals. Nominal crystal parameters are shown in Figure 23.

$\overline{RESET}$

This input is used to reset the internal state of the device and provide an orderly startup procedure. During powerup, $\overline{RESET}$ must be held below 0.8 volts: (1) at least t_{RC} after V_{CC} reaches 4.75 volts in order to provide sufficient time for the clock generator to stabilize, and (2) until V_{CC} Standby reaches 4.75 volts. $\overline{RESET}$ must be held low at least three E-cycles if asserted during powerup operation.

E (ENABLE)

This is an output clock used primarily for bus synchronization. It is TTL compatible and is the slightly skewed divide-by-four result of the device input clock frequency. It will drive one Schottky TTL load and 90 pF, and all data given in cycles is referenced to this clock unless otherwise noted.

$\overline{NMI}$ (NON-MASKABLE INTERRUPT)

An $\overline{NMI}$ negative edge requests an MCU interrupt sequence. $\overline{NMI}$ typically requires a 3.3 kΩ (nominal) resistor to V_{CC}. $\overline{NMI}$ has an internal pull-up resistor. $\overline{NMI}$ must be held low for at least 1.5 E-cycle to be recognized under all conditions.

$\overline{IRQ}$ (MASKABLE INTERRUPT REQUEST)

$\overline{IRQ}$ is a negative edge sensitive input which can be used to request an interrupt sequence.

$\overline{IRQ}$ typically requires an external 3.3 kΩ (nominal) resistor to V_{CC}. $\overline{IRQ}$ has an internal pull-up resistor.

$\overline{IRQ}$ must be held low for at least 1.5 E-cycle to be recognized under all conditions.

This input may be software tested (BIH, BIL instructions).

SC1 AND SC2 (STROBE CONTROL 1 AND 2)

The function of SC1 and SC2 depends on the operating mode. SC1 is configured as an output in all modes except single chip mode, whereas SC2 is always an output. SC1 and SC2 can drive one Schottky load and 90 pF.

Single-chip mode (Mode 7)

In Single-Chip Mode, SC1 and SC2 are configured as an input and output, respectively, and both function as Port C control lines (See functional port description).

Limited non MUX expanded mode (Mode 5)

In the limited non MUX expanded mode, both SC1 and SC2 are configured as outputs. SC1 functions as input/output select ($\overline{IOS5}$) and is asserted only when an address from $0018 to $007F or from $0180 to $01FF is available on the internal address bus.

SC2 is configured as Read/Write and is used to control the direction of data bus transfers. An MPU read is enabled when Read/Write and E are high.

MUX expanded modes (1,2,3 and 6)

In the MUX expanded modes both SC1 and SC2 are configured as outputs. SC1 functions as Address Strobe and can be used to demultiplex the eight least significant addresses and the data bus. A latch controlled by Address Strobe captures address on the negative edge, as shown in Figure 15.

SC2 is configured as Read/Write and is used to control the direction of data bus transfers. An MPU read is enabled when Read/Write and E are high.

PA0-PA7 (PORT A)

Port A is a mode independent 8-bit I/O port with each line an input or output as defined by the Port A Data Direction Register. The TTL compatible three-state output buffers can drive one Shottky TTL load and 30 pF, Darlington transistors, or CMOS devices using external pull-up resistors. It is configured as a data input port by $\overline{RESET}$. Unused lines can remain unconnected.

PB0-PB4 (PORT B)

Port B is a mode-independent, 5-bit, multipurpose I/O port. The voltage levels present on PB0, PB1, and PB2 on the rising edge of $\overline{RESET}$ determine the operating mode of the MCU.

PB0 can be programmed as :
- the timer input line
- the timer clock enable line
- the timer output line
- the UACC receive clock output line according to the timer control/status register (See timer section). PB1, PB2, PB3 and PB4 can be programmed as UACC lines (see UACC section). When any of the PB0 to PB4 line is not used by respectively the timer unit or the UACC, it can be used as a standard input/output port through Port B data direction and data registers.

The Port B three-state, TTL-compatible output buffers are capable of driving one TTL load and 30 pF or CMOS devices, using external pull up resistors.

PC0-PC7 (PORT C)

Port C can be configured as an I/O port, a bidirectional 8-bit data bus, or a multiplexed address/data bus depending on the operating mode. The TTL compatible three-state output buffers can drive one Schottky TTL load and 90 pF. Unused lines can remain unconnected.

See the Functional Port Description section for Port C mode description.

PD0-PD7 (PORT D)

Port D is configured as an 8-bit standard I/O port, as address outputs or as data inputs depending on the operating mode. Port D can drive one Schottky TTL load and 90 pF and is the only port with internal pullup resistors. Unused lines can remain unconnected.

See the Functional Port Description section for Port D mode description.

RESIDENT MEMORY

The EF6805CT provides 4096 bytes of on-board ROM and RAM 240 bytes of on-chip RAM.
Part of the RAM is powered through the V_{CC} standby pin and is maintainable during V_{CC} powerdown. This standby portion of the RAM consists of 80 bytes located from $0090 through $00DF.
Power must be supplied to V_{CC} standby if the internal RAM is to be used regardless of whether standby power operation is anticipated.
The RAM is controlled by the RAM control register. (See Figure 21 for memory map).

RAM CONTROL REGISTER ($0010)

The RAM Control Register includes two bits which can be used to control RAM accesses and determine the adequacy of the standby power source during powerdown operation.

7	6	5	4	3	2	1	0
STBY PWR	RAME	X	X	X	X	X	X

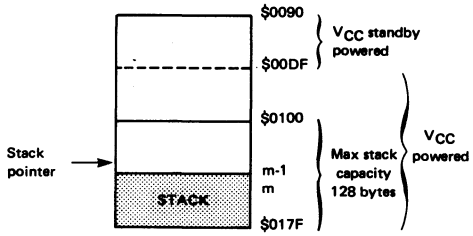
Bit 0-5 Not Used

Bit 6 RAME — RAM Enable. This Read/Write bit can be used to remove the entire RAM from the internal memory map. RAME is set (enabled) during Reset provided standby power is available on the positive edge of RESET. If RAME is clear, any access to a RAM address is external. If RAME is set (on RESET operation) and not in Mode 3, the RAM is included in the internal map.

Bit 7 STBY PWR — Standby Power. This bit is a Read/Write status bit which is cleared whenever V_{CC} Standby decreases below V_{SBB} (min). It can be set only by software and is not affected during reset.

It is intended that RAM be cleared and Standby PWR be set as part of a powerdown procedure which may be entered through $\overline{NMI}$.

FIGURE 20 – INTERNAL RAM MAP



ROM

The EF6805CT family provides an internal user ROM capacity of up to 4096 bytes including interrupt vectors. This ROM is mask programmable and its last address is located is $3FFF.

FIGURE 21 – MEMORY MAP

$0000	I/O and RAM	
$017F		
$0180	External space (in mode 2, 3 and 6 and only from $0180 to $01FF in mode 5)	
$2F7F		
$2F80	Reserved	
$2FFF		
$3000	USER ROM	
$3FEF		
$3FF0-3FF1	XMIT	IRQ VECTOR
$3FF2-3FF3	TIMER	IRQ VECTOR
$3FF4-3FF5	RCV	IRQ VECTOR
$3FF6-3FF7	SWI	VECTOR
$3FF8-3FF9	PORT C	IRQ VECTOR
$3FFA-3FFB	IRQ	VECTOR
$3FFC-3FFD	NMI	VECTOR
$3FFE-3FFF	RESET	VECTOR

Data Direction A	$0000
Data Direction B	$0001
I/O PORT A	$0002
I/O PORT B	$0003
Data Direction C	$0004
Data Direction D	$0005
I/O PORT C	$0006
I/O PORT D	$0007
Timer Counter Register	$0008
Timer Control / Status	$0009
Timer Prescaler Register	$000A
UACC Clock Register	$000B
XMIT Status Register	$000C
RCV Status / Fmat Reg.	$000D
UACC Data Register	$000E
PORT C Status / Control	$000F
RAM Standby Control	$0010
Reserved	$0011 – $0017
External Memory Space (in modes 1,2,3,5,6)	$0018 – $007F
Reserved	$0080 – $008F
Internal RAM	$0090 – $00FF
STACK RAM (see Figure 20)	$0100 – $017F

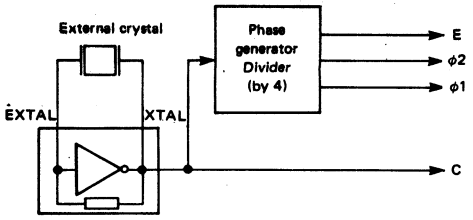
OSCILLATOR AND CLOCK SYSTEM

The EF6805CT family contains one crystal oscillator and one phase generator which controls all the MCU circuitry and supply all the internal synchronization signals.

External crystal (up to 5 MHz) or external signal applied to EXTAL pin can set oscillator on operating mode. When maximum speed is required, external clock signal has to be connected to XTAL pin and EXTAL pin pulled down to V_{SS}.

MCU cycle is provided in dividing by 4 the main frequency. When the UACC works with the internal clock as clock reference, it is necessary to choose a crystal or an external clock signal according to the UACC output frequency (4.9152 MHz for the standard frequencies of table 5 in UACC section).

FIGURE 22 – CLOCK CIRCUITRY



Nota : Peripherals can be synchronized by E signal.

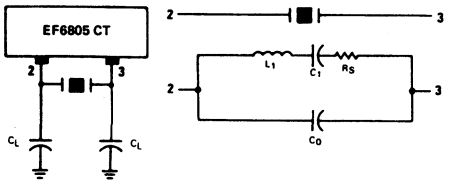
FIGURE 23 – EF6805CT FAMILY OSCILLATOR CHARACTERISTICS

(a) Nominal Recommended Crystal Parameters

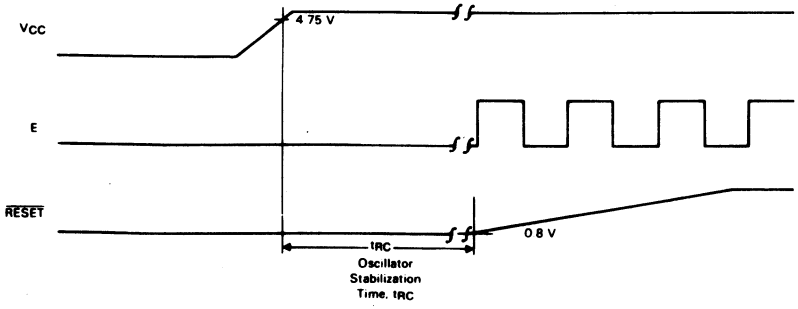
Nominal Crystal Parameters*

	3.58 MHz	4.00 MHz	5.0 MHz
RS	60 Ω	50 Ω	30-50 Ω
C_0	3.5 pF	6.5 pF	4-6 pF
C_1	0.015 pF	0.025 pF	0.01-0.02 pF
Q	>40 K	>30 K	>20 K

*NOTE: These are representative AT-cut crystal parameters only. Crystals of other types of cut may also be used.



(b) Oscillator Stabilization Time (t_{RC})



FUNCTIONAL PORT DESCRIPTION

STANDARD I/O PORT FUNCTION

Two registers, a Data Direction Register (DDR) and a Data Register (DR) are attached to each parallel I/O Port. Each pin can be programmed as an input or as an output by the corresponding bit of the DDR ("0" when programming an input).

All the DDR are reset after $\overline{\text{RESET}}$.

DDR are write only registers, thus they cannot be handled by Read/Modify/Write or bit manipulation instructions. When a pin is programmed as an input its value may be read at the corresponding bit position in the DR (low level forced to 0). When a pin is programmed as an output, modifying the corresponding bit in the Data Reg. modifies the level on this pin.

PORT A

This 8 bit port is always a standard I/O Port.

PORT B

This five bit port has an 8 bit Data Register : DRB5 to DRB7 are loaded with the mode type at the end of RESET. Standard function of this I/O port can be overrun by UACC or Timer unit.

PORT C

The functionality of the 8 bit port C depends on the operating mode ; two extra control I/O lines (SC1 and SC2) are attached to this port.

PORT C IN SINGLE CHIP MODE

In this mode SC1 acts as an input strobe on port C ($\overline{ISC}$) while SC2 acts as an output strobe on port C ($\overline{OSC}$) ; an extra 8 bit control and Status Register allows the port to operate in several different ways :

Bit 2,3,6 and 7 of this register control the $\overline{ISC}$ input function. $\overline{ISC}$ can be used as an interrupt request line ; this interrupt may be used to synchronize data exchange through PC lines, or independently.

Bit 0, 1 and 4 control the SC2 output lines

Port C control and status register

7	6	5	4	3	2	1	0	
ISC Flag	ISC IRQC Enable	X	Master/ slave select	Latch Enable	ISC active edge select	CSR1	CSR0	$000F

– Bit 2 : selects the active edge of SC1 ;
"1" = active on positive edge
"0" = active on negative edge

– Bit 3 : Latch Enable : when this bit is set, the lines which are programmed as inputs in the DDR are latched in the DR on the active edge of SC1. The DR bits programmed as outputs are not modified. When this bit is RESET, DR resumes standard operation.

– Bit 7 : ISC flag : this bit is set on the active edge of SC1 ; it is reset by a port C control / status register read followed by a port C Data register read or write.

– Bit 6 : Interrupt enable : when set, enables ISC flag as an $\overline{IRQC}$ interrupt.

– Bit 0 and 1 :

CSR1	CSR0	CONVERSATIONAL MODE
0	0	Handshake mode
0	1	Pulsed mode
1	0	SC2 stays low
1	1	SC2 stays high

– Bit 4 : Master / Slave select : this bit is interpreted only when bit 1 of CSR is cleared (handshake or pulsed mode). When set, this bit allows SC2 to go low after a MCU write in Port C Data Registers ; when reset, SC2 goes low after a MCU read.
Under pulse mode, SC2 stays low for one ϕ 2 clock cycle.
Under Handshake mode SC2 stays low until an active edge of SC1 input (see figure 5 for timing).

PORT C IN NON MULTIPLEXED EXPANDED MODE

Port C is configured as a bidirectional data bus (D7-D0) in the Expanded Non-Multiplexed Mode. The direction of data transfers is controlled by Read/Write (SC2). Data is clocked by E (Enable).

PORT C IN MULTIPLEXED EXPANDED MODES

Port C is configured as a time multiplexed address (A0-A7) and data bus (D7-D0) in the Expanded Multiplexed Modes ; Address Strobe (AS) is used to demultiplex the two buses. Port C is held in a high impedance state between valid address and data to prevent bus conflicts. Furthermore, in mode 1, PC7 = $\overline{IOS}$.

PORT D

This port is configured as an 8 bit standard I/O port, as address outputs or as data inputs depending on the operating mode.

PORT D IN MUX LIMITED EXPANDED MODE (1) AND SINGLE CHIP MODE (7)

In this mode, port D functions as a standard I/O port with each line configured by the port D Data Direction Register. Internal pull up resistors allow the port to directly interface with CMOS at 5 volt levels. External pull up resistors may be used.

PORT D IN NON MUX LIMITED EXPANDED MODE (5) AND MUX FULL EXPANDED MODE (6)

In these modes, port D is programmed after RESET as an input port. However, internal pull up resistors pull the lines high. The DDR can then be written to provide any combination of output address lines and input data lines. In mode 5, the address lines are taken out of A0 to A7 ; in mode 6 they are taken out of A8 to A13, M1 and $\overline{IOS1}$ signals.

PORT D IN MUX FULL EXPANDED MODES (2 and 3)

After RESET, this port is automatically programmed as outputs ; PD0 to PD5 provide the A8 to A13 address lines, PD6 and PD7 provide respectively the M1 (opcode fetch) and $\overline{IOS1}$ signals.

TIMER

The EF6805CT MCU timer circuitry is shown in figure 24.

The timer features :
- one 8 bit prescaler with automatic reloading
- one 8 bit counter
- one clock control unit
- one 8 bit addressable Read/Write prescaler register ($000A)
- one 8 bit addressable Read/Write counter Data register ($0008)
- one 8 bit addressable Read/Write control/status register ($0009).

The counter may be written by software or read through the counter data register. Read operation does not destroy the content of the counter. The counter is decremented by the clock pulses selected by the clock control unit from the positive edge of the prescaler output or of the PB0 input pin.
Whenever the counter underflows from $00 to $FF, the interrupt request bit (D7 in the control/status register) is set and the decounting starts.

4 bits are used to control the clock source and the PB0 pin :

D0 : Internal/external clock selection
When an external clock is used, its frequency must be inferior to maximum cycle frequency : MCU frequency of operation.
D1 : Clock output enable.
D2 : Prescaler control.
The prescaler output is gated or not by the PB0 input.
D3 : UACC receiver enable
PB0 is used (or not) to output the UACC receiver baud rate generator.

Only 5 configurations out of 16 are allowed on these four bits (see table 3).

2 bits are used to control the timer interrupt :

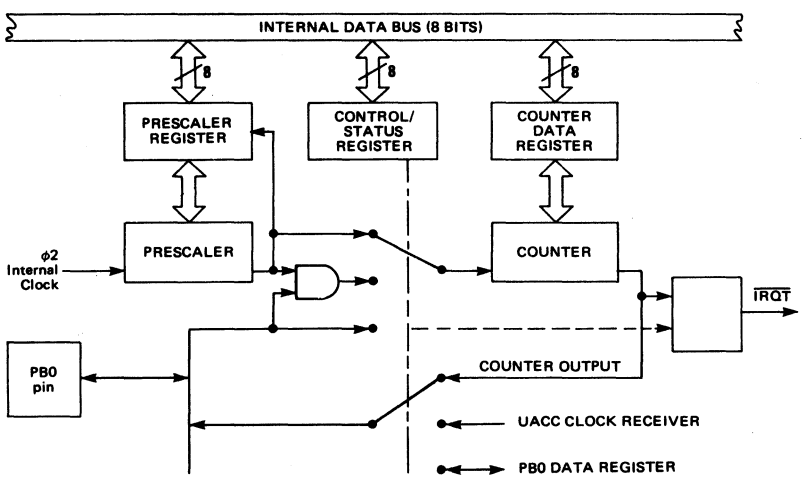
D6 : Mask interrupt
D7 : Interrupt request
D7 is set whenever the counter underflows. An interrupt request is sent to the interrupt unit when D7 = 1 and D6 = 0.
After an interrupt, D7 must be reset by software. A RESET operation resets D7 and sets D6.

TABLE 3 – TIMER PROGRAMMATION (CONTROL/STATUS REGISTER)

D0	D1	D2	D3	Counter clock inputs	PB0 pin	
H	L	L	L	External clock	External clock input	
L	L	L	L	Prescaler output	Standard I/O	PB0 has no dependency with timer
L	L	L	H	Prescaler output	UACC receiver clock	
L	L	H	L	Prescaler output AND gated by PB0	Clock enable input	
L	H	L	L	Prescaler output	MSB counter output	

D0 = D1 = D2 = D3 = 0 after RESET operation.

FIGURE 24 – TIMER SCHEMATIC



UNIVERSAL ASYNCHRONOUS COMMUNICATION CONTROLLER

The chip contains a full duplex, asynchronous serial communication unit. This unit includes a transmitter and a receiver which operate independently, at independent data rates but in the same data format. (See fig. 25 for UACC schematic description). The UACC communicates with the outside through pins PB1, to PB4 and with the MPU through 4 register addresses :

$000E : Receiver data register (read only register) or transmitter data register (write only register)

$000D : Receiver status register (Read only) or format register (write only)

$000C : Transmitter status register (read only)

$000B : Clock control register (write only).

REGISTER DESCRIPTION

CLOCK CONTROL REGISTER (CR) :

Transmitter and receiver clocks are provided by 2 independent baud rate generators. Rates and sources are selected through the clock control register

CR0, CR1, CR2 : Receiver rate selection (see table 5)

CR3, CR4, CR5 : Transmitter rate selection (see table 5)

CR6, CR7 : The common primary clock source of both baud rate generators can be selected as the $\phi 2$ internal clock or as an external clock delivered through the PB2 input pin. (See table 6). In this case the PB2 input frequency must be less than the maximum frequency of operation (f_0 max).

When using the internal source, PB2 pin may output the receiver or the transmitter clock or be used as a standard I/O.

In any case, a clock at 16 times the receiver baud rates may be delivered through the PB0 output pin (see Timer section). In any other respects, timer and UACC operations are independent.

FORMAT REGISTER (FR) :

FR0* : when set, it enables data reception on input pin PB3.

FR1* : Enables data carrier detection (SD) on input pin PB1 when set. (SD = $\overline{FR1} \cdot \overline{PB1}$).

FR2* : Enables data output on output pin PB4 when set.

FR3, FR4, FR5 : Reception and transmission data format (see table 7).

FR6 : Transmitter interrupt enable.

FR7 : Receiver interrupt enable.

*When PB1, PB3 and / or PB4 are not used by the UACC they can work as standard I/O.

RECEIVER STATUS REGISTER AND OPERATION

Receiver Status Register (SR) is a read only register.

SR0 : Receiver data register "Full"
SR2 : No data carrier detection
SR4 : Format error
SR5 : Data overrun
SR6 : Parity error
SR7 : Receiver interrupt request.

See table 4 for set and reset conditions of these status bits.
See figure 26 for the receiver operation flow chart.

TRANSMITTER STATUS REGISTER AND OPERATION

Transmitter status register :

SR1 : Transmitter data register "Empty"
SR3 : Transmitter interrupt request.

See table 4 for status bits set and reset conditions.
See figure 27 for transmitter operation flow chart.

REGISTER VALUES AFTER RESET :

Legend
– Status Register =SR
– Format Register =FR
– Clock Control Register =CR

	S7	S6	S5	S4	S3	S2	S1	S0
SR	0	0	0	0	0	0	1	0
FR	0	0	0	1	0	0	0	0
CR	1	1	0	0	0	1	0	0

SOFTWARE INITIALIZATION

Transmitter initialization (FR2 = 0).
When the MPU resets FR2, it forces the transmitter to its standby state (see figure 27) and sets SR1 to 1. The transmitter interrupt requests are disabled. As soon as the MPU sets FR2, the transmitter begins standard operation.

Receiver initialization (FR0 = 0).
When the MPU resets FR0, it forces the receiver to its standby state (see figure 26). In order to reset the receiver status register it is then necessary to read the status register and next read the receiver data register. SR4 and SR6 are not modified in this process but they cannot yield to any interrupt. Standard correct operations begin as soon as FR0 is set. (by FR1 = 1).
Whenever PB1 input is enabled as data carrier signal detection (SD), the standby state is enterred as soon as, and maintained as long as PB1 remains at high level. A low to high transition on SD activates standard operations.

TABLE 4 – STATUS BIT SET AND RESET CONDITIONS IN STANDARD OPERATION

(See RESET operation and software initialization sections for other operations).

STATUS REGISTER BIT	SET CONDITION	RESET CONDITION
SR0 Receiver data register "Full"	After data have been loaded in the data register from the shift register.	Status register read followed by a receiver data register read.
SR2 No data carrier signal detected	Negative edge of SD signal	Status register read followed by a data register read. Reset of FR1.
SR4, SR6 Format error, parity error	When an error is detected when loading the data register from the shift register.	If no error is detected when loading the data register from the shift register.
SR5 Overrun	When MPU reads data register and when next data word has been lost.	Status register read followed by a data register read.
SR7 Receiver interrupt request	When the following binary condition occurs (SR0+ SR2+ SR5) FR7 . FR0	Data register read operation.
SR1 Transmitter data register "Empty"	When shift register is loaded from data register.	Data register write.
SR3 Transmitter interrupt request	When the following binary condition occurs SR1 . FR6 . FR2.	Data register write operation.

TABLE 5 – MODULATION SPEED (Clock control register)

CR5 CR2	CR4 CR1	CR3 CR0	Speed* (bauds)	Internal $\phi 2$ divided by	External clock divided by
0	0	0	75	16384	2048
0	0	1	150	8192	1024
0	1	0	300	4096	512
0	1	1	600	2048	256
1	0	0	1200	1024	128
1	0	1	2400	512	64
1	1	0	4800	256	32
1	1	1	9600	128	16

*Using a 4.9152 MHz crystal.

TABLE 6 – CLOCK CONTROL

CR7	CR6	Clock	PB2 pin
0	0	Internal	Standard I/O
0	1	Internal	Receiver clock output multiplied by 16
1	0	Internal	Transmitter clock output multiplied by 16
1	1	Tx/Rx external clock	Clock input

Nota : Receiver clock multiplied by 16 can be output on PB0 (see Timer section).

FIGURE 25 – UACC SCHEMATIC DESCRIPTION

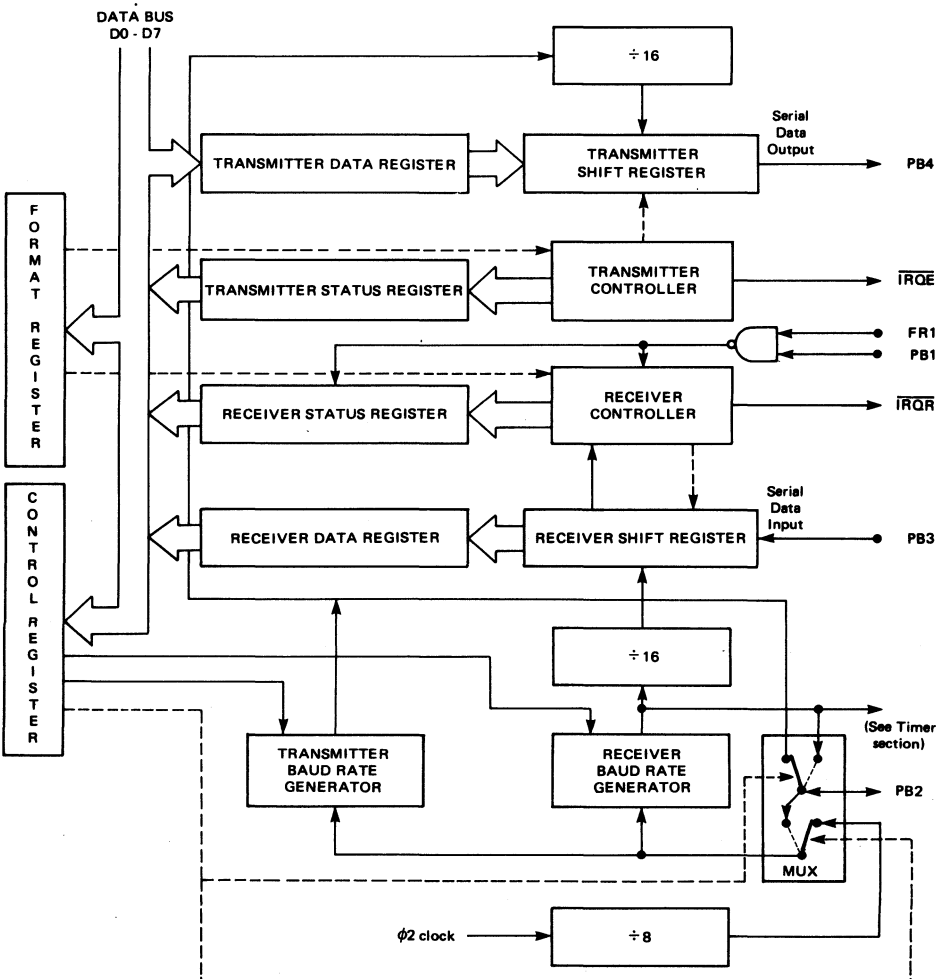


TABLE 7 – COMMON RECEPTION AND TRANSMISSION DATA FORMAT

FR5	FR4	FR3	Word length	Parity	Number of stop bits
0	0	0	7 bits	Even	2
0	0	1	7 bits	Odd	2
0	1	0	7 bits	Even	1
0	1	1	7 bits	Odd	1
1	0	0	8 bits	–	2
1	0	1	8 bits	–	1
1	1	0	8 bits	Even	1
1	1	1	8 bits	Odd	1

FIGURE 26 – RECEIVER OPERATION FLOWCHART

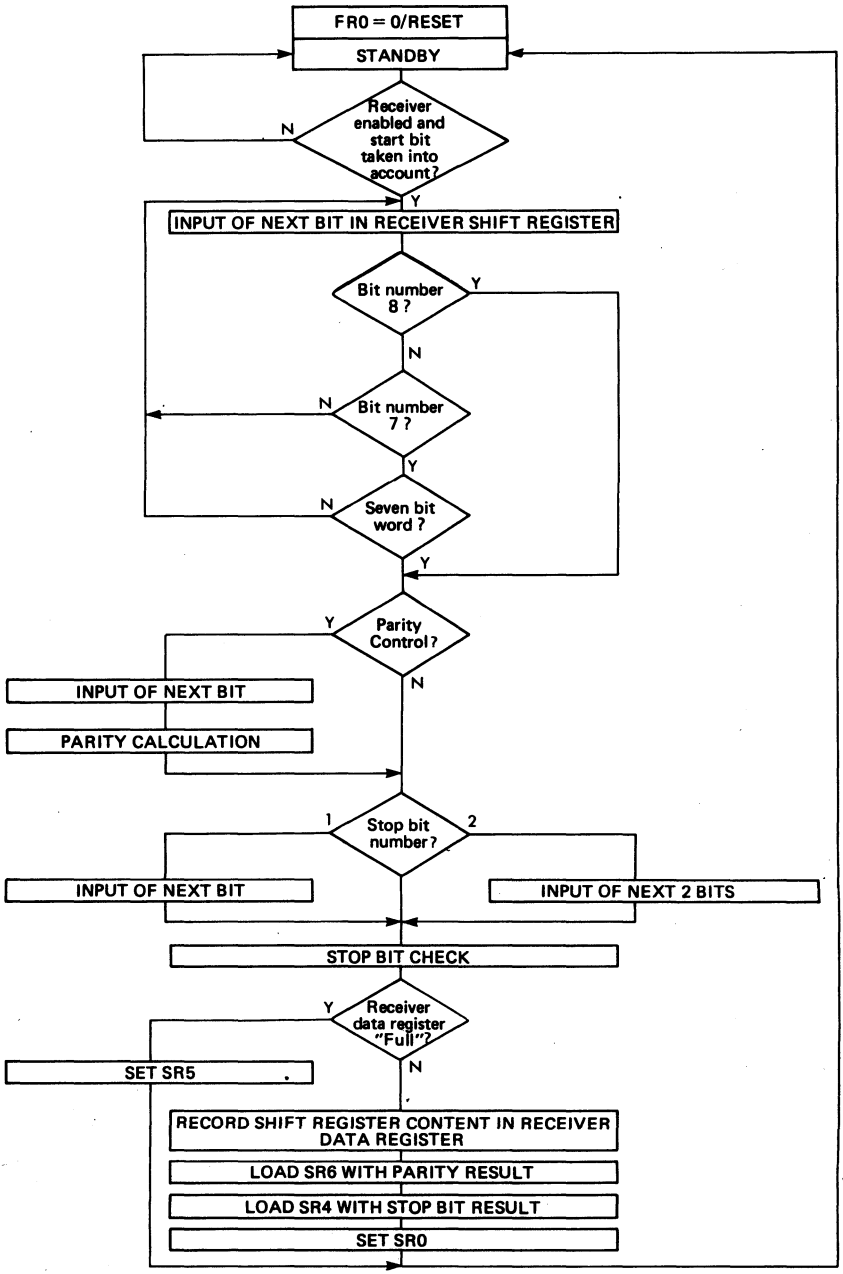
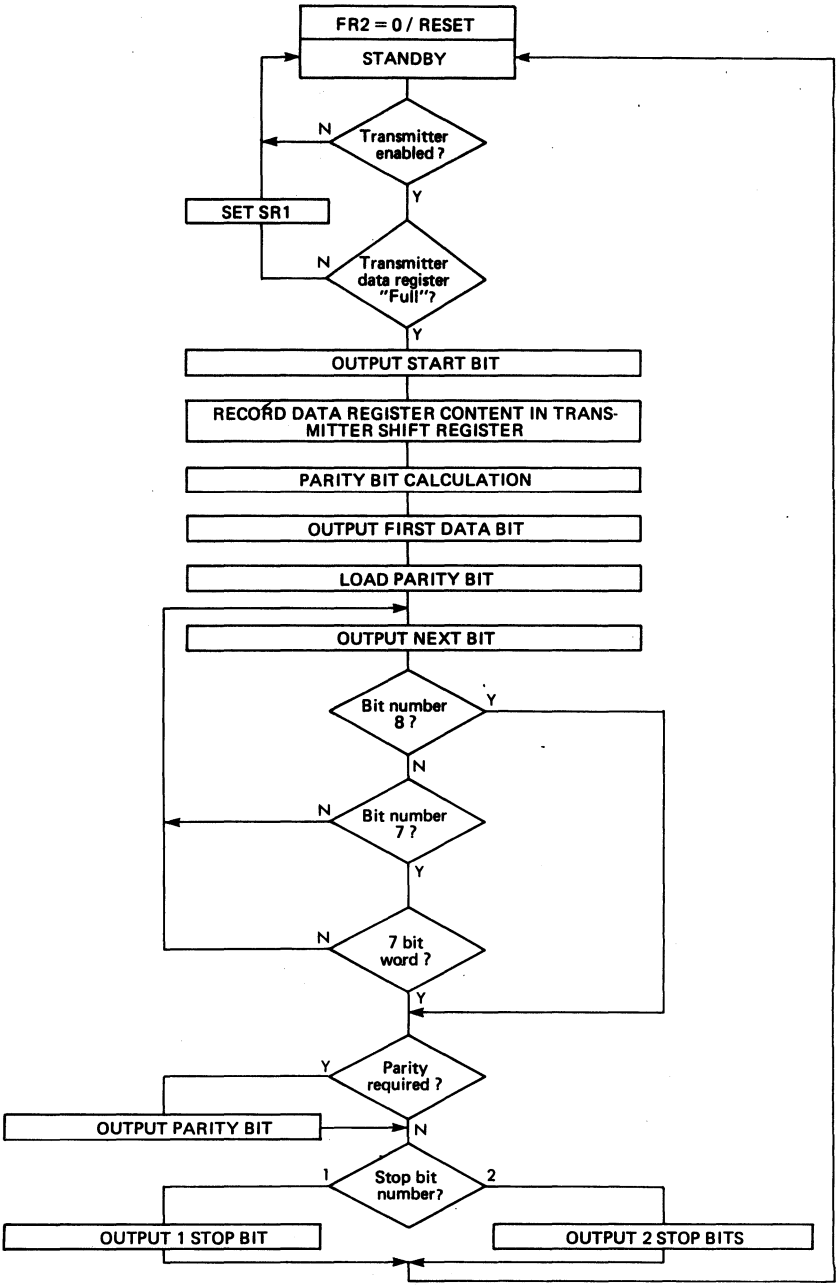


FIGURE 27 – TRANSMITTER OPERATION FLOWCHART



CPU DESCRIPTION

CPU REGISTERS

The EF6805CT Family CPU has five registers available to the programmer. They are shown in Figure 28 and are explained in the following paragraphs.

ACCUMULATOR (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

INDEX REGISTER (X)

The index register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit value that may be added to an instruction value to create an effective address. The index register can also be used for data manipulations using the read-modify-write instructions. The index register may also be used as a temporary storage area.

PROGRAM COUNTER (PC)

The program counter is an 14-bit register that contains the address of the next instruction to be executed.

STACK POINTER (SP)

The stack pointer is an 7 bit register that contains the address of the next free location on the stack. Initially, the stack pointer is set to location $017F and is decremented as data is being pushed onto the stack and incremented as data is being pulled from the stack. During a MCU reset or the Reset Stack Pointer (RSP) instruction, the stack pointer is set to location $017F. Subroutines and interrupts may be nested down to location $100 (128 bytes maximum) which allows the programmer to use up to 64 levels of subroutine calls. No instruction allows to read the stack pointer content.

CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each individual condition code register bit is explained in the following paragraphs.

HALF CARRY (H) — Set during ADD and ADC instructions to indicate that a carry occurred between bits 3 and 4.

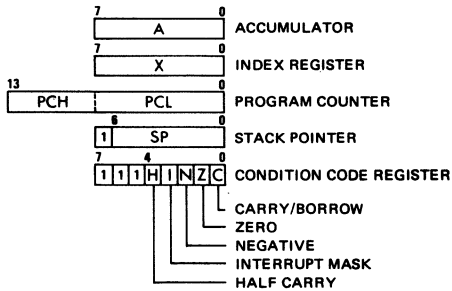
INTERRUPT (I) — This bit is set to mask (disable) the timer, UACC and external interrupts ($\overline{IRQ}$). If an interrupt occurs while this bit is set, the interrupt is latched and is processed as soon as the interrupt bit is cleared.

NEGATIVE (N) — Used to indicate that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in result equal to a logical one).

ZERO (Z) — Used to indicate that the result of the last arithmetic, logical, or data manipulation was zero.

CARRY/BORROW (C) — Used to indicate that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions plus shifts and rotates.

FIGURE 28 – PROGRAMMING MODEL



ADDRESSING MODES

The EF6805CT MCU has 10 addressing modes which are explained briefly in the following paragraphs. For additional details and graphical illustrations, refer to the 6805 Family User's Manual.

The term "effective address" (EA) is used in describing the address modes. EA is defined as the address from which the argument for an instruction is fetched or stored.

IMMEDIATE — In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

EA = PC+ 1 PC◄ PC+ 2

DIRECT — In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single 2-byte instruction. This includes the on-chip RAM and I/O registers and 128 bytes of ROM. Direct addressing is an effective use of both memory and time.

EA = (PC+ 1) PC◄ PC+ 2

EXTENDED — In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions using extended addressing are capable of referencing arguments anywhere in memory with a single 3-byte instruction. When using the assembler ,the programmer need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the shortest form of the instruction.

EA = (PC+ 1) AND (PC+ 2) PC◄ PC+ 3

RELATIVE — The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from − 126 to + 129 from the opcode address. The programmer need not worry about calculating

the correct offset when using the assembler, since it calculates the proper offset and checks to see if it is within the span of the branch.

BR* = (PC+ 1) if branch : EA = PC+ BR*, if not : EA = P C+ 2

* BR = Internal buffer register used for the address calculations.

INDEXED, NO OFFSET — In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

EA = X

INDEXED, 8-BIT OFFSET — In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. This addressing mode is useful in selecting the kth element in an n element table. With this 2-byte instruction, k would typically be in X with the address of the beginning of the table in the instruction. As such, tables may begin anywhere within the first 256 addressable locations and could extend as far as location 510 ($1FE is the last location at which the instruction may begin).

EA = X+ (PC+ 1) PC → PC+ 2

INDEXED, 16-BIT OFFSET — In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed, 8-bit offset, except that this 3-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing.

EA = X+ (PC+ 1) AND (PC+ 2) PC → PC+ 3

BIT SET/CLEAR — In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct address of the byte in which the specified bit is to be set or cleared. Thus, any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single 2-byte instruction.

BIT TEST AND BRANCH — The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit and condition (set or clear) which is to be tested is included in the opcode, and the address of the byte to be tested is in the single byte immediately following the opcode byte. The signed relative 8-bit offset is in the third byte and is added to the value of the PC if the branch condition is true. This single 3-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branching is from − 125 to + 130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code register. ɘe Cautior

EA1 = (PC+ 1), BR ÷ (PC+ 2) , if Branch : EA2 = PC+ BR*; if not : EA2 = PC+ 3

INHERENT — In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as control instruction with no other arguments, are included in this mode. These instructions are one byte long.

INSTRUCTION SET

The EF6805CT MCU has a set of 59 basic instructions, which when combined with the 10 addressing modes produce 207 usable opcodes. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS — Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operands. Refer to Table 8.

READ-MODIFY-WRITE INSTRUCTIONS — These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is included in read/write instructions though it does not perform the write. Refer to Table 9.

BRANCH INSTRUCTIONS - The branch instructions cause a branch from the program when a certain condition is met. Refer to table 10.

BIT MANIPULATION INSTRUCTIONS - These instructions are used on any bit in the first 256 bytes of memory. One group of instructions either sets or clears, the other group performs the bit test and branch operations. Refer to table 11.

CONTROL INSTRUCTIONS - The control instructions control the MCU operations during program execution. Refer to table 12.

Alphabetical listing - The complete instruction set is given in alphabetical order in table 13.

Opcode map summary - Table 14 is an opcode map for the instructions used by the CPU.

TABLE 8 – REGISTER / MEMORY INSTRUCTIONS

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
Load X from Memory	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
Store A in Memory	STA	–	–	–	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
Store X in Memory	STX	–	–	–	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
Add Memory to A	ADD	AB	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
Add Memory and Carry to A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
Subtract Memory	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND Memory to A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR Memory with A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
Jump Unconditional	JMP	–	–	–	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
Jump to Subroutine	JSR	–	–	–	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

TABLE 9 – READ / MODIFY / WRITE INSTRUCTIONS

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8 Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
Decrement	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
Clear	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
Complement	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
Negate (2's Complement)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
Rotate Left Thru Carry	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
Rotate Right Thru Carry	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
Logical Shift Left	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
Logical Shift Right	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
Arithmetic Shift Right	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
Test for Negative or Zero	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

TABLE 10 – BRANCH INSTRUCTIONS

		Relative Addressing Mode		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	4
Branch Never	BRN	21	2	4
Branch IFF Higher	BHI	22	2	4
Branch IFF Lower or Same	BLS	23	2	4
Branch IFF Carry Clear	BCC	24	2	4
(Branch IFF Higher or Same)	(BHS)	24	2	4
Branch IFF Carry Set	BCS	25	2	4
(Branch IFF Lower)	(BLO)	25	2	4
Branch IFF Not Equal	BNE	26	2	4
Branch IFF Equal	BEQ	27	2	4
Branch IFF Half Carry Clear	BHCC	28	2	4
Branch IFF Half Carry Set	BHCS	29	2	4
Branch IFF Plus	BPL	2A	2	4
Branch IFF Minus	BMI	2B	2	4
Branch IFF Interupt Mask Bit is Clear	BMC	2C	2	4
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	4
Branch IFF Interrupt Line is Low ($\overline{IRQ}$)	BIL	2E	2	4
Branch IFF Interrupt Line is High ($\overline{IRQ}$)	BIH	2F	2	4
Branch to Subroutine	BSR	AD	2	8

TABLE 11 – BIT MANIPULATION INSTRUCTIONS

		Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is set	BRSET n (n = 0....7)	—	—	—	2 • n	3	10
Branch IFF Bit n is clear	BRCLR n (n = 0....7)	—	—	—	01 + 2 • n	3	10
Set Bit n	BSET n (n = 0....7)	10 + 2 • n	2	7	—	—	—
Clear bit n	BCLR n (n = 0....7)	11 + 2 • n	2	7	—	—	—

TABLE 12 – CONTROL INSTRUCTIONS

		Inherent		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	11
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2

TABLE 13 – INSTRUCTION SET

	Addressing Modes										Condition Code				
Mnemonic	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			∧	●	∧	∧	∧
ADD		X	X	X		X	X	X			∧	●	∧	∧	∧
AND		X	X	X		X	X	X			●	●	∧	∧	●
ASL	X		X			X	X				●	●	∧	∧	∧
ASR	X		X			X	X				●	●	∧	∧	∧
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	∧	∧	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	∧
BRSET										X	●	●	●	●	∧
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLL	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	∧	∧	∧
COM	X		X			X	X				●	●	∧	∧	1
CPX		X	X	X		X	X	X			●	●	∧	∧	∧
DEC	X		X			X	X				●	●	∧	∧	●
EOR		X	X	X		X	X	X			●	●	∧	∧	●
INC	X		X			X	X				●	●	∧	∧	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	∧	∧	●
LDX		X	X	X		X	X	X			●	●	∧	∧	●
LSL	X		X			X	X				●	●	∧	∧	∧
LSR	X		X			X	X				●	●	0	∧	∧
NEG	X		X			X	X				●	●	∧	∧	∧
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	∧	∧	●
ROL	X		X			X	X				●	●	∧	∧	∧
RSP	X										●	●	●	●	●

Condition Code Symbols:

- H Half Carry (From Bit 3)
- I Interrupt Mask
- N Negative (Sign Bit)
- Z Zero
- C Carry/Borrow
- ∧ Test and Set if True, Cleared Otherwise
- • Not Affected

TABLE 14 – INSTRUCTION SET (CONTINUED)

	Addressing Modes										Condition Code				
Mnemonic	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	^	^	^
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	^	^	●
STX			X	X		X	X	X			●	●	^	^	●
SUB		X	X	X		X	X	X			●	●	^	^	^
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	^	^	●
TXA	X										●	●	●	●	●

Condition Code Symbols:

- H Half Carry (From Bit 3)
- I Interrupt Mask
- N Negative (Sign Bit)
- Z Zero
- C Carry/Borrow
- ^ Test and Set if True, Cleared Otherwise
- • Not Affected
- ? Load CC Register From Stack

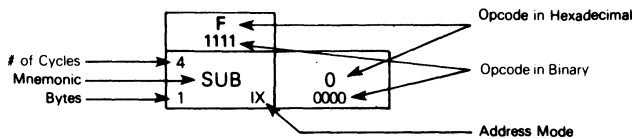
TABLE 15 – EF6805CT HMOS FAMILY OPCODE MAP

Hi / Low	Bit Manipulation		Branch	Read-Modify-Write					Control		Register / Memory					
	BTB 0 0000	BSC 1 0001	REL 2 0010	DIR 3 0011	INH 4 0100	INH 5 0101	IX1 6 0110	IX 7 0111	INH 8 1000	INH 9 1001	IMM A 1010	DIR B 1011	EXT C 1100	IX2 D 1101	IX1 E 1110	IX F 1111	
0 0000	10 BRSET0 3 BTB	7 BSET0 2 BSC	4 BRA 2 REL	6 NEG 2 DIR	4 NEG 1 INH	4 NEG 1 INH	7 NEG 2 IX1	6 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	4 SUB 2 DIR	5 SUB 3 EXT	6 SUB 3 IX2	5 SUB 2 IX1	4 SUB 1 IX	0 0000
1 0001	10 BRCLR0 3 BTB	7 BCLR0 2 BSC	4 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	4 CMP 2 DIR	5 CMP 3 EXT	6 CMP 3 IX2	5 CMP 2 IX1	4 CMP 1 IX	1 0001
2 0010	10 BRSET1 3 BTB	7 BSET1 2 BSC	4 BHI 2 REL								2 SBC 2 IMM	4 SBC 2 DIR	5 SBC 3 EXT	6 SBC 3 IX2	5 SBC 2 IX1	4 SBC 1 IX	2 0010
3 0011	10 BRCLR1 3 BTB	7 BCLR1 2 BSC	4 BLS 2 REL	6 COM 2 DIR	4 COMA 1 INH	4 COMX 1 INH	7 COM 2 IX1	6 COM 1 IX	9 SWI 1 INH		2 CPX 2 IMM	4 CPX 2 DIR	5 CPX 3 EXT	6 CPX 3 IX2	5 CPX 2 IX1	4 CPX 1 IX	3 0011
4 0100	10 BRSET2 3 BTB	7 BSET2 2 BSC	4 BCC 2 REL	6 LSR 2 DIR	4 LSRA 1 INH	4 LSRX 1 INH	7 LSR 2 IX1	6 LSR 1 IX			2 AND 2 IMM	4 AND 2 DIR	5 AND 3 EXT	6 AND 3 IX2	5 AND 2 IX1	4 AND 1 IX	4 0100
5 0101	10 BRCLR2 3 BTB	7 BCLR2 2 BSC	4 BCS 2 REL								2 BIT 2 IMM	4 BIT 2 DIR	5 BIT 3 EXT	6 BIT 3 IX2	5 BIT 2 IX1	4 BIT 1 IX	5 0101
6 0110	10 BRSET3 3 BTB	7 BSET3 2 BSC	4 BNE 2 REL	6 ROR 2 DIR	4 RORA 1 INH	4 RORX 1 INH	7 ROR 2 IX1	6 ROR 1 IX			2 LDA 2 IMM	4 LDA 2 DIR	5 LDA 3 EXT	6 LDA 3 IX2	5 LDA 2 IX1	4 LDA 1 IX	6 0110
7 0111	10 BRCLR3 3 BTB	7 BCLR3 2 BSC	4 BEQ 2 REL	6 ASR 2 DIR	4 ASRA 1 INH	4 ASRX 1 INH	7 ASR 2 IX1	6 ASR 1 IX	2 TAX 1 INH			5 STA 2 DIR	6 STA 3 EXT	7 STA 3 IX2	6 STA 2 IX1	5 STA 1 IX	7 0111
8 1000	10 BRSET4 3 BTB	7 BSET4 2 BSC	4 BHCC 2 REL	6 LSL 2 DIR	4 LSLA 1 INH	4 LSLX 1 INH	7 LSL 2 IX1	6 LSL 1 IX	2 CLC 1 INH		2 EOR 2 IMM	4 EOR 2 DIR	5 EOR 3 EXT	6 EOR 3 IX2	5 EOR 2 IX1	4 EOR 1 IX	8 1000
9 1001	10 BRCLR4 3 BTB	7 BCLR4 2 BSC	4 BHCS 2 REL	6 ROL 2 DIR	4 ROLA 1 INH	4 ROLX 1 INH	7 ROL 2 IX1	6 ROL 1 IX	2 SEC 1 INH		2 ADC 2 IMM	4 ADC 2 DIR	5 ADC 3 EXT	6 ADC 3 IX2	5 ADC 2 IX1	4 ADC 1 IX	9 1001
A 1010	10 BRSET5 3 BTB	7 BSET5 2 BSC	4 BPL 2 REL	6 DEC 2 DIR	4 DECA 1 INH	4 DECX 1 INH	7 DEC 2 IX1	6 DEC 1 IX	2 CLI 1 INH		2 ORA 2 IMM	4 ORA 2 DIR	5 ORA 3 EXT	6 ORA 3 IX2	5 ORA 2 IX1	4 ORA 1 IX	A 1010
B 1011	10 BRCLR5 3 BTB	7 BCLR5 2 BSC	4 BMI 2 REL						2 SEI 1 INH		2 ADD 2 IMM	4 ADD 2 DIR	5 ADD 3 EXT	6 ADD 3 IX2	5 ADD 2 IX1	4 ADD 1 IX	B 1011
C 1100	10 BRSET6 3 BTB	7 BSET6 2 BSC	4 BMC 2 REL	6 INC 2 DIR	4 INCA 1 INH	4 INCX 1 INH	7 INC 2 IX1	6 INC 1 IX	2 RSP 1 INH			3 JMP 2 DIR	4 JMP 3 EXT	5 JMP 3 IX2	4 JMP 2 IX1	3 JMP 1 IX	C 1100
D 1101	10 BRCLR6 3 BTB	7 BCLR6 2 BSC	4 BMS 2 REL	6 TST 2 DIR	4 TSTA 1 INH	4 TSTX 1 INH	7 TST 2 IX1	6 TST 1 IX	2 NOP 1 INH		8 BSR 2 REL	7 JSR 2 DIR	8 JSR 3 EXT	9 JSR 3 IX2	8 JSR 2 IX1	7 JSR 1 IX	D 1101
E 1110	10 BRSET7 3 BTB	7 BSET7 2 BSC	4 BIL 2 REL								2 LDX 2 IMM	4 LDX 2 DIR	5 LDX 3 EXT	6 LDX 3 IX2	5 LDX 2 IX1	4 LDX 1 IX	E 1110
F 1111	10 BRCLR7 3 BTB	7 BCLR7 2 BSC	4 BIH 2 REL	6 CLR 2 DIR	4 CLRA 1 INH	4 CLRX 1 INH	7 CLR 2 IX1	6 CLR 1 IX	2 TXA 1 INH			5 STX 2 DIR	6 STX 3 EXT	7 STX 3 IX2	6 STX 2 IX1	5 STX 1 IX	F 1111

Abbreviations for Address Modes

INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset

LEGEND



EF6805CT INTERRUPTS

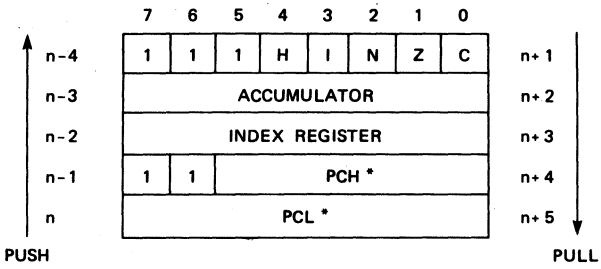
The EF6805CT Family supports three types of interrupt requests : maskable, non-maskable and software interrupts. Any interrupt is acted upon at the completion of current instruction ; a non-maskable interrupt ($\overline{NMI}$) is always recognized. Maskable interrupts are controlled by the condition code register (bit I) and by individual enable bits. The bit I controls all maskable interrupts. There are five types of maskable interrupts : $\overline{IRQ}$ (external), $\overline{IRQC}$ (Port C), $\overline{IRQR}$ (Receiver), $\overline{IRQE}$ (transmitter) and $\overline{IRQT}$ (timer), as shown in Figure 1.
All $\overline{IRQ}$ interrupts use hardware prioritized vectors ; each of them is vectored to a separate location ; all interrupt vector locations are shown in table 16.
The interrupt flowchart is depicted in Figure 29 and is common to each interrupt. During interrupt servicing the Program Counter, Index Register, Accumulator and Code Condition Register are pushed into the stack. The bit I is set to inhibit maskable interrupts and a vector is fetched corresponding to the current highest priority interrupt. The vector is transferred to the Program Counter and instruction execution is activated. Interrupt sequence and RESET timing are illustrated in Figures 30 and 31.
The interrupt service routine must end with a RTI (return from interrupt) instruction which allows the CPU to resume processing of the interrupted program.
RTI pulls the context out of the stack (see table 17 for Interrupt stacking order). RESET operation forces the stack pointer to $017F and sets the bit I.

TABLE 16 – INTERRUPT VECTOR LOCATIONS AND INTERRUPT PRIORITY

Interrupt	Description	Priority	Interrupt vectors MSB	Interrupt vectors LSB	Acting on
$\overline{RESET}$	Reset	1	3FFE	3FFF	level
$\overline{NMI}$	Non maskable external interrupt	2	3FFC	3FFD	negative edge
$\overline{IRQ}$	Maskable and soft testable external interrupt	3	3FFA	3FFB	negative edge
$\overline{IRQC}$	Maskable port C interrupt	4	3FF8	3FF9	level
SWI*	Software interrupt	–	3FF6	3FF7	–
$\overline{IRQR}$	UACC receiver maskable interrupt	5	3FF4	3FF5	level
$\overline{IRQT}$	Timer maskable interrupt	6	3FF2	3FF3	level
$\overline{IRQE}$	UACC transmitter maskable interrupt	7	3FF0	3FF1	level

*There is no priority between SWI and the EF6805CT interrupts. As soon as a SWI instruction is recognized by the CPU, this instruction is executed independently of the status of the other interrupt requests.

TABLE 17 – INTERRUPT STACKING ORDER



*For subroutine calls, only PCL and PCH are stacked.

FIGURE 29 – INTERRUPT FLOWCHART

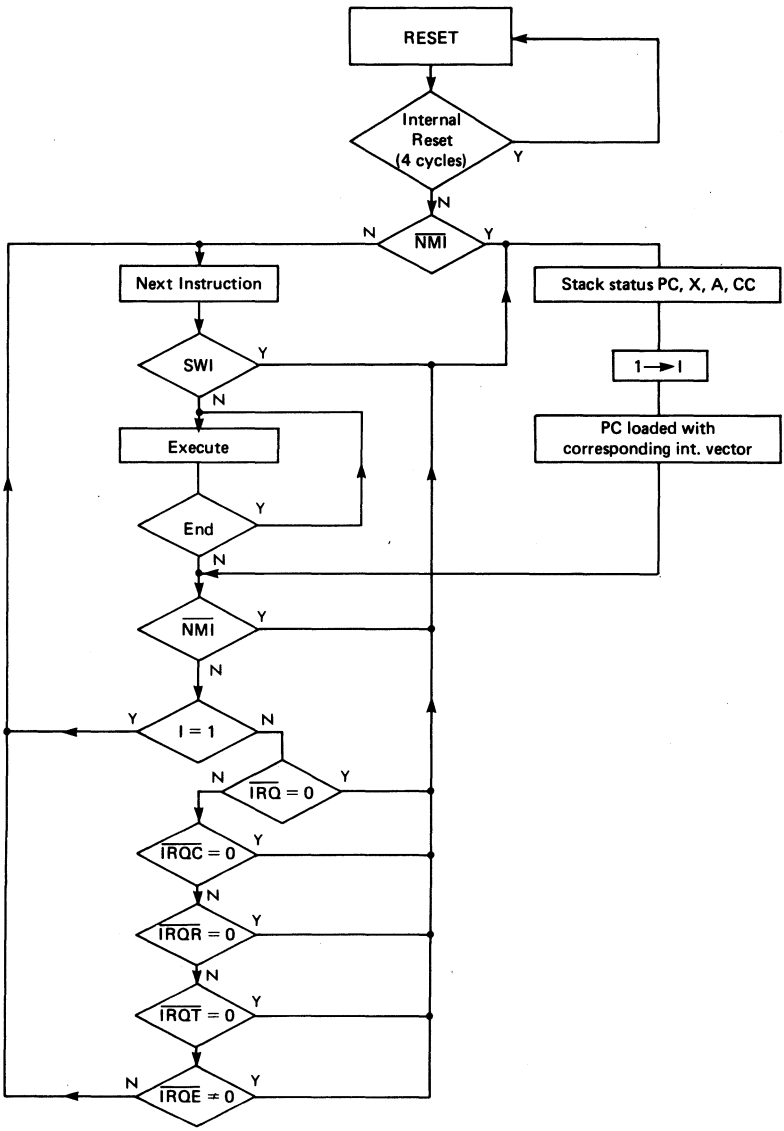


FIGURE 30 – INTERRUPT SEQUENCE

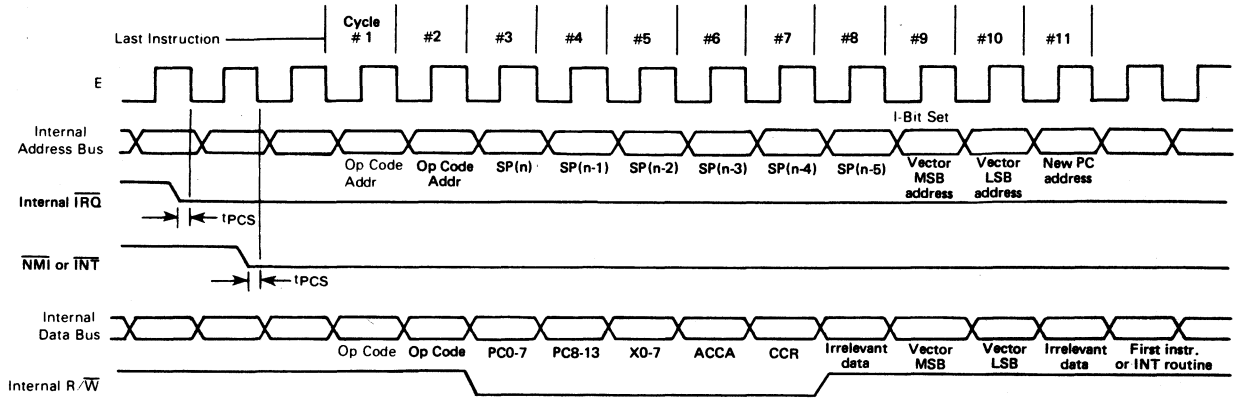
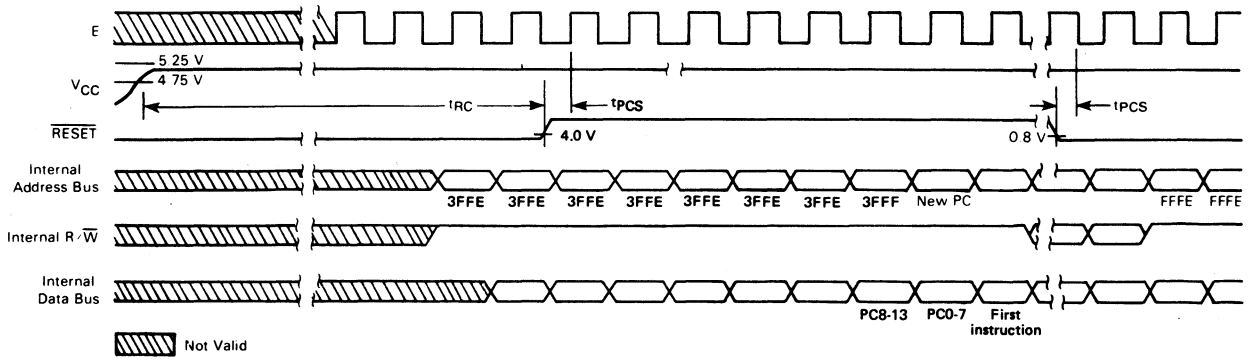


FIGURE 31– RESET TIMING



SUMMARY OF CYCLE-BY-CYCLE OPERATION

Table 18 provides a detailed description of the information present on the Address Bus, Data Bus, and the Read/Write (R/$\overline{W}$) line during each cycle of each instruction. The information is useful in comparing actual with expected results during debug of both software and hardware as the program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction. In general, instructions with the same addressing mode and number of cycles execute in the same manner. Exceptions are indicated in the table.

Not that during MPU reads of internal locations, the resultant value will not appear on the external Data Bus except in Mode 0. "High order" byte refers to the most significant byte of a 16-bit value.

TABLE 18 – CYCLE-BY-CYCLE OPERATION

Address Mode & Instructions	Cycles	M1	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
IMMEDIATE						
ADC EOR ADD LDA AND LDX BIT ORA CMP SBC CPX SUB	2	0 1	1 2	Op Code Address Op Code Address + 1	1 1	Op Code Operand Data
INHERENT						
CLC SEC CLI SEI NOP TAX RSP TXA	2	0 1	1 2	Op Code Address Op Code Address + 1	1 1	Op Code Irrelevant data
RTS	6	0 1 1 1 1 1	1 2 3 4 5 6	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer + 1 Stack Pointer + 2 Stack Pointer + 3	1 1 1 1 1 	Op Code Irrelevant Data Irrelevant Data Return Address (High Order Byte) Return Address (Low Order Byte) Irrelevant Data
RTI	9	0 1 1 1 1 1 1 1 1	1 2 3 4 5 6 7 8 9	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer + 1 Stack Pointer + 2 Stack Pointer + 3 Stack Pointer + 4 Stack Pointer + 5 Stack Pointer + 6	1 1 1 1 1 1 1 1 1	Op Code Irrelevant Data Irrelevant Data Contents of Cond. Code Reg. from Stack Contents of Accumulator from Stack Index Register Content Return Address (High Order Byte) Return Address (Low Order Byte) Irrelevant Data
SWI	12	0 1 1 1 1 1 1 1 1 1 1 1	1 2 3 4 5 6 7 8 9 10 11	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer – 1 Stack Pointer – 2 Stack Pointer – 3 Stack Pointer – 4 Stack Pointer – 5 Vector Address Vector Address + 1 Vector Address + 2	1 1 0 0 0 0 0 1 1 1 1	Op Code Irrelevant Data Program Counter (Low Order Byte) Program Counter (High Order Byte) Index Register Accumulator Condition Code Register Irrelevant Data Vector (High Order Byte) Vector (Low Order Byte) Irrelevant Data

TABLE 18 – CYCLE-BY-CYCLE OPERATION (CONTINUED)

Address Mode & Instructions	Cycles	M1	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
DIRECT						
JMP	3	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Final Address
		1	3	3FFF	1	Irrelevant Data
ADC CMP LDX ADD CPX ORA AND EOR SBC BIT LDA SUB	4	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Operand Address
		1	3	3FFF	1	Irrelevant Data
		1	4	Operand Address	1	Operand
STA STX	5	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Final Address
		1	3	3FFF	1	Irrelevant Data
		1	4	3FFF	1	"
		1	5	Final Address	0	Data to store
ASR DEC LSR CLR INC NEG COM LSL ROL ROR TST	6	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Operand Address
		1	3	3FFF	1	Irrelevant Data
		1	4	Operand Address	1	Operand
		1	5	3FFF	1	Irrelevant Data
		1	6	Operand Address (3FFF if TST)	0 *	Modified operand
JSR	7	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Subroutine Address
		1	3	3FFF	1	Irrelevant Data
		1	4	Subroutine Address		First subroutine instruction Op Code
		1	5	Stack Pointer	0	Return Address (Low Order Byte)
		1	6	Stack Pointer – 1	0	Return Address (High Order Byte)
		1	7	Stack Pointer – 2	1	Irrelevant Data

* R/$\overline{W}$ = 1 if TST

EXTENDED						
JMP	4	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Jump Address (High Order Byte)
		1	3	Op Code Address + 2	1	Jump Address (Low Order Byte)
		1	4	3FFF	1	Irrelevant Data
ADC EOR ADD LDA AND LDX BIT ORA CMP SBC CPX SUB	5	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Address of Operand (High Order Byte)
		1	3	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		1	4	3FFF	1	Irrelevant Data
		1	5	Operand Address	1	Operand
STA STX	6	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Destination Address (High Order Byte)
		1	3	Op Code Address + 2	1	Destination Address (Low Order Byte)
		1	4	3FFF	1	Irrelevant Data
		1	5	3FFF	1	Irrelevant Data
		1	6	Destination Address	0	Data to store
JSR	8	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Address of Subroutine (High Order Byte)
		1	3	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
		1	4	3FFF	1	Irrelevant Data
		1	5	Subroutine starting address	1	Op Code (First instruction)
		1	6	Stack Pointer	0	Return Address (How Order Byte)
		1	7	Stack Pointer – 1	0	Return Address (High Order Byte)
		1	8	Stack Pointer – 2	1	Irrelevant Data

TABLE 18 – CYCLE-BY-CYCLE OPERATION (CONTINUED)

Address Mode & Instructions	Cycles	M1	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
RELATIVE						
BCC (BHS) (BLO) BNE BCS BIH BLS BPL BEO BIL BMC BRA BHCC BLE BMI BRN BHCS	4	0 1 1 1	1 2 3 4	Op Code Address Op Code Address + 1 3FFF 3FFF	1 1 1 1	Op Code Branch Offset Irrelevant Data Irrelevant Data
BSR	8	0 1 1 1 1 1 1 1	1 2 3 4 5 6 7 8	Op Code Address Op Code Address + 1 Op Code Address + 2 3FFF 3FFF Stack Pointer Stack Pointer – 1 Stack Pointer – 2	1 1 1 1 1 0 0 1	Op Code Branch Offset Irrelevant Data Irrelevant Data Irrelevant Data Return Address (Low Order Byte) Return Address (High Order Byte) Irrelevant Data
INHERENT A, X						
ASR LSR CLR NEG COM ROL DEC ROR INC TST	4	0 1 1 1	1 2 3 4	Op Code Address Op Code Address + 1 3FFF 3FFF	1 1 1 1	Op Code Irrelevant Data Irrelevant Data Irrelevant Data
BIT SET OR CLEAR						
BCLRN BSETN	7	0 1 1 1 1 1 1	1 2 3 4 5 6 7	Op Code Address Op Code Address + 1 3FFF Operand Address 3FFF 3FFF Operand Address	1 1 1 1 1 1 0	Op Code Operand Address Irrelevant Data Operand Data Irrelevant Data Irrelevant Data New Operand Data
INDEXED (WITHOUT OFFSET)						
JMP	3	0 1 1	1 2 3	Op Code Address Op Code Address + 1 Address Bus 3FFF	1 1 1	Op Code Irrelevant Data Irrelevant Data
ADC EOR ADD LDA AND LDX BIT ORA CMP SBC CPX SUB	4	0 1 1 1	1 2 3 4	Op Code Address Op Code Address + 1 Address Bus 3FFF Operand Address	1 1 1 1	Op Code Irrelevant Data Irrelevant Data Operand Data
STA STX	5	0 1 1 1 1	1 2 3 4 5	Op Code Address Op Code Address + 1 Address Bus 3FFF Address Bus 3FFE Destination Address	1 1 1 1 0	Op Code Irrelevant Data Irrelevant Data Irrelevant Data Data to Store
ASR LSR CLR NEG COM ROL DEC TST INC	6	0 1 1 1 1 1	1 2 3 4 5 6	Op Code Address Op Code Address + 1 Address Bus 3FFF Operand Address "	1 1 1 1 1 0 *	Op Code Irrelevant Data Irrelevant Data Current Operand Data Irrelevant Data New Operand Data
JSR	7	0 1 1 1 1 1 1	1 2 3 4 5 6 7	Op Code Address Op Code Address + 1 Address Bus 3FFF Subroutine start Address Stack Pointer Stack Pointer – 1 Stack Pointer – 2	1 1 1 1 0 0 1	Op Code Irrelevant Data Irrelevant Data First Subroutine Op Code Return Address (Low Order Byte) Return Address (High Order Byte) Irrelevant Data

* R/$\overline{W}$ = 1 if TST

TABLE 18 – CYCLE-BY-CYCLE OPERATION (CONTINUED)

Address Mode & Instructions	Cycles	M1	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
INDEXED (1 BYTE OFFSET)						
JMP	4	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Offset
		1	3	3FFF	1	Irrelevant Data
		1	4	3FFF	1	Irrelevant Data
ADC CMP LDX ADD CPX ORA AND EOR SBC BIT LDA SUB	5	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address+ 1	1	Offset
		1	3	3FFF	1	Irrelevant Data
		1	4	3FFF	1	Irrelevant Data
		1	5	Operand Address	1	Operand Data
STA STX	6	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Offset
		1	3	3FFF	1	Irrelevant Data
		1	4	3FFF	1	Irrelevant Data
		1	5	3FFF	1	Irrelevant Data
		1	6	Destination Address	0	Data to Store
ASR INC ROL CLR LSL ROR COM LSR TST DEC NEG	7	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Offset
		1	3	3FFF	1	Irrelevant Data
		1	4	3FFF	1	Irrelevant Data
		1	5	Operand Address ((X) + Offset)	1	Operand Data
		1	6	" " " "	1	Irrelevant Data
		1	7	" " " "	0*	New Operand Data
JSR	8	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Offset
		1	3	3FFF	1	Irrelevant Data
		1	4	3FFF	1	Irrelevant Data
		1	5	Subroutine Start Address	1	First Subroutine Op Code
		1	6	Stack Pointer	0	Return Address (Low Order Byte)
		1	7	Stack Pointer - 1	0	Return Address (High Order Byte)
		1	8	Stack Pointer - 2	1	Irrelevant Data
INDEXED (2 BYTES OFFSET)						
JMP	5	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Offset (High Order Byte)
		1	3	Op Code Address + 2	1	Offset (Low Order Byte)
		1	4	3FFF	1	Irrelevant Data
		1	5	3FFF	1	Irrelevant Data
ADC CMP LDX ADD CPX ORA AND EOR SBC BIT LDA SUB	6	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Offset (High Order Byte)
		1	3	Op Code Address + 2	1	Offset (Low Order Byte)
		1	4	3FFF	1	Irrelevant Data
		1	5	3FFF	1	Irrelevant Data
		1	6	Operand Address	1	Operand Data
STA STX	7	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Offset (High Order Byte)
		1	3	Op Code Address + 2	1	Offset (Low Order Byte)
		1	4	3FFF	1	Irrelevant Data
		1	5	3FFF	1	Irrelevant Data
		1	6	3FFF	1	Irrelevant Data
		1	7	Destination Address	0	Data to store

* R/$\overline{W}$ = 1 if TST

TABLE 18 – CYCLE-BY-CYCLE OPERATION (CONTINUED)

Address Mode & Instructions	Cycles	M1	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
INDEXED (2 BYTES OFFSET) (CONTINUED)						
JSR	9	0	1	Op Code Address	1	Op Code
		1	2	Op Code Address + 1	1	Offset (High Order Byte)
		1	3	Op Code Address + 2	1	Offset (Low Order Byte)
		1	4	3FFF	1	Irrelevant Data
		1	5	3FFF	1	Irrelevant Data
		1	6	Subroutine start Address	1	First subroutine Op Code
		1	7	Stack Pointer	0	Return Address (Low Order Byte)
		1	8	Stack Pointer - 1	0	Return Address (High Order Byte)
		1	9	Stack Pointer - 2	1	Irrelevant Data.
BIT TEST AND BRANCH						
BRCLRn	10	0	1	Op Code Address	1	Op Code
BRSETn		1	2	Op Code Address + 1	1	Operand Address
		1	3	3FFF	1	Irrelevant Data
		1	4	Operand Address	1	Operand Data
		1	5	3FFF	1	Irrelevant Data
		1	6	3FFF	1	Irrelevant Data
		1	7	3FFF	1	Irrelevant Data
		1	8	Op Code Address + 2	1	Offset
		1	9	3FFF	1	Irrelevant Data
		1	10	3FFF	1	Irrelevant Data

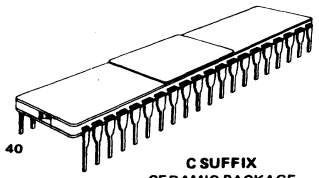
ORDERING INFORMATION

PART NUMBER	PACKAGE		OPER. TEMP.			QUALITY LEVEL			
	P	FN	L*	V	A	Std**	D	G	B
EF6805CT	•	•	•	•		•	Available on request		

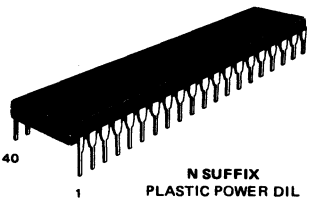
Examples : EF6805CTP, EF6805CTFN, EF6805CTPV, EF6805CTFNV

P : Plastic DIL, **FN** : SURPICOP (Plastic chip-carrier at JEDEC std 0.50" center leaded type A)
L* : 0°C to + 70°C, **V** : - 40°C to + 85°C, **A** : - 40°C to + 105°C, * : may be omitted.
Quality levels in accordance with NFC 96883 - ** : No end-suffix for standard level products.

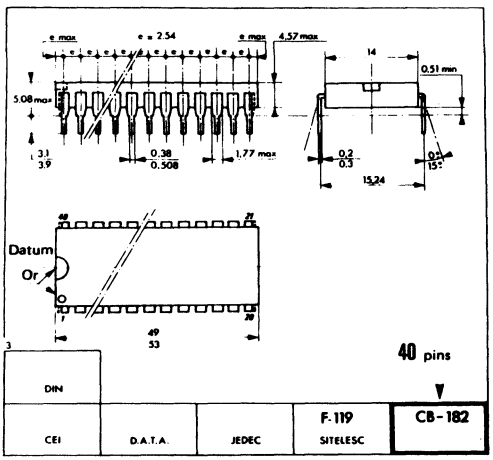
CASE CB-182



C SUFFIX
CERAMIC PACKAGE



N SUFFIX
PLASTIC POWER DIL



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

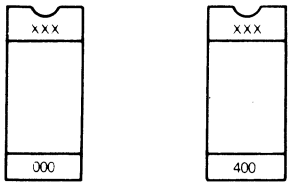
ORDERING INFORMATION

The information required when ordering a custom MCU is listed below. The ROM program may be transmitted to THOMSON SEMICONDUCTORS on EPROM(s) or an EFDOS/MDOS disk file.

To initiate a ROM pattern for the MCU it is necessary to first contact your local THOMSON SEMICONDUCTORS representative or distributor.

EPROMs

The ET2716 or ET2732 type EPROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The EPROM must be clearly marked to indicate which EPROM corresponds to which address space. The recommended marking procedure is illustrated below.



XXX = Customer ID

After the EPROM(s) are marked they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.

VERIFICATION MEDIA

All original pattern media (EPROMs or Floppy Disk) are filed for contractual purposes and are not returned. A computer listing of the ROM code will be generated and returned along with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed, and returned to THOMSON SEMICONDUCTORS. The signed verification form constitutes the contractual agreement for creation of the customer mask.

ROM VERIFICATION UNITS (RVUs)

Ten MCUs containing the customer's ROM pattern will be sent for program verification. These units will have been made using the custom mask but are for the purpose of ROM verification only. For expediency they are usually unmarked, packaged in ceramic, and tested only at room temperature and 5 volts. These RVUs are included in the mask charge and are not production parts. The RVUs are thus not guaranteed by THOMSON SEMICONDUCTORS Quality Assurance, and should be discarded after verification is completed.

FLEXIBLE DISKS

The disk media submitted must be single-sided, single-density, 8-inch, EFDOS compatible floppies. The customer must write the binary file name and company name on the disk with a felt-tip-pen. The minimum EFDOS system files as the absolute binary object file (filename .LO type of file) from the 6805 cross assembler must be on the disk. An object file made from a memory dump using the ROLLOUT command is also acceptable. Consider submitting a source listing as well as the following files : filename .LX (THEMIS/EXORciser* loadable format) and filename .SA (ASCII Source Code). These files will of course be kept confidential and are used 1) to speed up the process in-house if any problems arise, and 2) to speed up the user-to-factory interface if the user finds any software errors and needs assistance quickly from THOMSON SEMICONDUCTORS factory representatives.

EFDOS is THOMSON SEMICONDUCTORS' Disk Operating System available on development systems such as THEMIS, MONOCARD, etc.

Whenever ordering a custom MCU is required, please contact your local THOMSON SEMICONDUCTORS representative or THOMSON SEMICONDUCTORS distributor and/or complete and send the attached "MCU customer ordering sheet" to your local THOMSON SEMICONDUCTORS representative.

*THEMIS, MONOCARD are trademarks of THOMSON SEMICONDUCTORS, EXORciser is a registered trademark of Motorola Inc.

MCU CUSTOMER ORDERING SHEET

EF6805 FAMILY

Commercial reference : E F 6 8 | | | | | | | | | | |

Customer's marking : | | | | | | | | | | | | | | | |

Customer name : . . . . . .
Company : . . . . . .
Address : . . . . . .
Phone : . . . . . .

Application : . . . . . .

ROM capacity required : | | | | bytes

Customer part number :

Temperature range : ☐ 0 /+ 70°C
☐ −40/+ 85°C

Number of interrupt vectors :

Quality level : ☐ STD ☐ D ☐ G ☐ B

Package : ☐ plastic
☐ SURPICOP

Software support required ☐
☐ using the THOMSON SEMICONDUCTORS application lab.
☐ using an external lab.

Pattern supplied by the customer ☐

Pattern medias :

☐ EPROM reference :
☐ MDOS/EFDOS disk file (EXORciser/THEMIS)*
☐ Listing

* Requires prior factory approval

Yearly quantity forecasted :

– start of production date :
– for a shipment period of :

CUSTOMER CONTACT NAME : DATE : SIGNATURE :

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

THOMSON SEMICONDUCTORS

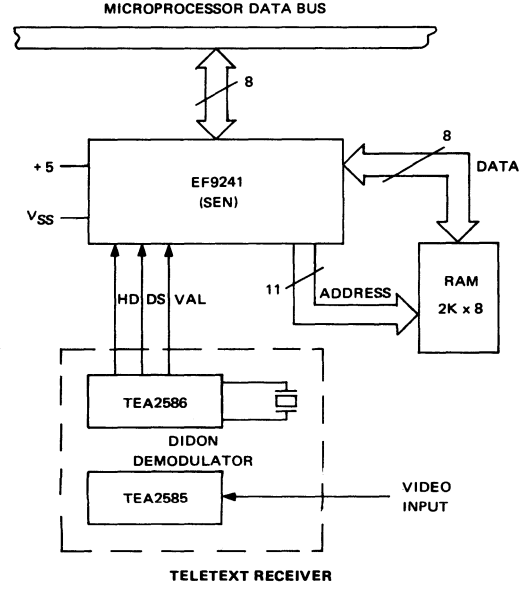
EF9241

ADVANCE INFORMATION

BROADCASTED DATA DEMULTIPLEXOR

The EF9241 (SEN) is a broadcasted data channel demultiplexor. Used in conjunction with a demodulator and a RAM, it constitues a complete receiver for CEEFAX DIDON or ANTIOPE standards.

- Programmable framing code
- Programmable packet format
  - Programmable packet address length and value
  - Programmable prefix length
  - Programmable data packet length
- Programmable odd parity check
- Programmable search mode
- Standard RAM managed on chip as a FIFO. 1 K x 8 or 2 K x 8 RAM size programmable
- Direct interface with 8 bit microprocessor data bus.

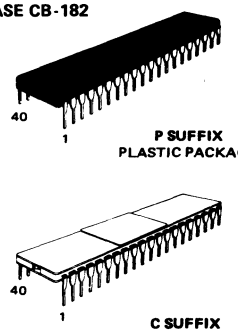


MOS

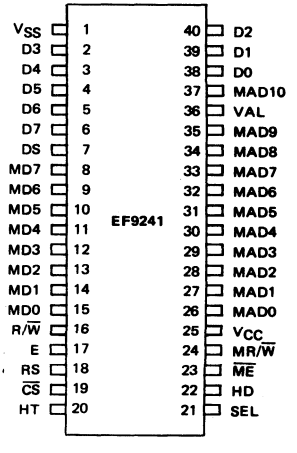
(N-CHANNEL, SILICON-GATE DEPLETION LOAD)

BROADCASTED DATA DEMULTIPLEXOR

CASE CB-182



PIN ASSIGNMENT



PP8301-A 1/2

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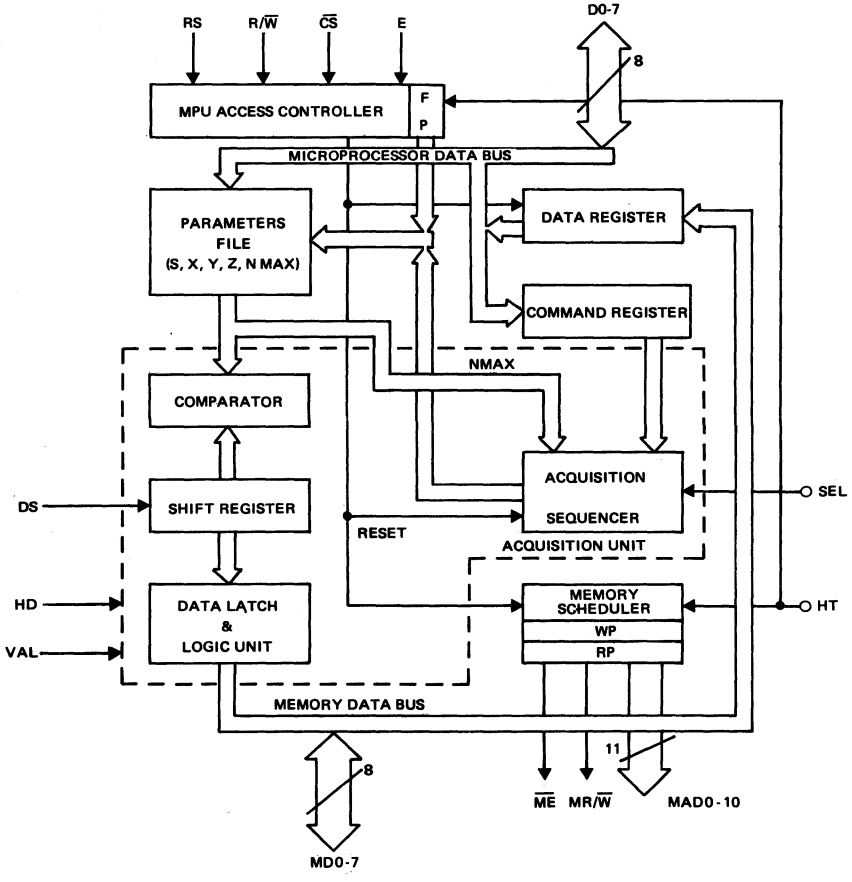


EF9241 INTERNAL STRUCTURE

THOMSON SEMICONDUCTORS

EF9340
EF9341

ADVANCE INFORMATION

SEMI-GRAPHIC CRT DISPLAY PROCESSOR

Two 40 pin circuits EF9340 (VIN) and EF9341 (GEN) and 16 K bits of standard static RAM are enough to build a complete semi-graphic display unit :

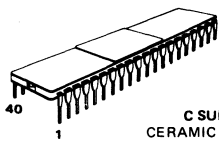
- Simple, low cost yet flexible, asynchronous interface with microprocessor
- Display of 25 or 21 rows of 40 characters
- On chip (GEN) 128 alphanumeric and 128 semi graphic character generator
- Easy extension up to 2 additional sets of 96 characters each
- One colour, double height, double width, negative (alphanumeric) or two colours (semi-graphic) and blinking are provided as parallel attributes
- Conceal, boxing, underlining as serial attributes
- Programmable roll up, roll down, zoom, and cursor display
- 50 Hz/60 Hz operation
- On chip R, G, B shift registers (VIN)
- Half dot frequency (3.5 MHz) clock input
- Vertical synchronization input
- Single +5 Volt supply
- TTL/MOS compatible I/O

MOS

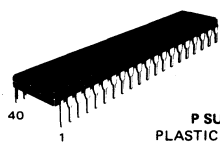
(N-CHANNEL, SILICON GATE)

SEMI-GRAPHIC CRT DISPLAY PROCESSOR

CASE CB-182

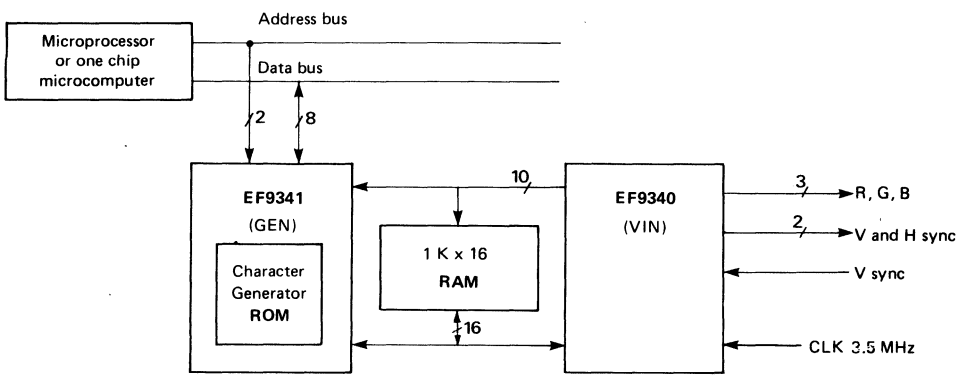


C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE

FIGURE 1 – TYPICAL DISPLAY UNIT



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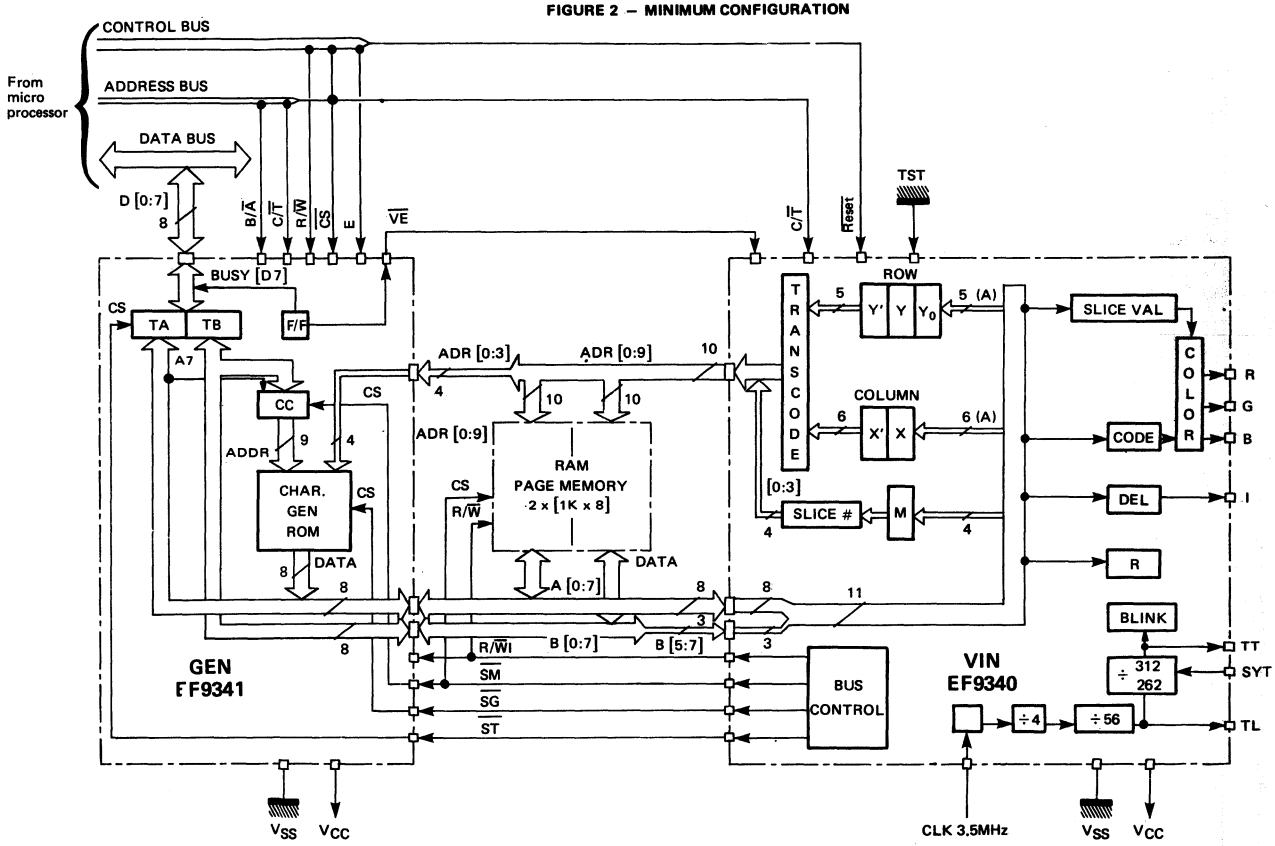
THOMSON COMPONENTS

FIGURE 2 – MINIMUM CONFIGURATION



GENERAL OPERATION DESCRIPTION

The display unit is organized around a 16 bit internal bus (fig.2) controlled by VIN. GEN contains a character generator and two 8 bit registers – TA and TB – which provide a buffered interface with a general purpose 8 bit bus. The display unit receives data and commands through these registers which perform as a mail box. VIN contains a Timing Generator, a Display Automaton and an Access Automaton.

TIMING GENERATOR

It divides the clock input at half the dot frequency (3.5 MHz) by 4 to get the window frequency. This frequency is divided to get the line frequency and the frame frequency. The size of a character being programmable, it occupies 1, 2 or 4 windows on the screen. Each window is 10 TV lines high and 8 dots wide. Timing Generator gives control over the bus to the display automaton for 40 window periods per line and 250 (or 210) lines per frame. Access automaton has control over the internal bus for the remaining time.

DISPLAY AUTOMATON

During each displayable window period ($\simeq$ 1.1 μs), the display automaton controls two read cycles on the internal bus.

On the first cycle, a window code (16 bits) is read from the page memory (table 1). Attribute field (7 bits) and character type field (4 bits) are latched in VIN.
Character code field (9 bits) is latched in CC registers.
Then window address register is incremented.
On the second cycle, address bus gives the slice number (0 – 9) to the character generator and a slice of 8 dots is read. Then Display Automaton delivers R, G, B signals and I (boxing command).
A set of 128 alphanumeric characters and a set of 128 standard semi-graphic characters are provided by GEN. Further extension is easily done using standard (1k x 8) ROM or RAM components (fig. 8).

ACCESS AUTOMATON

When TA register and then TB register of the mail box are written from the main bus with $C/\overline{T} = 1$, Access Automaton knows that a command is pending.
As soon as it gets control over the internal bus, it reads the mail box and gets the command.
A command may be :

- A cursor modification
- A display mode (ON/OFF, Roll up, etc...)
- A data transfer mode (Read/Write Page Memory, Read/Write Character Generator)

Data transfers are executed through the mail box addressed with $C/\overline{T} = 0$ and according to the current Data Transfer Mode.

The busy flip-flop gives the status of the mail box. It can be read in the MSB of the TA byte addressed with $C/\overline{T} = 1$.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} *	−0.3 to+ 7.0	Vdc
Input Voltage	V_{in} *	−0.3 to 7 V	Vdc
Operating Temperature Range	T_A	0 to+ 70	°C
Storage Temperature Range	T_{stg}	−55 to+ 150	°C
Max Power Dissipation	P_{DM}	0.75	W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

* With respect to V_{SS}

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage		V_{IL}	−0.3	–	0.8	Vdc
Input High Voltage (except SYT and CLK)		V_{IH}	2.2	–	V_{CC}	Vdc
Input Hith Voltage SYT and CLK		V_{IH}	3	–	V_{CC}	Vdc
Three State and Input Leakage current (except CLK)		I_{in}	–	–	10	µA
CLK input current	V_{IN} = 0.4 V	I_{IL}	–	–	−2	mA
Output High Voltage						
I_{load} = −150 µA	R, G, B, I	V_{OH}	2.4	–	–	V
I_{load} = −500 µA	Other outputs					
Output Low Voltage						
I_{load} = 0.4 mA	R, G, B, I	V_{OL}	–	–	0.4	V
I_{load} = 1.6 mA	Other outputs					
Power Dissipation						
VIN		P_D	–	200	–	mW
GEN				250		
Input Capacitance		C_{in}	–	–	10	pF

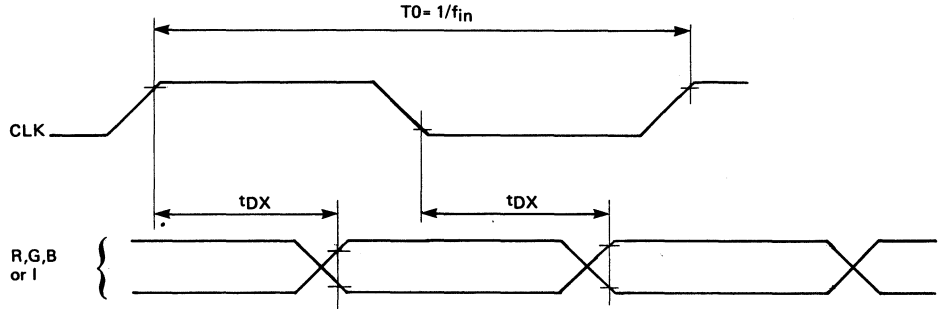
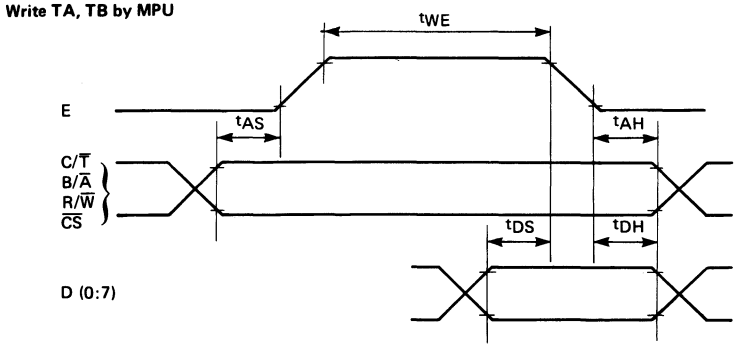


FIGURE 3 – R, G, B and I TIMING (VIN)

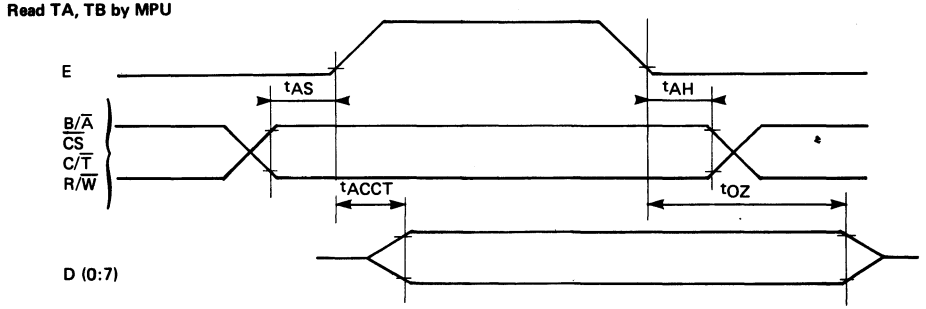
CLOCK R, G, B AND I TIMING CHARACTERISTICS (V_{CC} = 5.0 ± 5 %, V_{SS} 0, T_A = 0 – 70° C, CL = 70 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock frequency	f_{in}	3.4	–	3.6	MHz
R, G, B or I delay time from clock edge	t_{DX}	–	–	130	ns
R, G, B and I relative delay		–	5	–	ns

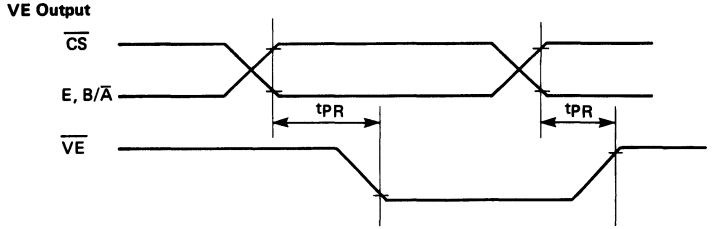
Write TA, TB by MPU



Read TA, TB by MPU



$\overline{VE}$ Output



Reference level : Input 0.8 and 2.2 V
Output 0.4 and 2.4 V

FIGURE 4 – PROCESSOR BUS TIMING CHART (GEN)

PROCESSOR BUS TIMING CHARACTERISTICS

(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70° C – C_L = 100 pF on all outputs

Characteristic	Symbol	Min	Typ	Max	Unit
Enable pulse duration	t_{WE}	200	—	—	ns
Address setup time	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	0	—	—	ns
Data setup time	t_{DS}	140	—	—	ns
Data hold time	t_{DH}	10	—	—	ns
T_A, T_B access time	t_{ACCT}	—	—	200	ns
Data off time	t_{OZ}	0	—	—	ns
$\overline{VE}$ delay time ($\overline{CS}$ = 0 ; E = B/$\overline{A}$ = 1)	t_{PR}	—	—	140	ns

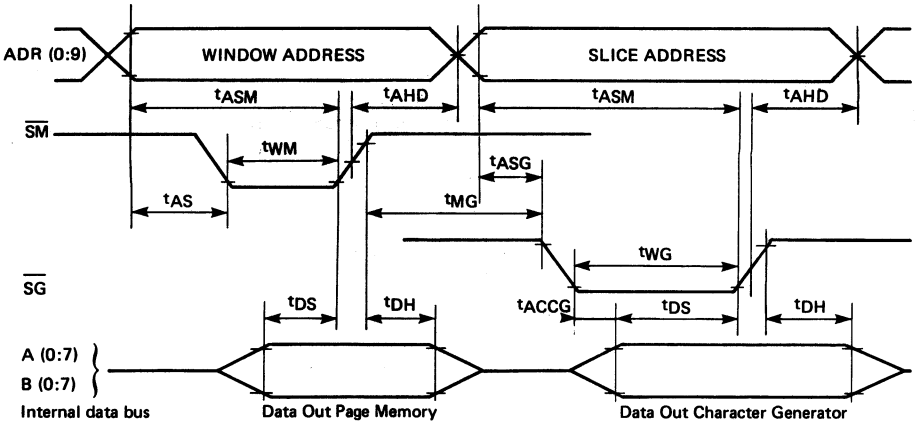


FIGURE 5 – INTERNAL BUS - DISPLAY READ CYCLES – TIMING CHART (R/$\overline{WI}$= 1)

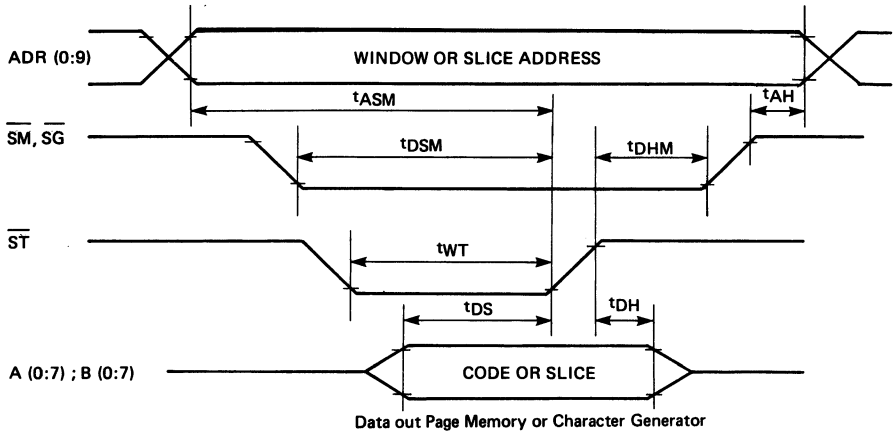


FIGURE 6 – INTERNAL BUS – FROM PAGE MEMORY OR CHARACTER GENERATOR TO MAIL BOX TRANSFER CYCLES (R/$\overline{WI}$= 1)

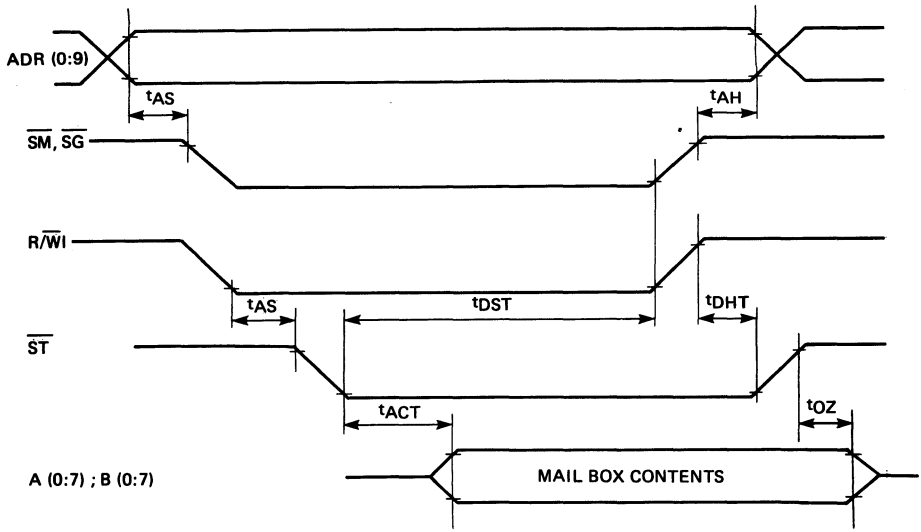


FIGURE 7 – INTERNAL BUS – FROM MAIL BOX TO PAGE MEMORY OR CHARACTER GENERATOR OR VIN TRANSFER CYCLES

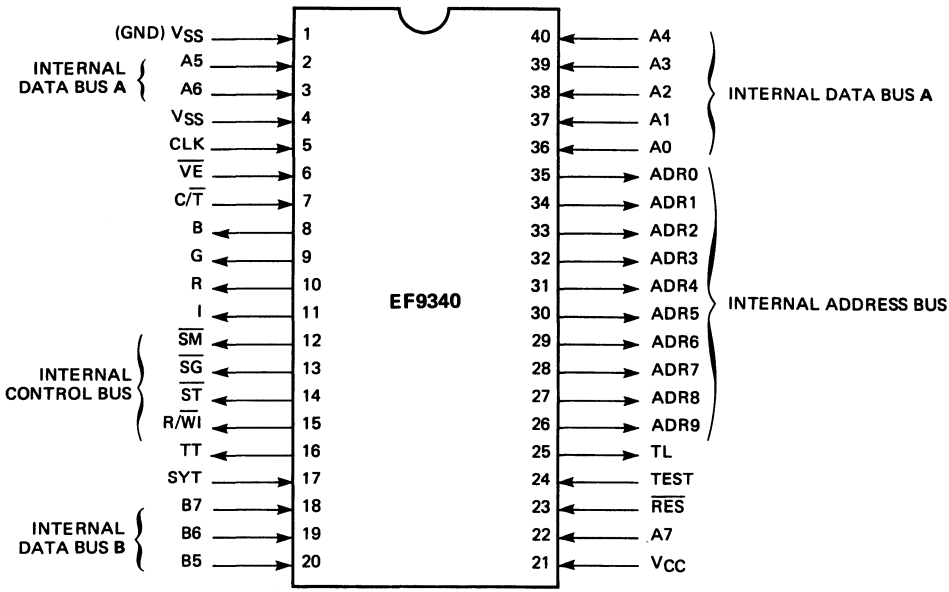
INTERNAL BUS TIMING CHARACTERISTICS

(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70° C, C_L = 100 pF on all outputs, f_{in} = 3.5 MHz)

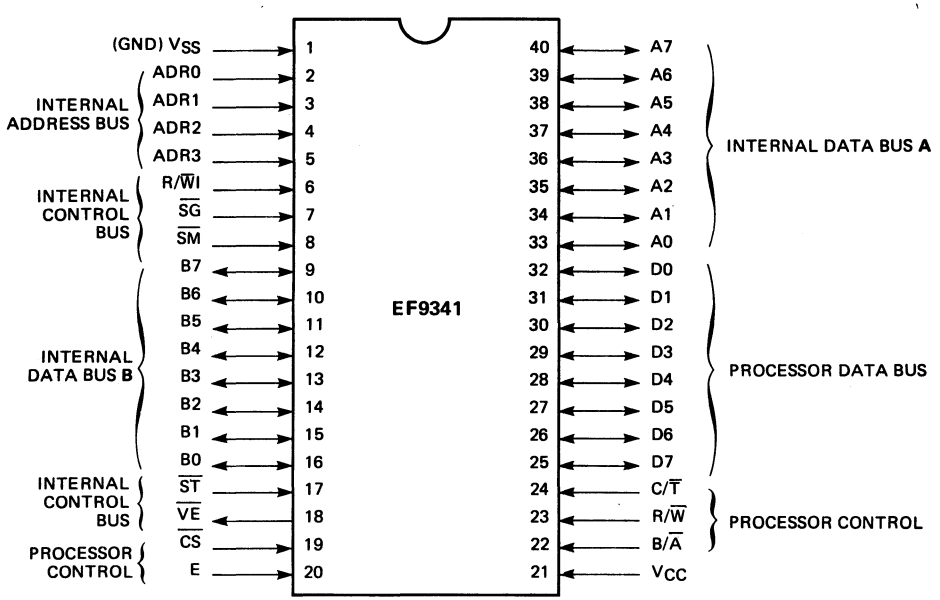
Characteristic	Symbol	Min	Typ	Max	Unit
Address setup time	t_{ASM}	460	–	–	ns
Address hold time	t_{AH}	0	–	–	ns
Strobe duration (display cycles)	t_{WM}	300	–	–	ns
	t_{WG}	380	–	–	ns
Address hold time (display cycles) (Ref. 1.5 V for $\overline{SM}$, $\overline{SG}$, ADR)	t_{AHD}	0	0	–	ns
Address to strobe	t_{ASG}	40	–	–	ns
Data setup time	t_{DS}	140	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Precharge Character Generator (in GEN)	t_{MG}	60	–	–	ns
Access to Character Generator (in GEN)	t_{ACCG}	–	–	240	ns
From $\overline{SM}$ or $\overline{SG}$ to $\overline{ST}$	t_{DSM}	400	–	–	ns
$\overline{SM}$ or $\overline{SG}$ hold time	t_{DHM}	0	–	–	ns
Write Mail Box strobe duration	t_{WT}	250	–	–	ns
Write setup time	t_{AS}	40	–	–	ns
From $\overline{ST}$ to $\overline{SM}$ or $\overline{SG}$	t_{DST}	350	–	–	ns
Access time to Mail Box (in GEN)	t_{ACT}	–	–	200	ns
$\overline{ST}$ hold time	t_{DHT}	60	–	–	ns
Mail Box off time	t_{OZ}	0	–	270	ns

Reference level : 0.8 V and 2 V on any input
0.4 V and 2.4 V on any output
} unless otherwise specified.

VIN PIN ASSIGNMENT



GEN PIN ASSIGNMENT



VIN SIGNAL DESCRIPTION

VIN controls several types of data transfers on the internal bus.
- From the mail box to VIN
- From the Page Memory to VIN
- From the Character Generator to VIN
- Between Mail Box and Page Memory
- Between Mail Box and Character Generator

VIN delivers R, G, B and synchronization signals to the CRT.

INTERNAL BUS INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
A(0:7) B(5:7)	I I	36, 37 38, 39 40, 2 3, 22 20-18	Internal data bus	VIN gets only eleven inputs out of the sixteen lines of the bidirectional internal data bus.
ADR(0:9)	O	35-26	Internal address bus	These ten TTL compatible outputs multiplex the page memory address with the slice number – ADR(0:3) – and the selection of an external character generator – ADR4.
R/$\overline{W}$I	O	15	Read/Write on Internal Bus	This TTL compatible output determines whether the page memory or the character generator gets read or written. A write is active low ("0").
$\overline{SM}$	O	12	Memory strobe	This TTL compatible output, when active, selects the page memory as source (R/$\overline{W}$I high) or destination (R/$\overline{W}$I low) on the internal bus. When $\overline{SM}$ goes active (low), ADR(0:9) and R/$\overline{W}$I are stable.
$\overline{SG}$	O	13	Character generator strobe	This TTL compatible output, when active, selects a character generator as source (R/$\overline{W}$I high) or destination (R/$\overline{W}$I low) on the internal bus. When $\overline{SG}$ goes active (low), ADR(0:4) and R/$\overline{W}$I are stable. $\overline{SM}$ and $\overline{SG}$ are never active at the same time.
$\overline{ST}$	O	14	Mail box strobe	This TTL compatible output, when active, selects the mail box as source (R/$\overline{W}$I low) or destination (R/$\overline{W}$I high) on the internal bus. $\overline{ST}$ may be active (low) at the same time as $\overline{SM}$ or $\overline{SG}$.

VIDEO INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
R G B	O	10 9 8	Red Green Blue	These three TTL/LS compatible outputs deliver the video signal. They are low during the vertical and horizontal blanking intervals.
TT	O	16	Vertical synchronization	This TTL compatible output is active (low) for two lines each field period. The field period is programmable at 262 lines (60 Hz) or 312 lines (50 Hz).
TL	O	25	Horizontal synchronization	This TTL compatible output is at line frequency. It can be programmed active low for 4 window periods (for composite signal generation) or active high for 16 window periods (to directly drive a monitor).
I	O	11	Boxing command	This TTL/LS compatible output is active high. I allows to insert R,G,B in an external video signal for captioning purposes, for example.
SYT	I	17	Vertical synchronization input	This high impedance, high noise margin input is internally sampled and memorized on the 12 th window period of each line. When the memorized signal goes from high to low, the line count is reset at the end of the present line. This input allows to vertically synchronize VIN on an external composite or AC line signal. This input should be grounded if not used.

OTHER PINS

V_{SS}	I	4		This input has to be grounded.
CLK	I	5	Clock input	External TTL clock input. (nominal value : 3.5 MHz)
$\overline{VE}$	I	6	VIN select	This TTL/MOS high impedance input must be wired to the corresponding GEN output. This input is active (low) each time the TB register of the mail box is accessed by the microprocessor.
$C/\overline{T}$	I	7	Command or transfer select	This TTL/MOS high impedance input determines whether a command ($C/\overline{T}$ high) or data ($C/\overline{T}$ low) is accessed by the processor in the mail box. $C/\overline{T}$ is latched on the falling edge of $\overline{VE}$ and the request is memorized.
$\overline{RES}$	I	23	Restart	When this TTL/MOS high impedance input goes low, the TL output goes high and remains in this state until the display mode register is loaded.
TST	I	24	Test	This pin must be grounded for normal operation.
V_{CC}	S	21	Power supply	+5 V
GND	S	1	Power supply	Ground.

GEN SIGNAL DESCRIPTION

GEN takes place in the video display unit between the internal 16 bit bus controlled by VIN and a general purpose 8 bit bus controlled by a processor. GEN contains :

- A character generator with 128 alphanumeric characters and 128 semigraphic characters.
- Two 8 bit registers - TA and TB - which perform as a mail box between the two buses.

PROCESSOR INTERFACE

GEN interfaces to a processor bus on the bidirectional data bus D (0:7) using $\overline{CS}$, B/$\overline{A}$, C/$\overline{T}$, $\overline{E}$ and R/$\overline{W}$ as control signals.

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
D(0:7)	I/O	32-25	Data bus	The bidirectional data lines D(0:7) allow command and data transfers between the GEN internal mail box and the processor. Data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a display unit read operation. A high level on a data pin is a logical "1".
E	I	20	Enable	The enable signal is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the mail box. This signal is usually derived from the processor clock.
$\overline{CS}$	I	19	Chip select	The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the display unit, when low, to read or write the internal mail box.
R/$\overline{W}$	I	23	Read/Write	This high impedance TTL/MOS compatible input determines whether the internal mail box gets written or read. A write is active low ("0").
B/$\overline{A}$	I	22	Register TA or TB select	This high impedance TTL/MOS compatible input selects either the TA register (B/$\overline{A}$ = 0) or the TB register (B/$\overline{A}$ = 1) of the mail box.
C/$\overline{T}$	I	24	Command or data transfer select	This high impedance TTL/MOS compatible input defines the contents of the mail box either as a command ($\overline{CT}$ = 1) or as a data transfer (C/$\overline{T}$ = 0). The C/$\overline{T}$ input of GEN and the C/$\overline{T}$ input of VIN must be wired together for correct operations.

VIN INTERFACE

NAME	PIN TYPE	N°	FUNCTION*	DESCRIPTION
$\overline{VE}$	O	18	VIN select	This TTL compatible output must be wired to the corresponding VIN input. This signal goes active (low) when the TB register is accessed by the processor.
A(0:7) B(0:7)	I/O	33-40 16-9	Internal data bus	These 16 bidirectional data lines allow data transfers between GEN, VIN and memory.
R/$\overline{WI}$ $\overline{SM}$ $\overline{SG}$ $\overline{ST}$	I	6 7 8 17	Control signals from VIN	These inputs must be wired to the corresponding VIN outputs.
ADR(0:3)	I	2-5	Slice address	These four inputs must be wired to the corresponding four outputs of VIN. When $\overline{SG}$ is active, they are stable and determine the BCD address of a character slice in the character generator.
V_{CC}	S	21	Power supply	+5 V
V_{SS}	S	1	Power supply	Ground.

MICROPROCESSOR INTERFACE

The complete display unit is accessed by the processor through 4 addresses when $\overline{CS}$ is low and E is high.

ADDRESS		ADDRESSED REGISTER		
C/$\overline{T}$	B/$\overline{A}$	R/$\overline{W}$ = 1 Read	R/$\overline{W}$ = 0 Write	Comments
0	0	TA	TA	A 16 bit data is read or written from/into the mail box
0	1	TB (1)	TB (1)	
1	0	Busy (2)	TA	A 16 bit command is written in the mail box or the busy flip-flop is read (4).
1	1	– (3)	TB (1)	

(1) Sets the busy flip-flop and activates $\overline{VE}$.
(2) Busy is read MSB on the MPU bus (D7). Other bits are don't care.
(3) Illegal operation.
(4) A valid command should be loaded at least 64 µs after power on or RESET without testing busy to reset it.

COMMAND – (C/$\overline{T}$ = 1)

When the mail box is written with a command, the busy flip-flop is set and GEN activates $\overline{VE}$. A Read command request ($\overline{VE}$ low and C/$\overline{T}$ high) is memorized by the access automaton of VIN. As soon as the access automaton takes control over the internal bus, it reads the command in the mail box ; this resets the busy flip-flop. 11 bits only out of the 16 bits of the command are read :

B (5:7) give the address of the register or the operation to perform.
A (0:7) give a parameter.
4 registers may be modified by a command :
the Cursor Register C, the Origin Register Y0, the Access Mode Register M and the Display and Timing Mode Register R.

COMMAND CODE																NAME	OPERATION
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	0									K (0 : 4)					Begin Row	X (0 : 5) ← 0 Y (0 : 4) ← K (0 : 4)
0	0	1								K (0 : 4)						Load Y	Y (0 : 4) ← K (0 : 4)
0	1	0								K (0 : 5)						Load X	X (0 : 5) ← K (0 : 5)
0	1	1														INC C	C ← C+1
1	0	0						K (0 : 7)								Load M	M (0 : 7) ← K (0 : 7)
1	0	1						K (0 : 7)								Load R	R (0 : 7) ← K (0 : 7)
1	1	0								K (0 : 5)						Load Y0	Y0 (0 : 5) ← K (0 : 5)
1	1	1															Not interpreted

The first 4 commands allow cursor handling :

- Initialization at the beginning of a row
- Vertical movement
- Horizontal movement
- Incrementation

DISPLAY AND TIMING MODE REGISTER R(0:7)

R(0:7) is an 8-bit register.
This register is loaded through a LOAD R command.
The 6 bits R(0:4) and R7 define the display modes.
The 2 bits R(5:6) define the timing modes.

Bit 0 : When R0 = 0, the display automaton is disabled. R, G, B and I outputs stay low.
When R0 = 1, the display automaton is enabled. When the display automaton is disabled, loading the R register with R0 = 1 may alter the page memory contents if not done during the vertical blanking intervals.

Bit 1 : When R1 = 0, the boxing attribute is disabled. I stays high, during the display periods.
When R1 = 1, the boxing attribute is enabled. R, G, B and I outputs are low out of the boxing zone. I is high in the boxing zone.
The CRT and VIN are supposed to be synchronized by a composite external video signal. I switches the boxed windows on the screen.

Bit 2 : When R2 = 0, the conceal attribute is disabled.
When R2 = 1, the conceal attribute is enabled.

Bit 3 : When R3 = 1, the service row is displayed at the top of the screen.
When R3 = 0, it is concealed.

R0	R1	Condition	I	R G B
0	–	–	0	Black
1	0	–	–	–
1	1	In boxing zone	1	–
1	1	Outside boxing zone	0	Black

Bit 4 : When R4 = 1, the cursor position is displayed. The character in the window alternates between normal and reverse video at blinking frequency. When blinking is disabled (R7 = 0), it is permanently reversed.
When R4 = 0, the cursor position is not displayed.

Bit 5 : When R5 = 0, TL is active low during 4 window periods.
When R5 = 1, TL is active high during 16 window periods.

Bit 6 : When R6 = 0, TT period is 262 lines (60 Hz).
When R6 = 1, TT period is 312 lines (≃ 50 Hz).

Bit 7 : When R7 = 0, blinking is disabled.
When R7 = 1, blinking is enabled.

CURSOR REGISTER C

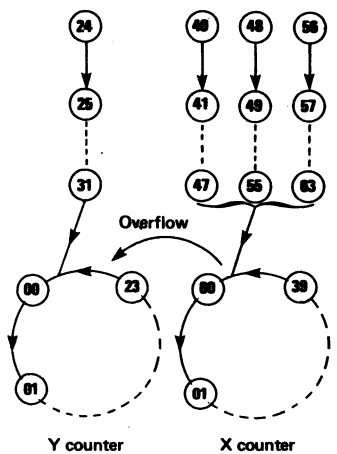
The cursor register C points to the page memory. It is subdivided into two counters X and Y :

X(0:5) points to a column. The decimal value of X comes from 00 to 39 when columns are addressed from left to right.

Y(0:4) points to a row. The decimal address of the service row is 31. The other rows are addressed from 00 to 23.

When the cursor is incremented, X is incremented. When X overflows, Y is automatically incremented as shown in the state diagram below.

Nota : the 11 bits of X and Y are transcoded to get a 10 bit binary address in the page memory.



STATE DIAGRAM

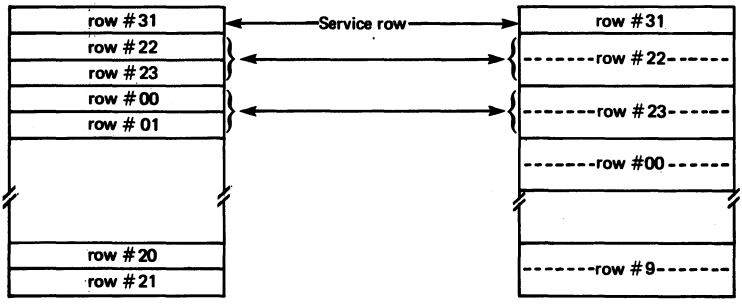
$Y_4 Y_3$		ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
00	X5 = 0	Y4	Y3	Y2	Y1	Y0	X4	X3	X2	X1	X0
10											
01	X5 = 1	1	1	Y2	Y1	Y0	Y4	Y3	X2	X1	X0
11	–	1	1	X5	X4	X3	1	1	X2	X1	X0

ORIGIN REGISTER Y0(0:5)

Y0(0:5) is a 6 bit register.
This register is loaded through a LOAD Y0 command.

Bit 0 to 4 : Y0 (0:4) give the number of the first row displayed directly after the service row.
A circular roll up or roll down may be commanded by incrementing or decrementing modulo 24 the value of Y0(0:4).

Bit 5 : Y0(5) = 1 sets the zoom mode : the first 12 rows are displayed in double height. If a character was already displayed in double height, it is now in quadruple height. The service row is always displayed in single height.
Y0(5) = 0 resets the zoom mode.



No zoom mode
First displayed row = 22

Zoom mode
First displayed row = 22

ACCESS MODE REGISTER M(0:7)

M(0:7) is an 8 bit register.
This register is loaded through a LOAD M command.
Subsequent data transfers are executed according to the current access mode (see "Data transfer".)

ACCESS MODE REG.								ACCESS MODE	SUBSEQUENT DATA TRANSFER
M7	M6	M5	M4	M3	M2	M1	M0		
0	0	0						Write	MP (C) ← T ; C ← C+1
0	0	1						Read	T ← MP (C) ; C ← C+1
0	1	0						Write without INC	MP (C) ← T
0	1	1						Read without INC	T ← MP (C)
1	0	0		N T				Write slice	GC (MP(C), NT) ← T ; NT ← NT+1
1	0	1		N T				Read slice	T ← GC (MP(C), NT) ; NT ← NT+1
1	1							Illegal	

NT : Slice number T : Mail Box C : Cursor MP : Page Memory GC : Character Generator

DATA TRANSFERS (C/$\overline{T}$ = 0)

When the mail box is written or read with C/$\overline{T}$ = 0, the busy flip flop is set and GEN activates $\overline{VE}$. A data transfer request is memorized by the access automaton of VIN. As soon as the access automaton takes control over the internal bus, it executes the request according to the contents of the M register.
M(0 : 3) is a modulo 10 counter referred to as NT (slice number)
M(5:7) defines an access mode (see table 3).

WRITE

It is the most commonly used data transfer : the contents of the mail box is written into the page memory location addressed by the cursor. Then the cursor is incremented.

READ

The page memory location addressed by the cursor is written into the mail box.
Then the cursor is incremented.
These two modes give sequential access to the page memory.

WRITE, READ WITHOUT INCREMENTATION

Same as above but the cursor is not incremented.

WRITE SLICE

This mode is used to load a RAM used as extended character generator.

The execution takes two cycles :

- A read without incrementation cycle is performed on the page memory. The character code is latched in the extended character code register. A7, B(5:7) are latched in VIN.
- The contents of the TA register of the mail box is written into the character generator. The address is given by the extended character code register and the contents of NT, which is sent on ADR(0:3). The extension condition B7 ∧ (B5 ∨ B6) is sent on ADR4. Then NT is incremented modulo 10.

READ SLICE

This mode is used to read a slice in any character generator.

The execution takes 2 cycles :

- The first cycle is identical to the first cycle of WRITE SLICE.
- On the second cycle, a character 8-bit slice is written into the mail box.

NOTA :

1. In READ or WRITE SLICE mode, the character code address is indirectly given by the cursor. The page memory must have been previously initialized.
2. **The first data transfer following the loading of any READ mode into the M register is triggered by a mail box read by the microprocessor. Consequently these first data are invalid.**
3. Any access of the mail box by the internal bus resets the busy flip flop. If the display is disabled, then the busy flip flop remains set for a maximum of 4 window periods, otherwise a maximum of 44 window periods.

TIMING GENERATOR AND INTERNAL BUS CYCLES

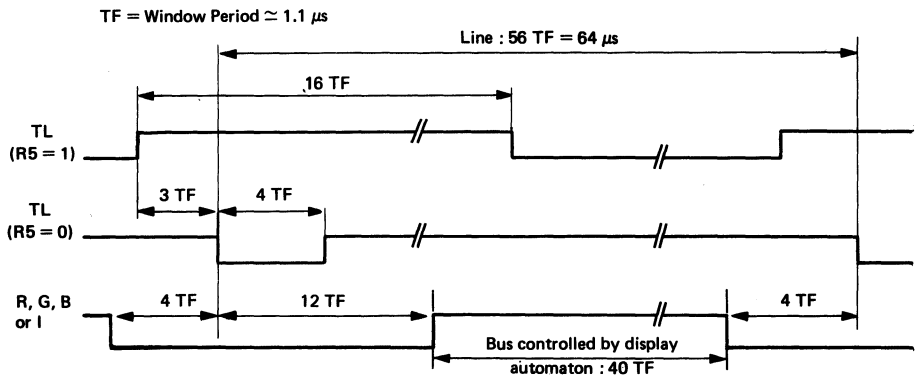
LINES AND FRAME

The input clock is at half the dot frequency (3.5 MHz). 8 dot periods (4 clock periods) make a window period. 56 window periods make a line period (≃ 64 µs).

TL output is at line frequency. The duration of TL is programmable through R5 (Display and Timing Generator Mode Register).

With R5 = 0, TL output is at "0" (low level) for 4 window periods (≃ 4.5 µs).

With R5 = 1 (Monitor Mode), TL output is at "1" (high level) for 16 window periods (18.3 µs). In this mode, TL may directly drive the horizontal deflection circuitry. To protect the Darlington from overloading, the TL output is set to "1" when a low level is applied on $\overline{RES}$ and remains in this state until reception of a LOAD R command.



262 line periods (if R6 = 0) or 312 line periods (if R6 = 1) make a frame period. The TT output is at frame period (60 Hz/50 Hz) and is low during 2 lines. SYT input resets the line count inside the frame : this input is triggered, then sampled when the 12th window of each line occurs. When the sample transits from 1 to 0, the line count will be reset on the next TL.

TIME SHARING OF THE BUS

When the display is enabled (R0 = 1), the timing generator gives control over the bus to the display automaton from the 40th line after TT to the 290th (if R6 = 1) or from the 32nd line to the 242nd (R6 = 0) and from the 13th to the 53rd window period of each line.

When the display is disabled (R0 = 0), the access automaton keeps control over the bus.

READING WINDOW CODES AND CHARACTER SLICES

During each displayable window period (≃ 1.1 µs), the display automaton controls two read cycles on the internal bus.

On the first cycle, ADR(0:9) address a window code in the page memory.

The page memory is strobed by $\overline{SM}$ and a 16 bit window code is read (table 1).

The 11 bits of the attribute field A (0 : 6) and type field, A7, B(5 : 7) are latched in the display automaton.

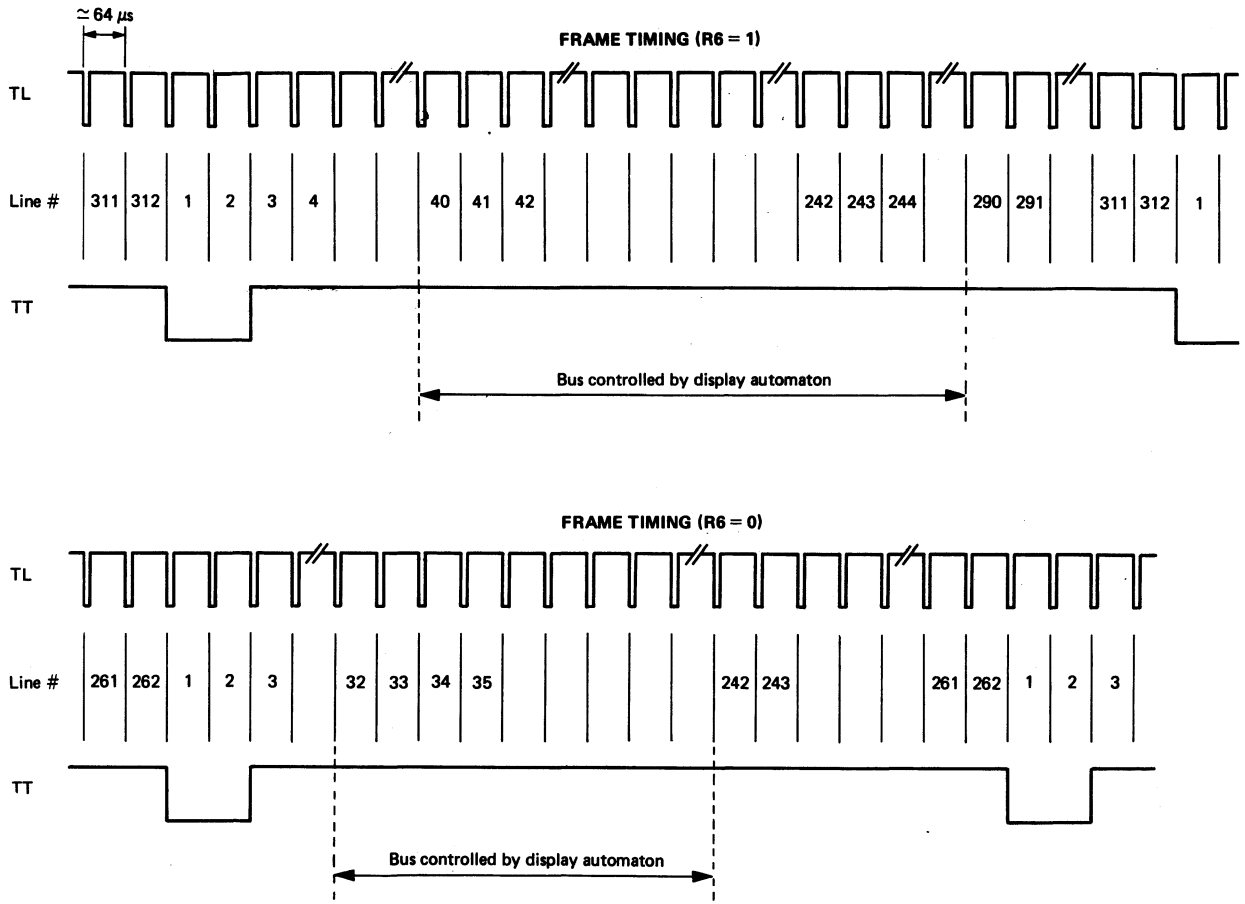
The 9 bits of the character code field A7, B(0 : 7) are latched in CC registers of the character generator.

CC register addresses one set of character and one character in the set.

A character is 10 slices of 8 bits each.

On the second cycle the slice number is given by ADR(0:3) and the extension select by ADR4. The character generator is strobed by $\overline{SG}$ and the value of the slice is read by the display automaton on the internal A(0:7) bus.

When a delimitor is addressed by CC, its contents is read in place of the value of the slice.


≃ 64 µs
FRAME TIMING (R6 = 1)
TL
Line #
311 312 1 2 3 4 40 41 42 242 243 244 290 291 311 312 1
TT
Bus controlled by display automaton
FRAME TIMING (R6 = 0)
TL
Line #
261 262 1 2 3 32 33 34 35 242 243 261 262 1 2 3
TT
Bus controlled by display automaton

INTERNAL BUS CYCLES

The different types of internal bus cycles are given in the table below :

CONTROL				ADDRESS BUS AD (0 : 9)	DATA BUS A(0:7), B(0:7)	CYCLE TYPE
R/$\overline{W}$I	$\overline{SM}$	$\overline{SG}$	$\overline{ST}$			
Read	Active			WINDOW ADDRESS (X', Y') or CURSOR (X, Y)	MP→ VIN, MP→ CC	1
Read		Active		SLICE ADDRESS (NT')	GC or CC→ VIN	2
Write			Active	–	T→VIN	3
Read	Active		Active	CURSOR (X, Y)	MP→T	4
Write	Active		Active	CURSOR (X, Y)	T→MP	5
Read		Active	Active	SLICE ADDRESS (NT)	GC→T	6
Write		Active	Active	SLICE ADDRESS (NT)	T→GC	7

MP : Page Memory T : Mail Box GC : Character Generator CC : Character Code Register

1, 2 : Used by display automaton
3 : Load command in access automaton
4 : Read MP
5 : Write MP
6 : Read Slice
7 : Write Slice

} Controlled by access automaton

NOTA :
In cycle type 2, slice address is at ADR(0:3).
ADR4 gives the extension condition B7 ∧ (B5 ∨ B6) which has been latched on the previous type 1 cycle.
ADR(5:9) are not used.

In cycle types 6 and 7, slice address is at ADR(0:3). ADR4 gives the extension condition B7 ∧ (B5 ∨ B6) which has been latched on the previous type 1 cycle (with cursor address).

In cycle types 4 to 7, two strobes are simultaneously active. When a memory is read, T is written and reciprocally.

CHARACTER ATTRIBUTES

SERIAL ATTRIBUTES, PARALLEL ATTRIBUTES

The shape to be displayed in a window is defined by :
- a pattern held in the character generators and addressed by the CC field of the window code.
- the actual value of the attributes.

The attributes are :
- C_0 (3 bits) and C_1 (3 bits) : 2 colours
- Blinking (1)
- Double height (1) , Double width (1)
- Reverse video (1)
- Boxing (1)
- Conceal (1)
- Underlining (1)

In any column 0 window, their implicit value is Co = black, not boxed, not concealed, not underlined. The window code defines the type of the character to be displayed in this window and the value of its parallel attributes (see table 1). The value of the remaining attributes is serially defined by scanning the windows from left to right (column 0 to 39) then up to down. Therefore, any other type of character gives the values of C_0 for a subsequent string of alphanumerics. Besides, a delimitor gives the value of the boxing, conceal and underlining attributes for the following windows. A boxing zone is a string of windows belonging to the same row, in which the boxing attribute value is 1.

DOUBLE HEIGHT, DOUBLE WIDTH

- A correct operation assumes that the same window code had been repeated in the page memory (twice for double height or double width, four times for double size).

- No double height windows are supposed to be held in service row.

- No double width character should begin in column 39.

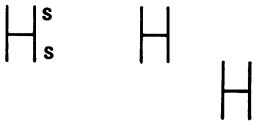
- Single sized, double width, double height and double sized characters may be mixed on a given row.

- But couple of rows bearing double height character should not be interleaved :

More precisely, this attribute defines a H parity for each row :

- service row is H even
- any row is H even if the preceding row does not hold any double height window.
- any row has an H parity reverse to the preceding row if the latter holds at least one double height window.

In the same way, double width define a W parity for the windows as double height for the rows.



legal Illegal

DISPLAY OF NON DELIMITOR TYPES OF CHARACTERS

The display automaton interprets the attributes in the following order :

Underlining

- type α : slice 9 is set in the pattern.

Blinking

- blinking : the pattern is periodically (0.5 Hz) reset. If the video is reversed (α type only), the phase of the blinking clock is complemented. In "cursor" position, the reset does not occur.

Reverse video — Cursor position

- reverse video : (α only). The pattern is complemented.
- cursor position : (any type). The pattern is periodically complemented. If blinking is disabled (R7 = 0), the pattern is permanently complemented.

Double height, double width (α only)

- double width : each bit of the pattern is horizontally doubled so as to get a 10 x 16 double pattern. If the window is W even, only the left pattern is kept. The right pattern is kept if the window is W odd.

- double height : the slices of the pattern are repeated so as to get a 20 x 8 double pattern. If the row is H even, the upper pattern is kept, otherwise lower pattern is kept.
  The double pattern is obtained by :

  – tripling slice 0
  – doubling slice 1 to 8
  – keeping slice 9

  Double height and double width may be combined to get a double size.

Colors

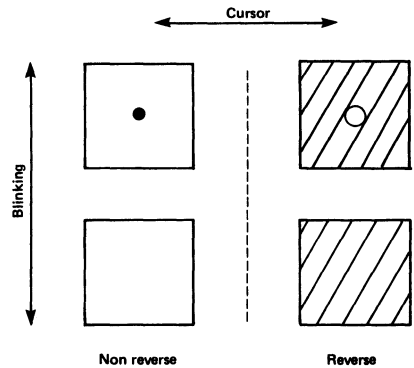
Each bit of the final 10 x 8 pattern corresponds to a pixel.

The color of the pixel is C_0 if the bit value is 0. Otherwise, it is C_1.

Boxing, conceal

If the conceal is enabled (R2 = 1), and if the window is in a conceal zone, then the colors in the window are reset to black.

If the boxing is enabled (R1 = 1), and if the window is out of a boxing zone, the color resets to black in the window and I output is low. The window is "transparent".



Non Reverse and reverse character display with blinking or in cursor position.

DISPLAY OF DELIMITORS

In the 10 x 8 implicit pattern associated with a delimitor, all the bits have the same value : 1.

"cursor" position : the pattern is periodically reset.

colors : same as any other type : a delimitor is displayed as a space in color C_1.

boxing : if the boxing is enabled (R5 = 1), and if the delimitor defines a boxing zone border, half of the window is transparent. Out of boxing zone, a delimitor is completely transparent.

Remark : the value of the lining and the conceal bits given by a delimitor is ignored in the window associated with this delimitor.

CHARACTER GENERATORS

GEN contains a CC register ; a standard 128 character α_0 set and a standard 128 semi graphic γ set.

Further extension of these character sets is easily done by adding 1 K x 8 standard ROM or RAM components (fig 8).

A latch CCE is loaded by the character code with $\overline{SM}$.

A quad 2 to 1 multiplexer transcodes 11 bits of logical address. – 96 character codes CCE (0 : 6) by 10 slice address codes ADR(0:3) – to 10 bits of physical address.

Logical Address

ADR3=0	CCE6	CCE5	CCE4	CCE3	CCE2	CCE1	CCE0	ADR2	ADR1	ADR0
ADR3=1	0	0	CCE4	CCE3	CCE2	CCE1	CCE0	CCE6	CCE5	ADR0

The external character generator is selected by ADR4 high and $\overline{SG}$ low. It is read or written whether R/$\overline{W}$I is high or low.

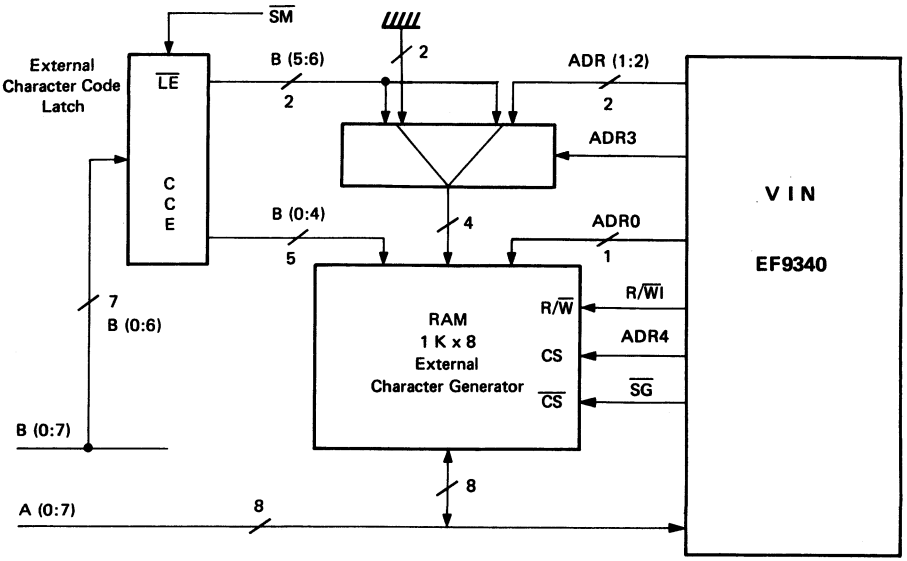


FIGURE 8 – ADDING AN EXTERNAL CHARACTER GENERATOR

TABLE 1 — CHARACTER CODES

WINDOW CODE IN PAGE MEMORY															COMMENTS			
Type and character code field									Attribute field									
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	Type	Implicite Attribute	Ad - hoc Serial Attribute	Remark
0	X	X	X	X	X	X	X	0	N	L	H	S	B_1	G_1	R_1	α_0 (128)		Underlined, C_0	in GEN
1	0	0	—	—	s	i	m	0	B_0	G_0	R_0	—	B_1	G_1	R_1	DEL			
1 1 1	0 1 1	1 0 1	X	X	X	X	X	0	N	L	H	S	B_1	G_1	R_1	α_1 (96)		C_0	EXTENSION
0	0	X	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γ_S (64)	Normal size, positive		in GEN
0	1	X	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γ_M (64)			
1	0	0	—	—	—	—	—	1	—	—	—	—	—	—	—	ILLEGAL			
1 1 1	0 1 1	1 0 1	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γ_1 (96)	Normal size		EXTENSION

Nota : Extension for α 1 and γ 1 may be mapped in only one 1 K x 8 RAM or ROM.

GLOSSARY :

α	:	Alphanumeric
γ	:	Semi-graphic
γS	:	Separated semi-graphic
γM	:	Mosaïc semi-graphic
DEL	:	Delimitor
m	:	Blanking
i	:	Boxing
s	:	Underlining
C_0 (R_0, G_0, B_0)	:	Background colour
C_1 (R_1, G_1, B_1)	:	Foreground colour
H	:	Double height
L	:	Double width
N	:	Reverse video (negative)
S	:	Stable (non blinking)
X	:	Character code
—	:	Don't care

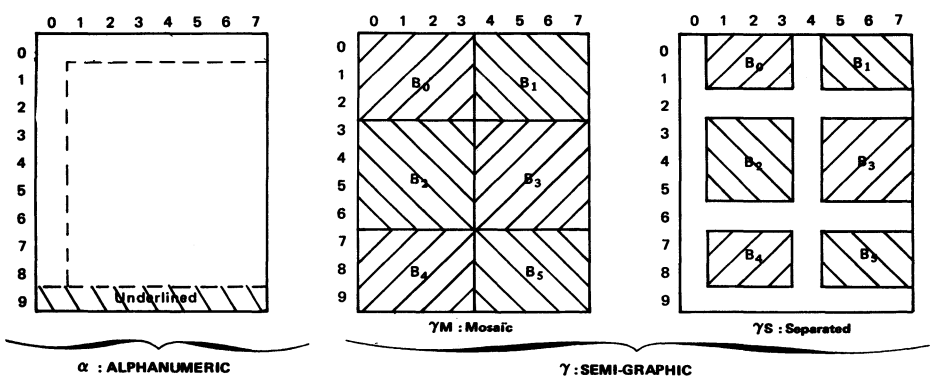


TABLE 2 – COMMAND CODE

COMMAND CODE																NAME	OPERATION
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	0									K (0 : 4)					Begin Row	X (0 : 5) ◄— 0 Y (0 : 4) ◄— K (0 : 4)
0	0	1								K (0 : 4)						Load Y	Y (0 : 4) ◄— K (0 : 4)
0	1	0								K (0 : 5)						Load X	X (0 : 5) ◄— K (0 : 5)
0	1	1														INC C	C ◄— C+ 1
1	0	0						K (0 : 7)								Load M	M (0 : 7) ◄— K (0 : 7)
1	0	1						K (0 : 7)								Load R	R (0 : 7) ◄— K (0 : 7)
1	1	0								K (0 : 5)						Load Y0	Y0 (0 : 5)◄—K (0 : 5)
1	1	1															Not interpreted

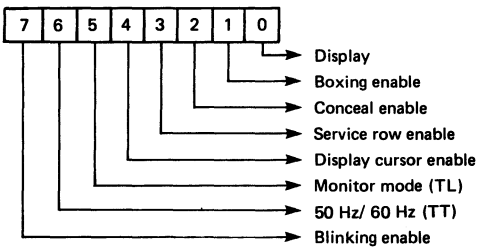
TABLE 3 – ACCESS MODE REGISTER

ACCESS MODE REG.								ACCESS MODE	SUBSEQUENT DATA TRANSFER
M7	M6	M5	M4	M3	M2	M1	M0		
0	0	0						Write	MP (C) ◄— T ; C ◄— C+ 1
0	0	1						Read	T ◄— MP (C) ; C ◄— C+ 1
0	1	0						Write without INC	MP (C) ◄— T
0	1	1						Read without INC	T ◄— MP (C)
1	0	0			N T			Write slice	GC (MP(C), NT)◄—T ; NT◄—NT+ 1
1	0	1			N T			Read slice	T◄—GC (MP(C), NT) ; NT◄—NT+ 1
1	1							Illegal	

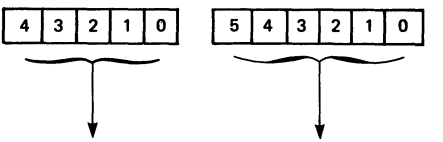
NT : Slice number T : Mail Box C : Cursor MP : Page Memory GC : Character Generator

REGISTERS

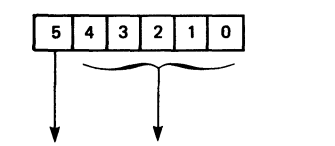
DISPLAY AND TIMING MODE REGISTER R



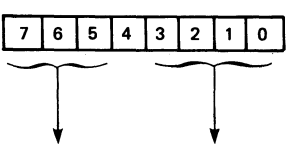
CURSOR REGISTER C



ORIGIN REGISTER Y0



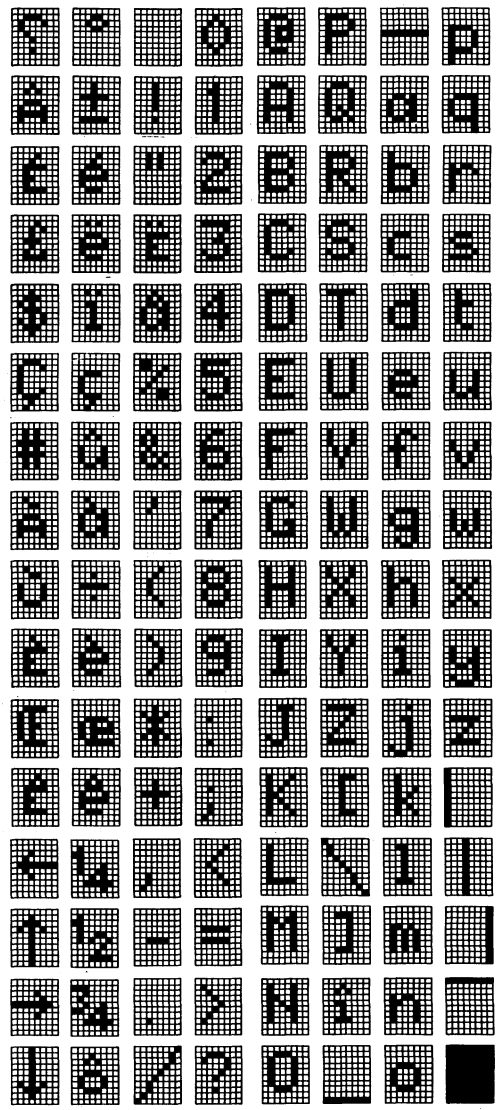
ACCESS MODE REGISTER M



ALPHANUMERIC CHARACTER SET

B7	0	0	0	0	0	0	0	0
B6	0	0	0	0	1	1	1	1
B5	0	0	1	1	0	0	1	1
B4	0	1	0	1	0	1	0	1

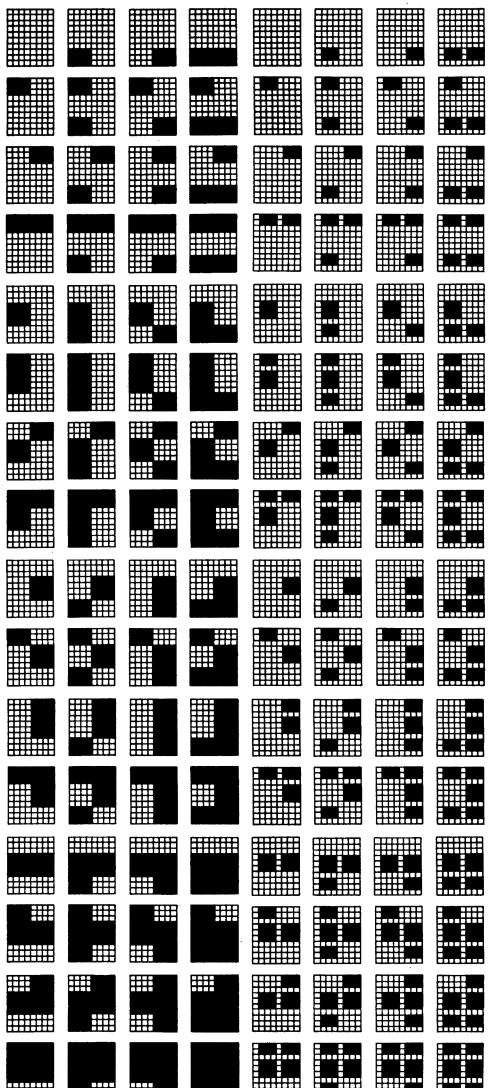
B3	B2	B1	B0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



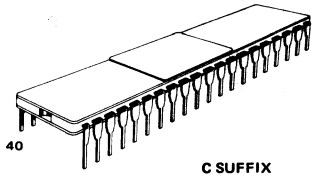
NOTA : Black dot= output high (GEN)

	MOSAIC Semi-graphic				SEPARATED Semi-graphic			
B7	0	0	0	0	0	0	0	0
B6	1	1	1	1	0	0	0	0
B5	0	0	1	1	0	0	1	1
B4	0	1	0	1	0	1	0	1

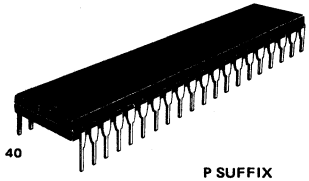
B3	B2	B1	B0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



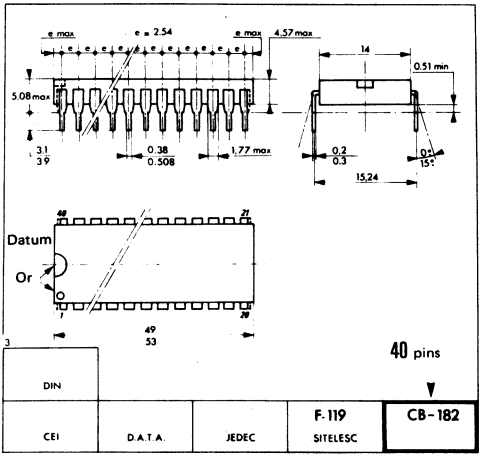
CASE CB-182



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



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Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

EF9365
EF9366

GRAPHIC DISPLAY PROCESSOR (GDP)

The GDP is a true high resolution graphic display processor, which contains all the functions required to process vector generation at a very high speed and to generate all the timing signals required for interfacing interlaced or non interlaced video data on a raster scan CRT display compatible with the CCIR 625 line 50 Hz standard.

The GDP flexibility results from its direct interfacing with any 8-bit MPU bus and its 11 internal registers.

The GDP's main features are :

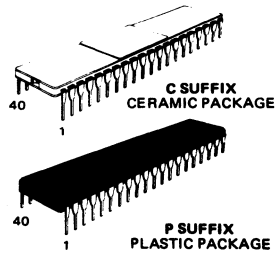
- Selectable resolutions in black and white or color :
  EF9365 : 512 x 512 (interlaced scan)
  256 x 256, 128 x 128, 64 x 64 (non interlaced scan)
  EF9366 : 512 x 256 (non interlaced scan)
- High speed vector plot well suited to animation (up to 1 500 000 dots/s. and an average value of 900 000 dots/s.) - 4 types of lines.
- Multiplexed address and refresh for 16K or 64K dynamic RAMs
- No limitation on the number of selectable memory planes (colors, grey levels or any other attributes)
- Multipage application capability
- On-chip full ASCII character generator (96) - maximum alphanumeric screen density : 85 x 57 - programmable sizes and orientations
- Direct interfacing with the monitor through the composite synchro and blanking signals
- Automatic allocation of display memory in refresh, write, dump, and display cycles
- Light pen registers and control signals
- Three types of interrupt requests
- Fully static design
- TTL compatible I/O
- Single + 5 volt supply.

MOS

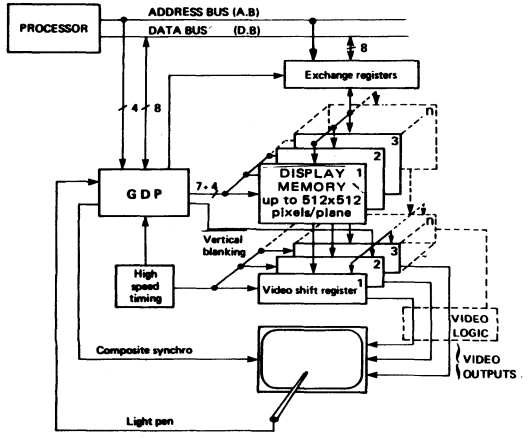
(N - CHANNEL, SILICON-GATE)

GRAPHIC DISPLAY PROCESSOR (GDP)

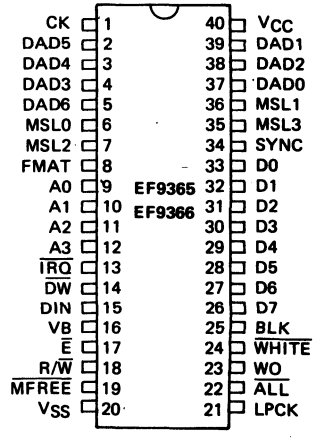
CASE CB-182



TYPICAL APPLICATION



PIN ASSIGNMENT



NT8132R2-A

THOMSON SEMICONDUCTORS
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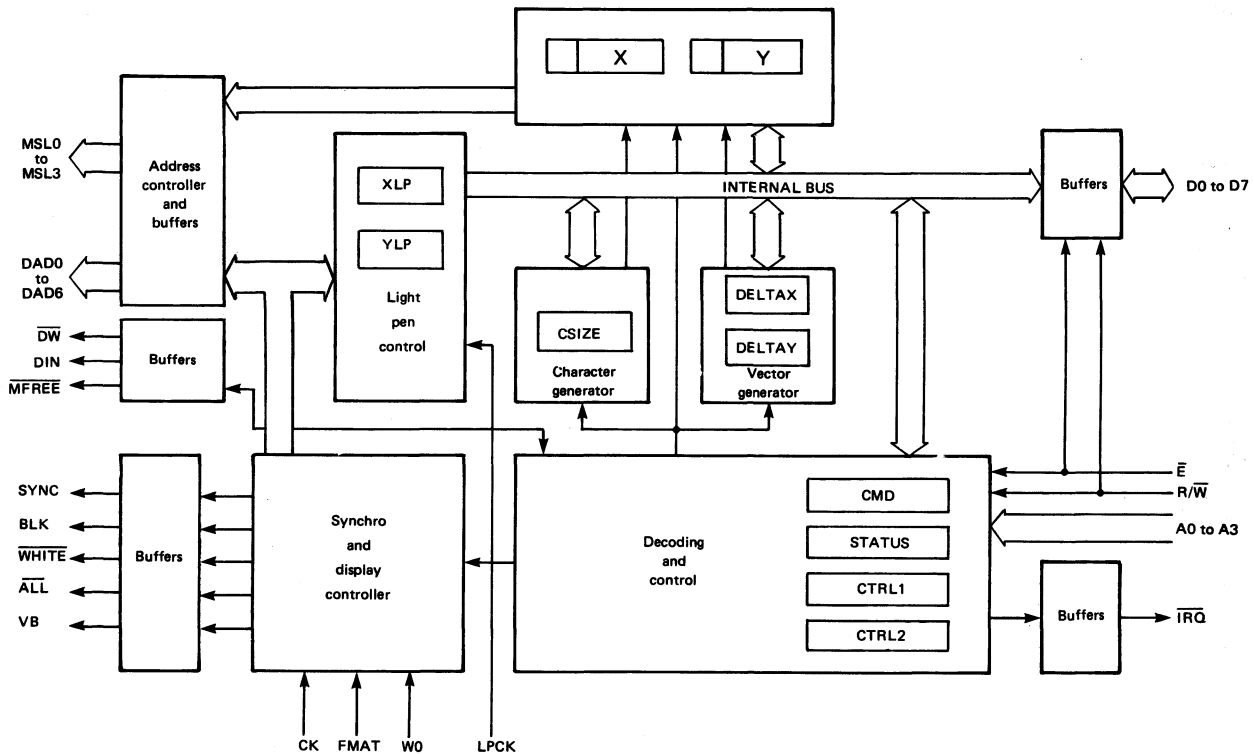
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

BLOCK DIAGRAM



GENERAL DESCRIPTION

Developed using NMOS technology, the GDP is an intelligent raster scan video display controller, fully programmable via an eight-bit microprocessor bus. Besides all the timing logic functions required to generate the video, sync and blanking signals, the GDP includes two hardwired display processors : a vector and a character generator.

This unique feature allows an ultrafast screen writing speed (the 512 dot diagonal may be written in less than 700 µs) at almost no microprocessor processing cost.

The GDP is particularly well-suited to all applications in which the display memory is not directly addressed by the MPU. This feature allows a total asynchronism between the MPU and the GDP memory cycles and preserves the whole MPU memory addressing space.

Nevertheless, where direct exchange between the microprocessor and the memory is necessary, the on-chip allocation controller will allow this exchange without display interference.

The GDP is programmable using 11 internal registers occupying 16 consecutive addresses. These registers can also be modified by the GDP's hardwired processors while a command is being executed.

Note : A summary of data codes and registers is given in the **Register address table.** Hexadecimal values are subscripted 16 and the register bits are numbered as follows :

MSB	7	6	5	4	3	2	1	0	LSB

MAXIMUM RATINGS

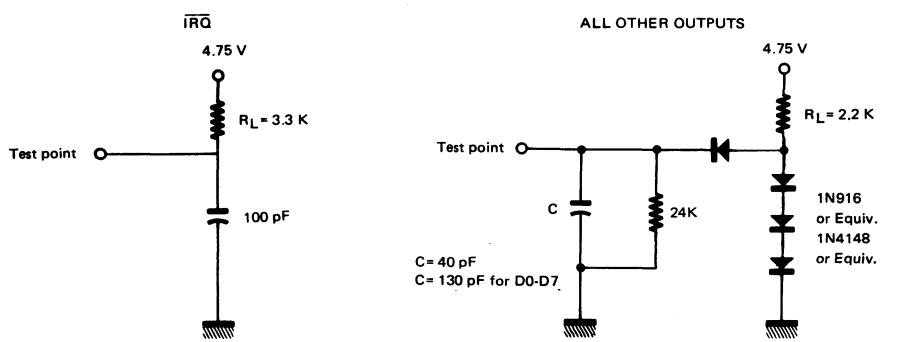
Parameter	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.3 to+ 7.0	V
Input voltage	V_{in}	−0.3 to+ 7.0	V
Operating temperature	T_A	0 to+ 70	°C
Storage temperature	T_{stg}	− 55 to+150	°C

The GDP inputs are protected against high static voltages and electric fields ; nevertheless, normal precautions should be taken to avoid voltages above the limit values on this high impedance circuit.

STATIC ELECTRICAL PARAMETERS (V_{CC} = 5V ± 5%, V_{SS} = 0, T_A = 0 to 70° C unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input high voltage except CK	V_{IH}	V_{SS}+ 2.2	–	V_{CC}	V
Input high voltage CK	V_{IHCK}	V_{SS} + 3.5	–	V_{CC}	V
Input low voltage	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Input leakage current (V_{in} = 0 to 5.25 V, V_{CC} = max)	I_{in}	–	1.0	2.5	µA
Output high voltage (I_{load} = −100 µA, V_{CC} = min)	V_{OH}	V_{SS} + 2.4	–	–	V
Output low voltage (I_{load} = 1.6 mA, V_{CC} = min)	V_{OL}	–	–	V_{SS} + 0.4	V
Supply current	I_{CC}	–	80	–	mA
Capacitance (V_{in} = 0, T_A = 25° C, f = 1.0 MHz)	C_{in}	–	–	12	pF
	C_{out}	–	–	12	pF

TEST LOADS

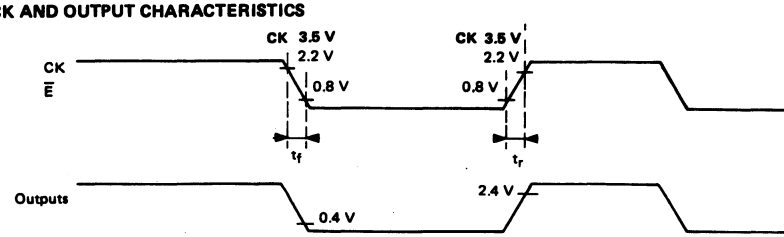


DYNAMIC OPERATING CONDITIONS

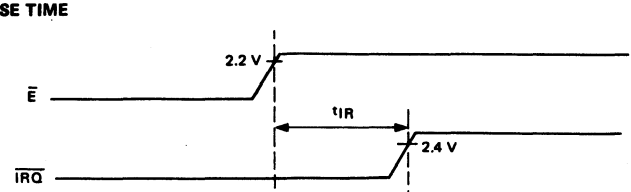
(V_{DD} = 5,0 V ± 5 %, V_{SS} = 0V ; T_A = 0 to+ 70° C unless otherwise noted)

Time (ns)	Symbol	Min	Max
Clock period	t_{CK}	560	
CK pulse width, low	t_{CKL}	330	
CK pulse width, high	t_{CKH}	190	
CK low to valid DAD	CKLDAD		320
CK high to valid DAD	CKHDAD		180
CK low to valid SYNC	CKLSYNC		300
CK low to valid BLK	CKLBLK		310
CK low to valid VB	CKLVB		500
CK low to valid $\overline{ALL}$	CKLALL		300
CK low to valid MSL	CKLMSL		300
CK low to valid $\overline{DW}$	CKLDW		310
CK low to valid $\overline{MFREE}$	CKLMFR		500
CK low to valid DIN	CKLDIN		310
CK low to valid $\overline{IRQ}$	CKLIRQ		1500
CK low to valid $\overline{WHITE}$	CKLWHI		530
$\overline{E}$ pulse width, low	t_{EL}	450	
$\overline{E}$ pulse width, high	t_{EH}	430	
Address pre-setup time	t_{AS}	160	
Address hold time	t_{AH}	10	
Data pre-setup time (write)	t_{DSW}	260	
Data setup time (read)	t_{DDR}		320
Data hold time (read)	t_{DHR}	10	
$\overline{IRQ}$ release time	t_{IR}		1600
LPCK high to $\overline{WHITE}$ high (if command 08_{16})	LPHW		1600
LPCK high to $\overline{IRQ}$ low	LPHIRQ		1600
LPCK high hold time	t_{LPCKH}	150	
CK and $\overline{E}$ rise times	t_r		20
CK and $\overline{E}$ fall times	t_f		20

CLOCK AND OUTPUT CHARACTERISTICS

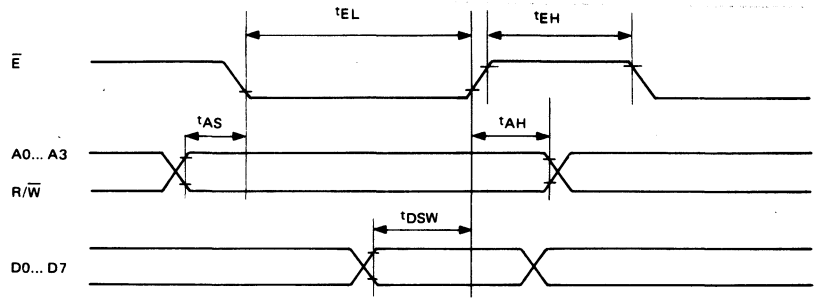


$\overline{IRQ}$ RELEASE TIME

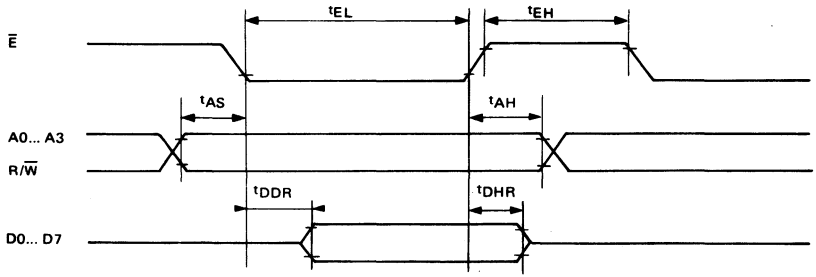


4/27

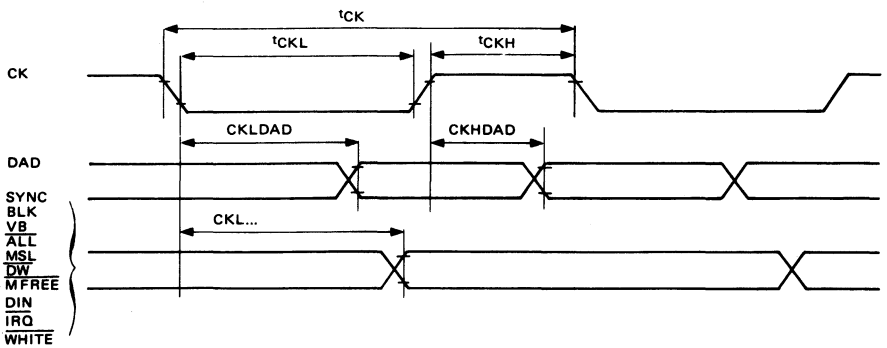
MICROPROCESSOR BUS, WRITE ACCESS



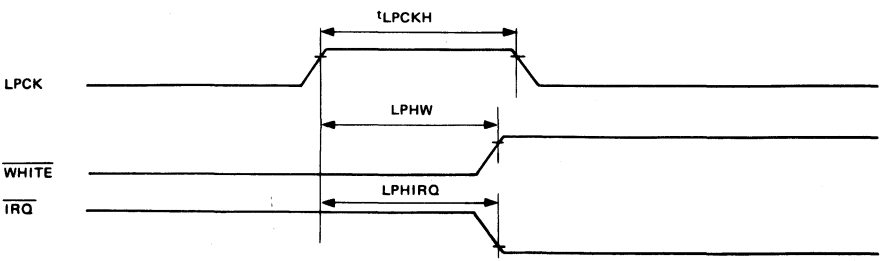
MICROPROCESSOR BUS, READ ACCESS



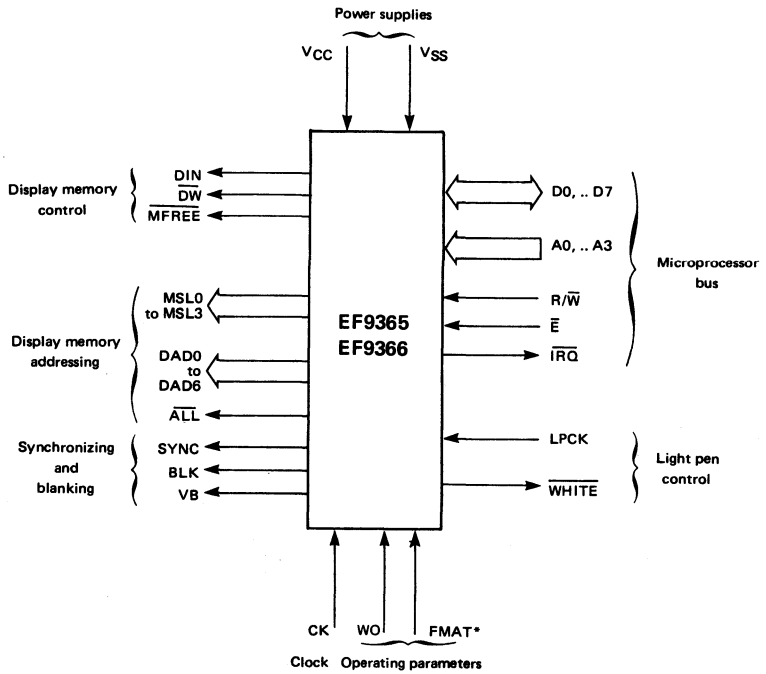
SYNCHRONOUS SIGNALS WITH CK INPUT



LIGHT PEN SIGNALS



PIN DESCRIPTION



*FMAT should be connected to V_{CC} in the EF9366.

POWER SUPPLY, CLOCK AND OPERATING PARAMETERS

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
V_{SS}	S	20	Power supply	Ground
V_{CC}	S	40	Power supply	+ 5 V
CK	I	1	Clock	Master clock. All internal processor states are modified on the falling edge of this signal. The whole circuit logic is static and the cycle of this clock needs only to be ajusted according to the shape and accuracy the synchronizing signals should feature. DAD memory address multiplexing signal. If CK is low, low addresses (or row addresses for the memory) are those that are output on DAD. For SYNC to be in compliance with the applicable CCIR standards (FMAT high) the input frequency on CK should be 1.750 MHz. If FMAT is low or for the EF9366, the frame frequency equals 50 Hz provided that the input frequency on CK is 1.7472 MHz.
FMAT	I	8	Format	EF9365 should be connected to V_{CC} for a 512 line vertical resolution (interlaced scan) and to V_{SS} for 256 lines or less (non-interlaced scan). The shape of the synchronizing signals, the address distribution on DAD and the MSL output functions are changed by this input. EF9366 : not used (should be connected to V_{CC}).
WO	I	23	Write only	When WO is high, memory refresh nor display no longer exist. The hard wired write processors may operate without being interrupted. The $\overline{ALL}$ signal is always high.

SYNCHRONIZING AND BLANKING SIGNALS

SYNC	O	34	Video monitor synchronizing	Video monitor line and frame sync signal. The SYNC signal complies with CCIR 625-line 50 Hz standard provided the CK frequency is 1.750 MHz and FMAT is high. If FMAT is low or for the EF9366, the frames are no longer interlaced and all comprise 312 lines. This output is not affected by the WO input and CTRL1 register.
BLK	O	25	Blanking	This signal is high apart from the display window (writing or refresh). It is always high if bit 2 in register CTRL1 is high, but it is not affected by the WO input.
VB	O	16	Vertical blanking	This signal is not affected by WO and register CTRL1. High during vertical blanking.

DISPLAY MEMORY ADDRESSING SIGNALS

DAD0 to DAD6	O	37,39, 38,4 3,2,5	Display address	Addresses that are multiplexed by the CK signal. Provided for the automatic refresh of the 16K or 64K dynamic memories.
MSL0 to MSL3	O	6,36 7,35	Memory select	Pixel write select signals (see section : **Display memory configuration.)**
$\overline{ALL}$	O	22	Access to all memory units	This signal makes it possible to discriminate between the collective memory accesses to all chips (display, refresh or erase), and the memory accesses to a single pixel for vector or character writing purposes. This signal is low for collective access.

DISPLAY MEMORY CONTROL SIGNALS

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
DIN	O	15	Display in	Selection of the memory data code corresponding to the display screen in the 'off' condition (active when high). For a black-and-white display (1 bit per pixel), DIN may directly be the storage entry data.
$\overline{DW}$	O	14	Display write	Display memory write signal. Active when low.
$\overline{MFREE}$	O	19	Memory free	Signal low during the next memory idle period following the $0F_{16}$ command. This signal allows exchanges between the microprocessor and the X and Y flagged memory segment without affecting the display.

MICROPROCESSOR BUS SIGNALS

D0-D7	I/O	33 to 26	Data bus	I/O buffers opening is controlled through $\overline{E}$, and the related direction through R/$\overline{W}$.
A0-A3	I	9 to 12	Address bus	Address of the register involved in microprocessor access.
R/$\overline{W}$	I	18	Read/write signal	Read/write signal. Write when low.
$\overline{E}$	I	17	Enable	Bus exchange synchronizing and enabling signal.
$\overline{IRQ}$	O	13	Interrupt request	Interrupt request towards the microprocessor, programmable through register CTRL1. Open drain output.

LIGHT PEN OPERATING SIGNALS

$\overline{WHITE}$	O	24	Forcing to white level	Forces white level on video signal, for use of the light pen. Active when low.
LPCK	I	21	Light pen strobe	Light pen input. When the mechanism is set, a rising edge loads into registers XLP and YLP the current display address and sets the XLP register's LSB high.

REGISTER DESCRIPTION

X AND Y REGISTERS (Addresses : 8_{16}, 9_{16}, A_{16}, B_{16})

The X and Y registers are 12-bit read-write registers. They indicate the position of the next dot to be written into the display memory. They have no connection at all with the video signal generating scan, but they point the write address, in the same way as the pen address on a plotter.

These 2 registers are incremented or decremented, prior to each write operation into the display memory, by the internal vector and character generators, or they may be directly positioned by the microprocessor.

This 2 x 12 bit write address covers a 4096 x 4096 point addressing space. Only the LSBs are used here, since the maximum definition of the picture actually stored is 512 x 512 pixels (picture elements).

The MSBs are either ignored or used to inhibit writing where the actual screen is regarded as being a window within a 4096 x 4096 space.

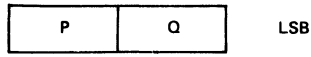
The above features along with the relative mode description of all picture component elements make it possible to automatically solve the great majority of edge cut-off problems.

DELTAX AND DELTAY REGISTERS (Addresses : 5_{16}, 7_{16}).

The DELTAX and DELTAY registers are 8-bit read-write registers. They indicate to the vector generator the projections of the next vector to be plotted, on the X and Y axes respectively. Such values are unsigned integers. The plotting of a vector is initiated by a write operation in the command register (CMD).

CSIZE REGISTER (Address : 3_{16})

The CSIZE register is an 8-bit read-write register. It indicates the scaling factors of X and Y registers for the symbols and characters. 98 characters are generated from a 5 x 8 pixel matrix defined by an internal ROM. In the standard version, it contains the alphanumeric characters in the ASCII code which may be printed, together with a number of special symbols.



Each symbol can be increased by a factor P(X) or Q(Y). These factors are independent integers which may each vary from 1 to 16 and which are defined by the CSIZE register. The symbol generation sequence is started after writing the ASCII code of the symbol to be represented in the CMD register.

CTRL1 REGISTER (Address : 1_{16}).

The CTRL1 register is a 7-bit read-write register, through which the general circuit operation may be fed with the required parameters.

Bit 0 : When low, this bit inhibits writing in display memory (equivalent to pen or eraser up).
When high, this bit enables writing in display memory (pen or eraser down).
This bit controls the $\overline{DW}$ output.

Bit 1 : When low, this bit selects the eraser.
When high, this bit selects the pen.
This bit controls the DIN output.

Bit 2 : When low, this bit selects normal writing mode (writing apart from the display and refresh periods, which are a requirement for the dynamic storages) in display memory.
When high, this bit selects the high speed writing mode : the display periods are deleted. Only the dynamic storage refresh periods are retained.

Bit 3 : When low, this bit indicates that the 4096 x 4096 space is being used (the 12 X and Y bits are significant)
When high, this bit selects the cyclic screen operating mode.

Bit 4 : When low, this bit inhibits the interrupt triggered by the light pen sequence completion.
When high, this bit enables the interrupt.

Bit 5 : When low, this bit inhibits the interrupt release by vertical blanking.
When high, this bit enables the interrupt.

Bit 6 : When low, this bit inhibits the interrupt indicating that the system is ready for a new command.
When high, this bit enables the interrupt.

Bit 7 : Not used. Always low in read mode.

CTRL2 REGISTER (Address : 2_{16})

The CTRL2 register is a 4-bit read/write register, through which the plotting of vectors and characters may be denoted by parameters.

Bit 0, 1 : These 2 bits define 4 types of lines (continuous, dotted, dashed, dash-dotted).

Bit 2 : When low, this bit defines straight writing.
When high, it defines tilted characters.

Bit 3 : When low, this bit defines writing along an horizontal line.
When high, this bit defines writing along a vertical line.

Bit 4, 5, 6, 7 : Not used. Always low in read mode.

CMD COMMAND REGISTER (Address : 0_{16})

The CMD register is an 8-bit write-only register. Each *write operation* in this register causes a command to be executed, upon completion of the time necessary for synchronizing the microprocessor access and the GDP's CK clock.

Several types of command are available :

- vector plotting
- character plotting
- screen erase
- light pen circuitry setting
- access to the display memory through an external circuitry.
- indirect modification of the other registers (commands that make it possible for the X, Y, DELTAX, DELTAY, CTRL1, CTRL2 and CSIZE registers to be amended or scratched).

STATUS REGISTER (Address 0_{16})

The STATUS register is an 8-bit read-only register. It is used to monitor the status of the executing statements entered into the circuit, and more specifically to avoid the need for modifying a register that is already used for the command currently executing.

Bit 0 : When low, this bit indicates that a light pen sequence is currently executing.
When high, it indicates that no light pen sequence is currently executing.

Bit 1 : This bit is high during vertical blanking. It is the VB signal recopy.

Bit 2 : When low, this bit indicates that a command is currently executing.
When high, this bit indicates that the circuit is ready for a new command.

Bit 3 : When low, this bit indicates that the X and Y registers point within the display window.
When high, this bit indicates that the X and Y registers are pointing outside the memory display.
This bit is the logic OR of the unused MSBs of the X and Y registers.

Bit 4 : When high, this bit indicates that an interrupt has been initiated by the completion of a light pen running sequence. Such an interrupt is enabled by bit 4 in CTRL1 register.

Bit 5 : When high, this bit indicates that an interrupt has been initiated by vertical blanking. Such an interrupt is enabled by bit 5 in CTRL1 register.

Bit 6 : When high, this bit indicates that an interrupt has been initiated by the completion of execution of a command. Such an interrupt is enabled by bit 6 in CTRL1 register.

Bit 7 : When high, this bit indicates that an interrupt has been initiated. It is the logic OR of bits 4, 5 and 6 in STATUS register. The $\overline{IRQ}$ output state is always the opposite of the status of this bit.

Note : Bits 4, 5, 6 and 7 are reset low by a read of the STATUS register.

XLP AND YLP REGISTERS (Addresses C_{16} and D_{16})

The XLP and YLP registers are read-only registers, with 7 and 8 bits respectively. Upon completion of a light pen running sequence, they contain the display address sampled by the first edge appearing rising on the LPCK input. The use of such registers is discussed in section : **Use of light pen circuitry.**

NOTES :

1. All internal registers may be read or written at any time by the microprocessor. However, the precautions outlined below should be observed :

   — Do not write into the CMD register if execution of the previous command is not completed (bit 2 of STATUS register).

   — Do not alter any register if it is used as an input parameter for the internal hardwired systems (e. g. : modifying the DELTAX register while a vector plotting sequence is in progress).

   — Do not read a register that is being asynchronously modified by the internal hardwired systems (e. g. : reading the X register while a vector plotting sequence is in progress may be erroneous if CK and $\overline{E}$ are asynchronous).

2. On powering up, the writing devices may have any status. Before entering a command for the first time, it is necessary to wait until all functions currently underway are completed, which information can be derived from the STATUS register.

SYSTEM OPERATING PRINCIPLE

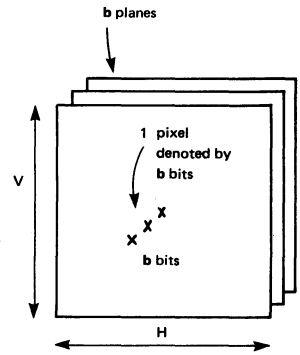
DISPLAY MEMORY CONFIGURATION

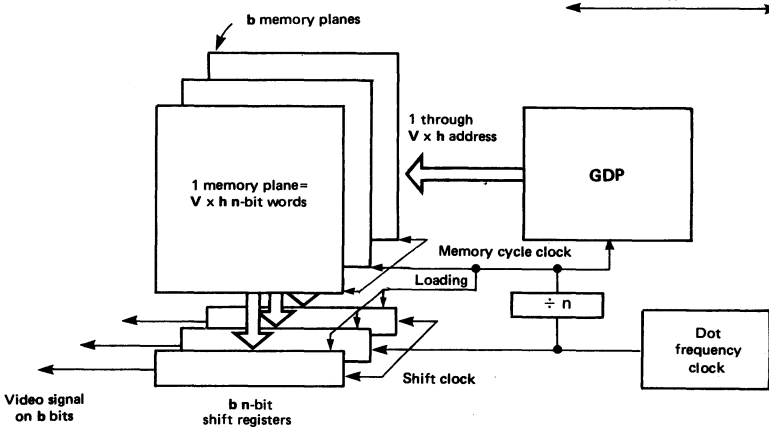
Assume a V x H pixel picture. Assume that each pixel is able to adopt 2^b different states. A V x H x b bit display memory is thus required.

In those applications where H features a high value, the video signal frequency exceeds the maximum frequency of memory read access.

Example : H = 512 with a television line frequency : the pixel succession period on the video signal is 70 ns.

It is mandatory that a line of H dots be cut into h adjoining segments of n bits each, read at the same time in the display memory, and thereafter converted to serial form to produce the video signal. h memory accesses per line are necessary. Each access loads b n-bit shift registers. The memory contains V x h x b n-bit words.





EF9365

The EF9365 circuit is designed to accomodate the following picture formats :

1. V= H= 512 or a lower power of 2
2. h= 64
3. n= 8, 4, 2 or 1
4. Any value for b (the addressing is similar for all memory planes. These planes are managed outside the actual circuit).

Circuit operation in the various formats outlined above occurs as described below :

512 x 512 pixel format (V= 512, h= 64, n= 8)

The FMAT input should be high. The memory is made up of V x h bytes= 32 K bytes per memory plane.

The byte address is made up of 15 bits :

- 14 are output in 2 runs on the DAD pins for the purpose of using 16 K x 1 bit dynamic RAMs,
- the 15th one is output on pin MSL3.

The 3 MSL0, 1 and 2 outputs allow to select one pixel out of the 8 featuring the same address, for pixel-to-pixel write applications. They issue the number of the involved pixel, encoded on 3 bits.

256 x 256 pixel format (V= 256, h= 64, n= 4)

The FMAT input should be low. The memory is made up of V x h x n bits, i.e. 16 K 4-bit words. The address of a 4-bit word is made up of 14 bits, which are output in 2 runs on the DAD pins.

Each of the 4 MSL pins is used to select one pixel in a 4-bit word for writing purposes. The 2 LSBs in the horizontal writing address are decoded before being output on the MSL pins. Such outputs are active when low.

Format less than 256 x 256 pixels (V= 128 or 64, h= 64, n= 2 or 1).

Such formats are achieved in the same way as for the 256 x 256 pixel format discussed above. Unrequired address bits are output on DAD7.

EF9366

The EF9366 circuit is designed to accomodate a (512 x 256) picture format : **V= 256, H= 512, h= 64, n= 8, b= any value.**

The memory is made up of 16 K bytes per memory plane. The byte address is made up of 14 bits which are output in two runs on the DAD pins. The 3 MSL0, MSL1, MSL2 outputs are used to select one pixel out of the 8 featuring the same address. They issue the number of the pixel, encoded on 3 bits. MSL3 is high, and is not used.

SIGNALS OUTPUT THROUGH THE DAD AND MSL PINS

The internal counters which address the display memory are made up of :

- 6 horizontal address bits (h = 64)
  $h_0, h_1, h_2, h_3, h_4, h_5$
- **9 vertical address bits** ($V \leqslant 512$)
  $t, V_0, V_1, V_2, V_3, V_4, V_5, V_6, V_7$

t is here the LSB. It denotes the line parity and changes every frame because of interlaced scan. Within a same frame, V_0 denotes the LSB.

The write address is made up of the 9 LSBs of the X and Y internal registers.

$$X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7, X_8$$
$$Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7, Y_8$$

The display address and write address are cross-referenced as follows :

EF9365

FMAT = 1

h_0	h_1	h_2	h_3	h_4	h_5	t	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7
X_3	X_4	X_5	X_6	X_7	X_8	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8

FMAT = 0

h_0	h_1	h_2	h_3	h_4	h_5	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7
X_2	X_3	X_4	X_5	X_6	X_7	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7

EF9366

h_0	h_1	h_2	h_3	h_4	h_5	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7
X_3	X_4	X_5	X_6	X_7	X_8	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7

DAD AND MSL OUTPUT STATUS TABLES

EF9365 FMAT = 1

		MSL				DAD						
$\overline{ALL}$	CK	0	1	2	3	0	1	2	3	4	5	6
0	0	X_0	X_1	X_2	V_1	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1					V_7	V_6	V_5	V_4	V_3	V_2	t
1	0	X_0	X_1	X_2	Y_2	X_8	X_7	X_6	X_5	X_4	X_3	Y_1
1	1					Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_0

If FMAT is high, the 128 refresh accesses are executed at 2 line intervals, for only one half of the memory, the 32 K-bytes being split into two 16 K-byte blocks. The V_1 output on MSL3 is used to switch over from one block to the other at 2 line intervals. During vertical blanking, such a refresh is achieved using 4 lines at 16 line intervals.

EF9365 FMAT = 0

		MSL				DAD						
$\overline{ALL}$	CK	0	1	2	3	0	1	2	3	4	5	6
0	0	0	0	0	0	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1					V_7	V_6	V_5	V_4	V_3	V_2	V_1
1	0	X_0 and X_1 decoded (active low)				X_7	X_6	X_5	X_4	X_3	X_2	Y_0
1	1					Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

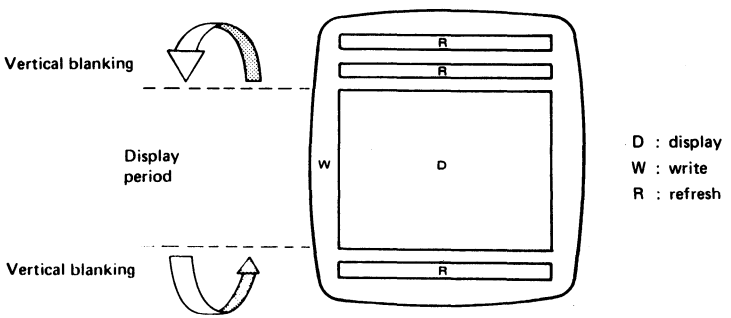
EF9366

		MSL				DAD						
$\overline{ALL}$	CK	0	1	2	3	0	1	2	3	4	5	6
0	0	X_0	X_1	X_2	1	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1				1	V_7	V_6	V_5	V_4	V_3	V_2	V_1
1	0				1	X_8	X_7	X_6	X_5	X_4	X_3	Y_0
1	1				1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

If FMAT is low or for the EF9366 : the 128 refresh accesses are executed at 2 display line intervals.

MEMORY OPERATION SEQUENCE ALONG ONE FRAME

Apart from the window where the memory is used for display purposes exclusively, write operations may be performed, except during 3 refresh periods.



The three period types, D, W and R, respectively, are indicated outside the circuit through the BLK and $\overline{ALL}$ signals :

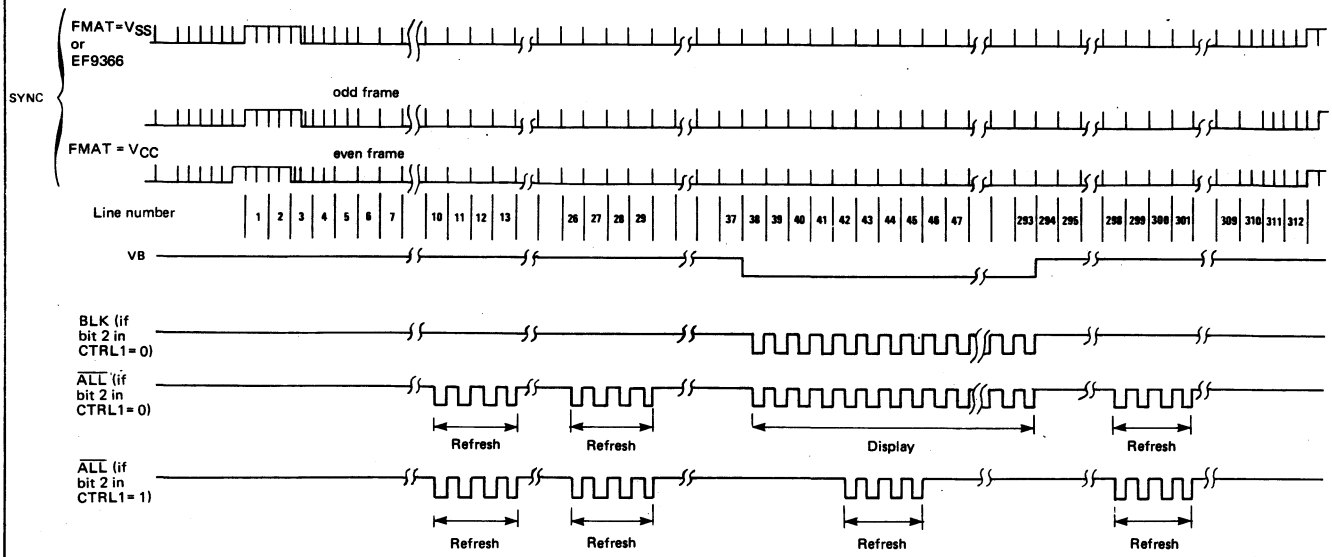
	BLK	$\overline{ALL}$
D	0	0
W	1	1
R	1	0

Exceptions :

- If bit 2 in register CTRL1 is high (high speed write), the display period is suppressed and 19 refresh cycles of 4 lines each are executed during one frame.
- As long as the WO input is high, the circuit is set to write mode, and BLK retains the same outline as it has under normal operating conditions.

  In these two cases, executing codes 04_{16}, 06_{16}, 07_{16} and $0C_{16}$ triggers a complete D sequence for a high-speed scan of all addresses. This lasts two frames if FMAT is high or one frame if FMAT is low and for the EF9366 version.

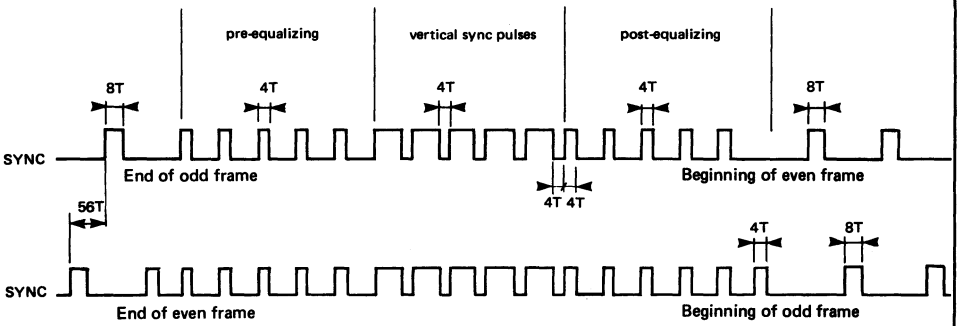
FRAME SEQUENCE



Note : $\overline{ALL}$ signal high denotes write periods.

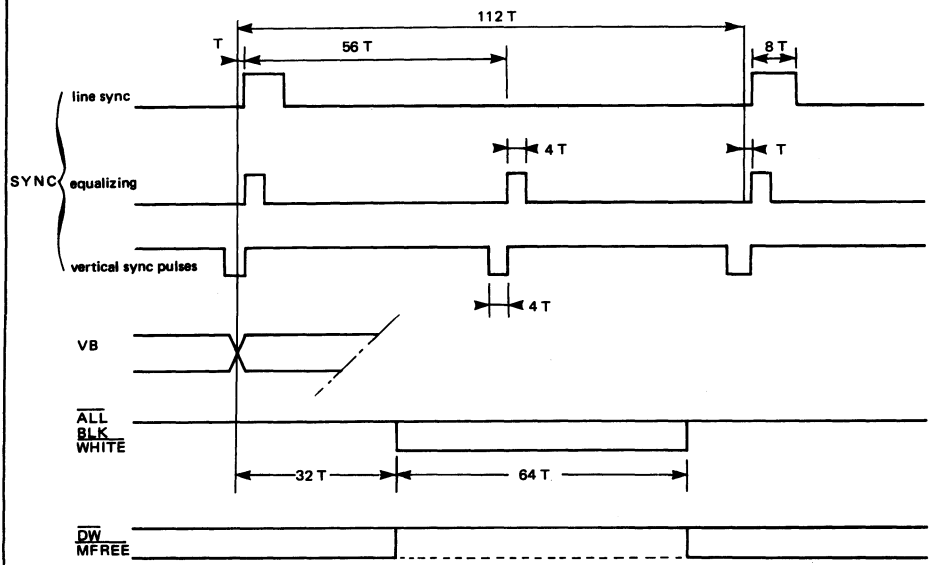
COMPOSITE SYNC AROUND FRAME SYNC

T : CK input period (570 ns in a typical application)



Note : If FMAT is low and for the EF9366 version, the pattern of the second line is repeated for each frame.

DETAILED LINE DIAGRAM



HARDWIRED WRITE PROCESSOR OPERATION IN DISPLAY MEMORY

The hardwired write processors are sequenced by the, master clock CK. They receive their parameters from the microprocessor bus. They control the X, Y write address, and the DIN, $\overline{DW}$, $\overline{MFREE}$ and $\overline{IRQ}$ outputs.

These harwired processors operate in continuous mode. In the event of conflicting access to the display memory, the display and refresh processors have priority.

Since command decoding is synchronous with the CK master clock, any write operation into the (CMD) command register triggers a synchronizing mechanism which engages the circuit for a maximum of 2 CK cycles when the $\overline{E}$ input returns high. The circuit remains engaged throughout command execution.

No further command should be entered as long as bit 2 in STATUS register is low.

VECTOR PLOTTING

The internal vector generator makes it possible to modify, within the display memory, all the dots which form the approximation of a straight line segment. All vectors plotted are described by the origin dot and the projections on the axes.

The starting point co-ordinates are defined by the X, Y register value, prior to the plotting operation.
Projections onto the axes are defined as absolute values by the DELTAX and DELTAY registers, with the sign in the command byte that initiates the vector plotting process.

The vector approximation achieved here is that established by J. F. BRESENHAM ("Algorithm for computer control of a digital plotter"). This algorithm is executed by a hardwired processor which allows for a further vector component dot to be written in each CK clock cycle.

During plotting, the display memory is addressed by the X, Y registers, which are incremented or decremented.

On completion of vector plotting, they point to the end of this vector.

All vectors may be plotted using any of the following line patterns : continuous, dotted, dashed, dash-dotted, according to the 2 LSBs in register CTRL2.

Irrespective of such patterns, the plotting speed remains unchanged. The "pen down-pen up" statement required for plotting non-continuous lines is controlled by the $\overline{DW}$ output.

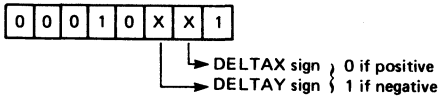
For a specified non-continuous line plotted vector, defined by DELTAX, DELTAY, CTRL2, CMD, the $\overline{DW}$ sequencing during the plotting process is always the same, irrespective of vector origin and of the nature of previous plots. This feature guarantees that a specified vector can be deleted by plotting it again after moving X and Y to the starting point, and complementing bit 1 in register CTRL1.

Since the vector plotting initiation command defines the sign of the projections onto the axes, all vectors may be plotted using 4 different commands.

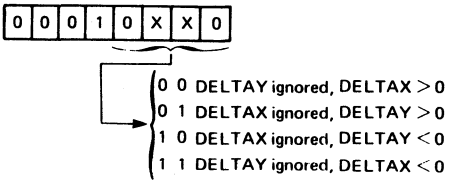
For increased programming flexibility, the system incorporates 16 different commands, supplemented by a set of 128 commands which make it possible to plot small size vectors by ignoring the DELTAX and DELTAY registers.

Such commands are as follows :

- Basic commands

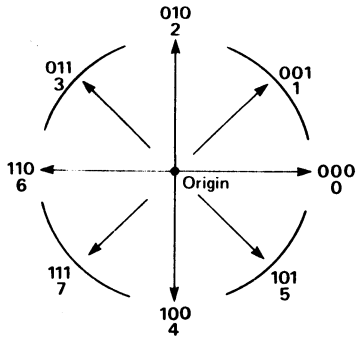


- Commands which allow ignoring the DELTAX or DELTAY registers by considering them as of zero value.

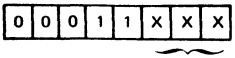


Note : Bits 1 and 2 always have the same sign meaning.

These 8 codes may be summarized by the following diagram :

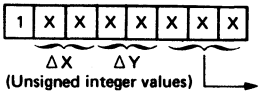


- Commands which allow ignoring the smaller of the two DELTAX and DELTAY registers, by considering it as being equal to the larger one, which is the same as plotting vectors parallel to the axes or diagonals, using a single DELTA register.



Same direction codes as above.

- Commands in which the two registers DELTAX and DELTAY may be ignored by specifying the projections through the CMD register (0 to 3 steps for each projection).



EXAMPLE : PLOTTING A DOTTED VECTOR

Origin : $\begin{cases} X = 47_{10} \\ Y = 75_{10} \end{cases}$

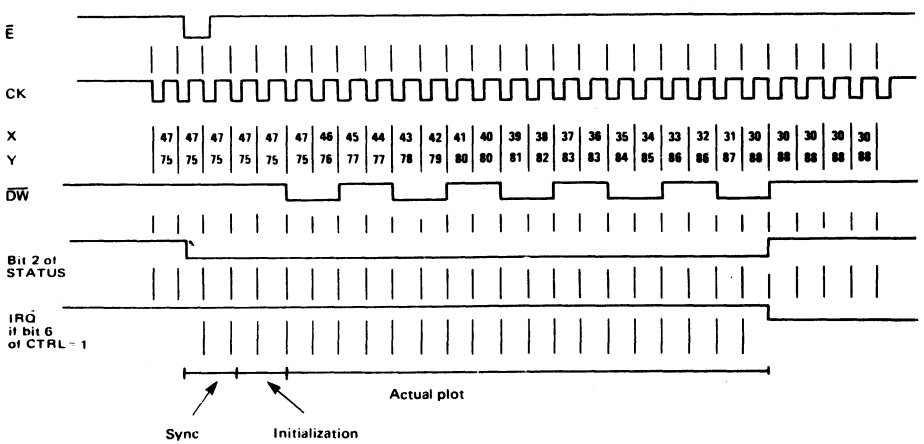
Projections: $\begin{cases} DELTAX = 17_{10} \\ DELTAY = 13_{10} \end{cases}$

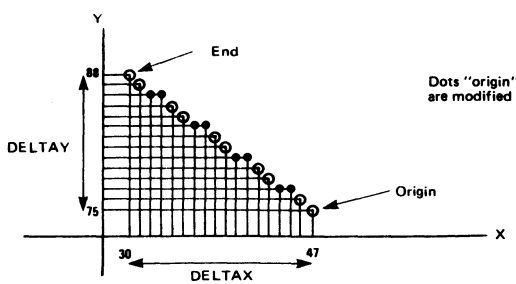
$CMD = 13_{16}$ Corresponding to
- Basic command,
- DELTAX < 0
- DELTAY > 0

$CTRL1 = 03_{16}$ Pen down

$CTRL2 = 1_{16}$ Dotted vector :
2 dots on,
2 dots off.

Plotting cycle sequence : (It is assumed that the vector generator is not interrupted by the display or refresh cycle).





Dots "origin" and "end" are modified

Display shows : ● unmodified dot
o dot on

Note :

Plotting a vector with DELTAX = DELTAY = 0 writes the dot X, Y in memory. It occupies the vector generator for synchronization, initialization and one write cycle.

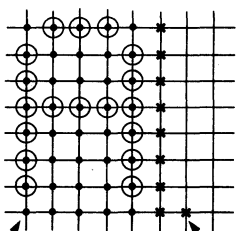
CHARACTER AND SYMBOL GENERATOR

The character generator operates in the same way as the vector generator, i.e. through incrementing or decrementing the X, Y registers, in conjunction with a $\overline{DW}$ output control.

It receives parameters from the CSIZE, CTRL2 and CMD registers. The characters plotted are selected, according to the CMD value, out of 98 matrices (97 8-dot high x 5-dot wide rectangular matrices, and one 4 dot x 4 dot matrix) defined in an internal ROM. Two scaling factors may be applied to the characters plotted using X and Y defined by the CSIZE register. The characters may be tilted, according to the content of register CTRL2.

Basic matrix

Upon completion of a character writing process, the X and Y registers are positioned for writing a further character next to the previous one, with a 1 dot spacing, i.e. Y is restored to its original value and X is incremented by 6.



• Unchanged
⊙ Altered dots
} if CMD = 41_{16} (in the ROM standard version)

× Computed dots, not defined into the ROM (not modifiable).

Scaling factors

Each individual dot in the 5 x 8 basic matrix may be replaced by a P x Q size block.

P : X co-ordinate scaling factor
Q : Y co-ordinate scaling factor

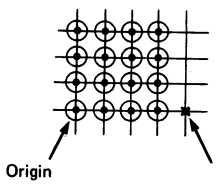
The character size becomes 5P x 8Q. Upon completion of the writing process, X is incremented by 6P. The CK clock cycle count required is 6P x 8Q.

P and Q may each take values from 1 through 16. They are defined by the CSIZE register. Each value is encoded on 4 bits, value 16 being encoded as 0_{16}.

In register CSIZE, P is encoded on the 4 MSBs and Q on the 4 LSBs.

Among the 97 rectangular matrices available in the standard ROM, 96 correspond to CMD values ranging from 20_{16} to $7F_{16}$, and the 97th matrix to $0A_{16}$. In the standard version, these values correspond to the 96 printable characters in the ASCII set. The 97th character is a 5P x 8Q block which may be used for deleting the other characters.

The 98th code ($0B_{16}$) is used to plot a 4P x 4Q graphic block. It locates X, Y, without spacing for the next symbol. Such a block makes it possible to pad uniform areas on the screen.



⊙ Modified dots
× Computed dot not defined in ROM (not modifiable)

Tilted characters

All characters may be modified to produce tilted characters or to mark the vertical co-ordinate with straight or tilted type symbols. Such changes may be achieved using bits 2 and 3 in register CTRL2.

Note : Scaling factors P and Q are always applied within the co-ordinates of the character before conversion.

Character deletion

A character may be deleted using either the same command code or command code $0A_{16}$. In either case, bit 1 in register CTRL1 should be inverted, the origin should be the same as prior to a character plotting operation, as should the scaling factors.

Note : Vector generator and character generator operate in similar ways :

	VECTOR	CHARACTER
Dimensions	DELTAX, DELTAY	CSIZE, tilting
$\overline{DW}$ modulation	Type of line	Character code

USE OF LIGHT PEN CIRCUITRY

A rising edge on the LPCK input is used to sample the current display address in the XLP and YLP registers, provided that this edge is present in the frame immediately following loading of the 08_{16} or 09_{16} code into the CMD register.

Here, the frame origin is counted starting with the VB falling edge. With code 08_{16}, the $\overline{WHITE}$ output recopies the BLK signal from the frame origin up to the rising edge on the LPCK input, or when VB starts rising again, if the LPCK input remains low for the entire frame. With code 09_{16}, the $\overline{WHITE}$ output is not activated.

The YLP address is 8-bit coded since there are 256 display lines in each frame. The XLP address is 6-bit coded since there are 64 display cycles in each line.

These 6 bits are left justified in the XLP register. XLP and YLP register contents match the write address if FMAT is low (or for the EF9366), but should be multiplied by 2 if FMAT is high, so as to be able to match the write address.

The address sampled into XLP corresponds to the current memory cycle. Dots detected by the light pen were addressed in the memory during the previous cycle. Hence, 1 should be subtracted from bit 2 in XLP register where the light pen electronic circuitry does not produce any additional delay.

If the rising edge on input LPCK occurs while VB is low, then the LSB in XLP is set high. This bit acts as a status signal which is reset to the low state by reading register XLP or YLP.

The rising edge first received (LPCK or VB) sets bit 0 in STATUS register high. An interrupt is initiated if bit 4 in CTRL1 is high.

When commands 08_{16} or 09_{16} have been decoded, bit 2 of the status register goes high (circuit ready for any further command) and bit 0 goes low (light pen operating sequence underway).

SCREEN BLANKING COMMANDS

Three commands (04_{16}, 06_{16}, 07_{16}) will set the whole display memory to a status corresponding to a "black display screen" condition. Another command ($0C_{16}$) may be used to set the whole memory to a status other than black (this condition being determined by bit 1 in register CTRL1).

The 4 commands outlined above use the planned scanning of the memory addresses achieved by the display stage. The X and Y registers are not affected by commands 04_{16} and $0C_{16}$. Hence, the time required is that corresponding to one frame (EF9366 or FMAT low) or two frames (FMAT high). The time corresponding to the completion of the frame currently executing when the CMD register is loaded, should be added to the above time.

For the screen blanking process, the frame origin is counted starting with the VB falling edge.
The only signals affected here are the $\overline{DW}$ output, which remains low when VB is low, and the DIN output which is forced high where the 04_{16}, 06_{16} and 07_{16} commands are entered.

Such commands are activated without requiring action by WO input or bit 2 in register CTRL1. While these commands are executing, bit 2 in STATUS register remains low.

EXTERNAL REQUEST FOR DISPLAY MEMORY ACCESS ($\overline{MFREE}$ OUTPUT)

On writing code $0F_{16}$ into the CMD register, the $\overline{MFREE}$ output is set low by the circuitry, during the next free memory cycle.

Apart from the display and refresh periods, this cycle is the first complete cycle that occurs after input $\overline{E}$ is reset high.

During this cycle, those addresses output on DAD and MSL correspond to the X and Y register contents : $\overline{DW}$ is high, $\overline{ALL}$ is high.

Should the memory be engaged in a display or refresh operation, (which is the case when $\overline{ALL}$ is low), then this cycle is postponed to be executed after $\overline{ALL}$ is reset high. The maximum waiting time is thus 64 cycles.

The $\overline{MFREE}$ signal may be used e. g. for performing a read or write operation into a register located between the display memory and the microprocessor bus.

INTERRUPTS OPERATION

An interrupt may be initiated by three situations denoted by internal signals :

- Circuit ready for a further command
- Vertical blanking signal
- Light pen sequence completed.

These three signals appear in real time in the STATUS register (bits 0, 1, 2). Each signal is cross-referenced to a mask bit in the register CTRL1 (bits 4, 5, 6).

If the mask bit is high, the first rising edge that occurs on the interrupt initiating signal sets the related interrupt flip-flop circuit high.

The outputs from these three flip-flop circuits appear in the STATUS register (bits 4, 5, 6). If one flip-flop circuit is high, bit 7 in the STATUS register is high, and pin $\overline{IRQ}$ is forced low.

A read operation in the STATUS register resets its 4 MSBs low, after input $\overline{E}$ is reset high.

The three interrupt control flip-flops are duplicated to prevent the loss of an interrupt coming during a read cycle of the STATUS register.

The status of bits 4, 5 and 6 corresponds to the interrupt control flip-flop circuit output, before input $\overline{E}$ goes low.

An interrupt coming during a read cycle of the STATUS register does not appear in bits 4, 5 and 6 during this read sequence, but during the following one. However, it may appear in bits 0, 1, 2 or on pin $\overline{IRQ}$.

TABLE 1 – REGISTER ADDRESS

ADDRESS REGISTER					REGISTER FUNCTIONS		Number of bits
Binary				Hexa	Read R/$\overline{W}$ = 1	Write R/$\overline{W}$ = 0	
A3	A2	A1	A0				
0	0	0	0	0	STATUS	CMD	8
0	0	0	1	1	CTRL 1 (Write control and interrupt control)		7
0	0	1	0	2	CTRL 2 (Vector and symbol type control)		4
0	0	1	1	3	CSIZE (Character size)		8
0	1	0	0	4	Reserved		—
0	1	0	1	5	DELTAX		8
0	1	1	0	6	Reserved		—
0	1	1	1	7	DELTAY		8
1	0	0	0	8	X MSBs		4
1	0	0	1	9	X LSBs		8
1	0	1	0	A	Y MSBs		4
1	0	1	1	B	Y LSBs		8
1	1	0	0	C	XLP (Light-pen)	Reserved	7
1	1	0	1	D	YLP (Light-pen)	Reserved	8
1	1	1	0	E	Reserved		—
1	1	1	1	F	Reserved		—

Reserved : These addresses are reserved for future versions of the circuit. In read mode, output buffers D0 D7 force a high state on the data bus.

TABLE 2 – COMMAND REGISTER

b7 b6 b5 b4 / b3 b2 b1 b0		0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0	0	Set bit 1 of CTRL1 : Pen selection	Vector generation (for b2, b1, b0 see small vector definition)	SPACE	0	@	P	`	p								
0 0 0 1	1	Clear bit 1 of CTRL 1 : Eraser selection		!	1	A	Q	a	q								
0 0 1 0	2	Set bit 0 of CTRL1 : Pen/Eraser down selection		"	2	B	R	b	r								
0 0 1 1	3	Clear bit 0 of CTRL 1 : Pen/Eraser up selection		#	3	C	S	c	s								
0 1 0 0	4	Clear screen		$	4	D	T	d	t								
0 1 0 1	5	X and Y registers reset to 0		%	5	E	U	e	u								
0 1 1 0	6	X and Y reset to 0 and clear screen		&	6	F	V	f	v								
0 1 1 1	7	Clear screen, set CSIZE to code "minsize" All other registers reset to 0 (except XLP, YLP)		'	7	G	W	g	w								
1 0 0 0	8	Light-pen initialization (WHITE forced low)	Special direction vectors (for b2, b1, b0 see small vector definition)	(	8	H	X	h	x								
1 0 0 1	9	Light-pen initialization		)	9	I	Y	i	y								
1 0 1 0	A	5 x 8 block drawing (size according to CSIZE)		*	:	J	Z	j	z								
1 0 1 1	B	4 x 4 block drawing (size according to CSIZE)		+	;	K	[	k	{								
1 1 0 0	C	Screen scanning : Pen or Eraser as defined by CTRL1		,	<	L	\	l	¦								
1 1 0 1	D	X register reset to 0		–	=	M	]	m	}								
1 1 1 0	E	Y register reset to 0		.	>	N	↑	n	¬								
1 1 1 1	F	Direct image memory access request for the next free cycle.		/	?	O	←	o	▒								

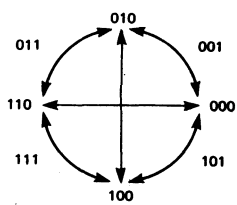
SMALL VECTOR DEFINITION :

b7	b6 b5	b4 b3	b2 b1 b0
1	|Δx|	|Δy|	Direction

Dimension

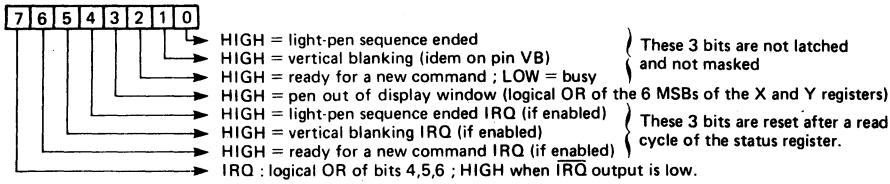
Δx or Δy		Vector length
0	0	0 step
0	1	1 step
1	0	2 steps
1	1	3 steps

Direction

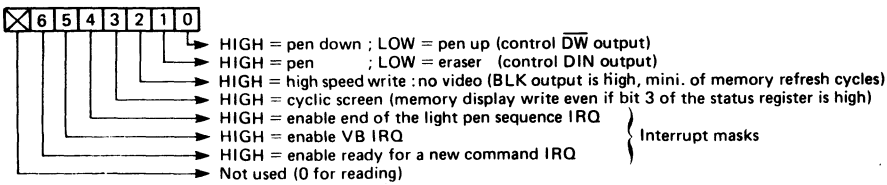


OTHER REGISTERS

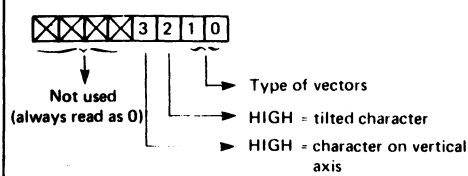
STATUS REGISTER (Read only)



CONTROL REGISTER 1 (Read/Write)

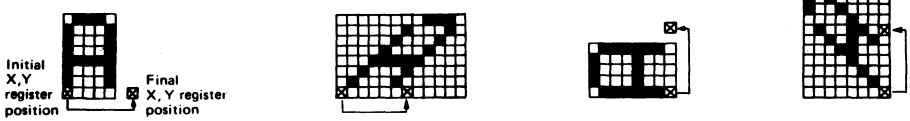


CONTROL REGISTER 2 (Read/Write)



b1	b0	Type of vectors	
0	0	——— continuous	
0	1	------- dotted	2 dots on, 2 dots off
1	0	– – – dashed	4 dots on, 4 dots off
1	1	—·—· dotted-dashed	10 dots on, 2 dots off, 2 dots on, 2 dots off.

Types of character orientations

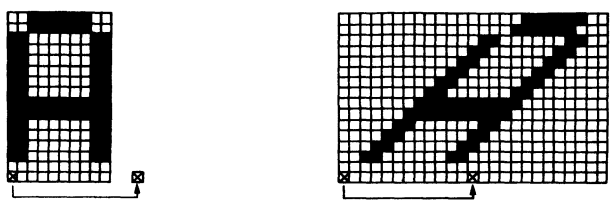


$b_3 = 0, b_2 = 0$ CSIZE = 11_{16}

$b_3 = 0, b_2 = 1$ CSIZE = 11_{16}

$b_3 = 1, b_2 = 0$ CSIZE = 11_{16}

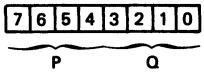
$b_3 = 1, b_2 = 1$ CSIZE = 11_{16}



$b_3 = 0, b_2 = 0$ CSIZE = 22_{16}

$b_3 = 0, b_2 = 1$ CSIZE = 22_{16}

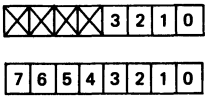
C-SIZE REGISTER (Read/Write)



P : Scaling factor on X axis
Q : Scaling factor on Y axis

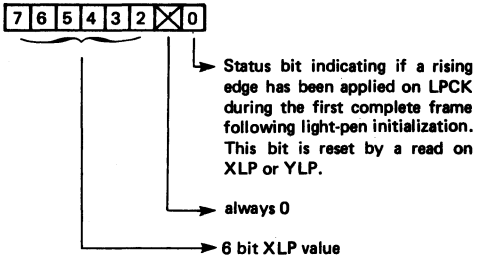
P and Q may take any value between 1 and 16. This value is given by the leftmost or rightmost 4 bits for P and Q respectively. Binary value (0) means 16.

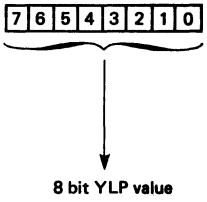
X AND Y REGISTERS (Read/Write)



The 4 leftmost MSBs are always 0.

XLP and YLP REGISTERS

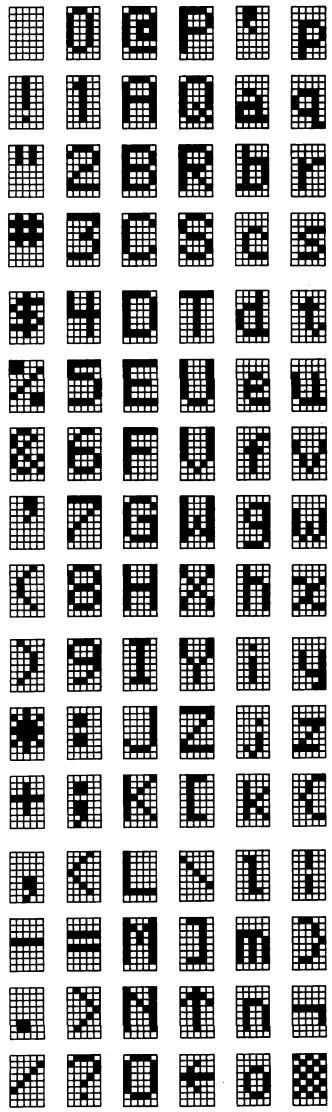




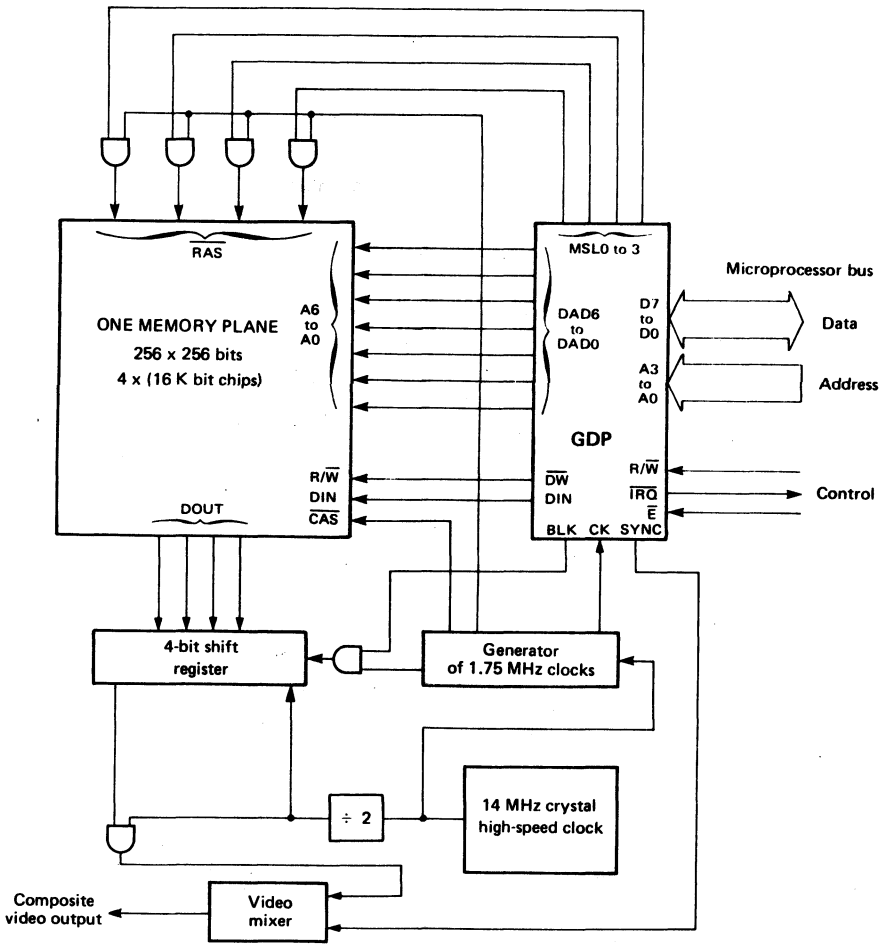
ASCII CHARACTER GENERATOR (5 x 8 matrix)

b7	0	0	0	0	0	0
b6	0	0	1	1	1	1
b5	1	1	0	0	1	1
b4	0	1	0	1	0	1

b3	b2	b1	b0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

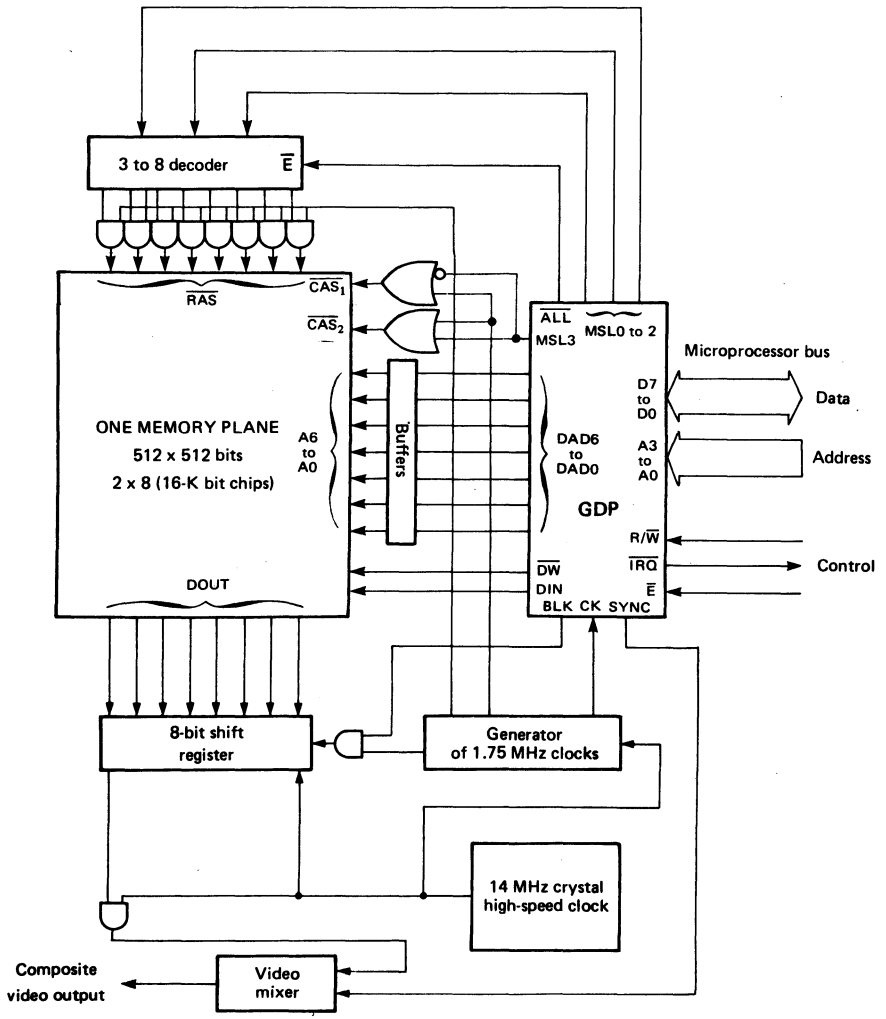


EXAMPLE OF AN APPLICATION OF THE EF9365 : 256 x 256 BLACK AND WHITE



Note : FMAT = V_{SS}

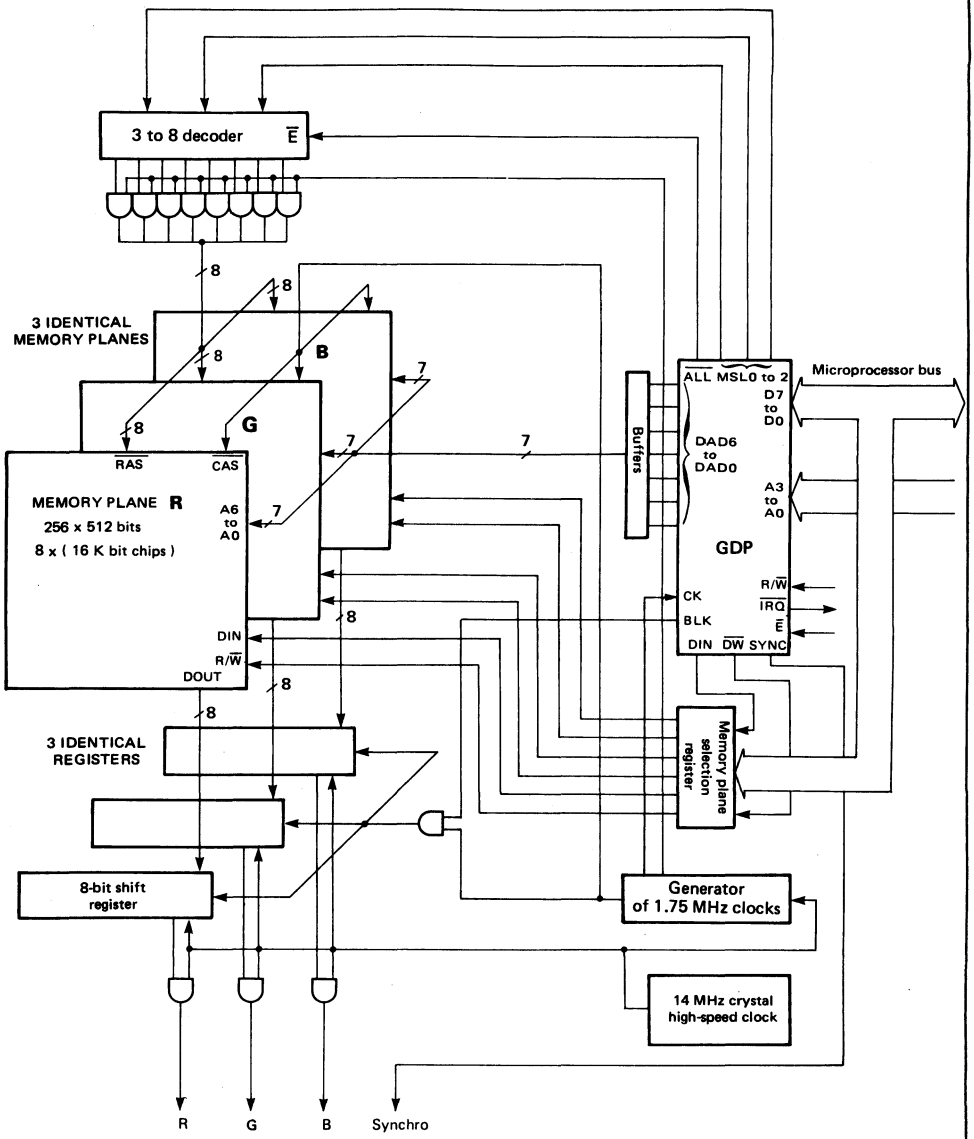
EXAMPLE OF AN APPLICATION OF THE EF9365 : 512 x 512 BLACK AND WHITE



Note : FMAT = V_{CC}

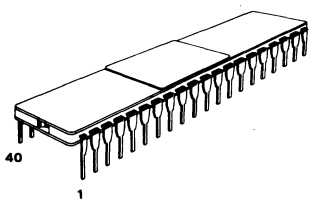
EXAMPLE OF AN APPLICATION OF THE EF9366 : 256 x 512 COLOUR

Eight colours may be obtained from the three basic colours red (R), green (G), blue (B)

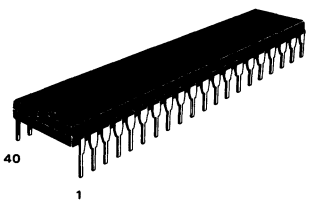


Note : FMAT = V_{CC}

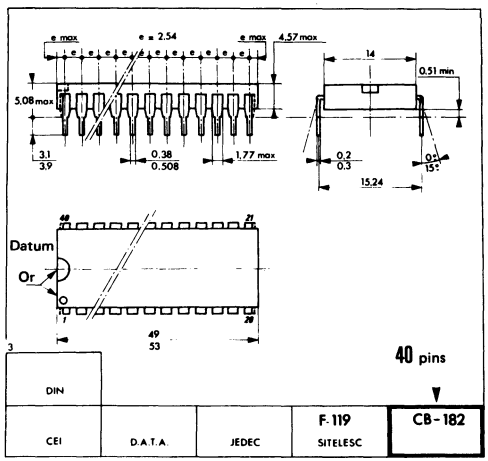
CASE CB-182



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

EF9367

ADVANCE INFORMATION

GRAPHIC DISPLAY PROCESSOR (GDP)

This GDP is a true high resolution graphic display processor, which contains all the functions required to process vector generation at a very high speed and to generate all the timing signals required for interfacing interlaced or non interlaced video data on a raster scan CRT display compatible with 525 line or the CCIR 625 line standards.

The GDP's main features are :

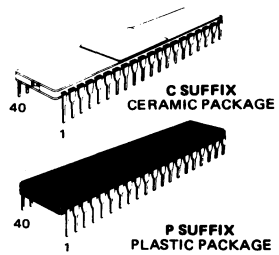
- Selectable resolutions in black and white or color :
  Vertical resolution : 525 line monitor (208 or 416). 625 line monitor (256 or 512).
  Horizontal resolution : 256, 320*, 384*, 512, 640*, 768*, 1024, full screen. (*) with external PROM.
- High speed vector plot well suited to animation - 4 types of lines.
- Multiplexed address and refresh for 16K or 64K dynamic RAMs.
- No limitation on the number of selectable memory planes (colors, grey levels or any other attributes)
- Multipage application capability
- On-chip full ASCII character generator (96) - maximum alphanumeric screen density : 170 x 57 - programmable sizes and orientations
- Direct interfacing with the monitor through the composite synchro and blanking signals
- Automatic allocation of display memory in refresh, write, dump, and display cycles
- Light pen registers and control signals
- Three types of interrupt requests
- Fully static design
- TTL compatible I/O
- Single + 5 volt supply.

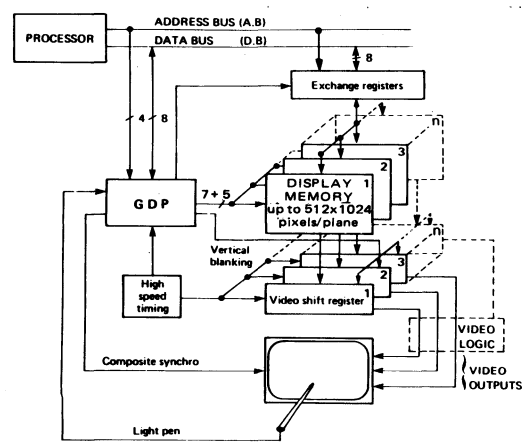
MOS

(N - CHANNEL, SILICON-GATE)

GRAPHIC DISPLAY PROCESSOR (GDP)

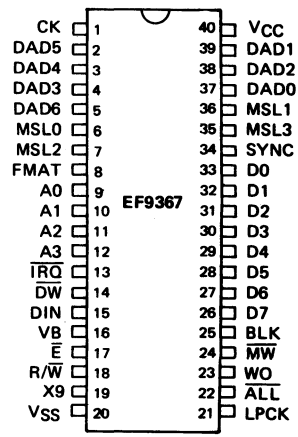
CASE CB-182





TYPICAL APPLICATION

PIN ASSIGNMENT

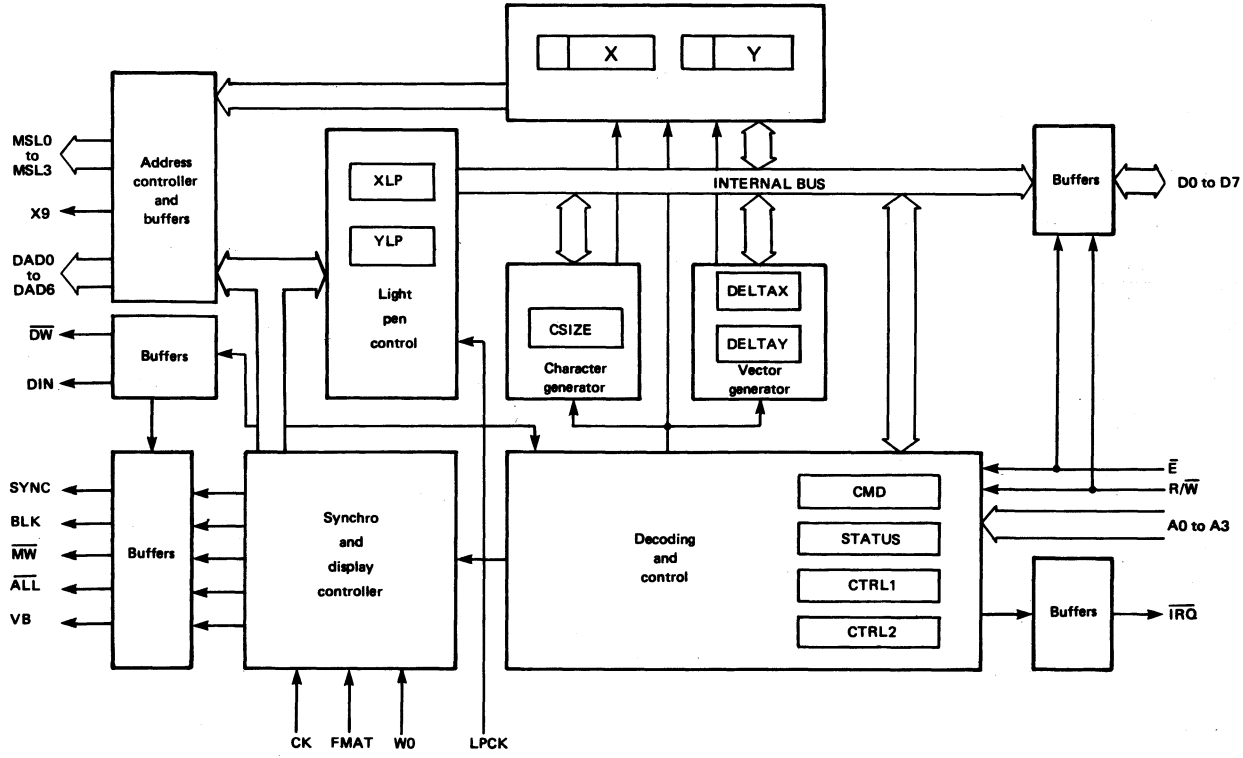


SP8248R2-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

BLOCK DIAGRAM



GENERAL DESCRIPTION

Developed using NMOS technology, the GDP is an intelligent raster scan video display controller, fully programmable via an eight-bit microprocessor bus. Besides all the timing logic functions required to generate the video, sync and blanking signals, the GDP includes two hardwired display processors : a vector and a character generator.

This unique feature allows an ultrafast screen writing speed (the 1024 dot diagonal may be written in less than 1.4 ms) at almost no microprocessor processing cost.

The GDP is particularly well-suited to all applications in which the display memory is not directly addressed by the MPU. This feature allows a total asynchronism between the MPU and the GDP memory cycles and preserves the whole MPU memory addressing space.

Nevertheless, where direct exchange between the microprocessor and the memory is necessary, the on-chip allocation controller will allow this exchange without display interference.

The GDP is programmable using 11 internal registers occupying 16 consecutive addresses. These registers can also be modified by the GDP's hardwired processors while a command is being executed.

Note : A summary of data codes and registers is given in the **Register address table.** Hexadecimal values are subscripted 16 and the register bits are numbered as follows :

MSB	7	6	5	4	3	2	1	0	LSB

MAXIMUM RATINGS

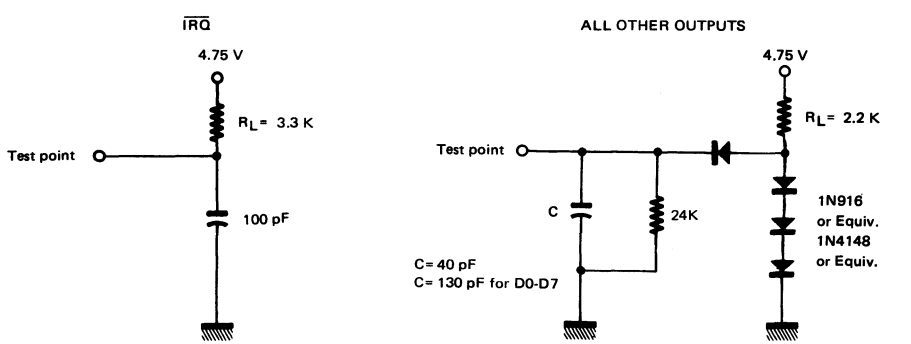
Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.3 to+ 7.0	V
Input voltage	V_{in}	−0.3 to+ 7.0	V
Operating temperature	T_A	0 to+ 70	°C
Storage temperature	T_{stg}	− 55 to+150	°C

The GDP inputs are protected against high static voltages and electric fields ; nevertheless, normal precautions should be taken to avoid voltages above the limit values on this high impedance circuit.

STATIC ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V ± 5 %, V_{SS} = 0, T_A = 0 to 70° C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage except CK	V_{IH}	V_{SS}+ 2.2	–	V_{CC}	V
Input high voltage CK	V_{IHCK}	V_{SS}+ 3.5	–	V_{CC}	V
Input low voltage	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Input leakage current (V_{in}= 0 to 5.25 V, V_{CC}= max)	I_{in}	–	1.0	2.5	µA
Output high voltage (I_{load}= −100 µA, V_{CC}=min)	V_{OH}	V_{SS} + 2.4	–	–	V
Output low voltage (I_{load}= 1.6 mA, V_{CC}= min)	V_{OL}	–	–	V_{SS} + 0.4	V
Supply current	I_{CC}	–	80	–	mA
Capacitance (V_{in} = 0, T_A = 25° C, f = 1.0 MHz)	C_{in}, C_{out}	–	–	12	pF

TEST LOADS

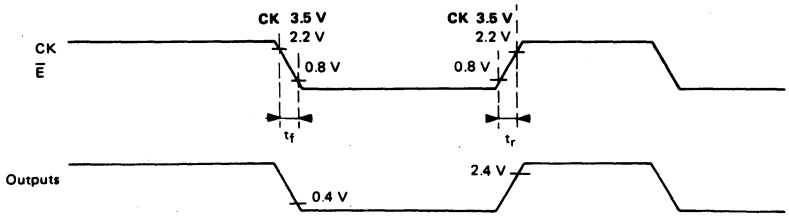


DYNAMIC OPERATING CONDITIONS

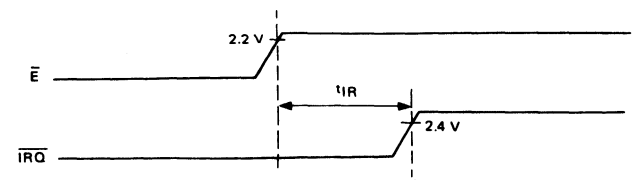
(V_{DD} = 5,0 V ± 5 %, V_{SS} = 0V ; T_A = 0 to + 70° C unless otherwise noted)

Time (ns)	Symbol	Min	Max
Clock period	t_{CK}	560	
CK pulse width, low	t_{CKL}	330	
CK pulse width, high	t_{CKH}	190	
CK low to valid DAD	CKLDAD		320
CK high to valid DAD	CKHDAD		180
CK low to valid SYNC	CKLSYNC		300
CK low to valid BLK	CKLBLK		310
CK low to valid VB	CKLVB		500
CK low to valid $\overline{ALL}$	CKLALL		300
CK low to valid $\overline{MSL}$	CKLMSL		300
CK low to valid $\overline{DW}$	CKLDW		310
CK low to valid $\overline{MFREE}$ low	CKLMFRL		330
CK low to valid $\overline{MFREE}$ high	CKLMFRH		500
CK low to valid DIN	CKLDIN		310
CK low to valid $\overline{IRQ}$	CKLIRQ		1500
CK low to valid $\overline{WHITE}$	CKLWHI		530
$\overline{E}$ pulse width, low	t_{EL}	450	
$\overline{E}$ pulse width, high	t_{EH}	430	
Address pre-setup time	t_{AS}	160	
Address hold time	t_{AH}	10	
Data pre-setup time (write)	t_{DSW}	195	
Data setup time (read)	t_{DDR}		320
Data hold time (read)	t_{DHR}	10	
$\overline{IRQ}$ release time	t_{IR}		1600
LPCK high to $\overline{WHITE}$ high (if command 08_{16})	LPHW		1600
LPCK high to $\overline{IRQ}$ low	LPHIRQ		1600
LPCK high hold time	t_{LPCKH}	150	
CK and $\overline{E}$ rise times	t_r		20
CK and $\overline{E}$ fall times	t_f		20

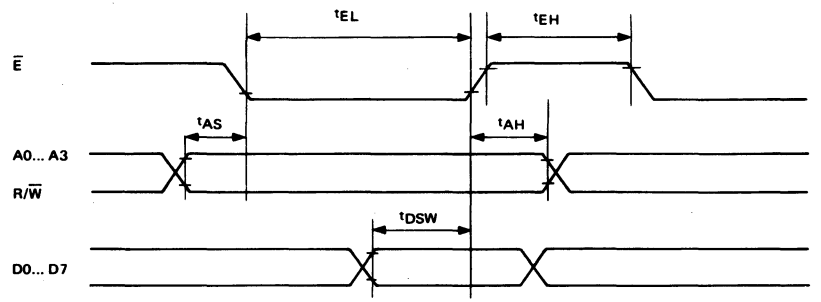
CLOCK AND OUTPUT CHARACTERISTICS



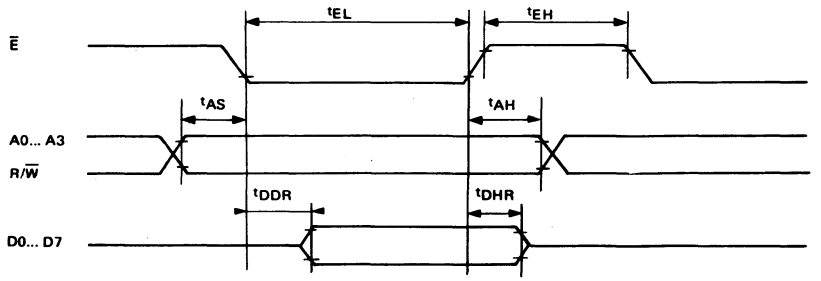
$\overline{IRQ}$ RELEASE TIME



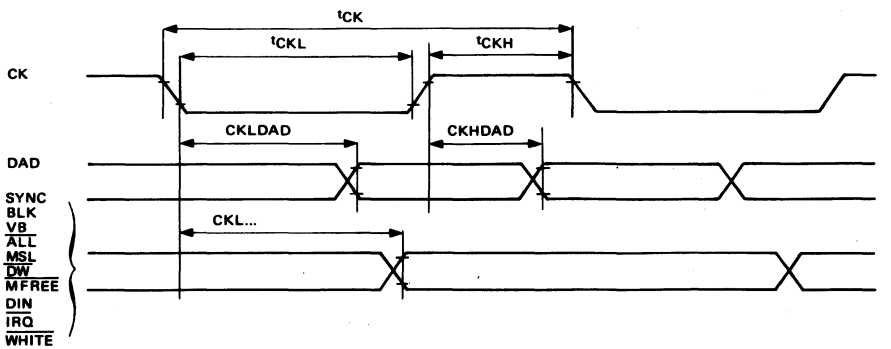
MICROPROCESSOR BUS, WRITE ACCESS



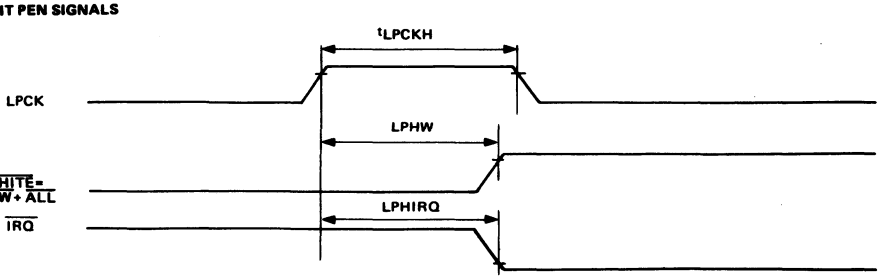
MICROPROCESSOR BUS, READ ACCESS



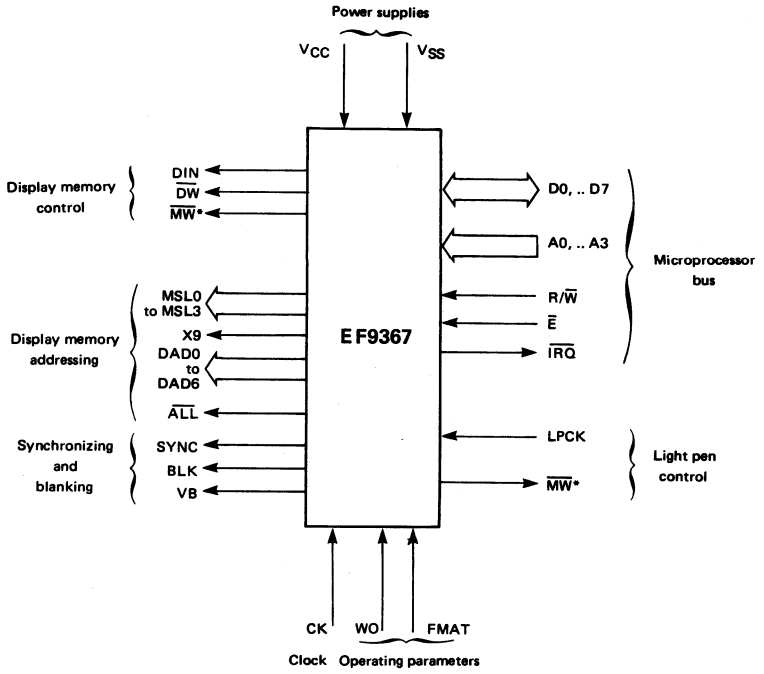
SYNCHRONOUS SIGNALS WITH CK INPUT



LIGHT PEN SIGNALS



PIN DESCRIPTION



*This pin outputs two items of data multiplexed by signal ALL.

POWER SUPPLY, CLOCK AND OPERATING PARAMETERS

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
V_{SS}	S	20	Power supply	Ground
V_{CC}	S	40	Power supply	+ 5 V
CK	I	1	Clock	Master clock. All internal processor states are modified on the falling edge of this signal. The whole circuit logic is static and the cycle of this clock needs only to be ajusted according to the shape and accuracy the synchronizing signals should feature. DAD memory address multiplexing signal. If CK is low, low addresses (or row addresses for the memory) are those that are output on DAD. The frequency of CK is a multiple of the image refresh frequency : - interlaced scanning : f (CK) = f (1/2 frame) x (625 or 525) x 96 - non-interlaced scanning : f (CK) = f (frame) x (312 or 262) x 96.
FMAT	I	8	Format	This pin is connected to V_{CC}, V_{SS}, CK or $\overline{CK}$ and sets the number of monitor and image lines : V_{CC} : 625 line monitor, interlaced synchronization, 512 lines displayed CK : 525 line monitor, interlaced synchronization, 416 lines displayed $\overline{CK}$: 525 line monitor, non-interlaced synchro, 208 lines displayed V_{SS} : 625 line monitor, non-interlaced synchro, 256 lines displayed.
WO	I	23	Write only	When WO is high, memory refresh nor display no longer exist. The hard wired write processors may operate without being interrupted. The $\overline{ALL}$ signal is always high.

SYNCHRONIZING AND BLANKING SIGNALS

SYNC	O	34	Video monitor synchronizing	Video monitor line and frame synchronization signal. For example, if CK is at 1.5 MHz and FMAT is high, signal SYNC is to CCIR 625 line 50 Hz standard. This output is independent of input WO and of register CTRL1.
BLK	O	25	Blanking	This signal is high apart from the display window (writing or refresh). It is always high if bit 2 in register CTRL1 is high, but it is not affected by the WO input.
VB	O	16	Vertical blanking	This signal is not affected by WO and register CTRL1. High during vertical blanking.

DISPLAY MEMORY ADDRESSING SIGNALS

DAD0 to DAD6	O	37,39, 38,4 3,2,5	Display address	Addresses that are multiplexed by the CK signal. Provided for the automatic refresh of the 16 K or 64 K dynamic memories.
X9	O	19	Memory address	Horizontal pointer extension bit for write operations (horizontal resolutions greater than 512).
MSL0 to MSL3	O	6,36 7,35	Memory select	Pixel write select signals (see section : **Display memory configuration.**)
$\overline{ALL}$	O	22	Access to all memory units	This signal makes it possible to discriminate between the collective memory accesses to all chips (display, refresh or erase), and the memory accesses to a single pixel for vector or character writing purposes. This signal is low for collective access.

DISPLAY MEMORY CONTROL SIGNALS

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
DIN	O	15	Display in	Selection of the memory data code corresponding to the display screen in the 'off' condition (active when high). For a black-and-white display (1 bit per pixel), DIN may directly be the storage entry data.
$\overline{DW}$	O	14	Display write	Display memory write signal. Active when low.
$\overline{MW}$	O	24	Memory available	This pin outputs $\overline{MFREE}$ and $\overline{WHITE}$ signals which are externally demultiplexed by signal $\overline{ALL}$: $\overline{MFREE} = \overline{MW} + ALL$; $\overline{WHITE} = \overline{MW} + \overline{ALL}$ **Memory free ($\overline{MFREE}$) :** Signal low during the next memory idle period following the $0F_{16}$ command. This signal allows exchanges between the microprocessor and the X and Y flagged memory segment without affecting the display. **Forcing to white level ($\overline{WHITE}$) :** Forces white level on video signal, for use of the light pen. Active when low.

MICROPROCESSOR BUS SIGNALS

D0-D7	I/O	33 to 26	Data bus	I/O buffers opening is controlled through $\overline{E}$, and the related direction through R/$\overline{W}$.
A0-A3	I	9 to 12	Address bus	Address of the register involved in microprocessor access.
R/$\overline{W}$	I	18	Read/write signal	Read/write signal. Write when low.
$\overline{E}$	I	17	Enable	Bus exchange synchronizing and enabling signal.
$\overline{IRQ}$	O	13	Interrupt request	Interrupt request towards the microprocessor, programmable through register CTRL1. Open drain output.

LIGHT PEN OPERATING SIGNALS

LPCK	I	21	Light pen strobe	Light pen input. When the mechanism is set, a rising edge loads into registers XLP and YLP the current display address and sets the XLP register's LSB high.

REGISTER DESCRIPTION

X AND Y REGISTERS (Addresses : 8_{16}, 9_{16}, A_{16}, B_{16})

The X and Y registers are 12-bit read-write registers. They indicate the position of the next dot to be written into the display memory. They have no connection at all with the video signal generating scan, but they point the write address, in the same way as the pen address on a plotter.

These 2 registers are incremented or decremented, prior to each write operation into the display memory, by the internal vector and character generators, or they may be directly positioned by the microprocessor.

This 2 x 12 bit write address covers a 4096 x 4096 point addressing space. Only the LSBs are used here, since the maximum definition of the picture actually stored is 512 x 1024 pixels (picture elements).

In practice, the GDP assumes that it has a memory space of 1024 x 512 (FMAT = V_{CC} or CK) or 1024 x 256 (FMAT = V_{SS} or $\overline{CK}$) and disables writing outside this space, unless bit 3 of CTRL 1 is set.

The above features along with the relative mode description of all picture component elements make it possible to automatically solve the great majority of edge cut-off problems.

DELTAX AND DELTAY REGISTERS (Addresses : 5_{16}, 7_{16}).

The DELTAX and DELTAY registers are 8-bit read-write registers. They indicate to the vector generator the projections of the next vector to be plotted, on the X and Y axes respectively. Such values are unsigned integers. The plotting of a vector is initiated by a write operation in the command register (CMD).

CSIZE REGISTER (Address : 3_{16})

The CSIZE register is an 8-bit read-write register. It indicates the scaling factors of X and Y registers for the symbols and characters. 98 characters are generated from a 5 x 8 pixel matrix defined by an internal ROM. In the standard version, it contains the alphanumeric characters in the ASCII code which may be printed, together with a number of special symbols.

Each symbol can be increased by a factor P(X) or Q(Y). These factors are independent integers which may each vary from 1 to 16 and which are defined by the CSIZE register. The symbol generation sequence is started after writing the ASCII code of the symbol to be represented in the CMD register.

CTRL1 REGISTER (Address : 1_{16}).

The CTRL1 register is a 7-bit read-write register, through which the general circuit operation may be fed with the required parameters.

Bit 0 : When low, this bit inhibits writing in display memory (equivalent to pen or eraser up).
When high, this bit enables writing in display memory (pen or eraser down).
This bit controls the $\overline{DW}$ output.

Bit 1 : When low, this bit selects the eraser.
When high, this bit selects the pen.
This bit controls the DIN output.

Bit 2 : When low, this bit selects normal writing mode (writing apart from the display and refresh periods, which are a requirement for the dynamic storages) in display memory.
When high, this bit selects the high speed writing mode : the display periods are deleted. Only the dynamic storage refresh periods are retained.

Bit 3 : When low, this bit indicates that the 4096 x 4096 space is being used (the 12 X and Y bits are significant)
When high, this bit selects the cyclic screen operating mode.

Bit 4 : When low, this bit inhibits the interrupt triggered by the light pen sequence completion.
When high, this bit enables the interrupt.

Bit 5 : When low, this bit inhibits the interrupt release by vertical blanking.
When high, this bit enables the interrupt.

Bit 6 : When low, this bit inhibits the interrupt indicating that the system is ready for a new command.
When high, this bit enables the interrupt.

Bit 7 : Not used. Always low in read mode.

CTRL2 REGISTER (Address : 2_{16})

The CTRL2 register is a 4-bit read/write register, through which the plotting of vectors and characters may be denoted by parameters.

Bit 0, 1 : These 2 bits define 4 types of lines (continuous, dotted, dashed, dash-dotted).

Bit 2 : When low, this bit defines straight writing.
When high, it defines tilted characters.

Bit 3 : When low, this bit defines writing along an horizontal line.
When high, this bit defines writing along a vertical line.

Bit 4, 5, 6, 7 : Not used. Always low in read mode.

CMD COMMAND REGISTER (Address : 0_{16})

The CMD register is an 8-bit write-only register. Each write operation in this register causes a command to be executed, upon completion of the time necessary for synchronizing the microprocessor access and the GDP's CK clock.

Several types of command are available :

- vector plotting
- character plotting
- screen erase
- light pen circuitry setting
- access to the display memory through an external circuitry.
- indirect modification of the other registers (commands that make it possible for the X, Y, DELTAX, DELTAY, CTRL1, CTRL2 and CSIZE registers to be amended or scratched).

STATUS REGISTER (Address 0_{16} or F_{16})

The STATUS register is an 8-bit read-only register. It is used to monitor the status of the executing statements entered into the circuit, and more specifically to avoid the need for modifying a register that is already used for the command currently executing.

Bit 0 : When low, this bit indicates that a light pen sequence is currently executing.
When high, it indicates that no light pen sequence is currently executing.

Bit 1 : This bit is high during vertical blanking. It is the VB signal recopy.

Bit 2 : When low, this bit indicates that a command is currently executing.
When high, this bit indicates that the circuit is ready for a new command.

Bit 3 : This bit when low indicates that registers X and Y are pointing within the assumed memory space.
This bit is obtained by applying the logical OR function to the unused most significant bits of registers X and Y.
If FMAT = V_{CC} or CK, the assumed memory space is 1024 x 512.
If FMAT = V_{SS} or $\overline{CK}$, the assumed memory space is 1024 x 256.

Bit 4 : When high, this bit indicates that an interrupt has been initiated by the completion of a light pen running sequence and that this interrupt has been enabled by bit 4 in CTRL1 register.

Bit 5 : When high, this bit indicates that an interrupt has been initiated by vertical blanking and that this interrupt has been enabled by bit 5 in CTRL1 register.

Bit 6 : When high, this bit indicates that an interrupt has been initiated by the completion of execution of a command and that this interrupt has been enabled by bit 6 in CTRL1 register.

Bit 7 : When high, this bit indicates that an interrupt has been initiated. It is the logic OR of bits 4, 5 and 6 in STATUS register. The $\overline{IRQ}$ output state is always the opposite of the status of this bit.

Note : Bits 4, 5, 6 and 7 are reset low by reading the STATUS register at address 0_{16}. Reading at address F_{16} does not modify their state.

XLP AND YLP REGISTERS (Addresses C_{16} and D_{16})

The XLP and YLP registers are read-only registers, with 7 and 8 bits respectively. Upon completion of a light pen running sequence, they contain the display address sampled by the first edge appearing rising on the LPCK input. The use of such registers is discussed in section : **Use of light pen circuitry.**

NOTES :

1. All internal registers may be read or written at any time by the microprocessor. However, the precautions outlined below should be observed :

   — Do not write into the CMD register if execution of the previous command is not completed (bit 2 of STATUS register).

   — Do not alter any register if it is used as an input parameter for the internal hardwired systems (e. g. : modifying the DELTAX register while a vector plotting sequence is in progress).

   — Do not read a register that is being asynchronously modified by the internal hardwired systems (e. g. : reading the X register while a vector plotting sequence is in progress may be erroneous if CK and $\overline{E}$ are asynchronous).

2. On powering up, the writing devices may have any status. Before entering a command for the first time, it is necessary to wait until all functions currently underway are completed, which information can be derived from the STATUS register.

SYSTEM OPERATING PRINCIPLE

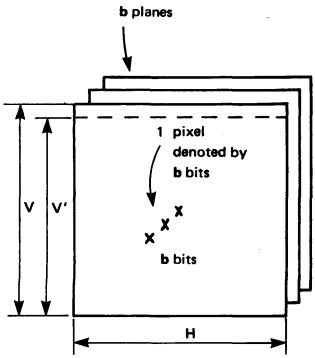
DISPLAY MEMORY CONFIGURATION

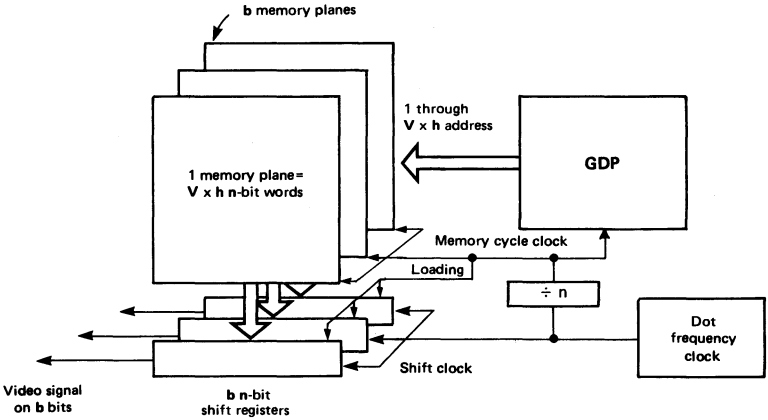
Assume a V x H pixel picture. Assume that each pixel is able to adopt 2^b different states. A V x H x b bit display memory is thus required.

In those applications where H features a high value, the video signal frequency exceeds the maximum frequency of memory read access.

Example : H = 512 with a television line frequency : the pixel succession period on the video signal is 83 ns.

It is mandatory that a line of H dots be cut into h adjoining segments of n bits each, read at the same time in the display memory, and thereafter converted to serial form to produce the video signal. h memory accesses per line are necessary. Each access loads b n-bit shift registers. The memory contains V x h x b n-bit words.





The EF9367 is designed for the following stored image formats :

- V = 512 or 256 (50 Hz)
- V' = 416 or 208 (60 Hz)
- H = h x n
- H = 1024 or lower multiples of 64
- h = 64
- n = 16, 8, 4, 2, 1 (or any value below 16 using external PROM encoding)
- b = any value (addressing is same for all memory planes, management of these planes is external to the GDP).

In so far as the overflow tests are concerned, the circuit assumes that it still has the maximum memory space for X (1024). The test for Y is effected in the following memory spaces :

512 if FMAT = V_{CC} or $\overline{CK}$
256 if FMAT = V_{SS} or $\overline{CK}$

512 or 256 vertical resolution : the displayed space is identical to the space in memory (unless a greater memory capacity is deliberately selected).

416 or 208 vertical resolution : the displayed space is smaller than the memory space.

Lines not displayed are displayable using an external adder to dejustify the display addresses (this arrangement may be used for smooth roll-up/roll down.

DAD AND MSL OUTPUT STATUS TABLES

The internal counters which address the display memory are made up of :

- 6 horizontal address bits (h = 64)
  $h_0, h_1, h_2, h_3, h_4, h_5$ (h_0 = LSB)
- 9 vertical address bits (V ⩽ 512)
  t, $V_0, V_1, V_2, V_3, V_4, V_5, V_6, V_7$

t is here the LSB. It denotes the line parity and changes every frame because of interlaced scan. Within a same frame, V_0 denotes the LSB.

The write address is made up of the LSBs of the X and Y internal registers.

$X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_9$
$Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7, Y_8$

The GDP produces addressing signals in the sequences shown in the tables opposite :

FMAT = V_{CC} or CK

		MSL				X_9	DAD						
$\overline{ALL}$	CK	0	1	2	3		0	1	2	3	4	5	6
0	0	X_0	X_1	X_2	V_1	X_9	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1						V_7	V_6	V_5	V_4	V_3	V_2	t
1	0	X_0	X_1	X_2	Y_2	X_9	X_8	X_7	X_6	X_5	X_4	X_3	Y_1
1	1						Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_0

FMAT = V_{SS} or $\overline{CK}$

		MSL				X_9	DAD						
$\overline{ALL}$	CK	0	1	2	3		0	1	2	3	4	5	6
0	0	X_0	X_1	X_2	1	X_9	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1						V_7	V_6	V_5	V_4	V_3	V_2	V_1
1	0	X_0	X_1	X_2	1	X_9	X_8	X_7	X_6	X_5	X_4	X_3	Y_0
1	1						Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

DESCRIPTION OF DISPLAYABLE FORMATS

NON INTERLACED SCANNING

256 x 512 or 208 x 512 pixel formats (H = 512, n = 8)

Input FMAT must be low or connected to $\overline{CK}$.
The memory is made up of 16 K bytes per memory plane. The byte address is made up of 14 bits which are output on two runs on the DAD pins. The three MSL0, MSL1, MSL2 outputs are used to select one pixel out of the eight featuring the same address. They issue the number of the pixel, encoded on three bits. MSL3 is high, and is not used.

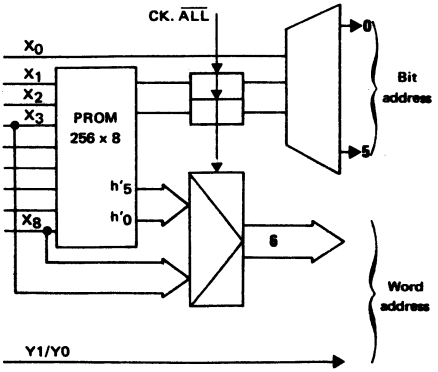
256 x 384 or 208 x 384 pixel formats (H = 384, n = 6)

Input FMAT must be low or connected to $\overline{CK}$.
The memory is organized as 16 K words x 6 bits.

The signals produced by the chip in the sequence indicated for the 256 x 512 format are transcoded externally as shown in the opposite diagram.

256 x 320 or 208 x 320 pixel formats (H = 320, n = 5)

The same schematic as for 384 horizontal resolution should be used with a memory organized in 5 bit words.



256 x 256 or 208 x 256 pixel formats (H = 256, n = 4)

Input FMAT must be low or connected to $\overline{CK}$.
The memory is made up of 16 K words x 4 bits. The word address is made up of 14 bits which are output in two runs on the DAD pins. One of the four chips is selected by decoding pins MSL1 and MSL2 (that leads to ignore X_0 : the X computation space is changed to 2048 pixels and horizontal overflow detected at 512 pixels).

INTERLACED SCANNING

512 x 1024 or 416 x 1024 pixel formats (H = 1024, n = 16)

Input FMAT must be connected to V_{CC} or CK.
The memory comprises 32 K words x 16 bits, organized in two blocks of 16 K words each.

The signals produced by the circuit in the sequence indicated for the 512 x 512 format are combined externally as shown at the end of the data sheet.

512 x 768 or 416 x 768 pixel formats (H = 768, n = 12)

Input FMAT must be connected to V_{CC} or CK.
The memory comprises 32 K words x 12 bits, organized in two blocks of 16 K words each.

The signals produced by the chip in the sequence indicated for the 512 x 512 format are transcoded externally as shown in the diagram below.

512 x 640 or 416 x 640 pixel formats (H = 640, n = 10)

The same schematic as below should be used with a memory organized in 10 bit words.

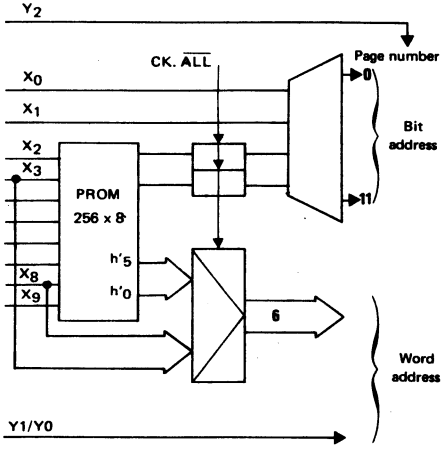
512 x 512 or 416 x 512 pixel formats (H = 512, n = 8)

The FMAT input should be tied to V_{CC} or CK. The memory is made up of V x h bytes = 32 K bytes per memory plane.

The byte address is made up of 15 bits :

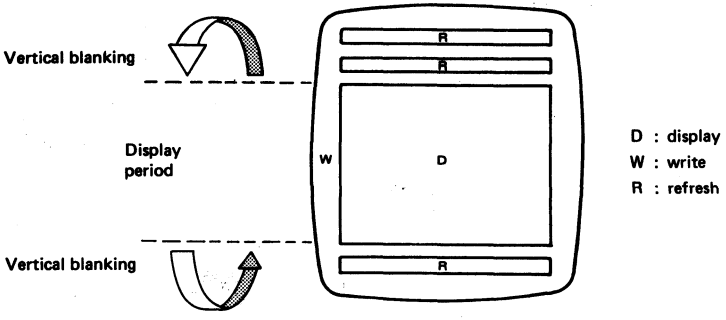
- 14 are output in 2 runs on the DAD pins for the purpose of using 16 K x 1 bit dynamic RAMs,
- the 15th one is output on pin MSL3.

The 3 MSL0, 1 and 2 outputs allow to select one pixel out of the 8 featuring the same address, for pixel-to-pixel write applications. They issue the number of the involved pixel, encoded on 3 bits.



MEMORY OPERATION SEQUENCE ALONG ONE FRAME

Apart from the window where the memory is used for display purposes exclusively, write operations may be performed, except during 3 refresh periods.



The three period types, D, W and R, respectively, are indicated outside the circuit through the BLK and $\overline{ALL}$ signals :

	BLK	$\overline{ALL}$
D	0	0
W	1	1
R	1	0

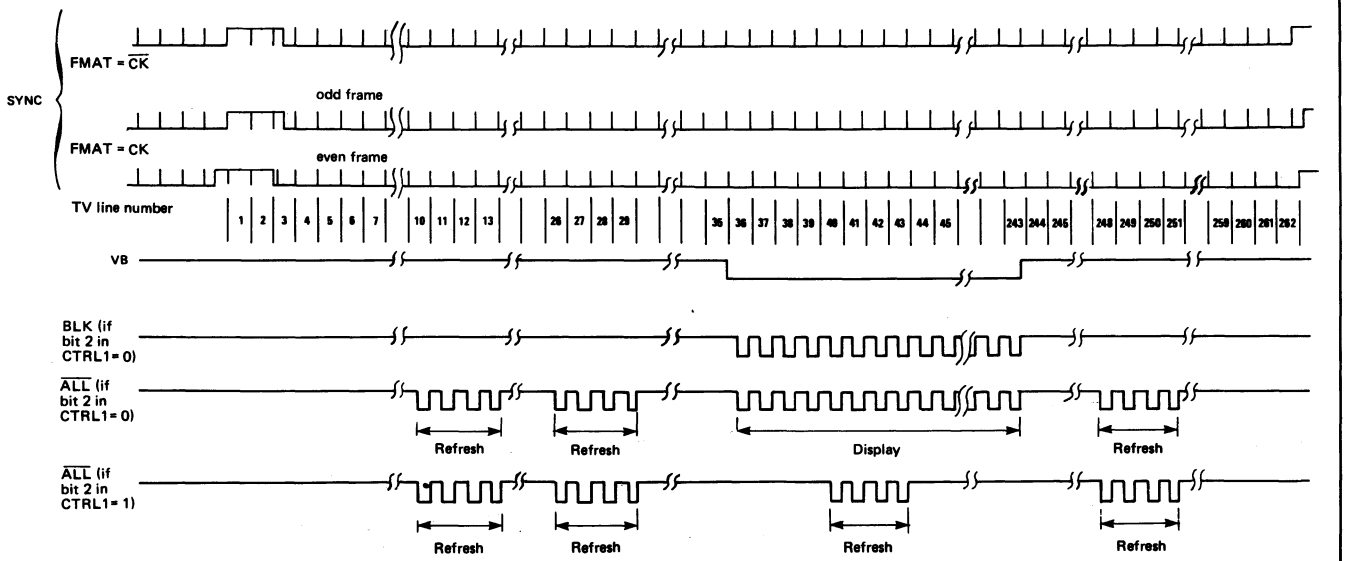
The refresh of dynamic RAMs is automatically performed by the GDP. During display, the memory is entirely refreshed each 4 lines (256 accesses).
During vertical blanking, 3 refresh cycles of 4 lines each are executed.

Exceptions :

- If bit 2 in register CTRL1 is high (high speed write), the display period is suppressed and 19 refresh cycles of 4 lines each are executed during one frame.
- As long as the WO input is high, the circuit is set to write mode, and BLK retains the same outline as it has under normal operating conditions.

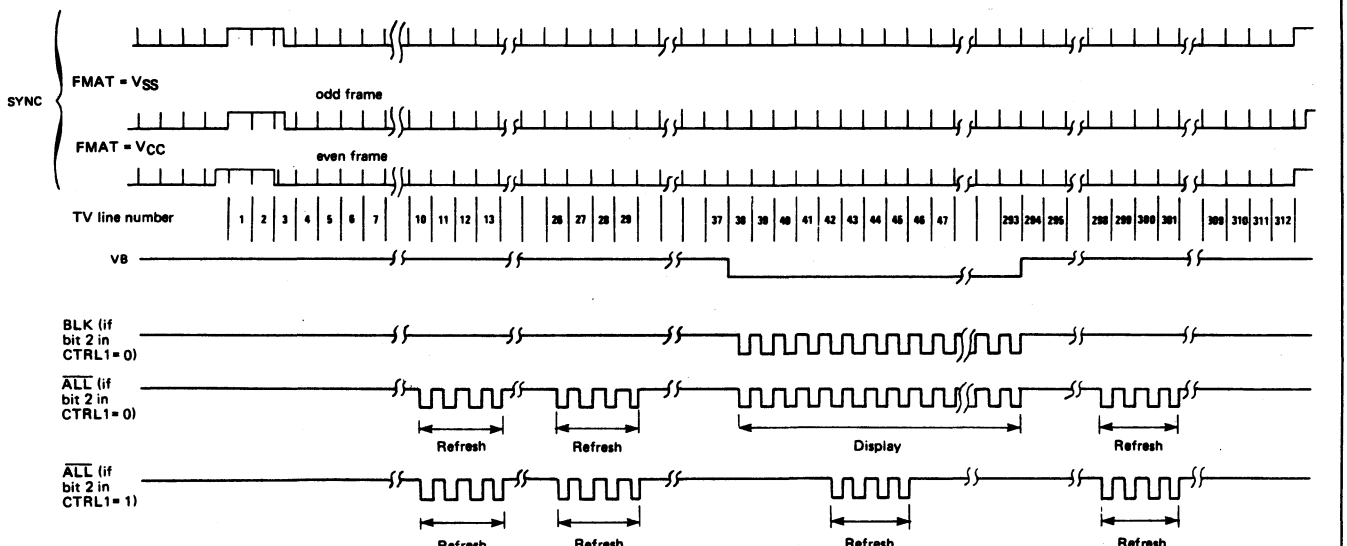
  In these two cases, executing codes 04_{16}, 06_{16}, 07_{16} and $0C_{16}$ triggers a complete D sequence for a high-speed scan of all addresses. This lasts two frames if FMAT is high (or tied to CK) and one frame if FMAT is low (or tied to $\overline{CK}$).

FRAME SEQUENCE – 525 LINE SYNCHRONIZATION



Note : $\overline{ALL}$ signal high denotes write periods.

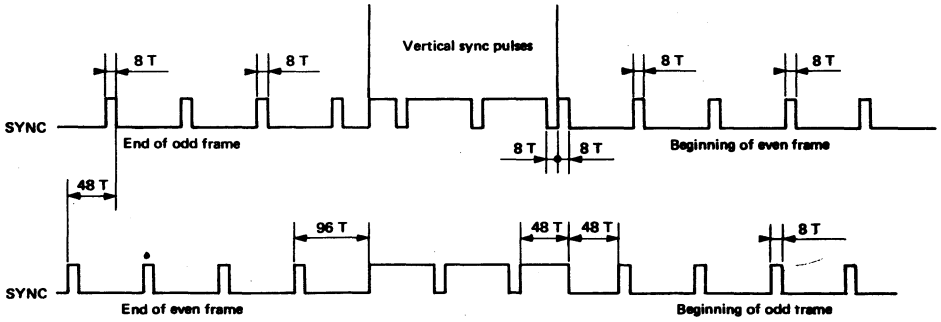
FRAME SEQUENCE – 625 LINE SYNCHRONIZATION



Note : $\overline{ALL}$ signal high denotes write periods.

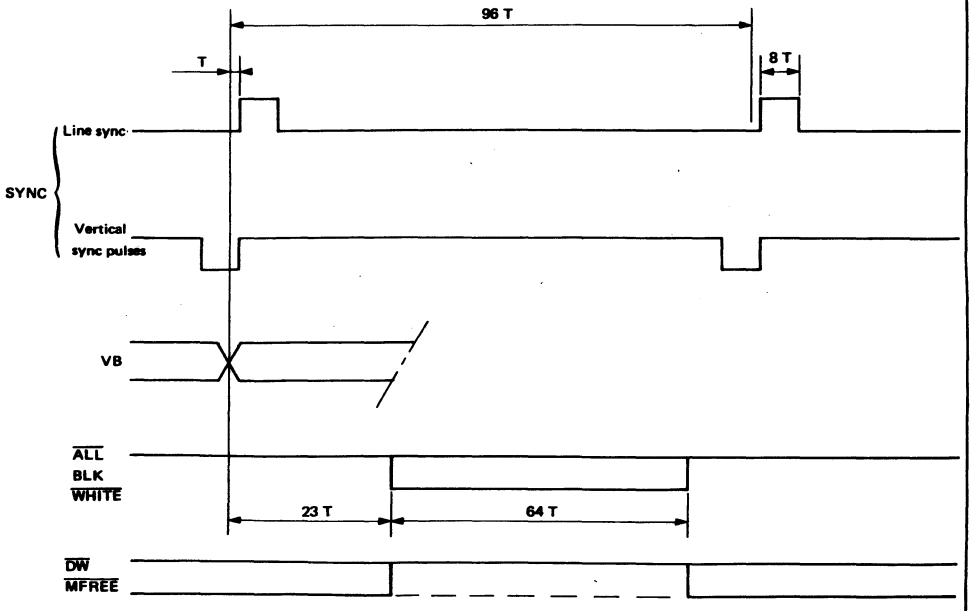
COMPOSITE SYNC AROUND FRAME SYNC

T : CK input period (667 ns in typical application where TV line duration is 64 μs)



Note : If FMAT is low or tied to $\overline{CK}$, the pattern of the second line is repeated for each frame.

DETAILED LINE DIAGRAM



HARDWIRED WRITE PROCESSOR OPERATION IN DISPLAY MEMORY

The hardwired write processors are sequenced by the, master clock CK. They receive their parameters from the microprocessor bus. They control the X, Y write address, and the DIN, $\overline{DW}$, $\overline{MW}$ and $\overline{IRQ}$ outputs.

These harwired processors operate in continuous mode. In the event of conflicting access to the display memory, the display and refresh processors have priority.

Since command decoding is synchronous with the CK master clock, any write operation into the (CMD) command register triggers a synchronizing mechanism which engages the circuit for a maximum of 2 CK cycles when the $\overline{E}$ input returns high. The circuit remains engaged throughout command execution.

No further command should be entered as long as bit 2 in STATUS register is low.

VECTOR PLOTTING

The internal vector generator makes it possible to modify, within the display memory, all the dots which form the approximation of a straight line segment. All vectors plotted are described by the origin dot and the projections on the axes.

The starting point co-ordinates are defined by the X, Y register value, prior to the plotting operation.
Projections onto the axes are defined as absolute values by the DELTAX and DELTAY registers, with the sign in the command byte that initiates the vector plotting process.

The vector approximation achieved here is that established by J. F. BRESENHAM ("Algorithm for computer control of a digital plotter"). This algorithm is executed by a hardwired processor which allows for a further vector component dot to be written in each CK clock cycle.

During plotting, the display memory is addressed by the X, Y registers, which are incremented or decremented.

On completion of vector plotting, they point to the end of this vector.

All vectors may be plotted using any of the following line patterns : continuous, dotted, dashed, dash-dotted, according to the 2 LSBs in register CTRL2.

Irrespective of such patterns, the plotting speed remains unchanged. The "pen down-pen up" statement required for plotting non-continuous lines is controlled by the $\overline{DW}$ output.

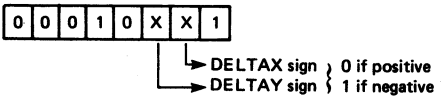
For a specified non-continuous line plotted vector, defined by DELTAX, DELTAY, CTRL2, CMD, the $\overline{DW}$ sequencing during the plotting process is always the same, irrespective of vector origin and of the nature of previous plots. This feature guarantees that a specified vector can be deleted by plotting it again after moving X and Y to the starting point, and complementing bit 1 in register CTRL1.

Since the vector plotting initiation command defines the sign of the projections onto the axes, all vectors may be plotted using 4 different commands.

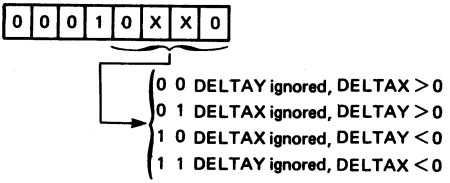
For increased programming flexibility, the system incorporates 16 different commands, supplemented by a set of 128 commands which make it possible to plot small size vectors by ignoring the DELTAX and DELTAY registers.

Such commands are as follows :

- Basic commands

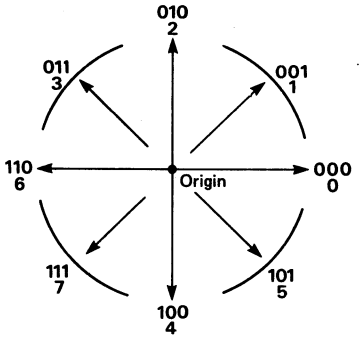


- Commands which allow ignoring the DELTAX or DELTAY registers by considering them as of zero value.

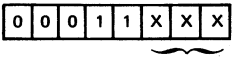


Note : Bits 1 and 2 always have the same sign meaning.

These 8 codes may be summarized by the following diagram :

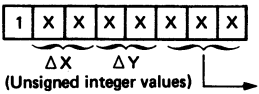


- Commands which allow ignoring the smaller of the two DELTAX and DELTAY registers, by considering it as being equal to the larger one, which is the same as plotting vectors parallel to the axes or diagonals, using a single DELTA register.



Same direction codes as above.

- Commands in which the two registers DELTAX and DELTAY may be ignored by specifying the projections through the CMD register (0 to 3 steps for each projection).



EXAMPLE : PLOTTING A DOTTED VECTOR

Origin : $X = 47_{10}$, $Y = 75_{10}$

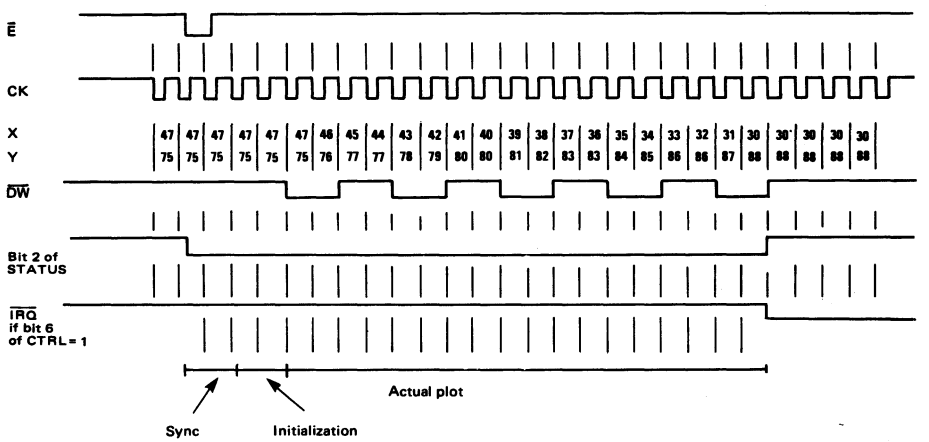
Projections: DELTAX = 17_{10}, DELTAY = 13_{10}

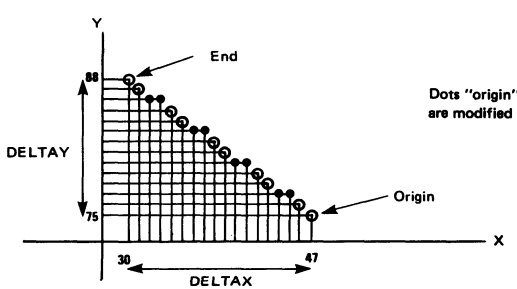
CMD = 13_{16} — Corresponding to
- Basic command,
- DELTAX < 0
- DELTAY > 0

CTRL1 = 03_{16} — Pen down

CTRL2 = 1_{16} — Dotted vector :
2 dots on,
2 dots off.

Plotting cycle sequence : (It is assumed that the vector generator is not interrupted by the display or refresh cycle).





Dots "origin" and "end" are modified

Display shows : ● unmodified dot
o dot on

Note :

Plotting a vector with DELTAX = DELTAY = 0 writes the dot X, Y in memory. It occupies the vector generator for synchronization, initialization and one write cycle.

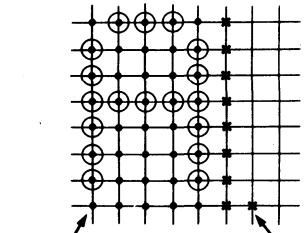
CHARACTER AND SYMBOL GENERATOR

The character generator operates in the same way as the vector generator, i.e. through incrementing or decrementing the X, Y registers, in conjunction with a $\overline{DW}$ output control.

It receives parameters from the CSIZE, CTRL2 and CMD registers. The characters plotted are selected, according to the CMD value, out of 98 matrices (97 8-dot high x 5-dot wide rectangular matrices, and one 4 dot x 4 dot matrix) defined in an internal ROM. Two scaling factors may be applied to the characters plotted using X and Y defined by the CSIZE register. The characters may be tilted, according to the content of register CTRL2.

Basic matrix

Upon completion of a character writing process, the X and Y registers are positioned for writing a further character next to the previous one, with a 1 dot spacing, i.e. Y is restored to its original value and X is incremented by 6.



• Unchanged
⊙ Altered dots
} if CMD = 41_{16} (in the ROM standard version)

× Computed dots, not defined into the ROM (not modifiable).

Scaling factors

Each individual dot in the 5 x 8 basic matrix may be replaced by a P x Q size block.

P : X co-ordinate scaling factor
Q : Y co-ordinate scaling factor

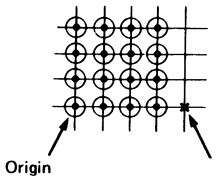
The character size becomes 5P x 8Q. Upon completion of the writing process, X is incremented by 6P. The CK clock cycle count required is 6P x 8Q.

P and Q may each take values from 1 through 16. They are defined by the CSIZE register. Each value is encoded on 4 bits, value 16 being encoded as 0_{16}.

In register CSIZE, P is encoded on the 4 MSBs and Q on the 4 LSBs.

Among the 97 rectangular matrices available in the standard ROM, 96 correspond to CMD values ranging from 20_{16} to $7F_{16}$, and the 97th matrix to $0A_{16}$. In the standard version, these values correspond to the 96 printable characters in the ASCII set. The 97th character is a 5P x 8Q block which may be used for deleting the other characters.

The 98th code ($0B_{16}$) is used to plot a 4P x 4Q graphic block. It locates X, Y, without spacing for the next symbol. Such a block makes it possible to pad uniform areas on the screen.



⊙ Modified dots
× Computed dot not defined in ROM (not modifiable)

Tilted characters

All characters may be modified to produce tilted characters or to mark the vertical co-ordinate with straight or tilted type symbols. Such changes may be achieved using bits 2 and 3 in register CTRL2.

Note : Scaling factors P and Q are always applied within the co-ordinates of the character before conversion.

Character deletion

A character may be deleted using either the same command code or command code $0A_{16}$. In either case, bit 1 in register CTRL1 should be inverted, the origin should be the same as prior to a character plotting operation, as should the scaling factors.

Note : Vector generator and character generator operate in similar ways :

	VECTOR	CHARACTER
Dimensions	DELTAX, DELTAY	CSIZE, tilting
$\overline{DW}$ modulation	Type of line	Character code

USE OF LIGHT PEN CIRCUITRY

A rising edge on the LPCK input is used to sample the current display address in the XLP and YLP registers, provided that this edge is present in the frame immediately following loading of the 08_{16} or 09_{16} code into the CMD register.

Here, the frame origin is counted starting with the VB falling edge. With code 08_{16}, the $\overline{MW}$ output recopies the BLK signal from the frame origin up to the rising edge on the LPCK input, or when VB starts rising again, if the LPCK input remains low for the entire frame. With code 09_{16}, the $\overline{MW}$ output is not activated.

The YLP address is 8-bit coded since there are 256 display lines in each frame. The XLP address is 6-bit coded since there are 64 display cycles in each line.

These 6 bits left-justified in register XLP indicate the number of the segment (h = 0 to 63) to which the point indicated by the light pen belongs.

The address sampled into XLP corresponds to the current memory cycle. Dots detected by the light pen were addressed in the memory during the previous cycle. Hence, 1 should be subtracted from bit 2 in XLP register where the light pen electronic circuitry does not produce any additional delay.

If the rising edge on input LPCK occurs while VB is low, then the LSB in XLP is set high. This bit acts as a status signal which is reset to the low state by reading register XLP or YLP.

The rising edge first received (LPCK or VB) sets bit 0 in STATUS register high. An interrupt is initiated if bit 4 in CTRL1 is high.

When commands 08_{16} or 09_{16} have been decoded, bit 2 of the status register goes high (circuit ready for any further command) and bit 0 goes low (light pen operating sequence underway).

SCREEN BLANKING COMMANDS

Three commands (04_{16}, 06_{16}, 07_{16}) will set the whole display memory to a status corresponding to a "black display screen" condition. Another command ($0C_{16}$) may be used to set the whole memory to a status other than black (this condition being determined by bit 1 in register CTRL1).

The 4 commands outlined above use the planned scanning of the memory addresses achieved by the display stage. The X and Y registers are not affected by commands 04_{16} and $0C_{16}$. Hence, the time required is that corresponding to one frame (FMAT = 0 or $\overline{CK}$) or two frames (FMAT = 1 or CK). The time corresponding to the completion of the frame currently executing when the CMD register is loaded, should be added to the above time.

For the screen blanking process, the frame origin is counted starting with the VB falling edge.
The only signals affected here are the $\overline{DW}$ output, which remains low when VB is low, and the DIN output which is forced high where the 04_{16}, 06_{16} and 07_{16} commands are entered.

Such commands are activated without requiring action by WO input or bit 2 in register CTRL1. While these commands are executing, bit 2 in STATUS register remains low.

EXTERNAL REQUEST FOR DISPLAY MEMORY ACCESS ($\overline{MW}$ OUTPUT)

On writing code $0F_{16}$ into the CMD register, the $\overline{MW}$ output is set low by the circuitry, during the next free memory cycle.

Apart from the display and refresh periods, this cycle is the first complete cycle that occurs after input $\overline{E}$ is reset high.

During this cycle, those addresses output on DAD and MSL correspond to the X and Y register contents : $\overline{DW}$ is high, $\overline{ALL}$ is high.

Should the memory be engaged in a display or refresh operation, (which is the case when $\overline{ALL}$ is low), then this cycle is postponed to be executed after $\overline{ALL}$ is reset high. The maximum waiting time is thus 64 cycles.

The $\overline{MW}$ signal may be used e. g. for performing a read or write operation into a register located between the display memory and the microprocessor bus.

INTERRUPTS OPERATION

An interrupt may be initiated by three situations denoted by internal signals :

- Circuit ready for a further command
- Vertical blanking signal
- Light pen sequence completed.

These three signals appear in real time in the STATUS register (bits 0, 1, 2). Each signal is cross-referenced to a mask bit in the register CTRL1 (bits 4, 5, 6).

If the mask bit is high, the first rising edge that occurs on the interrupt initiating signal sets the related interrupt flip-flop circuit high.

The outputs from these three flip-flop circuits appear in the STATUS register (bits 4, 5, 6). If one flip-flop circuit is high, bit 7 in the STATUS register is high, and pin $\overline{IRQ}$ is forced low.

A read operation in the STATUS register at address 0_{16} resets its 4 MSBs low, after input $\overline{E}$ is reset high (a read at address F_{16} maintains their value).

The three interrupt control flip-flops are duplicated to prevent the loss of an interrupt coming during a read cycle of the STATUS register.

The status of bits 4, 5 and 6 corresponds to the interrupt control flip-flop circuit output, before input $\overline{E}$ goes low.

An interrupt coming during a read cycle of the STATUS register does not appear in bits 4, 5 and 6 during this read sequence, but during the following one. However, it may appear in bits 0, 1, 2 or on pin $\overline{IRQ}$.

TABLE 1 – REGISTER ADDRESS

ADDRESS REGISTER					REGISTER FUNCTIONS		Number of bits
Binary				Hexa	Read R/$\overline{W}$ = 1	Write R/$\overline{W}$ = 0	
A3	A2	A1	A0				
0	0	0	0	0	STATUS	CMD	8
0	0	0	1	1	CTRL 1 (Write control and interrupt control)		7
0	0	1	0	2	CTRL 2 (Vector and symbol type control)		4
0	0	1	1	3	CSIZE (Character size)		8
0	1	0	0	4	Reserved		—
0	1	0	1	5	DELTAX		8
0	1	1	0	6	Reserved		—
0	1	1	1	7	DELTAY		8
1	0	0	0	8	X MSBs		4
1	0	0	1	9	X LSBs		8
1	0	1	0	A	Y MSBs		4
1	0	1	1	B	Y LSBs		8
1	1	0	0	C	XLP (Light-pen)	Reserved	7
1	1	0	1	D	YLP (Light-pen)	Reserved	8
1	1	1	0	E	Reserved		—
1	1	1	1	F	STATUS	Reserved	8

Reserved : These addresses are reserved for future versions of the circuit. In read mode, output buffers D0-D7 force a high state on the data bus.

TABLE 2 – COMMAND REGISTER

b7 b6 b5 b4 / b3 b2 b1 b0		0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0	0	Set bit 1 of CTRL1 : Pen selection	Vector generation (for b2, b1, b0 see small vector definition)	SPACE	0	@	P	`	p								
0 0 0 1	1	Clear bit 1 of CTRL 1 : Eraser selection		!	1	A	Q	a	q								
0 0 1 0	2	Set bit 0 of CTRL1 : Pen/Eraser down selection		"	2	B	R	b	r								
0 0 1 1	3	Clear bit 0 of CTRL 1 : Pen/Eraser up selection		#	3	C	S	c	s								
0 1 0 0	4	Clear screen		$	4	D	T	d	t								
0 1 0 1	5	X and Y registers reset to 0		%	5	E	U	e	u								
0 1 1 0	6	X and Y reset to 0 and clear screen		&	6	F	V	f	v								
0 1 1 1	7	Clear screen, set CSIZE to code "minsize" All other registers reset to 0 (except XLP, YLP)		'	7	G	W	g	w								
1 0 0 0	8	Light-pen initialization ($\overline{\text{WHITE}}$ forced low)	Special direction vectors (for b2, b1, b0 see small vector definition)	(	8	H	X	h	x								
1 0 0 1	9	Light-pen initialization		)	9	I	Y	i	y								
1 0 1 0	A	5 x 8 block drawing (size according to CSIZE)		*	:	J	Z	j	z								
1 0 1 1	B	4 x 4 block drawing (size according to CSIZE)		+	;	K	[	k	{								
1 1 0 0	C	Screen scanning : Pen or Eraser as defined by CTRL1		,	<	L	\	l	¦								
1 1 0 1	D	X register reset to 0		–	=	M	]	m	}								
1 1 1 0	E	Y register reset to 0		.	>	N	↑	n	¬								
1 1 1 1	F	Direct image memory access request for the next free cycle.		/	?	O	←	o	▒								

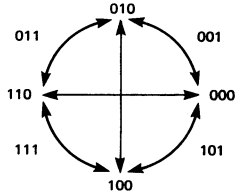
SMALL VECTOR DEFINITION :

b7	b6 b5	b4 b3	b2 b1 b0
1	|ΔX|	|ΔY|	Direction

Dimension

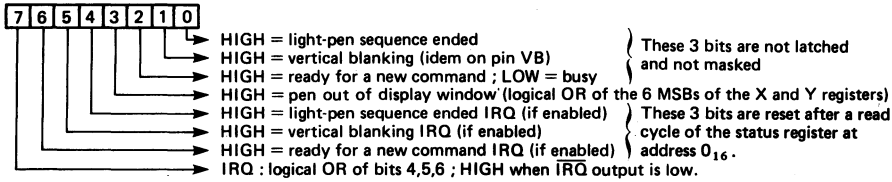
ΔX or ΔY		Vector length
0	0	0 step
0	1	1 step
1	0	2 steps
1	1	3 steps

Direction

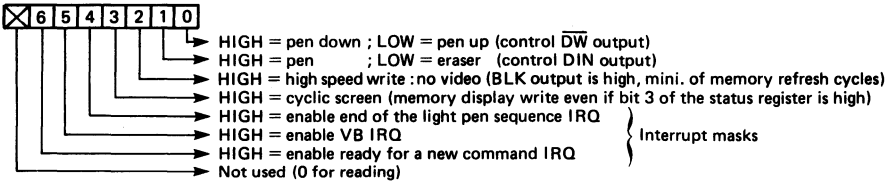


OTHER REGISTERS

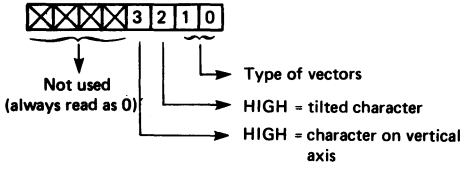
STATUS REGISTER (Read only)



CONTROL REGISTER 1 (Read/Write)

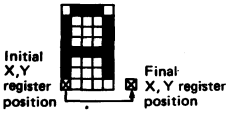


CONTROL REGISTER 2 (Read/Write)

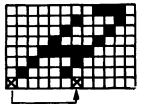


b1	b0	Type of vectors	
0	0	——— continuous	
0	1	- - - - - - dotted	2 dots on, 2 dots off
1	0	— — — dashed	4 dots on, 4 dots off
1	1	— · — · dotted-dashed	10 dots on, 2 dots off, 2 dots on, 2 dots off.

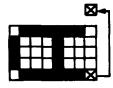
Types of character orientations



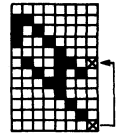
$b_3 = 0, b_2 = 0$
CSIZE = 11_{16}



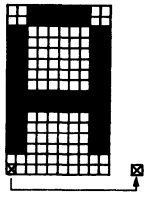
$b_3 = 0, b_2 = 1$
CSIZE = 11_{16}



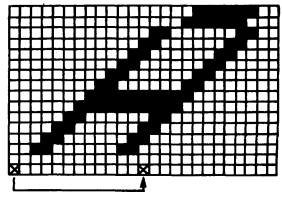
$b_3 = 1, b_2 = 0$
CSIZE = 11_{16}



$b_3 = 1, b_2 = 1$
CSIZE = 11_{16}

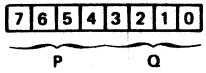


$b_3 = 0, b_2 = 0$
CSIZE = 22_{16}



$b_3 = 0, b_2 = 1$
CSIZE = 22_{16}

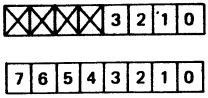
C-SIZE REGISTER (Read/Write)



P : Scaling factor on X axis
Q : Scaling factor on Y axis

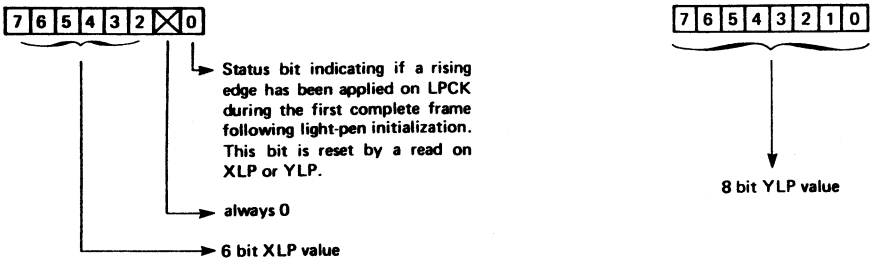
P and Q may take any value between 1 and 16. This value is given by the leftmost or rightmost 4 bits for P and Q respectively. Binary value (0) means 16.

X AND Y REGISTERS (Read/Write)



The 4 leftmost MSBs are always 0.

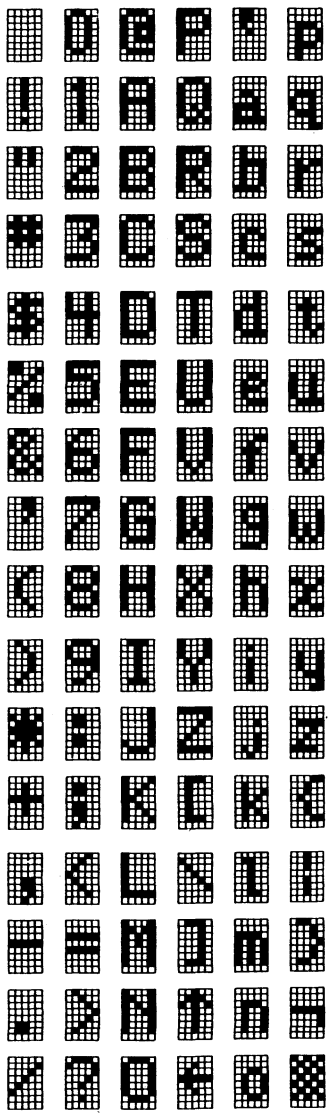
XLP and YLP REGISTERS



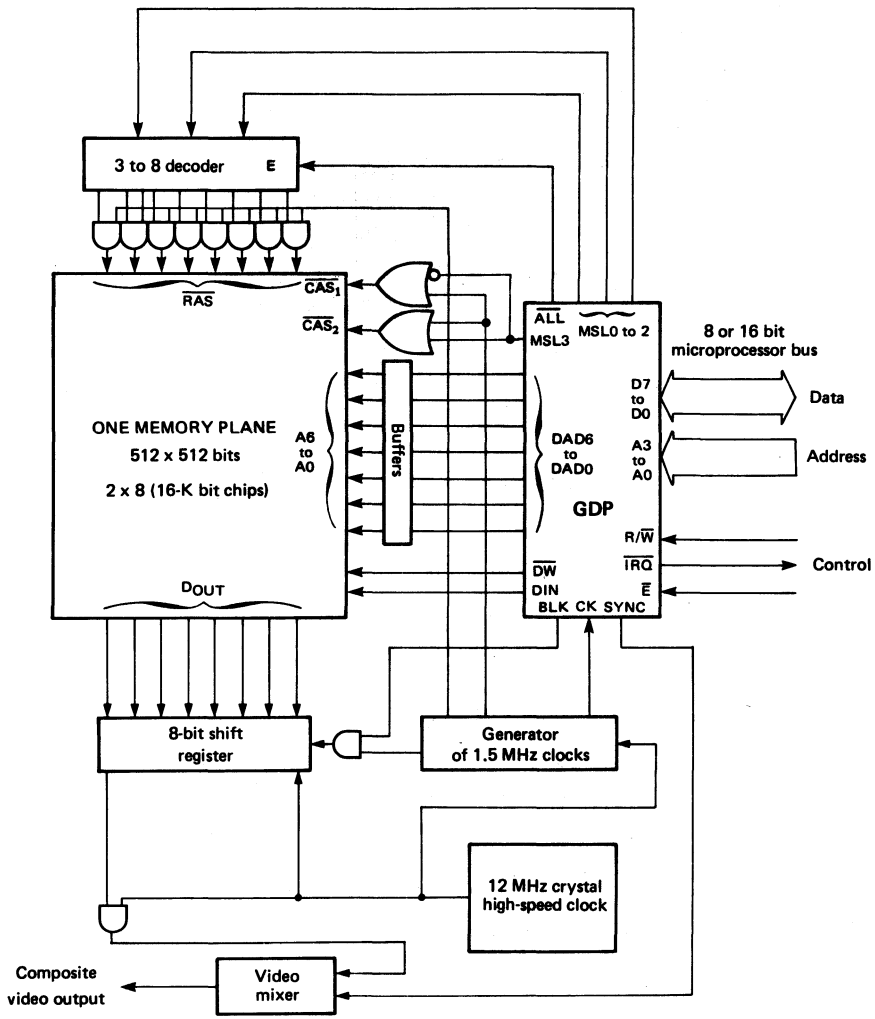
ASCII CHARACTER GENERATOR (5 x 8 matrix)

b7	0	0	0	0	0	0
b6	0	0	1	1	1	1
b5	1	1	0	0	1	1
b4	0	1	0	1	0	1

b3	b2	b1	b0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



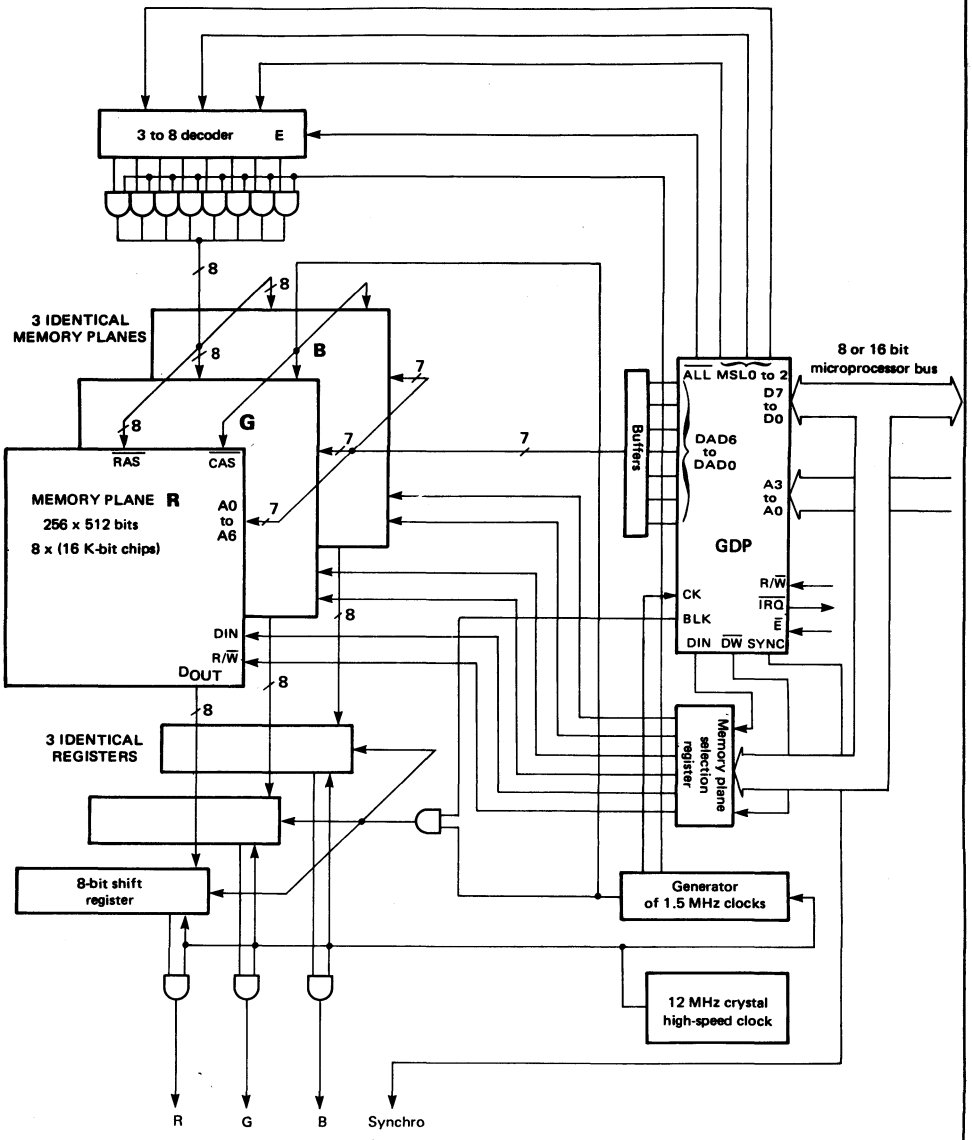
EXAMPLE OF A MONOCHROME APPLICATION : 512 x 512 or 416 x 512



Note : FMAT = V_{CC} : 512 x 512 resolution - 50 Hz 625 line interlaced scanning
FMAT = CK : 416 x 512 resolution - 60 Hz 525 line interlaced scanning.

EXAMPLE OF A COLOR APPLICATION : 208 x 512 or 256 x 512

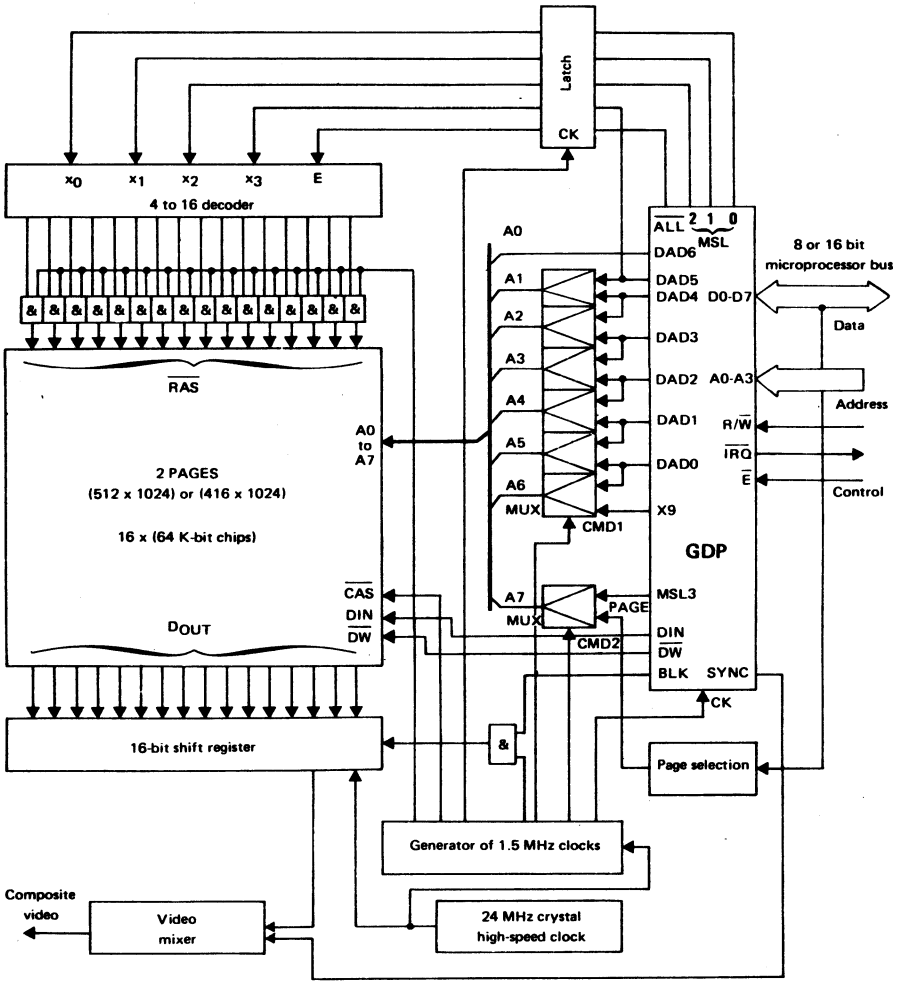
Eight colours may be obtained from the three basic colours red (R), green (G), blue (B)



Note : FMAT = V_{SS} : 256 x 512 resolution - 50 Hz 625 line non interlaced scanning
FMAT = $\overline{CK}$: 208 x 512 resolution - 60 Hz 525 line non interlaced scanning.

EXAMPLE OF A MONOCHROME, MULTIPAGE APPLICATION : 512 x 1024 or 416 x 1024

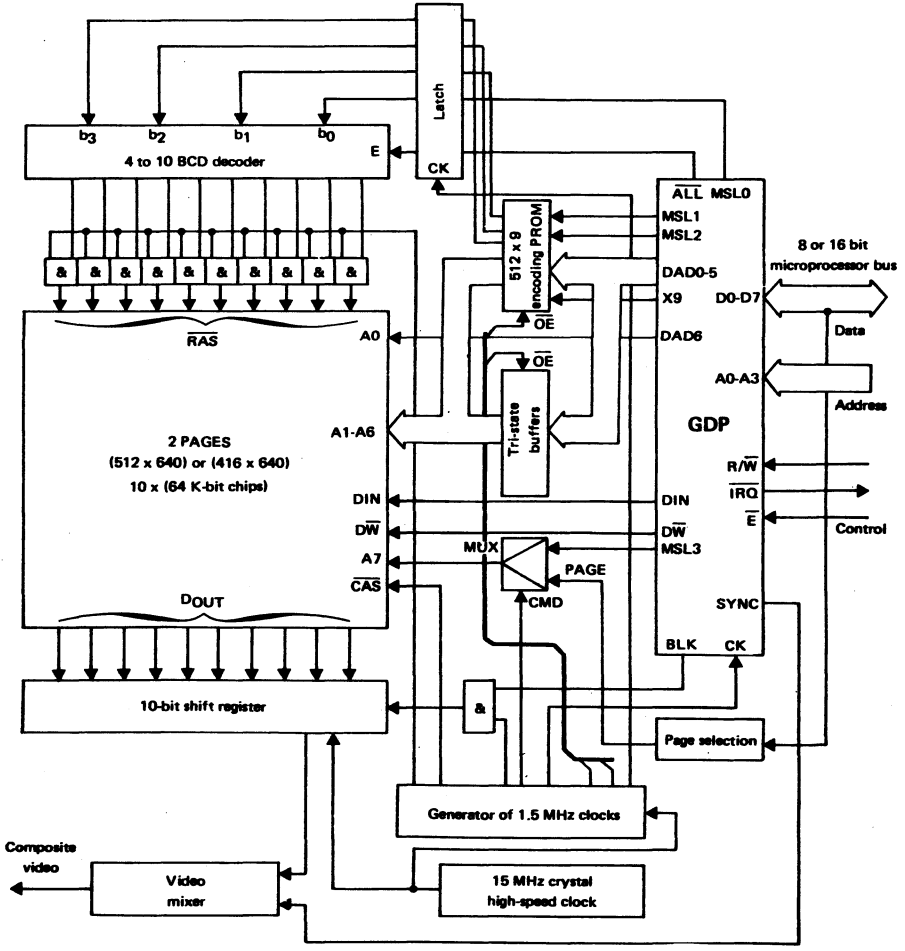
(See page 30 for MUX command law)



Note : FMAT = V_{CC} : 512 x 1024 resolution - 50 Hz 625 line interlaced scanning
FMAT = CK : 416 x 1024 resolution - 60 Hz 525 line interlaced scanning.

EXAMPLE OF A MONOCHROME, MULTIPAGE APPLICATION : 512 x 640 or 416 x 640

(See page 30 for PROM encoding)



Note : FMAT = V_{CC} : 512 x 640 resolution - 50 Hz 625 line interlaced scanning.
FMAT = CK : 416 x 640 resolution - 60 Hz 525 line interlaced scanning.

MUX COMMAND LAW

Following table indicates MUX command principles.

Selected MUX input				Output	Comment
Read cycles		Write cycles		Address bit	
$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$		
DAD6	DAD6	DAD6	DAD6	A_0	No MUX
DAD5(h_0)	DAD5	DAD4(X_4)	DAD5	A_1	These six MUX are driven identically by CMD1
DAD4(h_1)	DAD4	DAD3(X_5)	DAD4	A_2	
DAD3(h_2)	DAD3	DAD2(X_6)	DAD3	A_3	
DAD2(h_3)	DAD2	DAD1(X_7)	DAD2	A_4	
DAD1(h_4)	DAD1	DAD0(X_8)	DAD1	A_5	
DAD0(h_5)	DAD0	X_9	DAD0	A_6	
MSL3	PAGE	MSL3	PAGE	A_7	Driven by CMD2

PROM CODING PRINCIPLES

The PROM coding consists in the use of the 10 horizontal address bits (X_0, - - - -, X_9) to access the 640 pixels (organized in 64 segments of 10 pixels each).

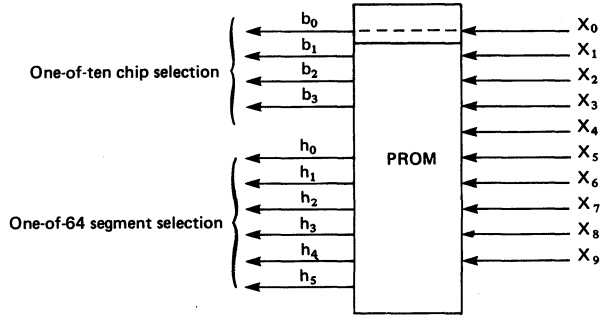
The 4 bits (b_0, b_1, b_2, b_3) are coding decimal numbers. Parity is maintained by BCD coding ; X_0 signal is therefore not coded inside the PROM and provides directly b_0.

Example : Considering the pixel with decimal abscissa X = 378 (17A in hexadecimal). This pixel is inside the 38th segment (h = 37 dec. or 25 hex.) with an abscissa x = 8.

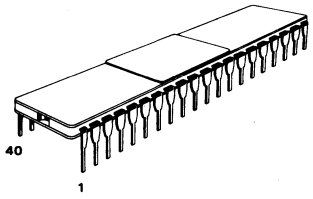
The binary number 0101111010 (17A hex.) must be encoded into 1001011000 (258 hex.).

This principle allows transcoding of all horizontal address values. Transcoding must only be active (PROM selection) during write cycles ($\overline{ALL}$ = 1) when horizontal addresses are output ($\overline{RAS}$).

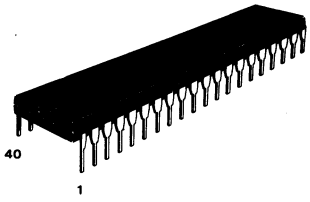
Note : This transcoding system may be adapted to other horizontal resolutions as 320, 384, 768. Horizontal resolutions are multiples of 64.



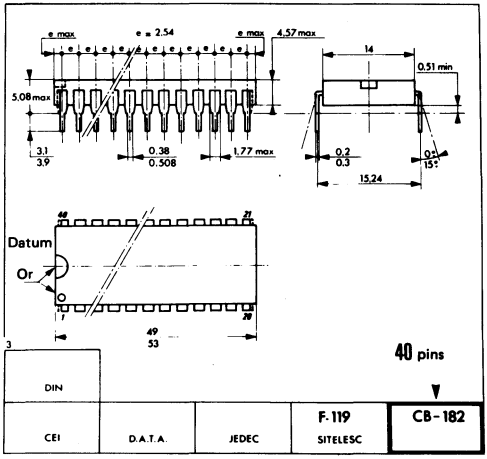
CASE CB-182



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

EFB7510

SINGLE CHIP ASYNCHRONOUS FSK MODEM

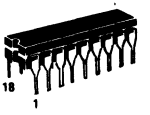
The EFB7510 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem.
Operating at rates up to 75, 150 or 1200 bits per second, it is compatible with the applicable Bell and CCITT recommended standards for 202 and V23 type modems.
This device provides the essential RS-232/CCITT V.24, V.25 and V.54 terminal control signal at TTL levels.

- Monolithic device includes both transmit and receive filters
- Standard low cost crystal (3.579 MHz)
- ± 5 % power supplies : + 5 V, - 5 V
- Separate analog and digital ground pins reduce system noise problems
- Available clock for UART (19.200 Hz)
- Reference voltage internally generated, to avoid noise and supply drift
- Back channel included
- 1.200 bauds, half-duplex two-wire operation or full-duplex four-wire operation
- Fixed compromise line equalizer
- No external precision component needed
- Low power consumption : 100 mW typical
- Direct interface to the THOMSON SEMICONDUCTORS EF6850, UART.

CMOS

SINGLE CHIP
ASYNCHRONOUS
FSK MODEM

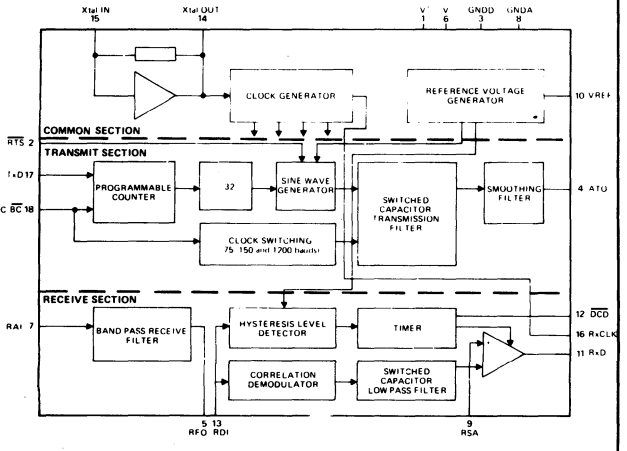
CASE CB-181



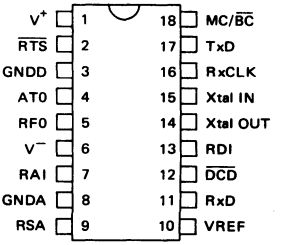
J SUFFIX
CERDIP PACKAGE

C SUFFIX
CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



NT8336-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

ABSOLUTE MAXIMUM RATINGS *

Rating	Symbol	Value	Unit
Supply voltage	V^+	+ 7 V	V
Supply voltage	V –	– 7 V	V
Analog input range	V_{in}	$V^- \leqslant V_{IN} \leqslant V^+$	V
Digital input range (excepted MC/$\overline{BC}$)	V_I	$GNDD \leqslant V_I \leqslant V^+$	V
MC/$\overline{BC}$ input range	V_I	$V^- \leqslant V_I \leqslant V^+$	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{stg}	- 55 to+ 125	°C
Pin temperature (Soldering, 10 s)		260	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL OPERATING CHARACTERISTICS

Parameter	Symbol	Min	Nominal	Max	Unit
Positive Supply Voltage	V+	4.75	5.0	5.25	V
Negative Supply Voltage	V-	- 5.25	- 5.0	- 4.75	V
V^+ Operating current	I_{CC}	–	–	10	mA
V^- Operating current	I_{BB}	- 10	–	–	mA

D.C. AND OPERATING CHARACTERISTICS

($T_A = 0°C$ to + 70°C, $V^+ = +5\ V \pm 5\ \%$, $V^- = -5\ V \pm 5\ \%$, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

DIGITAL INTERFACE

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input Current ($V_{IL\ min} \leqslant V_I \leqslant V_{IH\ max}$)	I_I	–	–	1	mA
Output low level current (V_{OL} = 0.4 V)	I_{OL}	1.6	–	–	mA
Output high level current (V_{OH} = 2.8 V)	I_{OH}	–	–	- 250	µA
Input low voltage (except MC/$\overline{BC}$)	V_{IL}	GNDD	–	0.8	V
Input high voltage (except MC/$\overline{BC}$)	V_{IH}	2.4	–	V^+	V
Input low voltage, MC/$\overline{BC}$	V_{IL}	V^-	–	- 4	V
Input intermediate voltage, MC/$\overline{BC}$	V_{II}	GNDD	–	GNDD + 0.8	V
Input high voltage, MC/$\overline{BC}$	V_{IH}	2.4	–	V^+	V

Note : 1 – Typical values are for T_A = 25° C and nominal power supply values.

D.C. AND OPERATING CHARACTERISTICS (continued)

($T_A = 0°C$ to $+70°C$, $V^+ = +5\ V \pm 5\ \%$, $V^- = 5\ V \pm 5\ \%$, GNDA = 0 V, GNDD = 0 V, unless otherwise specified)

ANALOG INTERFACE, RECEIVE FILTER

Parameter		Symbol	Min	Typ (1)	Max	Unit
Input leakage current, ($-3\ V < V_{IN} < 3\ V$)	RAI	T_{BRI}	–	±1	±3	µA
Input resistance,	RAI	R_{IRI}	1	3	–	MΩ
Output offset voltage	RFO	V_{OGSR}	–	–	±300	mV
Output voltage swing, ($R_L \geq 10\ k\Omega$)	RFO	V_{ORI}	–	–	±2	V
Load capacitance,	RFO	C_{LRI}	–	–	20	pF
Load resistance,	RFO	R_{LRI}	10	–	–	kΩ
Input voltage swing		V_{IRI}	-3	–	+3	V
Signal frequency distortion products at maximum signal level		C_{DPR}	–	-40	–	dB

ANALOG INTERFACE RECEIVE DEMODULATOR INPUT (RDI)

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input current	I_{in}	-1	–	1	µA
Maximum detection level to valid $\overline{DCD}$ output	N_1	1.1	1.3	1.5	V
Minimum detection level to valid $\overline{DCD}$ output	N_2	–	0.92	–	V
Hysteresis effect	N1/N2	1.26	–	1.6	
		2	2.9	4	dB

ANALOG INTERFACE, RECEIVE SLICER ADJUST (RSA)

Parameter	Symbol	Min	Typ	Max	Unit
Input current	I_{in}	-1	–	+1	µA
Input voltage	V_I	V_{REF}	$V_{REF}/2$	GNDA	V

ANALOG INTERFACE, TRANSMIT OUTPUT (ATO)

Parameter		Symbol	Min	Typ (1)	Max	Unit
Output DC offset, ($\overline{RTS}$ connected to V_{DD})		V_{OS}	–	–	±250	mV
Load capacitance		C_L	–	–	20	pF
Load resistance		R_L	10	–	–	kΩ
Output voltage swing (R_L = 10 kΩ, C_L = 20 pF)	390 Hz	V_O	2	2.6	3.3	V_{PP}
	450 Hz/390 Hz ampl. ratio	–	-1	0.5	+1	dB
	490 Hz/390 Hz ampl. ratio	–	-1	-0.7	+1	dB
	1300 Hz	V_O	2	2.8	3.6	V_{PP}
	2100 Hz/1300 Hz ampl. ratio	–	-2.3	-1.5	-0.7	dB
$\overline{RTS}$ attenuation ratio efficiency		–	55	–	–	dB

(1) Typical values for $T_A = 25°C$ and nominal power supply values.

ANALOG INTERFACE, REGULATED VOLTAGE (V_{REF})

Parameter	Symbol	Min	Typ (1)	Max	Unit
Output voltage	V_{OR}	- 2.5	- 2	- 1.5	V
Load resistance	R_{LR}	10	–	–	kΩ
Load capacitance	C_{LR}	–	–	20	pF

(1) Typical values for T_A = 25°C and nominal power supplies values.

DYNAMIC CHARACTERISTICS

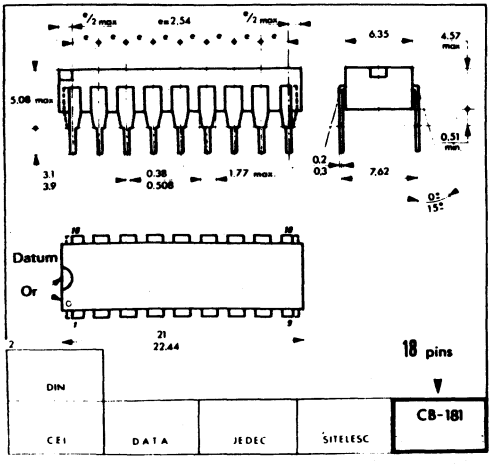
RECEIVE FILTER TRANSFER CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Absolute passband gain at 2100 Hz (V_{RFO}, R_L = ∞)		G_{AR}	- 3.2	- 2.9	- 2.6	dB
Gain relative to gain at 2100 Hz - Maximum input signal	380 Hz	G_{RR}	–	- 65	- 55	dB
	460 Hz	"	–	- 65	- 55	dB
	1100 Hz	"	- 4.7	- 4.4	- 4.1	dB
	2800 Hz	"	- 23	- 20	- 17	dB
	10000 Hz	"	- 10	- 8.5	- 7	dB

DIGITAL INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
Capacitance	C_{IB}	–	–	10	pF
Input rise-time, fall-time, measured between 0.8 V and 2.4 V	t_{THL}, t_{TLH}	–	20	–	ns
Output rise-time, fall time between 0.4 V and 2.8 V (1)	t_{THL}, t_{TLH}	–	50	–	ns

(1) Driving one 74L or 74LS TTL load plus 30 pF.



CASE CB-181

J SUFFIX
CERDIP PACKAGE

C SUFFIX
CERAMIC PACKAGE

PIN DESCRIPTION

COMMON SECTION

NAME	N°	FUNCTION	DESCRIPTION
V^+	1	Positive power supply	+ 5 V
V^-	6	Negative power supply	- 5 V
GNDA	8	Ground	Pin 8 serves as the ground return for the analog circuits of the transmit and receive section. The analog ground is not internally connected to the digital ground. The digital and analog grounds should be tied together as close as possible to the system supply ground.
GNDD	3	Ground	Pin 3 serves as the digital ground return for the internal clock. The digital ground is not internally connected to the analog ground. The digital and analog grounds should be tied together as close as possible to the system supply ground.
Xtal IN	15	Oscillator input	This pin corresponds to the input of the inverter of the oscillator. It is normally connected to an external crystal, but may also be connected to a pulse generator. The nominal frequency of the oscillator is 3.579545 MHz.
Xtal OUT	14	Oscillator output	This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating.
VREF	10	Regulated voltage	This output carries an internally regulated reference voltage. By means of an external potentiometer connected between VREF and GNDA, an adjustable reference voltage may be applied to RSA. The adjustment of RSA is to optimize the discrimination of high and low frequencies of the same channel. The voltage applied to RSA is approximately VREF/2.

TRANSMIT SECTION

$\overline{RTS}$	2	Request to send	When a low state is present on input $\overline{RTS}$, the EFB7510 delivers on output ATO a sinusoidal signal at a frequency which depends on input TXD. When a high state is present on input $\overline{RTS}$, output ATO is tied to the analog ground.
TxD	17	Transmit data	This input selects the high frequency or low frequency at the TRANSMITTED CARRIER output pin (ATO) : • a high state selects the low frequency, • a low state selects the high frequency. For correct operation, inputs TxD and MC/$\overline{BC}$ must not be simultaneously low while power-on.
MC/$\overline{BC}$	18	Main channel/ back channel	This input selects transmission on the main channel or back channel, and defines the modulation rate, according to European or American standards. (refer to functional description).
ATO	4	Analog transmit output	When a low state is present on $\overline{RTS}$, the EFB7510 delivers on output ATO a sinusoidal signal centered on the analog ground, with an amplitude of 2.8 V peak to peak.

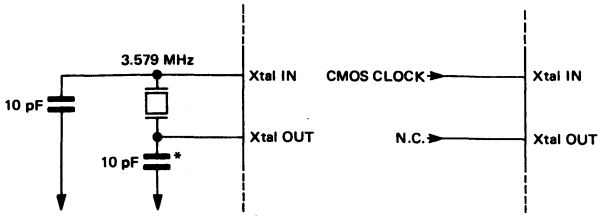
RECEIVE SECTION

RAI	7	Receive analog input	Input for analog signals of amplitude lower than 6 V peak to peak and centered on analog ground.
RFO	5	Receive filter output	This analog output must be connected to a high-pass filter and slicer, with sufficient gain to satisfy the level detection conditions.

NAME	N°	FUNCTION	DESCRIPTION
RDI	13	Receive demodulator input	This is the input of the demodulator. First, the analog signals are passed through level detection comparators and zero crossing detector.
RSA	9	Receive slicer adjust	Input of the decision comparator optimizing discrimination between high and low frequencies.
$\overline{DCD}$	12	data carrier detect	This output is low when the EFB7510 receives on input RDI a sinusoidal signal with amplitude higher than N1. This output is high when the EFB7510 receives on input RDI a sinusoidal signal with amplitude lower than N2. Within the N1 – N2 range, the detection system presents an hysteresis.
RxD	11	Receive data	This output is low when a high frequency signal is present on input RDI, and high when a low frequency signal is present on input RDI. Without CARRIER on pin RAI, this output is high.
RxCLK	16	Receive clock	This output delivers a clock signal, the frequency of which is 16 times of demodulation rate.

CLOCK GENERATION

Crystal :
NYMPH, NYP 035A-18



*Capacitor values vary with different crystal manufacturers

FUNCTIONAL DESCRIPTION

With a minimum number of external components, the EFB7510 performs all the functions of modulation, demodulation and filtering necessary to meet the requirements of CCITT Recommendation V.23 and BELL Standard 202.

This circuit is in four parts :

- a modulator,
- a demodulator,
- a clock generator,
- a reference voltage generator.

Note : The description of the demodulator also covers a subsystem, external to the circuit proper and having the following functions :

- high-pass filter,
- amplification,
- slicer.

MODULATOR

When input $\overline{RTS}$ is low, output ATO delivers a sinusoidal signal, the frequency of which depends on MC/$\overline{BC}$ and TxD.

DEMODULATOR

When the analog signal on RDI conforms to certain criteria, output $\overline{DCD}$ detects it and output RxD delivers a digital signal, the logic state of which depends on the analog signal frequency.

CLOCK GENERATOR

This part of the circuit generates from a 3.58 MHz crystal all the internal clocks necessary to the correct performance of the EFB7510 : ie clocks for the switched capacitor filters as well as those for the sinewave generator. The circuit also delivers on RxCLK a clock needed by the receive UART.

REFERENCE VOLTAGE GENERATOR

This part of the circuit generates a regulated voltage on VREF which is used to adjust detection thresholds. It is independent of power supply values.

FUNCTIONAL CHARACTERISTICS

MODULATOR

- Modulation conditions:

$\overline{RTS}$	ATO
"L"	FSK modulated signal
"H"	GNDA

- Transmitted frequencies :
(for details of frequency selection see PIN DESCRIPTION - ATO)

MC/$\overline{BC}$	Modulation rate	TxD	R.35 and V.23 Recommendations (Hz)	Frequency generated from a 3.58 MHz crystal	Error (Hz)
GNDD	75 bauds	"H" "L"	390 ± 2 450 ± 2	389.52 450.20	- 0.48 + 0.20
V^-	150 bauds	"H" "L"	390 ± 2 490 ± 2	389.52 489.39	- 0.48 - 0.61
V^+	1 200 bauds	"H" "L"	1 300 ± 10 2 100 ± 10	1 299.70 2 097.40	- 0.34 - 2.61

DEMODULATOR

- **Frequencies received on RDI**

Analog signals centered on analog ground are received on input RDI. The receive modulation rate is 1 200 bauds.

Frequencies to detect are as follows :

Modulation rate	Frequencies (Hz) (Recommendation V.23)	Frequencies (Hz) (Recommendation BELL 202)
1 200 bauds	1 300 ± 16 2 100 ± 16	1 200 ± 16 2 200 ± 16

- **Level detection conditions**

Input RDI drives a signal detector the output of which ($\overline{DCD}$) is at logic "0" if the level of signal RDI is higher than N1. The output of this detector is at logic "1" if the level of signal RDI is lower than N2. This detector has a hysteresis effect : N1/N2.

- **Timing detection conditions**

The timing performance of the level detector ($\overline{DCD}$) conforms to CCITT Recommendation V.24.

Under normal working conditions, output $\overline{DCD}$ is :

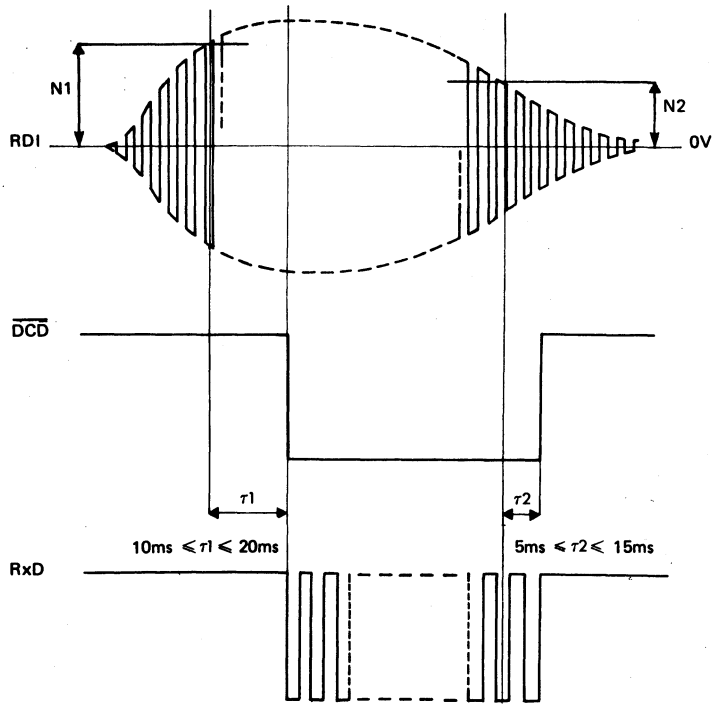
- low if signal RDI conforms to the level detection condition,
- high if signal RDI does not conform to the level detection conditions.

Output $\overline{DCD}$ goes from high to low when signal RDI conforms to the level detection conditions for 20 ms or more.

Output $\overline{DCD}$ does not go from high to low when signal RDI conforms to the level detection conditions for 10 ms or less.

Output $\overline{DCD}$ goes from low to high when signal RDI does not conform to the level detection conditions for 15 ms or more.

Output $\overline{DCD}$ does not go from low to high when signal RDI does not conform to the level detection conditions for 5 ms or less.



- **Demodulated signal**

Under normal working conditions, signal RxD conforms to the following table :

Level received on RDI	$\overline{DCD}$	Frequency received on RAI (Hz)	RxD
> N1	"L"	1 200 to 2 200	"X"
< N2	"H"	any	"H"

- **Clock generator**

The clock generated by the EFB7510 and supplied on output RxCLK must have the following characteristics :

Frequency : 19 200 Hz (± 1 %)
Logic state duration : Compatible to the UART clock specification.

- **Reference voltage generator**

The VREF output carries a regulated reference voltage. An external potentiometer, connected between VREF and GNDA, can supply a regulated voltage to input RSA.

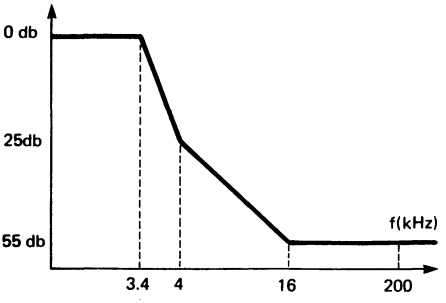
Adjustment of RSA optimizes the discrimination between the high and low frequencies.

TYPICAL PERFORMANCES

These typical performances are achieved with the environment described further. (See Annex II).

- **Transmitted spectrum**

The signal transmitted from output ATO conforms to the following specification, whatever the transmitted data:



- **Receiver**

Measurement conditions

Local transmit level : −2 dBm on 75 baud back channel.
Receive level : −25 dBm, with 511 bit pseudo-random test pattern.

Isochronous distortion

Table below shows the typical isochronous distortion values obtained with the EFB7510, which conform to the CCETT specifications for videotex applications. The characteristics of CCETT lines used for measurements are given in Annex I.

Line	Distortion
Line 1 (flat)	10 %
Line 2	14 %
Line 3	12 %
Line 4	14 %

Bit error rate

The typical bit error rates versus white noise are as follows.

	S/N	BER
On line 1	6.4 dB	2.10^{-3}
On line 2	5.5 dB	2.10^{-3}
On line 3	6.8 dB	2.10^{-3}
On line 4	6.5 dB	2.10^{-3}

ENVIRONMENTAL FUNCTIONAL DESCRIPTION

(See diagram shown next page)

Transmit section (A)

The transmit section comprises a single operational amplifier capable of driving a load of 600 Ω, which can also be used to adjust the transmit level.

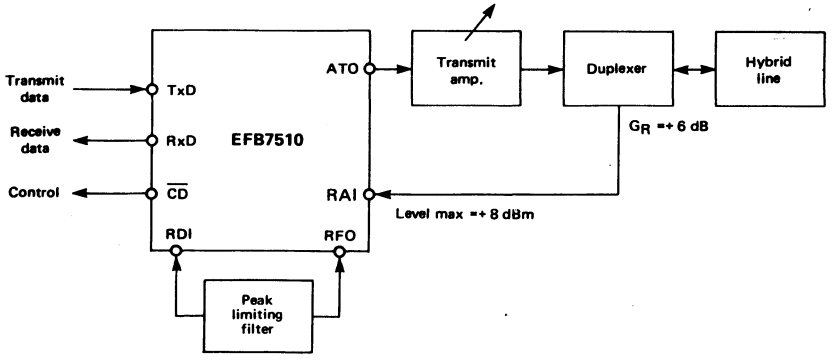
Duplexer (A)

This amplifier provides the 2 wire/4 wire separation function and enables a low cost standard non differential transformer (ratio 1:1) to be used. The duplexer principle provides a gain of 6 dB for the received signal.

Peak-limiting filter

This section is made of two operational amplifiers and performs three functions :

- peak-limiting amplifier, designed to meet the signal detector levels according to the signal received from the phone line.
- High-pass filter (12 dB per octave) to overcome the DC component of the signal to be demodulated.
- Low-pass filter to protect against the inherent noise of the receive filter.



CALCULATION OF CIRCUIT ELEMENTS

The following factors must be considered in calculating the external components in the EFB7510 application :

- Signal attenation introduced by the receive filter is 3 dB.
- The maximum permissible level at RAI input is 6 Vpp (+ 8 dBm).

Note : the reference frequency is 2100 or 2200 Hz.

- A 2.5 dB hysteresis is introduced within the two signal detection level N1 and N2, in accordance with CCITT Recommendation V.23.

To be centered, the two limit values of the CARRIER DETECT signal are therefore :

- Upper : - 44.25 dBm, or 13.5 mVpp
- Lower : - 46.75 dBm, or 10 mVpp

- For a correct operation of the EFB7510 signal detector, the peak-limiting filter must remain linear up to - 44 dBm on line.
- At input RDI, the upper threshold level N1 of the signal detector is 3 Vpp (2.7 dBm), and must correspond to the minimum signal level received from the line transformer. With a duplexer reception gain of + 6 dB, the peak-limiting filter gain is defined by :

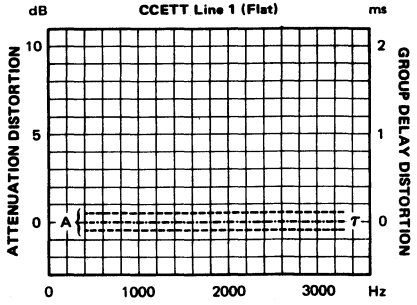
$$A = 44 - 6 + 3 + 2.7 = 43.7 \text{ dB (a ratio of 153)}$$

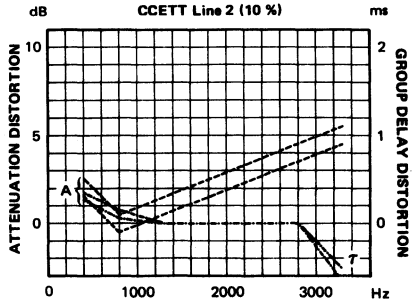
A typical application of the EFB7510 is shown next page.

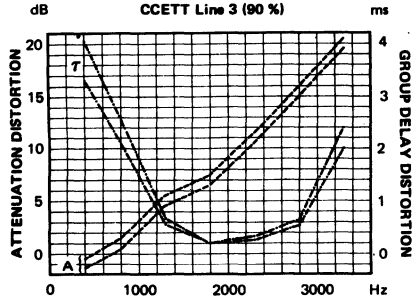
Note : The peak-limiting filter gain must be adjusted according to the minimum level on line. With a minimum level of :

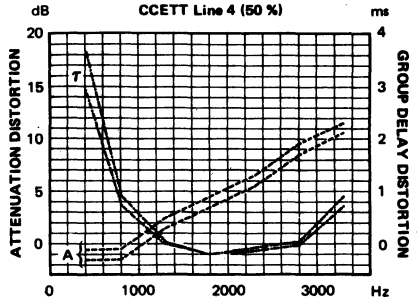
- - 38 dBm, A = 37.7 dB
- - 33 dBm, A = 32.7 dB.

ANNEX I

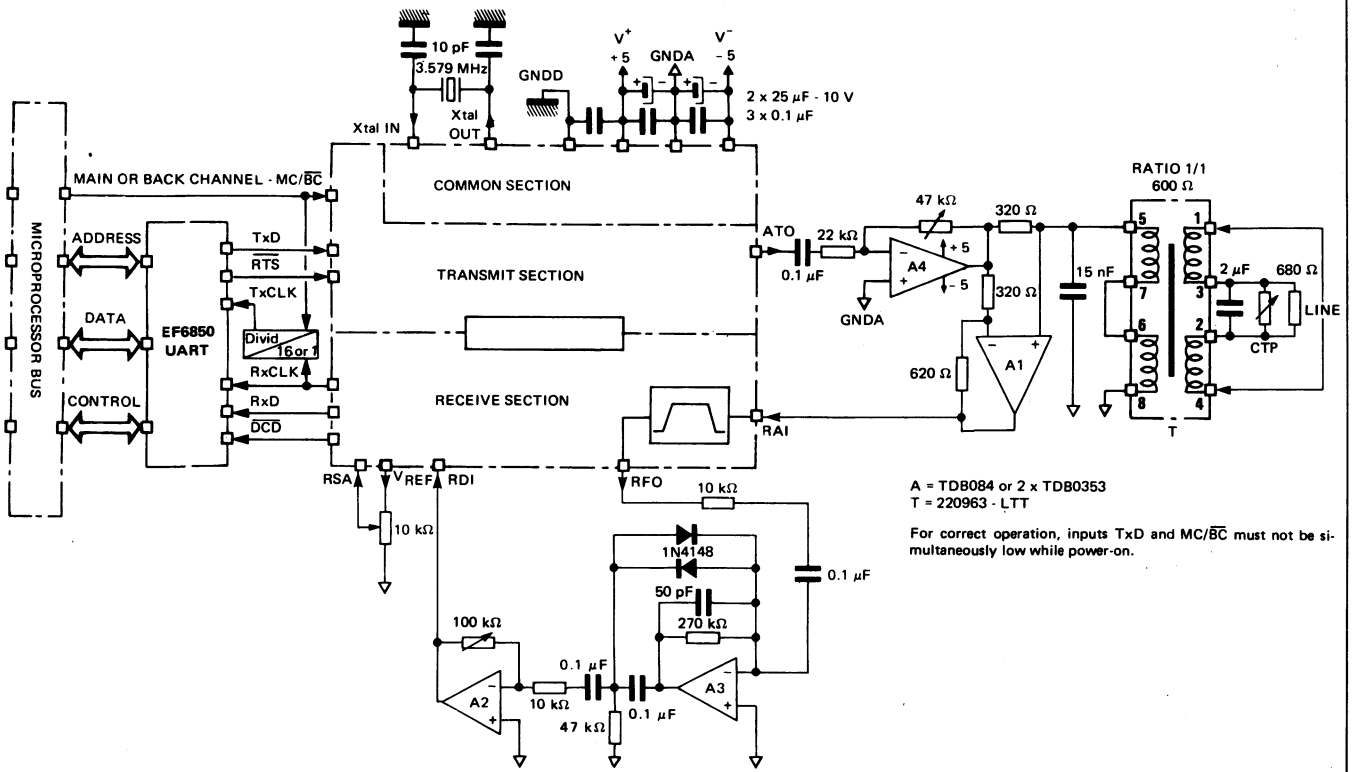








ANNEX II : TYPICAL APPLICATION OF EFB7510



A = TDB084 or 2 x TDB0353
T = 220963 - LTT

For correct operation, inputs TxD and MC/$\overline{BC}$ must not be simultaneously low while power-on.

NOTES

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

Printed in France

THOMSON SEMICONDUCTORS

TEA2017

PRODUCT PREVIEW

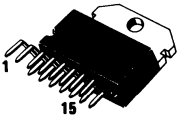
HORIZONTAL AND VERTICAL DEFLECTION MONITOR

Horizontal and vertical deflection circuit, the TEA 2017 is particulary intended for the black and white TV receivers and display video units.

- Direct drive of frame yoke (up to ± 1 A)
- Capability to drive a line darlington
- Built-in frame separator without external components
- Muting output
- Frame output protection against short-circuits
- Very few external components.
- Integrated flyback generator.

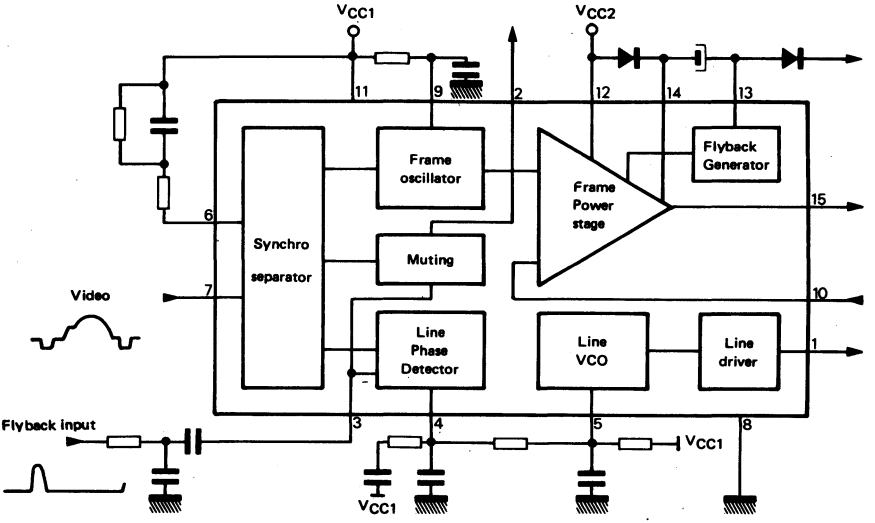
HORIZONTAL AND VERTICAL DEFLECTION MONITOR

CASE CB-501



SP SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



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THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

MAXIMUM RATINGS

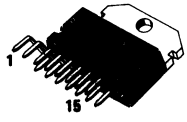
Rating	Symbol	Value	Unit
Direct vertical supply voltage	V_{CC2}	30	V
Flyback vertical peak voltage	V_{FB}	60	V
Vertical output current	I_{OV}	±1.5	A
Horizontal supply voltage	V_{CC1}	20	V
Storage and junction temperature	T_j , T_{stg}	- 40 + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Max junction-case thermal resistance	$R_{th(j-c)}$	3	°C/W
Max junction-ambient thermal resistance	$R_{th(j-a)}$	40	°C/W

PIN CONFIGURATION

CASE CB-501



1 Line output
2 Muting output
3 Line flyback input
4 Phase detector
5 Line oscillator
6 Synchro separator
7 Video input
8 Ground
9 Frame oscillator
10 Power amplifier negative input
11 V_{CC1}
12 V_{CC2}
13 Flyback generator
14 V_{CC} power stage
15 Frame output

ELECTRICAL CHARACTERISTICS

$T_{amb} = 25°C$; $V_{CC1} = 10$ V ; $V_{CC2} = 24$ V (Unless otherwise specified).

Characteristic	Symbol	Min	Typ	Max	Unit
Horizontal supply voltage (Pin 11)	V_{CC1}	8	–	20	V
Horizontal supply current (Pin 11)	I_{CC1}	–	15	–	mA
Vertical supply voltage (Pin 14)	V_{CC2}	10	–	30	V
Vertical supply current (Pin 14) - V_{CC2} = 30 V without load	I_{CC2}	–	25	–	mA
Video input (Pin 7)					
Input threshold voltage		–	4	–	V
Video input signal		0.4	–	4	V_{pp}
Flyback input (Pin 3)					
Input impedance		–	5.6	–	kΩ
Line output (Pin 1)					
Output current					
Peak value		–	- 500	–	mA
DC value		–	- 180	–	
Control pulse width		–	22	–	µs
Line oscillator (Pin 5)					
Threshold voltage					
Low level		–	3.2	–	V
High level		–	7	–	V
Supply voltage influence on frequency	$\frac{\Delta F/F}{\Delta V/V}$	–	0.4	–	%
Phase comparator (Pin 4)					
Control voltage		–	3 to 7	–	V
Control current		–	± 0.5	–	mA
Control sensibility (see fig. application n° 1)		–	750	–	Hz/µs
Pull in range (see fig. application n° 1)		–	± 800	–	Hz
Frame oscillator (Pin 9)					
Threshold voltage					
Low level		–	2	–	V
High level		–	3.1	–	V
Saw tooth voltage with synchronization		–	1	–	V_{pp}
Output power stage (Pin 15)					
Output saturation voltage					
To ground I = 1 A		–	–	0.8	V
To V_{CC} I = 1 A		–	–	2.4	V
Muting (Pin 2)					
Output voltage (muting on : no video signal)		–	8	–	V
Output voltage (muting off)		–	0.2	–	V

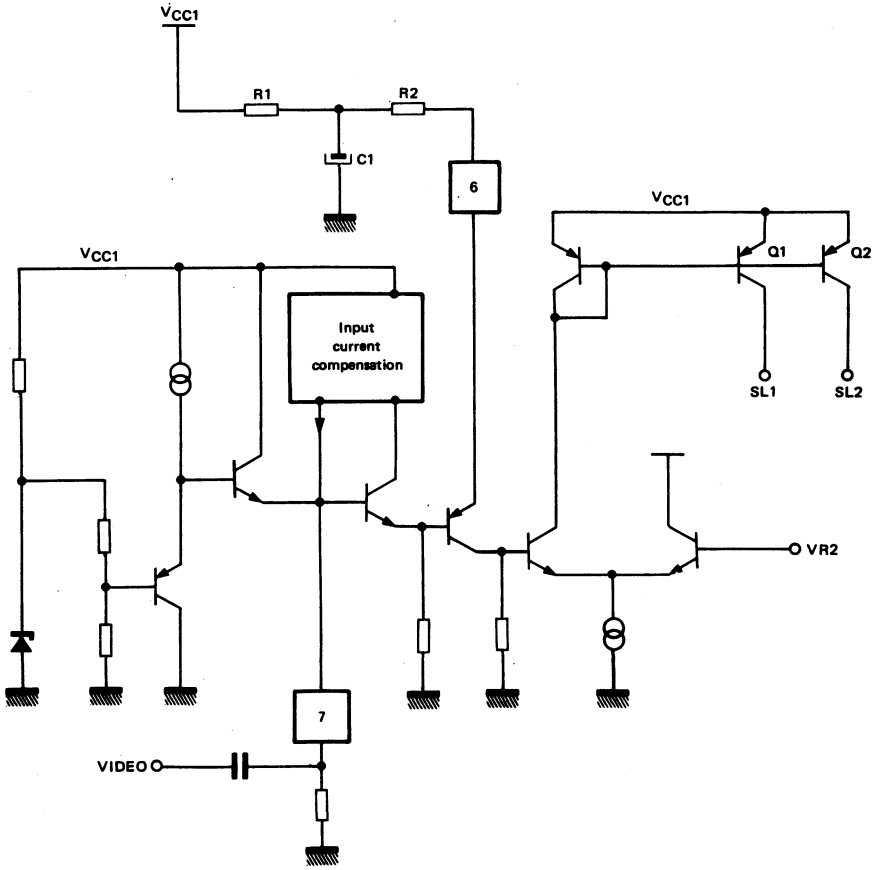
GENERAL DESCRIPTION

The TEA 2017 performs all of the video and power functions required to provide signals for the direct drive of a line darlington and the frame yoke.

It contains :

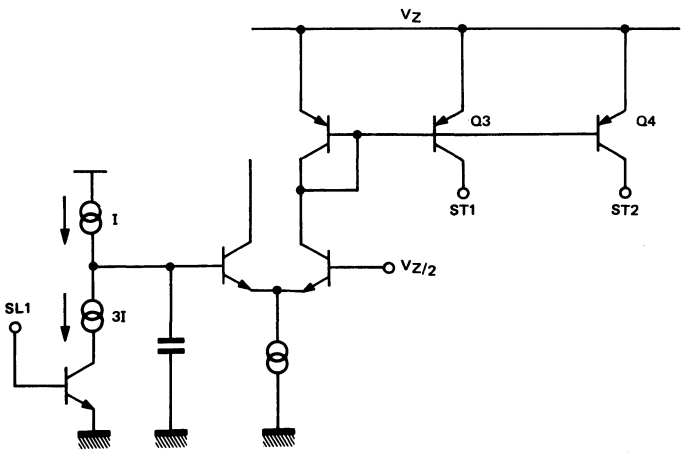
- A synchronizing separator with the slice level of synchro separation determined by the external components.
- An integrated frame synchronizing separator without external components.
- A saw tooth generator for the frame with synchronization allowed during the last fourth of the free run period.
- A power amplifier for direct drive of the frame yoke with overload, short circuit and thermal protections.
- A line phase detector and a voltage control oscillator.
- An open collector output for the direct drive of a line darlington.
- A muting output.

SYNCHRONIZATION SEPARATOR CIRCUIT



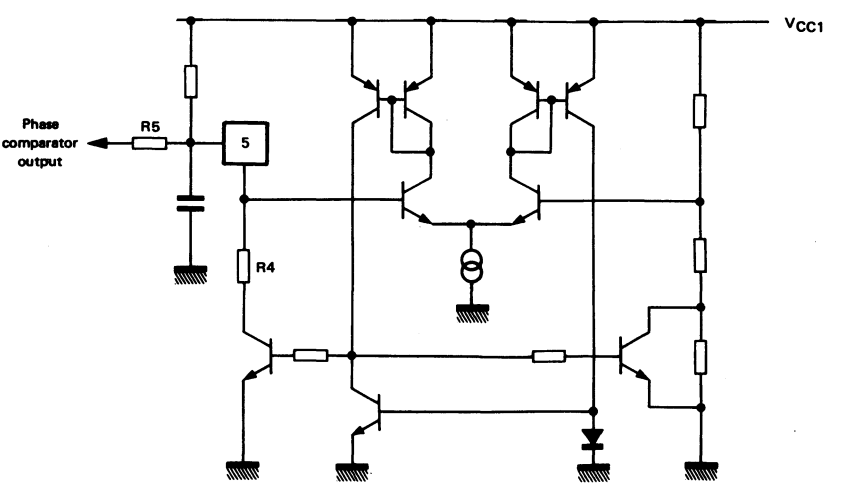
The sync-tip DC level on pin 7 is clamped to 2.5 V. The slice level of sync-separation present on capacitor C1 depends on the value of resistor R1 and R2. When the video signal on pin 7 decreases under the capacitor voltage the transistors Q1 and Q2 provide current for the other parts of the circuit.

FRAME SEPARATOR



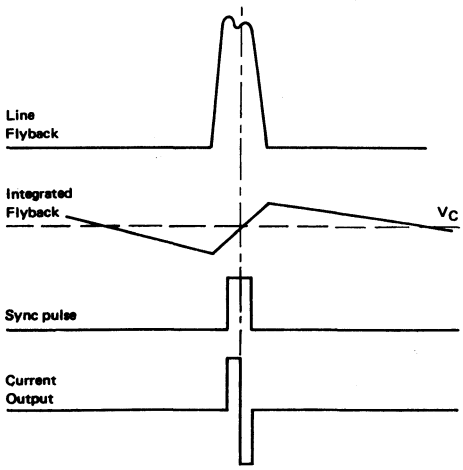
The sync-pulse allows the discharging of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync pulse permits the complete discharging of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

LINE OSCILLATOR

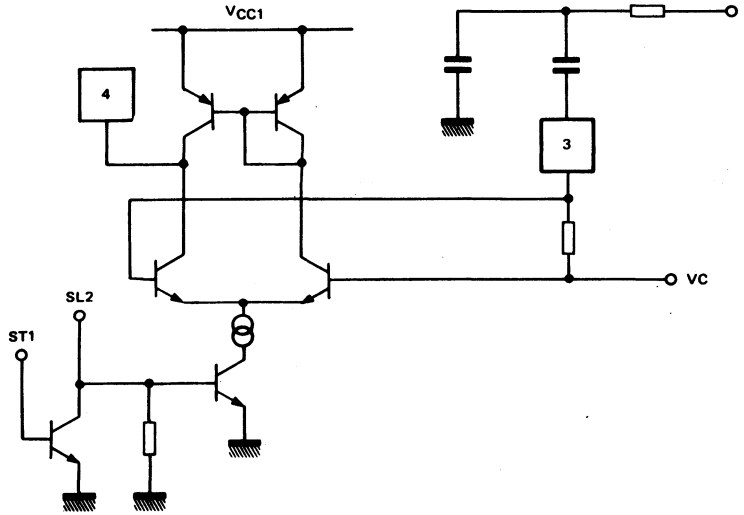


The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depend on the internal resistor R4. The voltage control is applied on resistor R5.

PHASE COMPARATOR



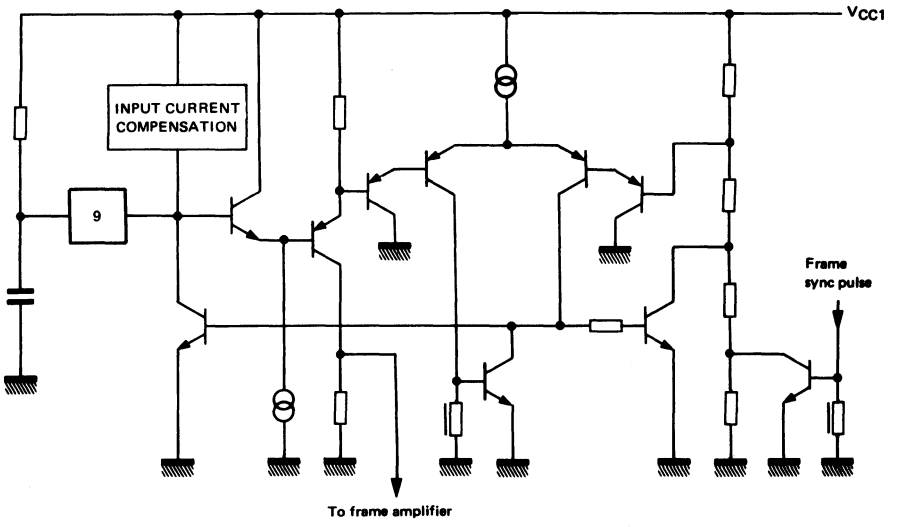
The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 3 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 3 superior to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.



LINE OUTPUT (PIN 1)

It is an open collector output which is able to drive pulse current of 500 mA for a rapid discharging of the darlington base. The output pulse time is 22 μs for a 64 μs period.

FRAME OSCILLATOR



The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last fourth of the free run period. The input current during the charge of the capacitor is less than 1 μA.

FRAME OUTPUT AMPLIFIER

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.

Its positive input is directly connected to the invert of the frame saw tooth.

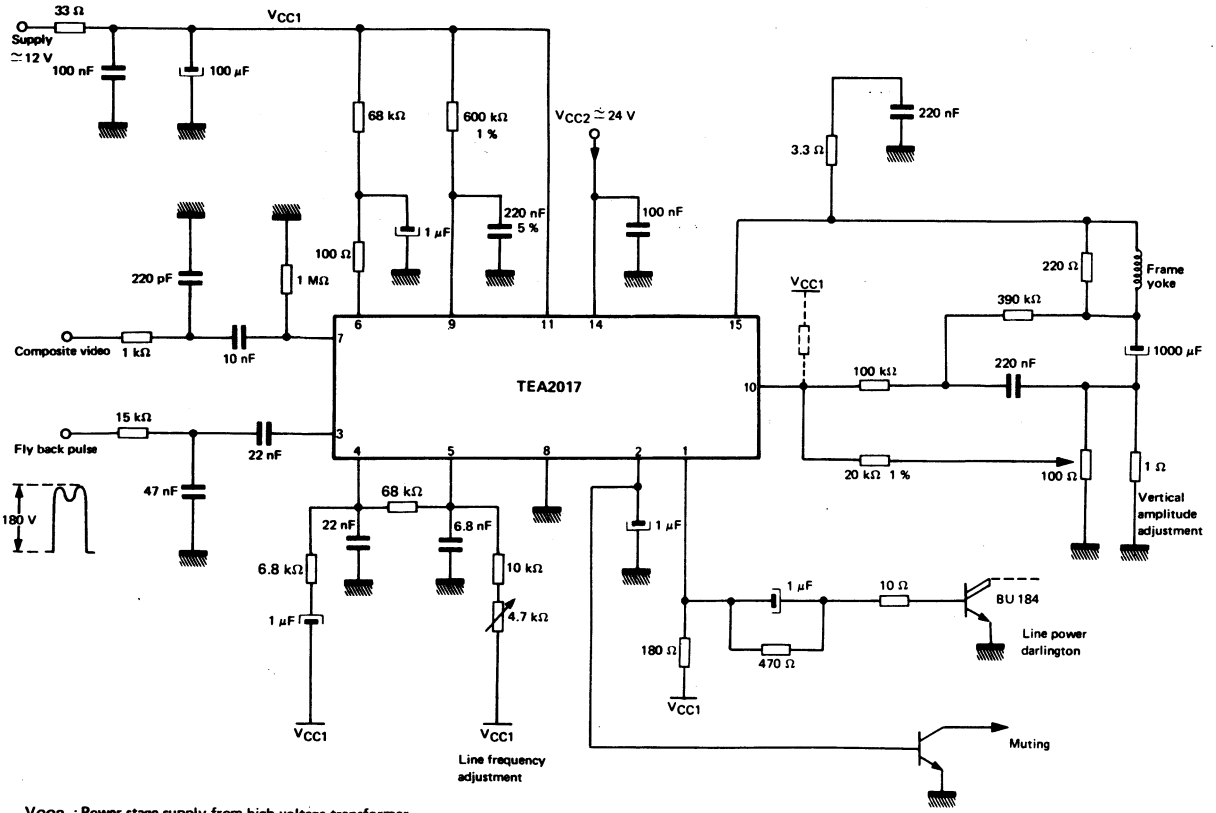
MUTING OUTPUT

It delivers voltage pulse during the line fly-back if there is no video signal on the input. The output impedance is 1 kΩ.

APPLICATION N° 1

TYPICAL BLACK-WHITE TV APPLICATION FOR 14" - 110° SCREEN

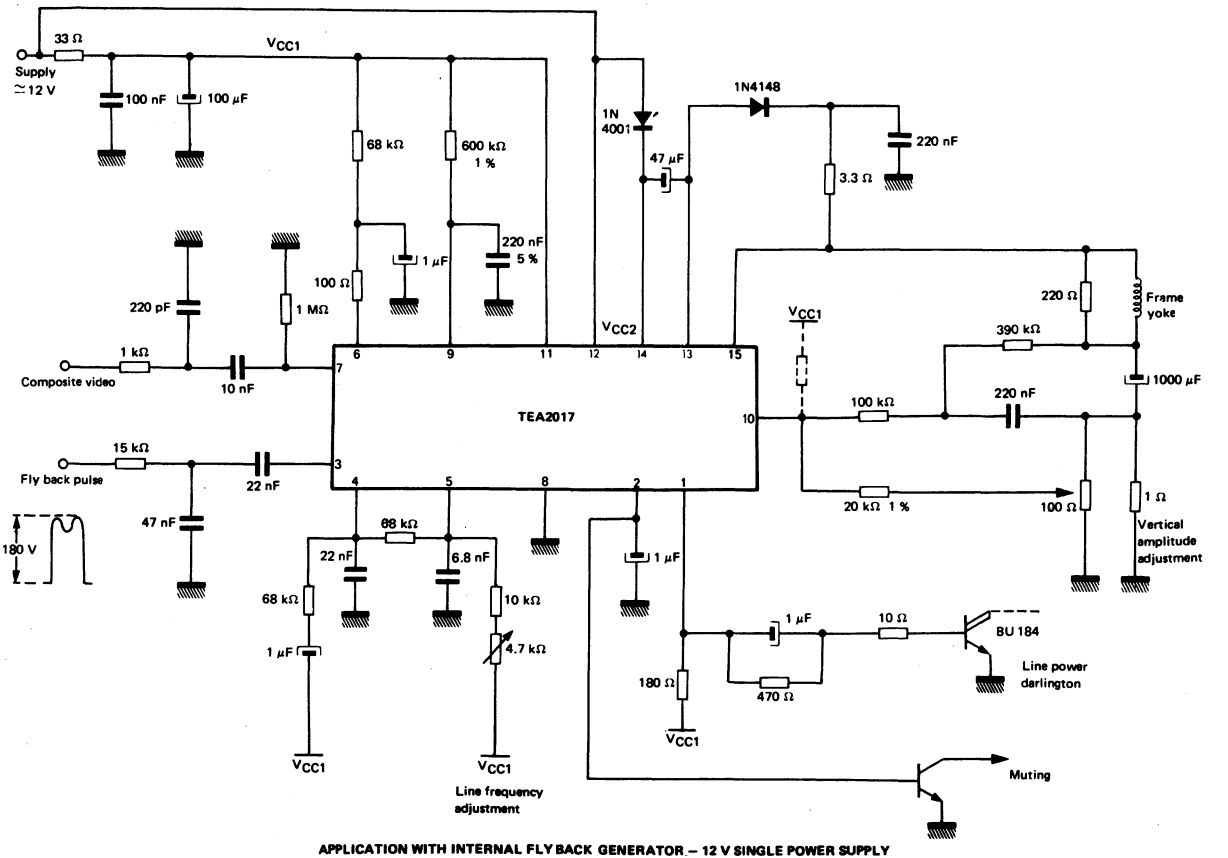
(with yoke L = 27 mH, R = 15 Ω, Ipp = 0.5 A)



V_{CC2} : Power stage supply from high voltage transformer.
V_{CC1} must be perfectly filtered.

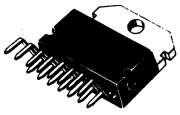
APPLICATION N° 2

TYPICAL BLACK-WHITE TV APPLICATION FOR 14" - 110° SCREEN
(with yoke L = 27 mH, R = 15 Ω, Ipp = 0.5 A)

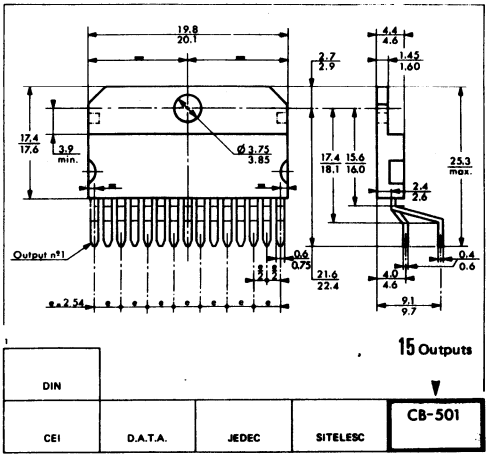


APPLICATION WITH INTERNAL FLY BACK GENERATOR – 12 V SINGLE POWER SUPPLY

CASE CB-501



SP SUFFIX
PLASTIC PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TEA2585

ADVANCE INFORMATION

DATA AND SYNCHRO SEPARATOR FOR DIDON DEMODULATION

The IC TEA 2585 is used with the IC TEA 2586 to realize a complete system of DIDON demodulation.

The TEA2585 IC realizes the extraction of numerical data present in a composite television signal using only the line synchronization (SLT) and the identificating bit train. The DC level of the input composite video signal is filtered.

After the signal is tracked out a reference level to allow a pre-separation which produces the CAG impulsion.

The synchronization extraction is made at a constant level by the use of a AGC loop. The resulting signal is treated to be compatible with TTL levels.

An automatic gain controlled amplifier is used to pull out the video part of the composite signal.

The numerical data extraction optimization implicates an extraction around the average level of the signal. The IC realizes the acquisition and the storage of the average level.

The research of this value necessitates three states :

- RAZ during the line synchronization SLT,
- peak detection during the inhibition window ($\overline{f}$) (after SLT),
- averaging during the window W.

The IC delivers an impulsed current to detect the identificating bit-train. This current launches a circuit tuned on the half bit frequency which is the identificating bit train frequency.

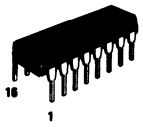
The inhibition window generator can be piloted by the synchronization of the IC or by an external synchronization signal.

- High video input impedance
- Synchronization and numerical data extraction of the video signal.

For operating principles of DIDON demodulator, refer to NA-021A application note.

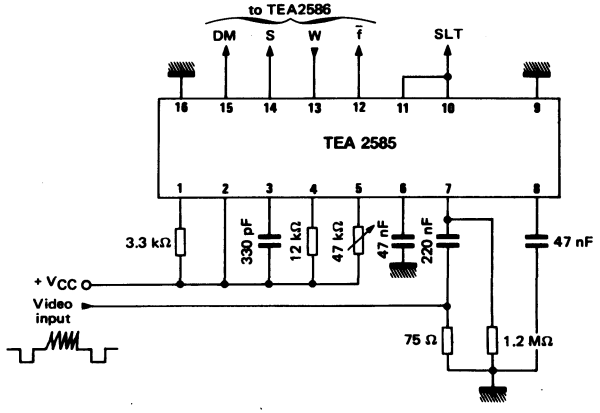
DATA AND SYNCHRO SEPARATOR FOR DIDON DEMODULATION

CASE CB-79



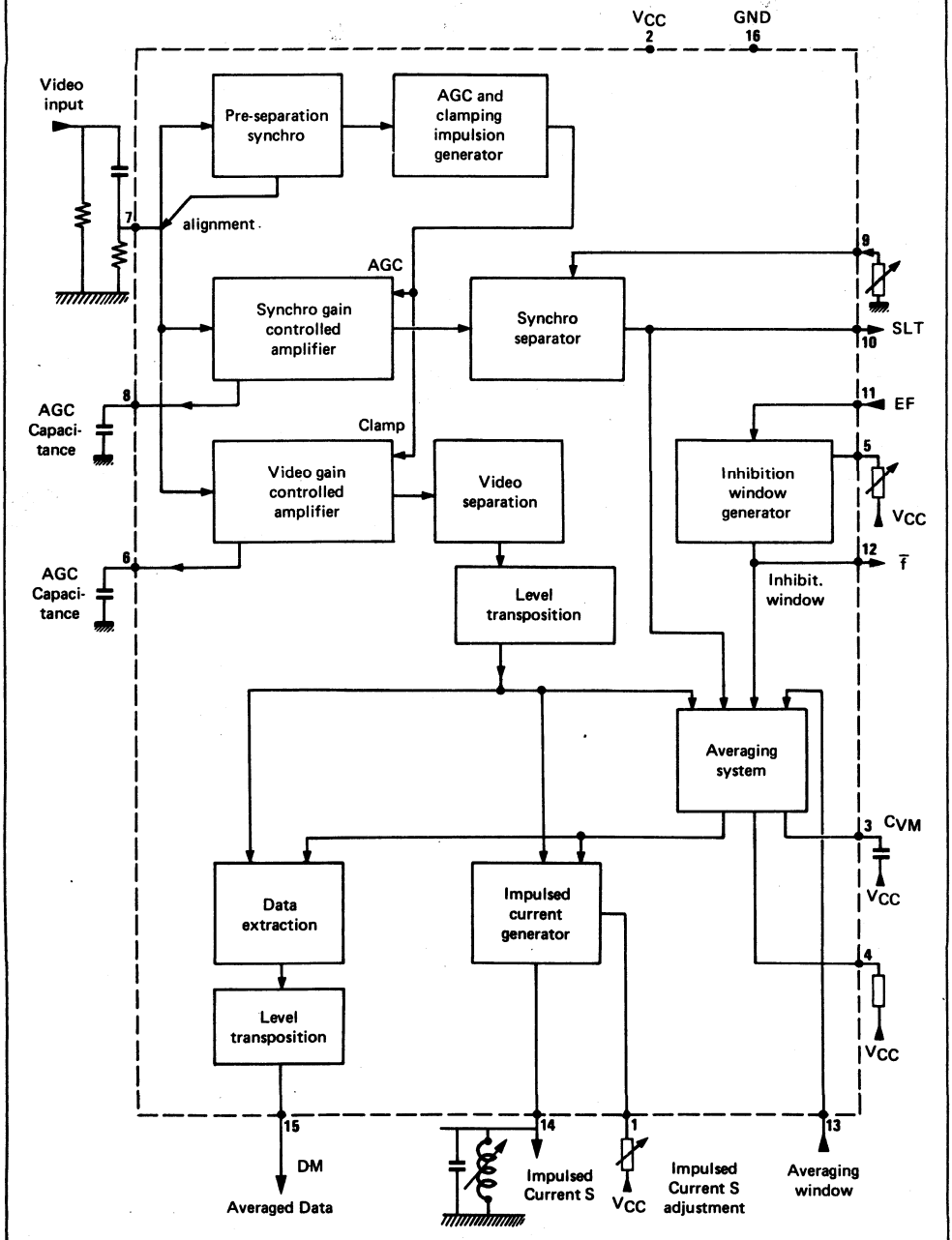
DP SUFFIX
PLASTIC PACKAGE

SIMPLIFIED APPLICATION

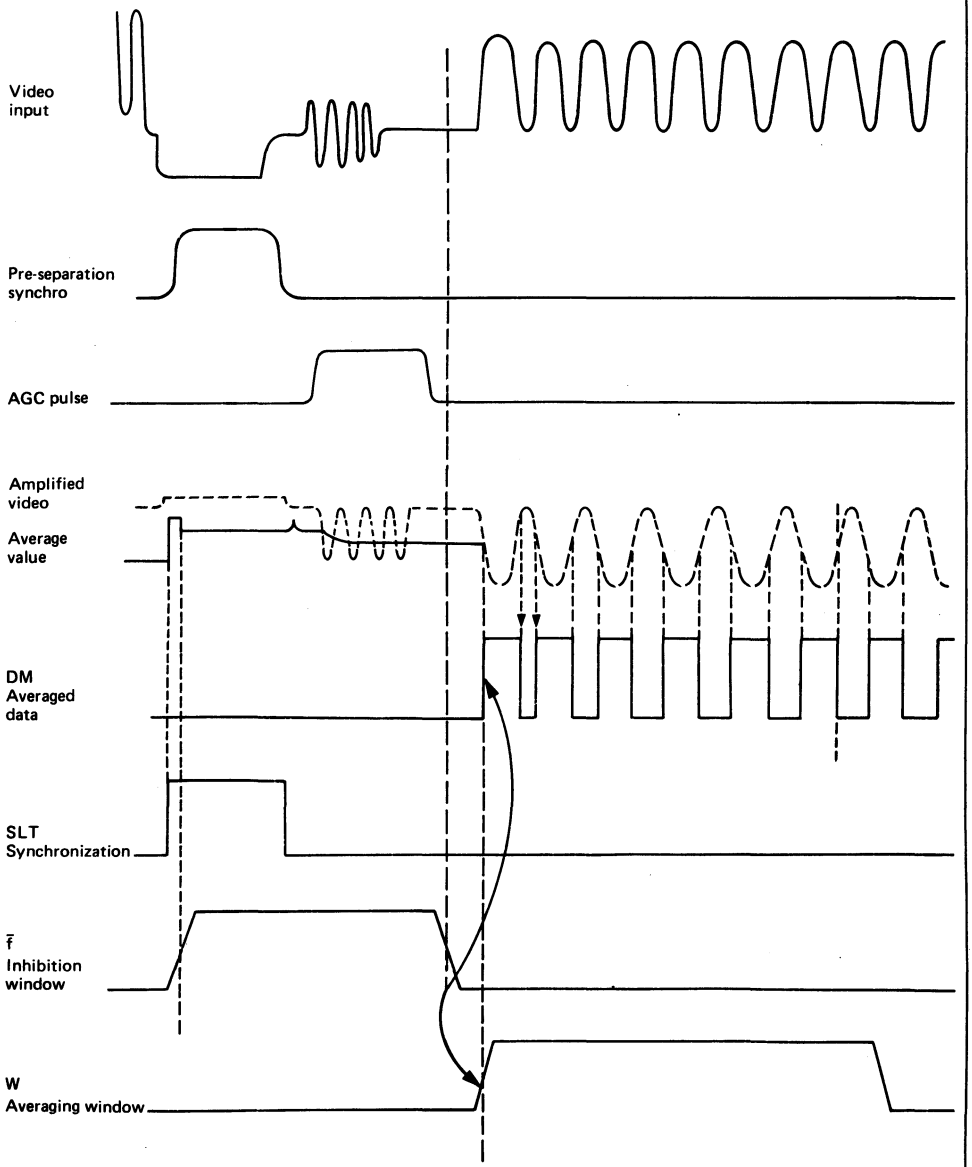


SP8219R1-A 1/7

BLOCK DIAGRAM



WAVEFORMS



For other waveforms, refer to NA-021A application note on general operating principle of DIDON demodulator.

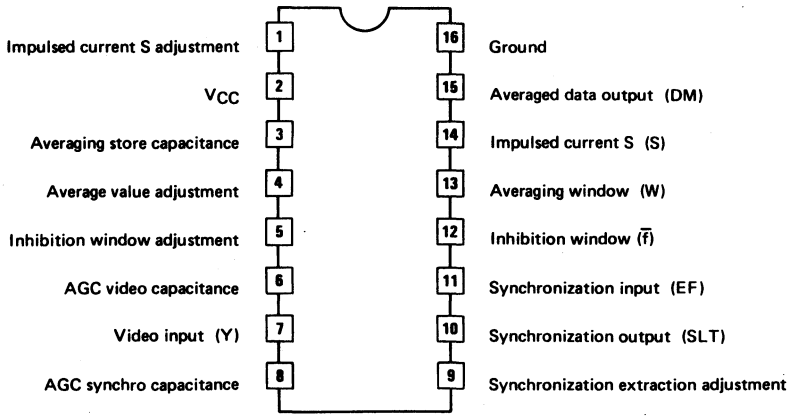
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	13.2	V
Maximum operating temperature		70	°C
Maximum junction temperature	T_j	150	°C
Storage temperature	T_{stg}	- 65,+ 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C ; V_{CC} = 12 V (unless otherwise specified).

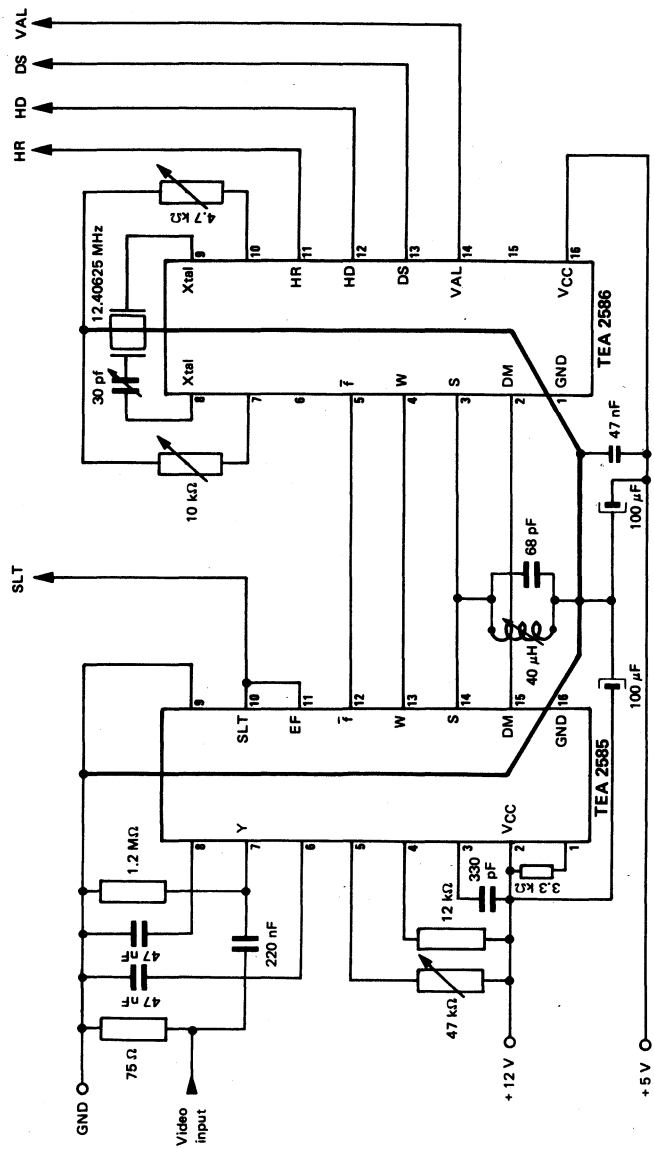
Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage (pin 2)		V_{CC}	10.8	12	13.2	V
Supply current (pin 2)		I_{CC}	–	40	–	mA
Composite video input voltage (pin 7)	Y	V_{in}				V_{PP}
Data (peak to peak)			0.3	0.7	2	
Synchro pulse (peak to peak)			0.1	0.3	1	
Input impedance (pin 7)			–	100	–	kΩ
Line - frame synchronization output (pin 10)	SLT					
Output low voltage		V_{OL}	0	–	0.4	V
Low level output current		I_{OL}	0	–	2	mA
Output high voltage		V_{OH}	2.4	–	5.5	V
High level output current		I_{OH}	- 0.4	–	0	mA
Line - frame synchronization input (pin 11)	EF					
Input low voltage		V_{IL}	–	–	0.6	V
Low level input current		I_{IL}	–	–	- 0.1	mA
Input high voltage		V_{IH}	2.2	–	–	V
High level input current		I_{IH}	–	–	0.4	mA
Inhibition window output (pin 12)	$\bar{f}$					
Output low voltage		V_{OL}	–	–	0.3	V
Low level output current		I_{OL}	–	–	0.2	mA
Output high voltage		V_{OH}	3.5	–	5	V
High level output current		I_{OH}	- 1	–	0	mA
Averaging window input (pin 13)	W					
Input low voltage		V_{IL}	–	–	0.6	V
Low level input current		I_{IL}	–	–	- 0.1	mA
Input high voltage		V_{IH}	2.2	–	–	V
High level input current		I_{IH}	–	–	0.4	mA
Impulsed current (pin 14) - Adjust by R on pin 1	S					
1 kΩ resistance on pin 14 to ground (tuned circuit deconnected)			0.2	–	3	mA
Averaged data (pin 15)	DM					
Output low voltage		V_{OL}	–	–	0.5	V
Low level output current		I_{OL}	–	–	0.4	mA
Output high voltage		V_{OH}	2.5	–	4.5	V
High level output current		I_{OH}	- 0.4	–	0	mA

DYNAMIC CHARACTERISTICS

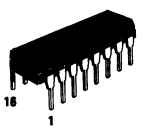
T_{amb} = + 25°C ; V_{CC} = 12 V (unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Line - frame synchronization output (pin 10)	SLT					
Rise time (transition between 0.6 and 2.2 V on C= 20 pF)		t_r	–	–	40	ns
Fall time (transition between 0.6 and 2.2 V on C= 20 pF)		t_f	–	–	40	ns
Width of SLT measured at 2.2 V ($V_{synchro}$= 300 mV ; V_{video}= 700 mV)		t_{SLT}	–	5	–	µs
Averaged data (pin 15)	DM					
Rise time (transition between 0.6 and 2.2 V on C= 20 pF)		t_r	–	–	25	ns
Fall time (transition between 0.6 and 2.2 V on C= 20 pF)		t_f	–	–	25	ns

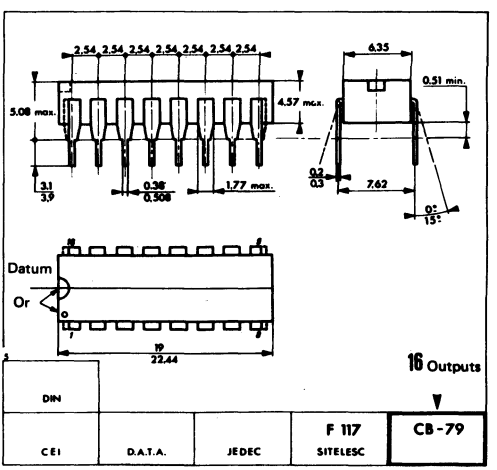
APPLICATION CIRCUIT
(for French standard)



CASE CB-79



DP SUFFIX
PLASTIC PACKAGE



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NOTES

THOMSON SEMICONDUCTORS

TEA2586

ADVANCE INFORMATION

DATA CLOCK GENERATOR AND TELETEXT IDENTIFICATION FOR DIDON DEMODULATOR

The IC TEA 2586 is used with the TEA 2585 to realise a complete system of DIDON demodulation.

This IC realizes the clock regeneratlon from a numerical data train. It generates also the validation signal which confirms the presence of teletext transmission. The IC realizes also the averaging window necessary for data extraction from the video signal.

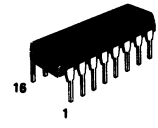
- Clock regeneration from a numerical data train
- Validation signal generation
- Averaging window generation

Data (DS) and validation (VAL) phasing on the selected clock (HD).

For operating principles of DIDON demodulator, refer to NA-021A application note.

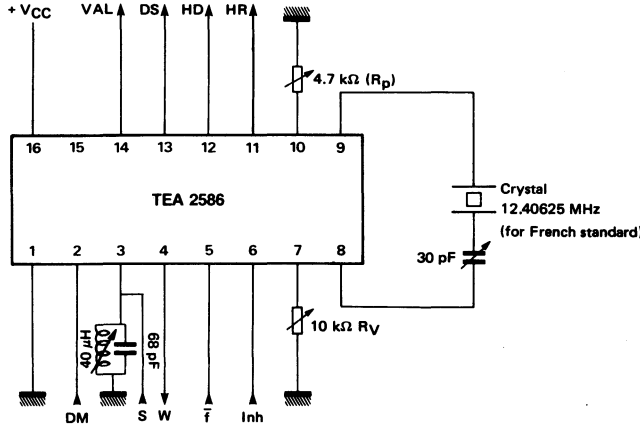
DATA CLOCK GENERATOR AND TELETEXT IDENTIFICATION FOR DIDON DEMODULATOR

CASE CB-79



DP SUFFIX
PLASTIC PACKAGE

SIMPLIFIED APPLICATION



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THOMSON COMPONENTS

CLOCK RESEARCH AND DATA PHASING

A local oscillator at twice bit frequency provides 4 clock signals by successive inversions and divisions. Each clock is phased at 90° on the others. A new division of each clock and a logic comparison with the averaged data, permits to realize a phase voltage converter during the bit identification train. The comparison of this voltage with a window of voltage permits to select, by sampling, a clock (HD) (phased at 45° on the averaged data). The selected clock is present until the next sampling (in the next line). The sampling pulse is given by count of the reference clock. The averaged data are phased on HD to give DS signal.

VALIDATION GENERATION (VAL)

The validation signal is produced by count of the selected clock. After it is phased around the end of byte synchronization.

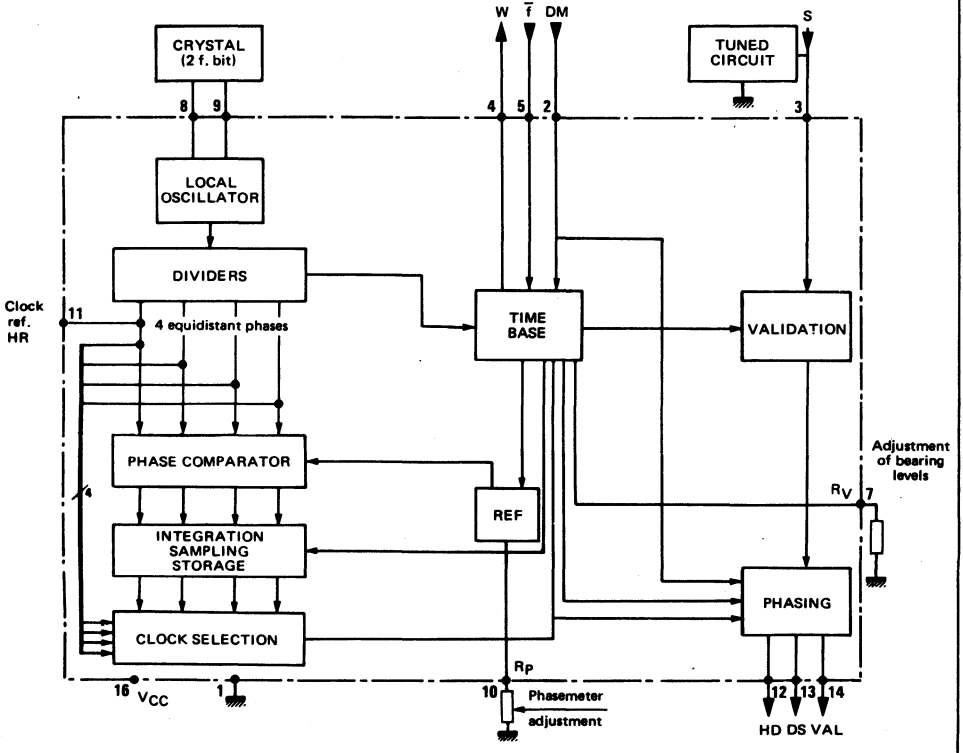
AVERAGING WINDOW

This signal appears simultaneously with the averaged data until the phasemeter sampling.

INHIBITION SIGNAL

A low level on this pin stops the transmission of DS, VAL. The presence of the bit identification train is controlled by a peak detection of the tuned circuit voltage, during the bit identification train, which produces the identificators Ψ and φ.

BLOCK DIAGRAM



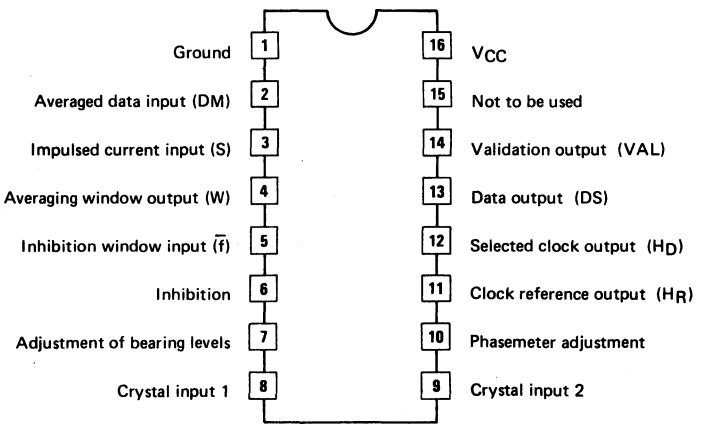
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	5.25	V
Maximum operating temperature	T_{oper}	70	°C
Maximum junction temperature	T_j	150	°C
Storage temperature	T_{stg}	- 65,+ 150	°C

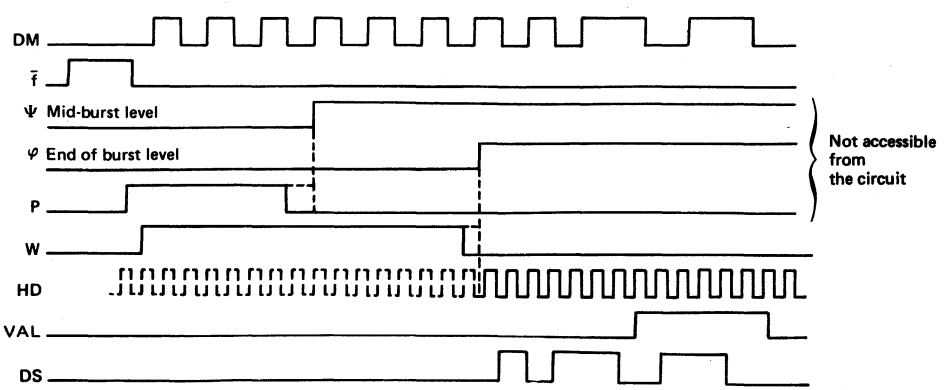
THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

PIN CONFIGURATION



TIMING DIAGRAM

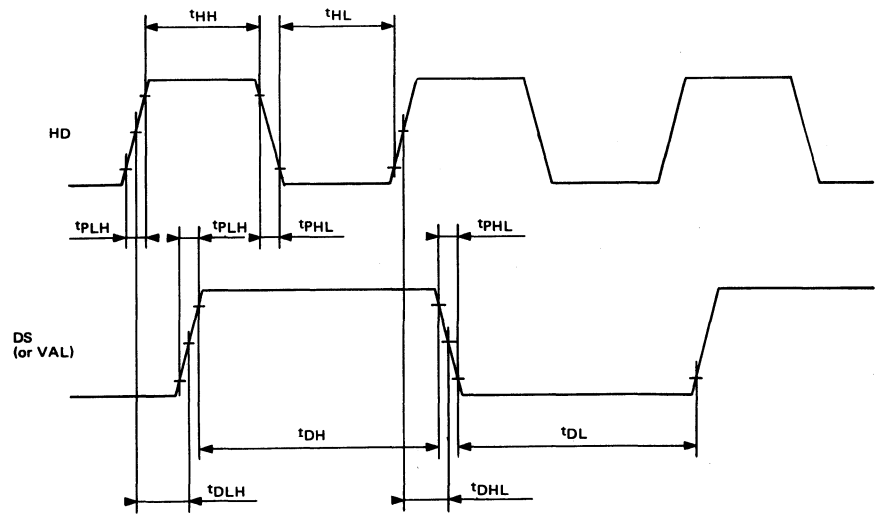


ELECTRICAL CHARACTERISTICS

$T_{amb} = +25°C$; $V_{CC} = 5$ V (unless otherwise specified).

Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage (pin 16)		V_{CC}	4.75	5	5.25	V
Supply current (pin 16)		I_{CC}	–	100	–	mA
Averaged data input (pin 2)	DM					
Input low voltage		V_{IL}	–	–	0.7	V
Low level input current		I_{IL}	–	–	0.4	mA
Input high voltage		V_{IH}	1.2	–	–	V
High level input current		I_{IH}	–	–	40	μA
Averaging window output (pin 4)	W					
Output low voltage		V_{OL}	–	–	0.4	V
Low level output current		I_{OL}	–	–	0.1	mA
Output high level		V_{OH}	2.5	–	–	V
High level output current		I_{OH}	–0.4	–	–	mA
Inhibition window (pin 5)	$\overline{f}$					
Input low level		V_{IL}	–	–	0.6	V
Low level input current		I_{IL}	–	–	–0.2	mA
Input high voltage		V_{IH}	2.5	–	–	V
High level input current		I_{IH}	–	–	1	mA
Clock reference output (pin 11)	HR					
Output low voltage		V_{OL}	–	–	0.6	V
Low level output current		I_{OL}	–	–	2	mA
Output high voltage		V_{OH}	2.4	–	–	V
High level output current		I_{OH}	–0.4	–	–	mA
Data clock output (pin 12)	HD					
Output low voltage		V_{OL}	–	–	0.6	V
Low level output current		I_{OL}	–	–	2	mA
Output high voltage		V_{OH}	2.4	–	–	V
High level output current		I_{OH}	–0.4	–	–	mA
Data output (pin 13)	DS					
Output low voltage		V_{OL}	–	–	0.6	V
Low level output current		I_{OL}	–	–	2	mA
Output high voltage		V_{OH}	2.4	–	–	V
High level output current		I_{OH}	–0.4	–	–	mA
Validation output (pin 14)	VAL					
Output low voltage		V_{OL}	–	–	0.6	V
Low level output current		I_{OL}	–	–	2	mA
Output high voltage		V_{OH}	2.4	–	–	V
High level output current		I_{OH}	–0.4	–	–	mA

DYNAMIC CHARACTERISTICS



DYNAMIC CHARACTERISTICS FOR FRENCH STANDARD

T_{amb} = + 25°C, V_{CC} = 5 V (unless otherwise specified)

CLOCK OUTPUT (HD) - pin 12

Parameter	Symbol	Min	Typ	Max	Unit
High level duration (measured at V_{OH} = 2.4 V with t_{bit} = 140 ns)	t_{HH1}	40	–	72	ns
Low level duration (measured at V_{OL} = 0.6 V)	t_{HL1}	–	60	–	ns
Propagation delay time from low to high level (measured between 0.6 and 2.4 V on C = 20 pF)	t_{PLH}	–	–	25	ns
Propagation delay time from high to low level (measured between 2.4 and 0.6 V on C = 20 pF)	t_{PHL}	–	–	20	ns

DATA OUTPUT (DS) - pin 13 or VALIDATION OUTPUT (VAL) - pin 14

High level duration (measured at V_{OH} = 2.4 V with t_{bit} = 140 ns)	t_{DH1}	115	–	137	ns
Low level duration (measured at V_{OL} = 0.6 V)	t_{DL1}	115	–	142	ns
Rise delay time from HD low to DS (or VAL) low	t_{DLH}	3	–	15	ns
Delay time from HD low to DS (or VAL) high	t_{DHL}	0	–	10	ns
Propagation delay time from low to high level (measured between 0.6 and 2.4 V on C = 20 pF)	t_{PLH}	–	–	20	ns
Propagation delay time from high to low level (measured between 2.4 and 0.6 V on C = 20 pF)	t_{PHL}	–	–	10	ns

DYNAMIC CHARACTERISTICS FOR OTHER STANDARDS

As the bit duration is different from French standard, the following parameters are obtained as follows :

CLOCK OUTPUT (HD)

$$t_{HH2} = t_{HH1} + \frac{t_{bit} - 140}{2}$$

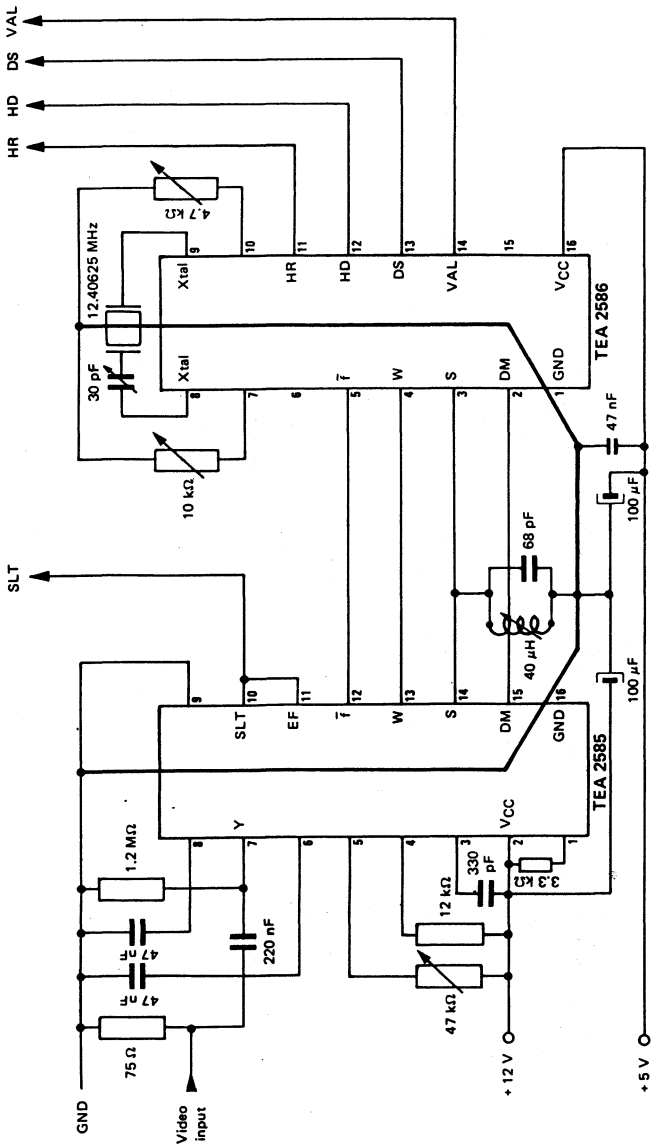
$$t_{HL2} = t_{HL1} + \frac{t_{bit} - 140}{2}$$

DATA OUTPUT (DS) or VALIDATION OUTPUT (VAL)

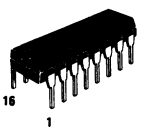
$$t_{DH2} = t_{DH1} + t_{bit} - 140$$

$$t_{DL2} = t_{DL1} + t_{bit} - 140$$

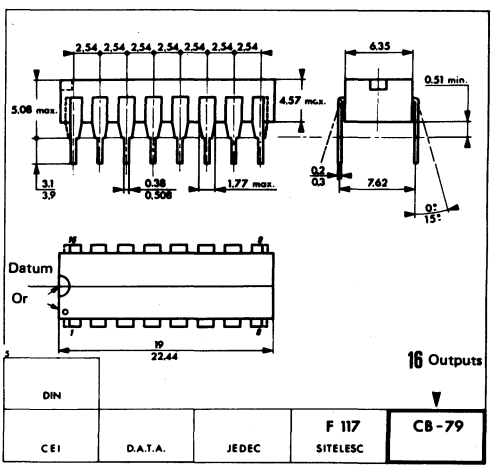
APPLICATION CIRCUIT
(for French standard)



CASE CB-79



DP SUFFIX
PLASTIC PACKAGE



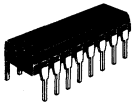
This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

AF AMPLIFIERS

AF AMPLIFIERS

CB-21 (QUIL14)



CB-79 (DIL16)

CB-98 (DIL8)

CB-109 (QUIL12)

CB-155 (QUIL12)

SINGLE PORTABLE RADIO AF AMPLIFIERS

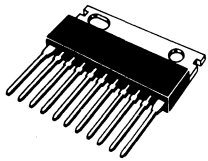
Operating supply voltage (V)	Output power (W) d = 10 % f = 1 kHz $R_L = 2\ \Omega$	$R_L = 4\ \Omega$	$R_L = 8\ \Omega$	R_L = ...	Fully protected	Bridge-able	Part number	Package	Page
4	–	0.35	–	–	–	–	TBA820M*	CB-98	437
6	–	0.75	0.45	–	–	–	TBA820M	CB-98	437
	–	1.0	–	–	–	–	TCA830SM	CB-98	447
9	–	1.6	1.2	–	–	–	TBA820M	CB-98	437
	–	1.6	1.2	–	–	–	TBA820	CB-21	429
	–	2.0	1.6	–	–	–	TCA830SM	CB-98	447
	–	2.0	1.6	–	–	–	TCA830SR	CB-109	455
	3.4	2.5	–	–	–	–	TBA810S,AS	CB-109/CB-155	421
	3.4	2.5	–	–	–	–	TEA2021	CB-313	539
12	–	–	2.3	–	–	–	TCA830SM	CB-98	447
	–	–	2.3	–	–	–	TCA830SR	CB-109	455
	5.5	4.0	–	–	–	–	TBA810P,AP	CB-109/CB-155	411
	5.5	4.0	–	–	–	–	TEA2021	CB-313	539

*3 V operation

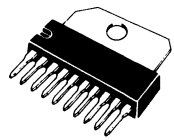
DUAL PORTABLE RADIO AF AMPLIFIERS

Operating supply voltage (V)	Output power per channel (W) d = 10 % f = 1 kHz $R_L = 2\ \Omega$	$R_L = 4\ \Omega$	$R_L = 8\ \Omega$	R_L = ...	Fully protected	Bridge-able	Part number	Package	Page
4	–	0.4	–	–	–	•	TEA2025*	CB-79	557
6	–	1.0	–	–	–	•	TEA2025	CB-79	557
9	–	2.3	1.3	–	–	•	TEA2025	CB-79	557
12	–	3.5 (10 W)**	–	–	•	•	TEA2024	CB-313	547
14.4	–	5.0	3.0 (10.5 W)**	–	•	•	TEA2024	CB-313	547

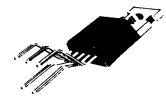
* : 3 V operation
** : Bridge application.



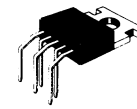
CB-173 (SIL11)



CB-313 (SIL10)



CB-360 (SIL5)



CB-367 (SIL5)

SINGLE CAR RADIO AF AMPLIFIERS

Operating supply voltage (V)	Output power (W) d = 10 % R_L = 1.6 Ω	R_L = 2 Ω	f = 1 kHz R_L = 4 Ω	R_L = 8 Ω	Fully protected	Bridge-able	Part number	Package	Page
12	–	5.5	4.0	–	–	–	TBA810P,AP	CB-109/CB-155	411
	–	5.5	4.0	–	–	–	TBA810CB,ACB	CB-109/CB-155	399
	–	5.5	4.0	–	–	–	TEA2021	CB-313	539
	8.0	5.5	–	–	•	•	TDA2003V,H	CB-360/CB-367	499
14.4	–	7.0	6.0	–	–	–	TBA810P,AP	CB-109/CB-155	411
	–	7.0	6.0	–	–	–	TBA810CB,ACB	CB-109/CB-155	399
	–	7.0	6.0	–	–	–	TEA2021	CB-313	539
	12.0	10.0	6.0	–	•	•	TDA2003V,H	CB-360/CB-367	499

4

SINGLE T.V. RECEIVER AF AMPLIFIERS

Operating supply voltage (V)	Output power (W) d = 10 % R_L = 2 Ω	R_L = 4 Ω	f = 1 kHz R_L = 8 Ω	R_L = 16 Ω	Fully protected	Bridge-able	Part number	Package	Page
18	–	–	4.5	–	–	–	TBA800,A	CB-109/CB-155	391
	–	9.0	5.0	–	•	–	TCA940,E	CB-109/CB-155	461
24	–	–	–	5.0	–	–	TBA800,A	CB-109/CB-155	391
	–	12.0	8.0	–	•	–	TNA2006V,H	CB-360/CB-367	513

SINGLE HI FI APPLICATIONS (INCLUDING T.V.)

Operating supply voltage (V)	Output power (W) d = 1 % R_L = 2 Ω	R_L = 4 Ω	f = 1 kHz R_L = 8 Ω	R_L = ...	Fully protected	Bridge-able	Part number	Package	Page
24	–	15.0	–	–	–	–	TDA1111	CB-173	489
	–	15.0	–	–	•	–	TDA1102	CB-173	471
28	–	14.0	9.0	–	•	–	TDA2030V,H	CB-360/CB-367	525
	–	20.0	10.4	–		–	TDA1111	CB-173	489
	–	20.0	10.4	–	•	–	TDA1102	CB-173	471
32	–	18.0	12.0	–	•	–	TDA2030V,H***	CB-360/CB-367	525

***Peak DC voltage : 42 V.

THOMSON SEMICONDUCTORS

TBA800
TBA800 A

AF AMPLIFIERS
AMPLIFICATEURS BF

The TBA800 is an integrated monolithic power AF amplifier for use in TV receivers, phonographs, tape recorders.
Due to suitable configuration of internal circuit, the following advantages can be provided :
- **The high idling current stability obtained from a built-in temperature and voltage-compensating network makes thermal runaway impossible.**
- **Open-loop gain is high enough to allow a great amount of feedback (low distorsion) and keep a sufficient closed loop-gain (high sensitivity).**
- **The differential preamplifier, fed from a controlled constant-current source, provides good immunity against power-supply ripple ; the use of PNP transistors in the preamplifier lets D.C. input reference voltage be zero.**
- **The exceptional D.C. output voltage stability and minimized potential loss, give to the output stage high power capability.**
- **Others highlights incluse : few external components and not any adjustment, ability to use an area of the printed circuit board as a heat sink.**

Le circuit intégré monolithique TBA800 est un amplificateur BF de puissance destiné aux téléviseurs, électrophones, magnétophones.
Grâce à une disposition convenable du schéma électrique interne, il a été possible d'obtenir les avantages suivants :
- Régulation du courant de repos en fonction de la tension d'alimentation et de la température, donc suppression du risque d'emballement thermique.
- Gain de boucle ouverte élevé, donc possibilité d'appliquer un taux de contre-réaction important (distorsion réduite) tout en conservant une sensibilité correcte.
- Préamplificateur à structure différentielle, donc grande immunité aux parasites de l'alimentation en raison du gain de mode commun réduit pour ce type de circuit.
- Etage d'entrée à transistors PNP, ce qui permet d'appliquer le signal en un point dont le potentiel continu de référence est à la masse.
- Régulation de la tension continue de sortie, avec une faible dispersion, ce qui garantit le fonctionnement symétrique de l'étage de puissance.
- Possibilité d'utiliser une partie du circuit imprimé comme radiateur.
- Absence de réglage et nombre de composants extérieurs réduit.

AF AMPLIFIERS
AMPLIFICATEURS BF

CASES / BOITIERS

CB-109

TBA 800

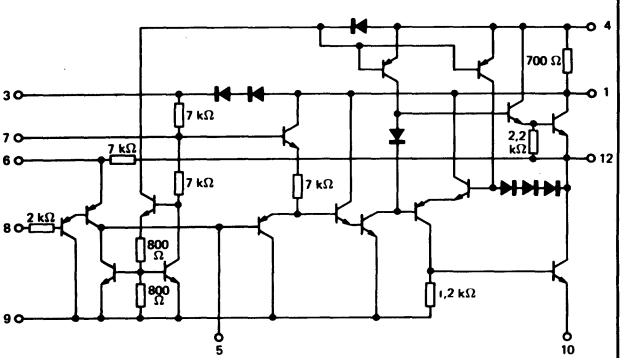
CB-155

TBA 800 A

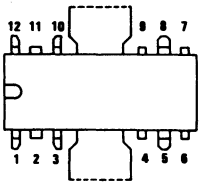
PLASTIC PACKAGES
BOITIERS PLASTIQUE

4

BLOCK DIAGRAM
SCHEMA ELECTRIQUE



PINS CONFIGURATIONS
BROCHAGES



Tab must be grounded
L'ailette doit être réunie à la masse

1 V_{CC}
2 **Not to use**
Ne pas utiliser
3 V_{CC} (− 2 x VD)
4 **Bootstrap**
Bootstrap
5 **Compensation**
Compensation
6 **Feed-back network**
Réseau de contre-réaction
7 **Preamplifier decoupling**
Découplage du préamplificateur
8 **Input / Entrée**
9 **Substrate and preamplifier ground**
Substrat et masse du préamplificateur
10 **Output stage ground**
Masse de l'étage de sortie
11 **Not to use**
Ne pas utiliser
12 **Output / Sortie**

NT 7607

THOMSON SEMICONDUCTORS
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Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

LIMITING VALUES
VALEURS LIMITES ABSOLUES

Supply voltage *Tension d'alimentation*	V_{CC}	30	V
Peak output current (non repetitive) *Courant crête en sortie non répétitif*	I_O	2	A
Peak output current (repetitive) *Courant crête en sortie répétitif*	I_O	1,5	A
Storage temperature *Température de stockage*	T_{stg}	−40 +150	°C °C
Junction temperature *Température de jonction*	T_j	−40 +150	°C °C

THERMAL CHARACTERISTICS
CARACTERISTIQUES THERMIQUES

* With tabs soldered to printed circuit with minimized copper area
Dissipateur soudé à une surface réduite de circuit imprimé

Junction-case thermal resistance *Résistance thermique (jonction-boîtier)*	$R_{th(j-c)}$	12 max	°C/W
Junction-ambient thermal resistance *Résistance thermique (jonction-ambiante)*	$R_{th(j-a)}$*	70 max	°C/W

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C (Note 1)

	Test conditions *Conditions de mesure*		Min.	Typ.	Max.	
Supply voltage *Tension d'alimentation*		V_{CC}	5		30	V
Quiescent output voltage (pin 12) *Tension de repos (broche 12)*	V_{CC} = 24 V	V_O	11	12	13	V
Quiescent current (pin 1) *Courant de repos (broche 1)*	V_{CC} = 24 V	I_{CC}		9	20	mA
Bias current (pin 8) *Courant d'entrée (broche 8)*	V_{CC} = 24 V	I_B		1	5	μA
Output power *Puissance de sortie*	V_{CC} = 24 V R_L = 16 Ω f = 1 kHz d = 10 %	P_O	4,4	5		W

Note 1 The characteristics above were obtained using the circuit shown in figure 1
Mesuré dans les conditions de la figure 1

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

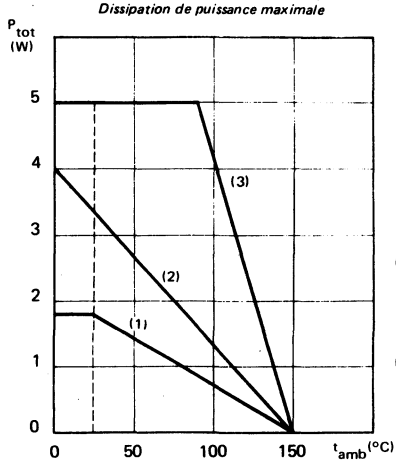
T_{amb} = 25°C (Note 1)

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Maximum input voltage peak *Tension d'entrée de crête maximale*		V_I		220			mV
Sensitivity *Sensibilité*	V_{CC} = 24 V R_L = 16 Ω P_O = 5 W R_f = 56 Ω f = 1 kHz	S			80		mV
Input resistance (pin 8) *Impédance d'entrée (broche 8)*		Z_I			5		MΩ
Frequency response (−3 dB) *Bande passante (−3 dB)*	V_{CC} = 24 V C3 = 330 pF R_L = 16 Ω R_f = 56 Ω	B			40 - 20 000		Hz
Distortion *Distorsion*	V_{CC} = 24 V P_O = 50 mW → 2,5 W R_L = 16 Ω R_f = 56 Ω f = 1 kHz	d			0,5		%
Voltage gain (open loop) *Gain de tension en boucle ouverte*	V_{CC} = 24 V R_L = 16 Ω f = 1 kHz	A_V			80		dB
Voltage gain (closed loop) *Gain de tension en boucle fermée*	V_{CC} = 24 V R_L = 16 Ω R_f = 56 Ω f = 1 kHz	A_V		39	42	45	dB
Input noise voltage *Tension de bruit à l'entrée*	V_{CC} = 24 V R_G = 0 B (−3 dB) = 40 - 20 000 Hz	V_n			5		μV
Input noise current *Courant de bruit à l'entrée*	V_{CC} = 24 V B (−3 dB) = 40 - 20 000 Hz	I_n			0,2		nA
Efficiency *Rendement*	V_{CC} = 24 V P_O = 5 W R_L = 16 Ω f = 1 kHz	η			75		%

4

GENERAL CHARACTERISTICS
CARACTERISTIQUES GENERALES

MAXIMUM POWER DISSIPATION
Dissipation de puissance maximale



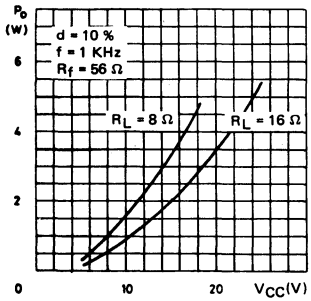
(1) : Without heatsink
Sans radiateur

(2) : With a 25°C/W heatsink
Avec radiateur de 25°C/W

(3) : With infinite heatsink
Avec radiateur infini

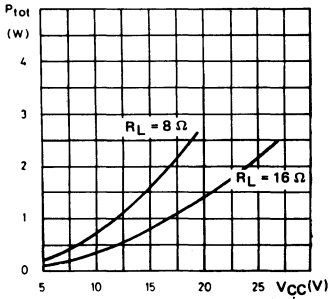
Output power vs. supply voltage.

Puissance de sortie en fonction de la tension d'alimentation.



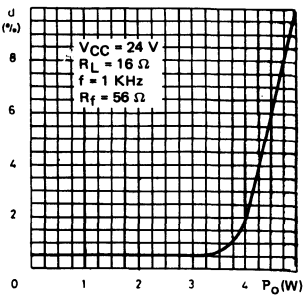
Maximum power dissipation vs. supply voltage.

Puissance dissipée maximale en fonction de la tension d'alimentation.



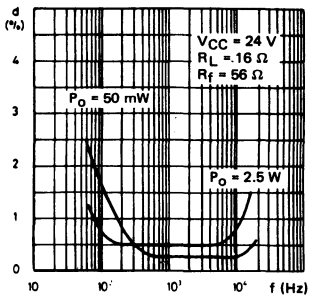
Distortion vs. output power.

Distorsion en fonction de la puissance de sortie.



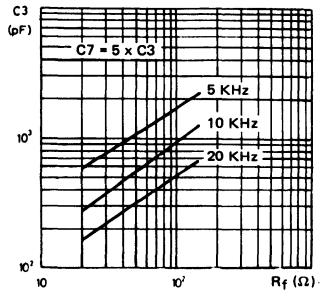
Distortion vs. fréquency.

Distorsion en fonction de la fréquence.



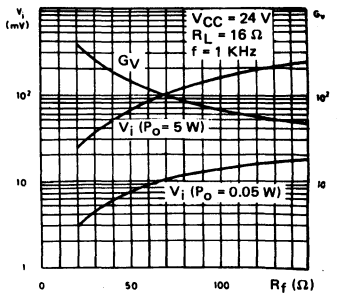
Value of C3 vs. R_f for various values of B.

Valeur de C3 en fonction de R_f pour différentes bandes passantes.



Voltage gain (closed loop) and input voltage vs. R_f.

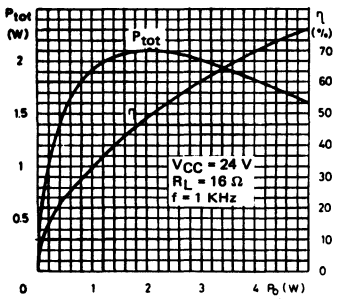
Gain en tension (bande fermée) et tension d'entrée en fonction de R_f.



4

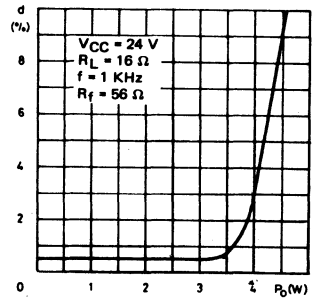
Power dissipation and efficiency vs. output power.

Puissance dissipée et rendement en fonction de la puissance de sortie.



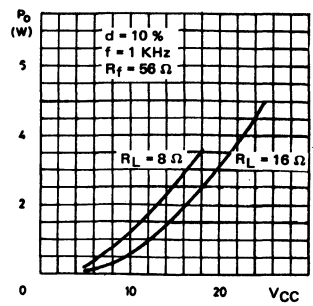
Distorsion vs. output power. Load connected to earth (see fig. 2).

Distorsion en fonction de la puissance de sortie. Charge à la masse (voir fig. 2).



Output power vs. supply voltage. Load connected to earth (see fig. 2).

Puissance de sortie en fonction de la tension d'alimentation. Charge à la masse (voir fig. 2).



APPLICATION AND TEST CIRCUITS
SCHÉMAS D'APPLICATION ET DE MESURE

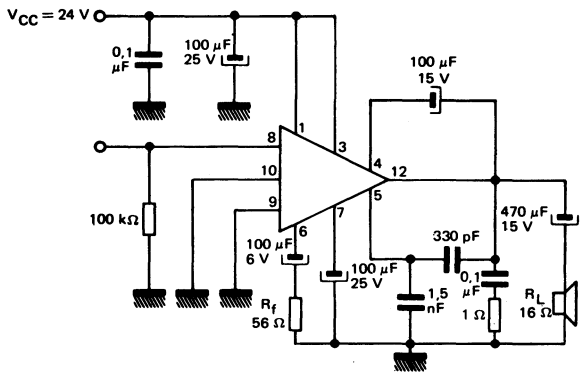
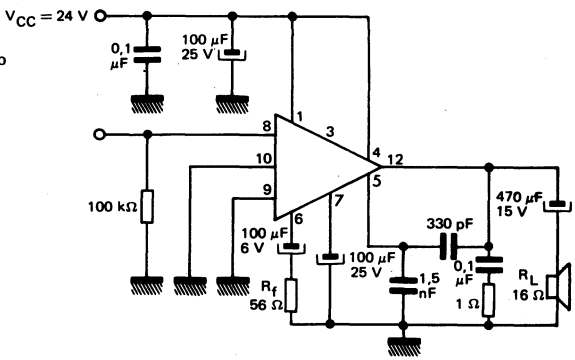


Figure 1

Load connected to earth, with bootstrap
Charge à la masse, avec bootstrap

Figure 2

load connected to earth, without bootstrap
Charge à la masse, sans bootstrap



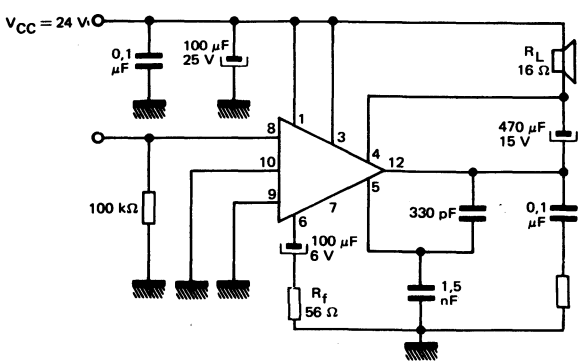
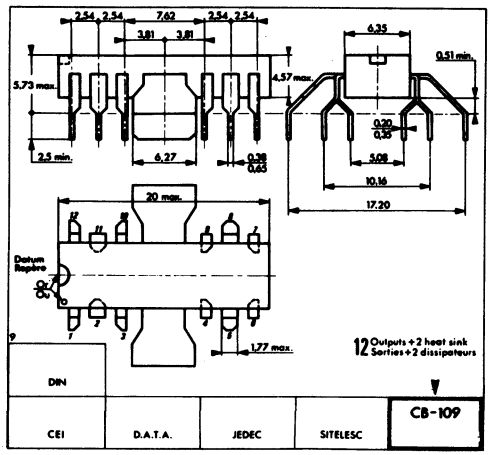


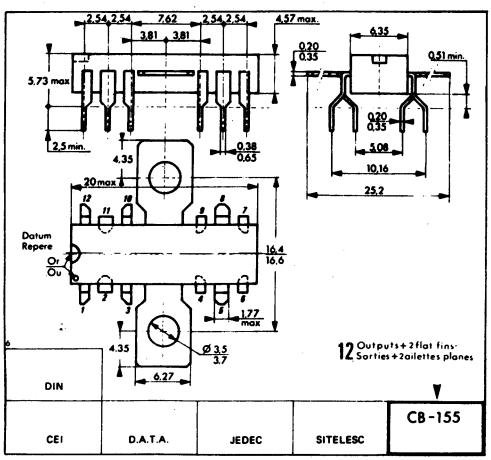
Figure 3

Load connected to supply, with bootstrap
Charge à l'alimentation, avec bootstrap

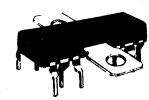


CASE / BOITIER
CB-109

PLASTIC PACKAGE
BOITIER PLASTIQUE



CASE / BOITIER
CB-155



PLASTIC PACKAGE
BOITIER PLASTIQUE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TBA810 CB
TBA810 ACB

AF AMPLIFIER
AMPLIFICATEUR BF

The TBA810 CB is an improvement of monolithic integrated circuit TBA810 S. Following advantages are provided:

- **Higher output power:**

  7 W at V_{CC} = 16 V, R_L = 4 Ω or and at V_{CC} = 14,4 V, R_L = 2Ω

- **Low noise**
- **Higher supply voltage ripple rejection**
- **Load dump protection up to 40 V**

The circuit is protected against overheating, output short circuits (V_{CC} ≤15 V), polarity inversion and fortuitous open ground.

Le TBA810 CB est une amélioration du circuit intégré monolithique TBA810 S. Il présente les avantages suivants:

- Puissance de sortie plus élevée:

  7 W pour V_{CC} = 16 V, R_L = 4 Ω et pour V_{CC} = 14,4 V, R_L = 2Ω.

- Bruit faible
- Meilleure réjection de l'ondulation d'alimentation
- Protection contre la déconnexion de la batterie.

Ce circuit est protégé contre les températures excessives, les court-circuits en sortie (V_{CC} ≤15 V), l'inversion de polarité et les coupures accidentelles d'une connexion de masse.

AF AMPLIFIER
AMPLIFICATEUR BF

CASES / BOITIERS

CB-109

TBA810 CB

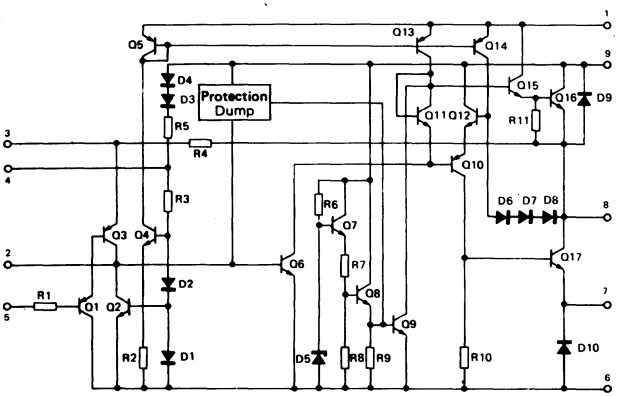
CB-155

TBA810 ACB

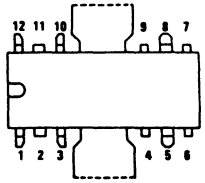
PLASTIC PACKAGES
BOITIERS PLASTIQUE

4

BLOCK DIAGRAM
SCHEMA ELETRIQUE



PIN CONFIGURATION
BROCHAGE



Tab must be grounded
L'ailette doit être réunie à la masse

1 V_{CC}	**7 Ripple rejection** Filtrage
2 Not to use Ne pas utiliser	**8 Input** / Entrée
3 Not to use Ne pas utiliser	**9 Substrate and preamplifier ground** Substrate et masse du préamplificateur
4 Bootstrap Boostrap	**10 Output stage ground** Masse de l'étage de sortie
5 Compensation Compensation	**11 Not to use** Ne pas utiliser
6 Feed-back network Réseau de contre-réaction	**12 Output** / Sortie

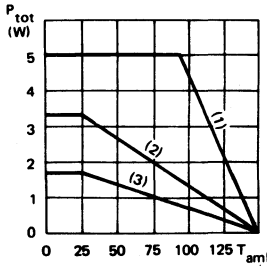
NT8026 1/12

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

Maximum power dissipation
Dissipation de puissance maximale

TBA 810 CB

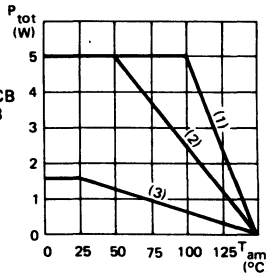


(1) With infinite heat sink
Avec radiateur infini

(2) With a 10°C/W heat sink - TBA 810 ACB
With a 25°C/W heat sink - TBA 810 CB
Avec radiateur de 10°C - TBA 810 ACB
Avec radiateur de 25°C - TBA 810 CB

(3) Without heat sink
Sans radiateur

TBA 810 ACB



LIMITING VALUES
VALEURS LIMITES ABSOLUES

Peak supply voltage (50 ms) *Tension d'alimentation crête*	V_{CC}	40	V
DC supply voltage *Tension d'alimentation continue*	V_{CC}	28	V
Supply voltage *Tension d'alimentation*	V_{CC}	20	V
Peak output current (non repetitive) *Courant crête en sortie non répétitif*	I_O	4	A
Peak output current (repetitive) *Courant crête en sortie répétitif*	I_O	3	A
Junction temperature *Température de jonction*	T_j	- 40 + 150	°C °C
Storage temperature *Température de stockage*	T_{stg}	- 40 + 150	°C °C

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C Note 1 V_{CC} = 14,4 V (Unless otherwise stated) *(Sauf indications contraires)*

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Supply voltage (pin 1) *Tension d'alimentation (broche 1)*		V_{CC}		4		20	V
Quiescent output voltage (pin 12) *Tension de repos (broche 12)*	V_{CC} = 14,4 V	V_O		6,4	7,2	8	V
Quiescent current *Courant de repos*	V_{CC} = 14,4 V	I_{CC}			12	20	mA
Bias current (pin 8) *Courant d'entrée (broche 8)*	V_{CC} = 14,4 V	I_B			0,4		µA
Output power *Puissance de sortie*	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 14,4 V	P_O		5,5	6		W
	d = 10 % R_L = 2 Ω f = 1 kHz V_{CC} = 14,4 V	P_O		5,5	7		W
Input voltage saturation (sine wave) *Tension d'entrée de saturation (sinusoïdale)*		V_{Irms}		220			mV
Sensitivity *Sensibilité*	P_O = 6 W V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz R_f = 56 Ω	S			75		mV
	P_O = 6 W V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz R_f = 22 Ω	S			30		mV
	P_O = 7 W V_{CC} = 14,4 V R_L = 2 Ω f = 1 kHz R_f = 56 Ω	S			55		mV
	P_O = 7 W V_{CC} = 14,4 V R_L = 2 Ω f = 1 kHz R_f = 22 Ω	S			20		mV
Input resistance (pin 8) *Impédance d'entrée (broche 8)*		Z_I			5		MΩ

Note 1 : The characteristics above were obtained using the circuit shown in figure 14
Mesuré dans les conditions de la figure 14

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C Note 1 (Unless otherwise stated) *(Sauf indications contraires)*

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Frequency response (−3 dB) *Bande passante (−3 dB)*	V_{CC} = 14,4 V R_L = 4 Ω / 2 Ω C3 = 820 pF C3 = 1500 pF	B			40 - 20.000 40 - 10.000		Hz Hz
Distortion *Distorsion*	V_{CC} = 14,4 V P_O = 50 mW → 2,5 W R_L = 4 Ω / 2 Ω f = 1 kHz	d			0,3		%
Voltage gain (open loop) *Gain de tension en boucle ouverte*	V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz	A_V			80		dB
Voltage gain (closed loop) *Gain de tension en boucle fermée*	V_{CC} = 14,4 V R_L = 4 Ω / 2 Ω f = 1 kHz	A_V		34	37	40	dB
Input noise voltage *Tension de bruit à l'entrée*	V_{CC} = 16 V B (−3 dB) = 40-15 000 Hz	v_n			2		μV
Input noise current *Courant de bruit à l'entrée*	V_{CC} = 16 V B (−3 dB) = 40 - 15 000 Hz	i_n			80		pA
Efficiency *Rendement*	V_{CC} = 14,4 V P_O = 6 W R_L = 4 Ω f = 1 kHz	η			75		%
Supply voltage rejection *Réjection de l'ondulation d'alimentation*	V_{CC} = 14,4 V R_L = 4 Ω V_{ripple} = 1 Vrms f = 100 Hz	SVR		40	48		dB

THERMAL CHARACTERISTICS
CARACTERISTIQUES THERMIQUES

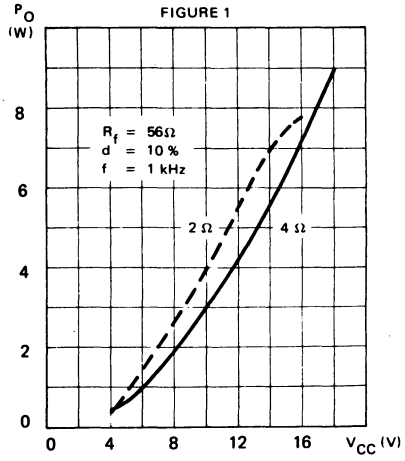
*With tabs soldered to printed circuit with minimized copper area
Dissipateur soudé à une surface réduite de circuit imprimé

Junction-case thermal resistance *Résistance thermique jonction-boîtier*		$R_{th(j-c)}$	max	12 (TBA 810 CB) 10 (TBA 810 ACB)	°C/W
Junction-ambient thermal resistance *Résistance thermique jonction-ambiante*		$R_{th(j-a)}$	max	70* (TBA 810 CB) 80 (TBA 810 ACB)	°C/W

Note 1 : The characteristics above were obtained using the circuit shown in figure 14
Mesuré dans les conditions de la figure 14

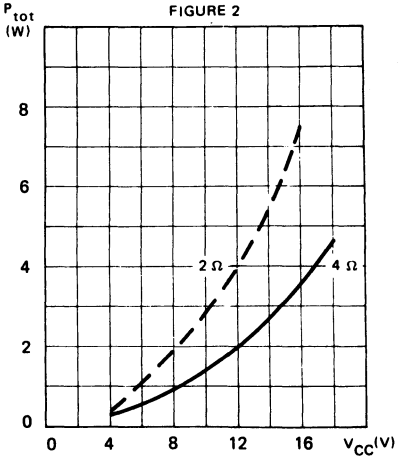
TYPICAL POWER OUTPUT VERSUS SUPPLY VOLTAGE
PUISSANCE DE SORTIE TYPIQUE EN FONCTION DE LA TENSION D'ALIMENTATION

FIGURE 1



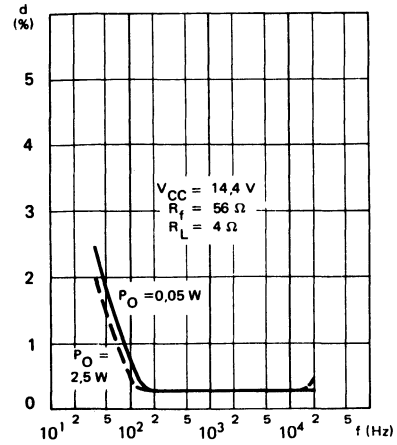
MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (sine wave operation)
PUISSANCE DISSIPEE MAXIMALE EN FONCTION DE LA TENSION D'ALIMENTATION (Onde sinusoïdale)

FIGURE 2



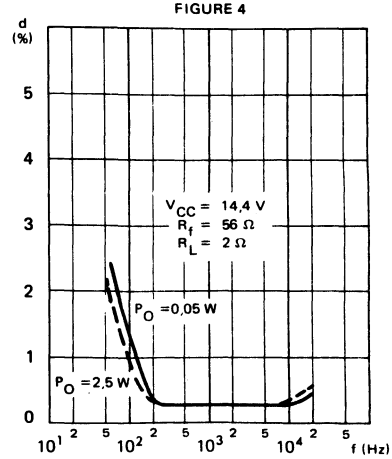
TYPICAL DISTORSION VERSUS FREQUENCY
DISTORSION TYPIQUE EN FONCTION DE LA FREQUENCE

FIGURE 3



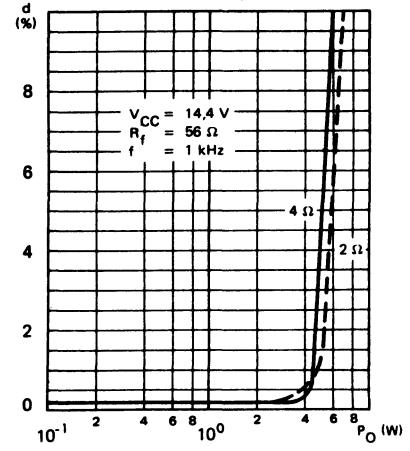
TYPICAL DISTORSION VERSUS FREQUENCY
DISTORSION TYPIQUE EN FONCTION DE LA FREQUENCE

FIGURE 4



TYPICAL DISTORSION VERSUS OUTPUT POWER
DISTORSION TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE

FIGURE 5



TYPICAL VALUE OF C3 VERSUS R_f FOR VARIOUS VALUES OF B
VALEUR TYPIQUE DE C3 EN FONCTION DE R_f POUR DIFFERENTES BANDES PASSANTES

FIGURE 6

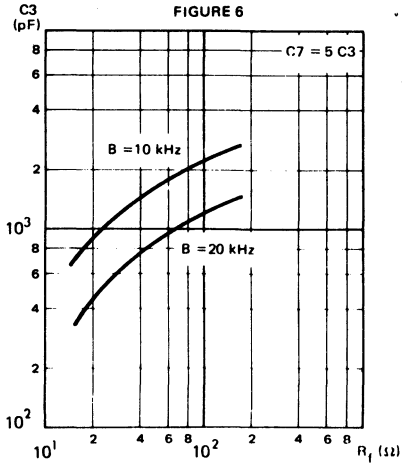
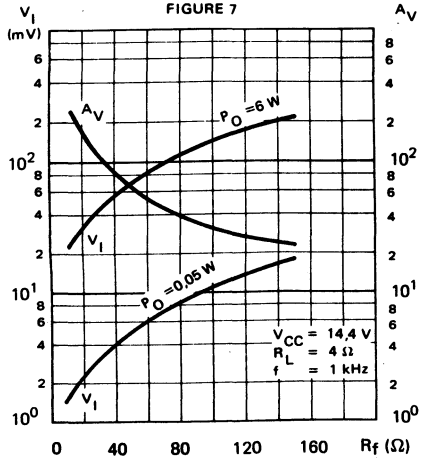


FIGURE 8

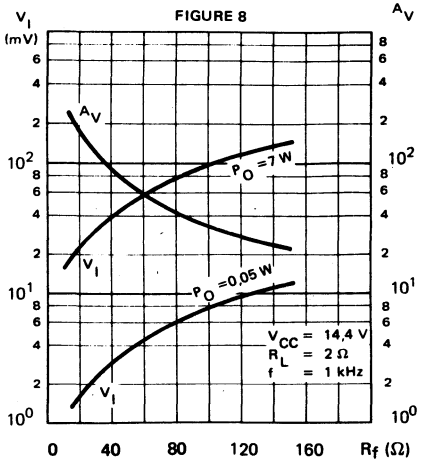
TYPICAL RELATIVE VOLTAGE GAIN (CLOSED LOOP) AND TYPICAL INPUT VOLTAGE VERSUS FEEDBACK RESISTANCE (R_f)
GAIN EN TENSION TYPIQUE (EN BOUCLE FERMEE) ET TENSION D'ENTREE TYPIQUE EN FONCTION DE LA RESISTANCE DE CONTRE REACTION (R_f)

FIGURE 7



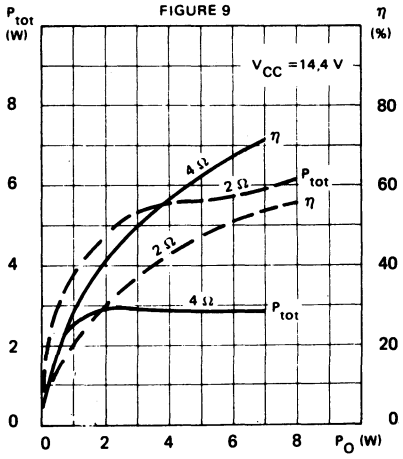
TYPICAL RELATIVE VOLTAGE GAIN (CLOSED LOOP) AND TYPICAL INPUT VOLTAGE VERSUS FEEDBACK RESISTANCE (R_f)
GAIN EN TENSION TYPIQUE (EN BOUCLE FERMEE) ET TENSION D'ENTREE TYPIQUE EN FONCTION DE LA RESISTANCE DE CONTRE REACTION (R_f)

FIGURE 8



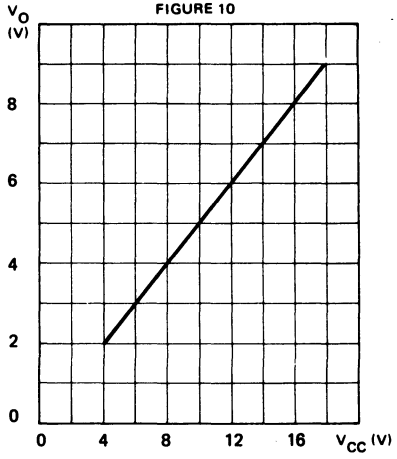
TYPICAL POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER
PUISSANCE DISSIPEE TYPIQUE ET RENDEMENT EN FONCTION DE LA PUISSANCE DE SORTIE

FIGURE 9



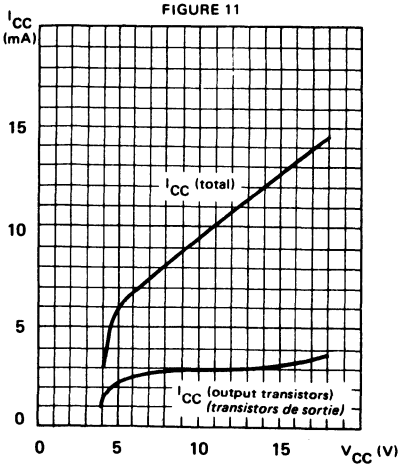
TYPICAL QUIESCENT OUTPUT VOLTAGE (Pin 12) VERSUS SUPPLY VOLTAGE
TENSION DE SORTIE TYPIQUE AU REPOS (Broche 12) EN FONCTION DE LA TENSION D'ALIMENTATION

FIGURE 10



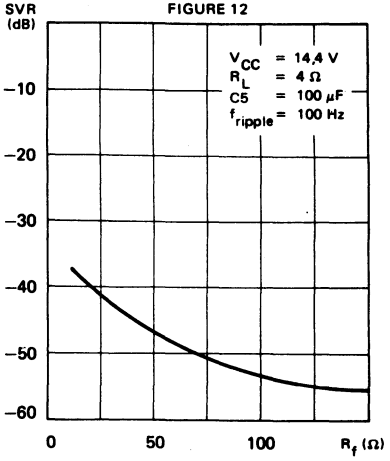
TYPICAL QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE
COURANT DE REPOS TYPIQUE EN FONCTION DE LA TENSION D'ALIMENTATION

FIGURE 11



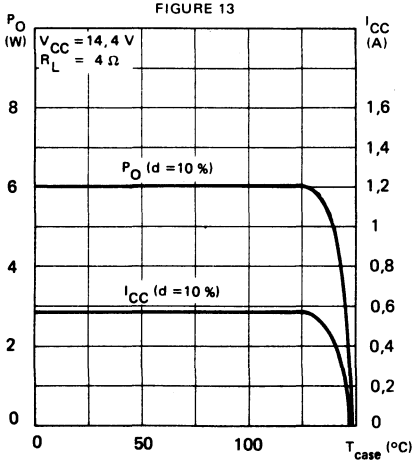
TYPICAL SUPPLY VOLTAGE REJECTION RATIO VERSUS FEEDBACK RESISTANCE
TAUX DE REJECTION DE L'ONDULATION D'ALIMENTATION EN FONCTION DE LA RESISTANCE DE CONTRE-REACTION

FIGURE 12



OUTPUT POWER AND SUPPLY CURRENT VERSUS PACKAGE TEMPERATURE
PUISSANCE DE SORTIE ET COURANT D'ALIMENTATION EN FONCTION DE LA TEMPERATURE DE BOITIER

FIGURE 13



THERMAL PROTECTION

A thermal limiting circuit is internally provided on TBA 810 CB to prevent chip temperature exceeding 150°C. This protection offers the following advantages :

1 – An overload on the output (even if permanent), or an above-limit ambient temperature can be withstood.

2 – The heatsink can be designed with smaller safety margins compared with that of a conventional power audio amplifier.

The TBA 810 CB will remain undamaged in the event of excessive junction temperature : all that happens is that P_O (and therefore P_{tot}) are reduced (Fig. 13).

PROTECTION THERMIQUE

Le TBA 810 CB comprend un circuit interne de limitation thermique qui empêche la température de la pastille de dépasser 150°C. Cette protection présente deux avantages :

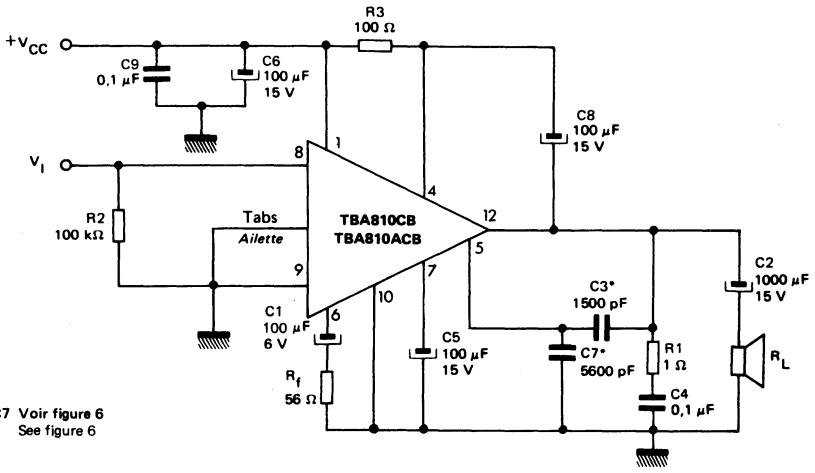
1 – Une surcharge sur la sortie (même permanente) ou un dépassement de la température ambiante limite ne sont pas destructifs pour le circuit.

2 – Le radiateur peut être calculé avec des marges de sécurité inférieures à celles qui seraient nécessaires pour un circuit ordinaire.

Au cas d'une température de jonction excessive le TBA 810 CB ne sera pas endommagé. La puissance de sortie, et donc la puissance dissipée seront simplement réduites (Fig. 13).

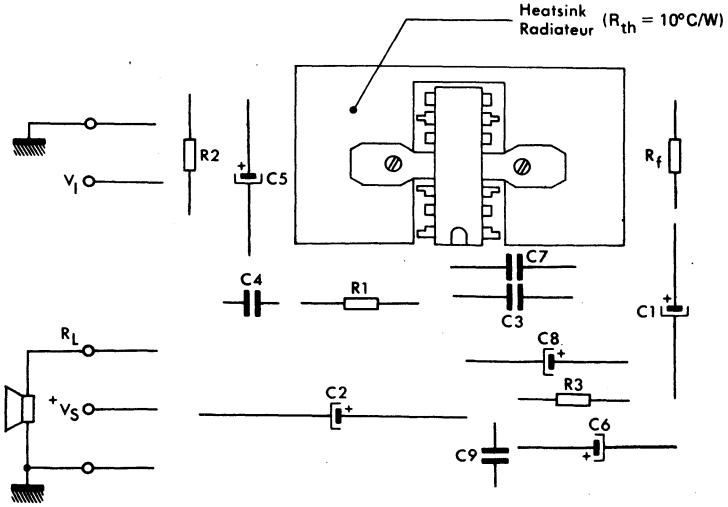
TEST AND APPLICATION CIRCUIT
CIRCUIT DE MESURE ET D'APPLICATION

FIGURE 14



*C3, C7 Voir figure 6
See figure 6

P.C. BOARD AND COMPONENT LAYOUT FOR THE TEST AND APPLICATION CIRCUIT OF FIG. 14
CIRCUIT IMPRIME ET COMPOSANTS DU CIRCUIT DE LA FIG. 14 (VUE COTE COMPOSANTS)



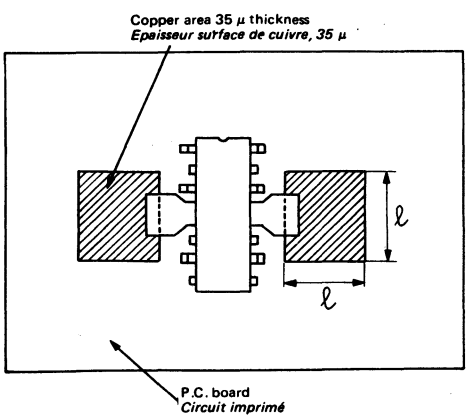
MOUNTING INSTRUCTIONS

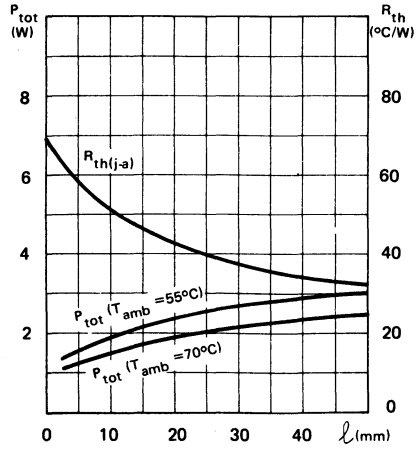
The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heatsink (see maximum power dissipation, page 2) or by soldering them to an area of copper on the printed circuit board (Fig. 15). During soldering, tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

INSTRUCTIONS DE MONTAGE

La puissance dissipée dans le circuit peut être evacuée soit en fixant les ailettes sur un radiateur extérieur (voir dissipation de puissance maximum, page 2), soit en les soudant à une surface de cuivre du circuit imprimé (Fig. 15). Dans ce dernier cas, le temps de soudure ne doit pas dépasser 12 secondes et la température des ailettes doit rester inférieure à 260°C.

FIGURE 15 : TBA 810 CB MOUNTING EXAMPLE
EXEMPLE DE MONTAGE DU TBA 810 CB





BUILT-IN PROTECTION SYSTEMS

Load dump protection

The load dump case occurs in a car when the engine is running and the battery is disconnected : voltage spikes on the power line are supplied by the alternator since there is no clamping effect due to battery capacitance.

The TBA 810 CB was designed to withstand a pulse train on pin 1, of the type shown in Fig. 16. Providing an LC filter is included, as shown in Fig. 17, a much higher pulse train amplitude (up to 100 V_{peak}) is allowed on the supply line with no damage to the device.

SYSTEMES DE PROTECTION

Protection contre la déconnexion de la batterie

Dans une automobile, lorsque le moteur tourne, si la batterie est déconnectée, les surtensions produites par l'alternateur se retrouvent sur la ligne d'alimentation puisque l'écrêtage dû à l'effet "capacité" de la batterie ne se produit plus.

Le TBA 810 CB a été conçu pour supporter sans dommage sur la broche 1 un train d'impulsion semblable à celui décrit Fig. 16. Si un filtre LC (Fig. 17) a été prévu, les impulsions peuvent avoir une amplitude plus grande (jusqu'à 100 V) sans danger pour le circuit.

FIGURE 16

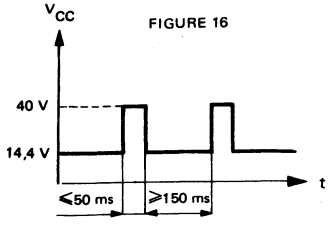
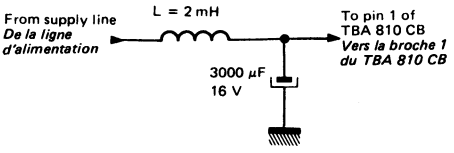


FIGURE 17



BUILT-IN PROTECTION SYSTEMS (continued)

Short-circuit protection

The TBA 810 CB can withstand a permanent short-circuit across the load for a supply voltage up to 15 V.

Polarity inversion protection

High current (up to 5 A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1 A fuse (normally connected in series with the supply). This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

Open ground protection

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TBA 810 CB, protection diodes are included to avoid any damage.

Inductive load protection

A protection diode is provided between pin 12 and pin 1 (see the internal schematic diagram) to allow use of the TBA 810 CB with inductive loads.

In particular, the TBA 810 CB can drive the coupling transformer for audio modulation in CB transmitters.

DC voltage protection

The maximum operating DC voltage on the TBA 810 CB is 20 V.

However the device can withstand a DC voltage up to 28 V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

SYSTEMES DE PROTECTION (suite)

Protection contre les court-circuits

Le TBA 810 CB peut supporter un court-circuit permanent de la charge pour une tension d'alimentation jusqu'à 15 V.

Protection contre l'inversion de polarité

Un courant élevé (jusqu'à 5 A) peut être supporté sans dommage, par le circuit pendant une durée supérieure au temps nécessaire pour faire fondre le fusible rapide 1 A qui doit normalement être prévu en série avec l'alimentation. Cette caractéristique a été prévue pour éviter une destruction due à l'inversion des fils d'alimentation durant le montage du poste dans la voiture.

Protection contre la coupure de la masse

Lorsque le poste de radio est en marche et si la connexion de masse est accidentellement ouverte, un amplificateur basse fréquence courant sera en général détruit. Le TBA 810 CB comprend des diodes de protection qui évitent toute détérioration.

Protection pour charge inductive

Une diode de protection a été prévue entre les broches 1 et 12 (voir schéma électrique) pour permettre l'utilisation du TBA 810 CB avec une charge inductive.

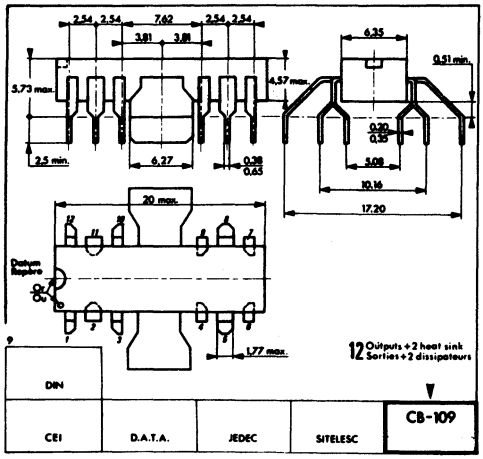
Cela permet, en particulier au TBA 810 CB, d'attaquer le transformateur de couplage pour la modulation basse fréquence des émetteurs en "bande amateurs".

Protection pour la tension continue d'alimentation

La tension maximale d'alimentation du TBA 810 CB est 20 V.

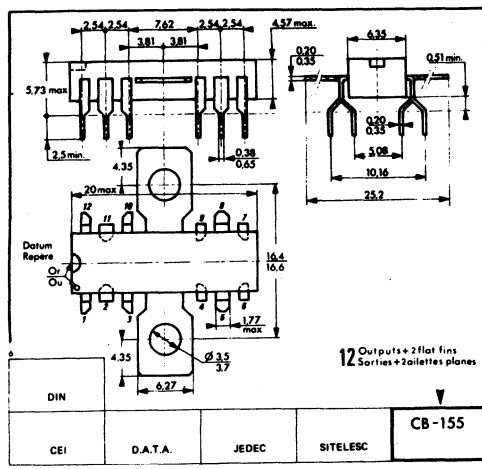
Toutefois le circuit peut supporter une alimentation atteignant 28 V, ce qui peut se produire en hiver lorsque deux batteries sont utilisées en série pour faire démarrer le moteur.

4



CASE / BOITIER
CB-109

PLASTIC PACKAGE
BOITIER PLASTIQUE



CASE / BOITIER
CB-155

PLASTIC PACKAGE
BOITIER PLASTIQUE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TBA810 P
TBA810 AP

AF AMPLIFIER
AMPLIFICATEUR BF

The TBA810 P is an improvement of monolithic integrated circuit TBA810 S. Following advantages are provided :

- **Higher outpout power :**

  6 W at V_{CC} = 16 V, R_L = 4 Ω or 7 W at V_{CC} = 14,4 V, R_L = 2Ω.

- **Lower noise figure**
- **Higher supply voltage ripple rejection.**

The circuit is protected against overheating, output short circuits ($V_{CC} \leqslant 15$ V), polarity inversion and fortuitous open ground.

Le TBA810 P est une amélioration du circuit intégré monolithique TBA810 S.
Il présente les avantages suivants :

- Puissance de sortie plus élevée :

  6 W pour V_{CC} = 16 V, R_L = 4 Ω ou 7 W pour V_{CC} = 14,4 V, R_L = 2 Ω.

- Facteur de bruit plus faible.
- Meilleure réjection de l'ondulation d'alimentation.

Ce circuit est protégé contre les températures excessives, les court-circuits en sortie ($V_{CC} \leqslant 15$ V), l'inversion de polarité et les coupures accidentelles d'une connexion de masse.

AF AMPLIFIER
AMPLIFICATEUR BF

CASES / BOITIERS

CB-109

TBA810 P

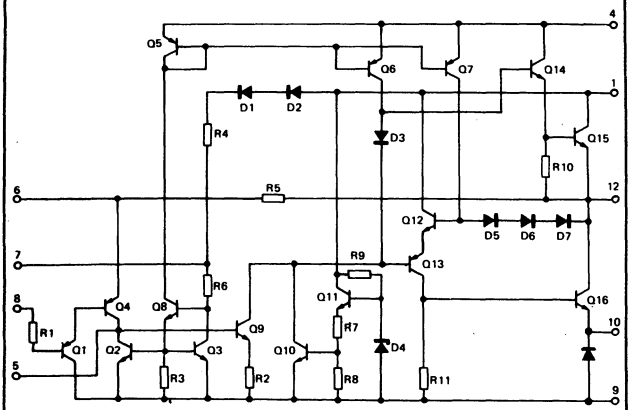
CB-155

TBA810 AP

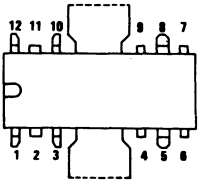
PLASTIC PACKAGES
BOITIERS PLASTIQUE

4

BLOCK DIAGRAM
SCHEMA ELECTRIQUE



PINS CONFIGURATION
BROCHAGES



Tab must be grounded
L'ailette doit être réunie à la masse

1 V_{CC}
2 **Not to use**
Ne pas utiliser
3 **Not to use**
Ne pas utiliser
4 **Bootstrap**
Bootstrap
5 **Compensation**
Compensation
6 **Feed-back network**
Réseau de contre-réaction
7 **Preamplifier decoupling**
Découplage du préamplificateur
8 **Input** / Entrée
9 **Substrate and preamplifier ground**
Substrat et masse du préamplificateur
10 **Output stage ground**
Masse de l'étage de sortie
11 **Not to use**
Ne pas utiliser
12 **Output** / Sortie

NT7841

THOMSON SEMICONDUCTORS
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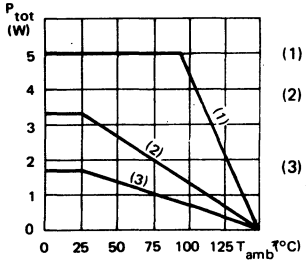
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

Maximum power dissipation
Dissipation de puissance maximale

TBA 810 P

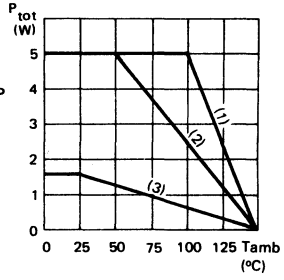


(1) With infinite heat sink
Avec radiateur infini

(2) With a 10°C/W heat sink - TBA 810 AP
With a 25°C/W heat sink - TBA 810 S
Avec radiateur de 10°C - TBA 810 AP
Avec radiateur de 25°C - TBA 810 P

(3) Without heat sink
Sans radiateur

TBA 810 AP



LIMITING VALUES
VALEURS LIMITES ABSOLUES

Supply voltage *Tension d'alimentation*	V_{CC}	20	V
Peak output current (non repetitive) *Courant crête en sortie non répétitif*	I_O	4	A
Peak output current (repetitive) *Courant crête en sortie répétitif*	I_O	3	A
Junction temperature *Température de jonction*	T_j	−40 +150	°C °C
Storage temperature *Température de stockage*	T_{stg}	−40 +150	°C °C

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C Note 1 (Unless otherwise stated) *(Sauf indications contraires)*

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Supply voltage (pin 1) *Tension d'alimentation (broche 1)*		V_{CC}		4		20	V
Quiescent output voltage (pin 12) *Tension de repos (broche 12)*	V_{CC} = 14,4 V	V_O		6,4	7,2	8	V
Quiescent current *Courant de repos*	V_{CC} = 14,4 V	I_{CC}			12	20	mA
Bias current (pin 8) *Courant d'entrée (broche 8)*	V_{CC} = 14,4 V	I_B			0,4		µA
Output power *Puissance de sortie*	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 14,4 V	P_O		5,5	6		W
	d = 10 % R_L = 2 Ω f = 1 kHz V_{CC} = 14,4 V	P_O		5,5	7		W
Input voltage saturation (sine wave) *Tension d'entrée de saturation (sinusoïdale)*		V_I		220			mV
Sensitivity *Sensibilité*	P_O = 6 W V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz R_f = 56 Ω	S			75		mV
	P_O = 6 W V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz R_f = 22 Ω	S			30		mV
	P_O = 7 W V_{CC} = 14,4 V R_L = 2 Ω f = 1 kHz R_f = 56 Ω	S			55		mV
	P_O = 7 W V_{CC} = 14,4 V R_L = 2 Ω f = 1 kHz R_f = 22 Ω	S			20		mV
Input resistance (pin 8) *Impédance d'entrée (broche 8)*		Z_I			5		MΩ

Note 1 : The characteristics above were obtained using the circuit shown in figure 14
Mesuré dans les conditions de la figure 14

4

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C Note 1 (Unless otherwise stated) *(Sauf indications contraires)*

	Test conditions *Conditions de mesure*			Min. Typ. Max.	
Frequency response (−3 dB) *Bande passante (−3 dB)*	V_{CC} = 14,4 V R_L = 4 Ω / 2 Ω C3 = 820 pF C3 = 1500 pF	B		40 - 20.000 40 - 10.000	Hz Hz
Distortion *Distorsion*	V_{CC} = 14,4 V P_O = 50 mW ÷ 2,5 W R_L = 4 Ω / 2 Ω f = 1 kHz	d		0,3	%
Voltage gain (open loop) *Gain de tension en boucle ouverte*	V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz	A_V		80	dB
Voltage gain (closed loop) *Gain de tension en boucle fermée*	V_{CC} = 14,4 V R_L = 4 Ω / 2 Ω f = 1 kHz	A_V		34 37 40	dB
Input noise voltage *Tension de bruit à l'entrée*	V_{CC} = 16 V B (−3 dB) = 40 - 15 000 Hz	v_n		2	μV
Input noise current *Courant de bruit à l'entrée*	V_{CC} = 16 V B (−3 dB) = 40 - 15 000 Hz	i_n		80	
Efficiency *Rendement*	V_{CC} = 14,4 V P_O = 6 W R_L = 4 Ω f = 1 kHz	η		75	%
Supply voltage rejection *Réjection de l'ondulation d'alimentation*	V_{CC} = 14,4 V R_L = 4 Ω f_{ripple} = 100 Hz	SVR		40 48	dB
Supply current *Courant d'alimentation*	P_O = 6 W V_{CC} = 14,4 V R_L = 4 Ω	I_{CC}		600	mA

THERMAL CHARACTERISTICS
CARACTERISTIQUES THERMIQUES

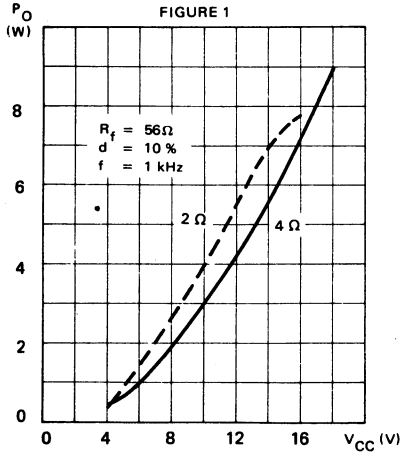
*With tabs soldered to printed circuit with minimized copper area
Dissipateur soudé à une surface réduite de circuit imprimé

Junction-case thermal resistance *Résistance thermique jonction-boîtier*		$R_{th(j-c)}$	max	12 (TBA 810 P) 10 (TBA 810 AP)	°C/W
Junction-ambient thermal resistance *Résistance thermique jonction-ambiante*		$R_{th(j-a)}$	max	70* (TBA 810 S) 80 (TBA 810 AP)	°C/W

Note 1 : The characteristics above were obtained using the circuit shown in Figure 14
Mesuré dans les conditions de la figure 14

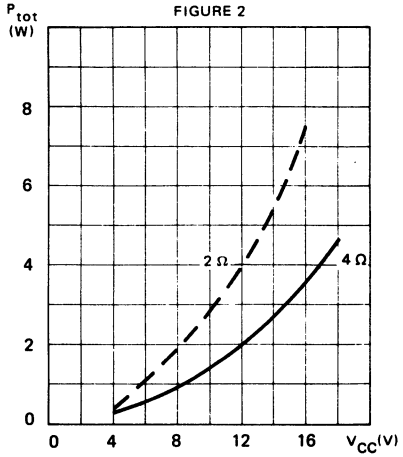
TYPICAL POWER OUTPUT VERSUS SUPPLY VOLTAGE
PUISSANCE DE SORTIE TYPIQUE EN FONCTION DE LA TENSION D'ALIMENTATION

FIGURE 1



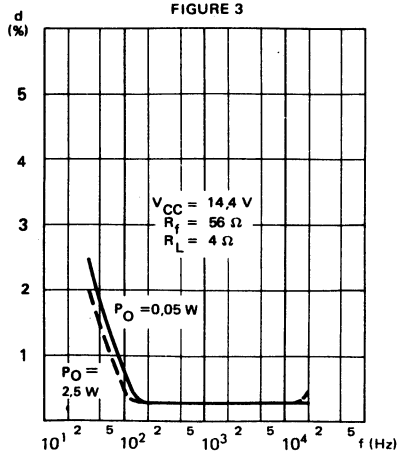
MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (sine wave operation)
PUISSANCE DISSIPEE MAXIMALE EN FONCTION DE LA TENSION D'ALIMENTATION (Onde sinusoïdale)

FIGURE 2



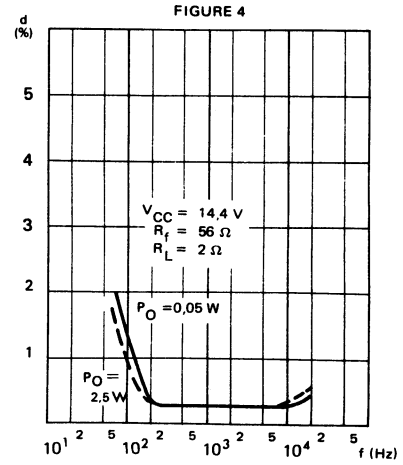
TYPICAL DISTORSION VERSUS FREQUENCY
DISTORSION TYPIQUE EN FONCTION DE LA FREQUENCE

FIGURE 3



TYPICAL DISTORSION VERSUS FREQUENCY
DISTORSION TYPIQUE EN FONCTION DE LA FREQUENCE

FIGURE 4



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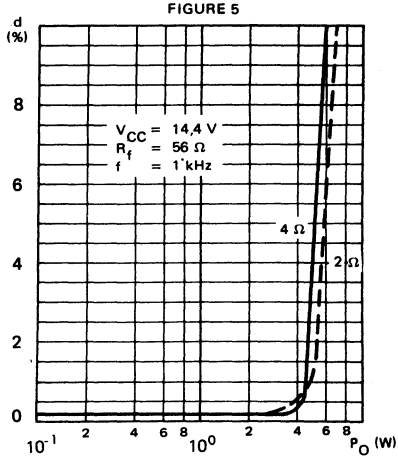
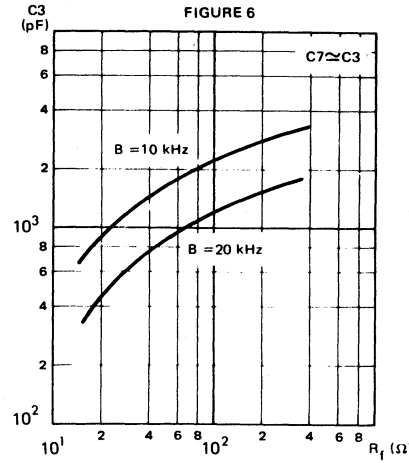
TYPICAL DISTORSION VERSUS OUTPUT POWER
DISTORSION TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE

FIGURE 5



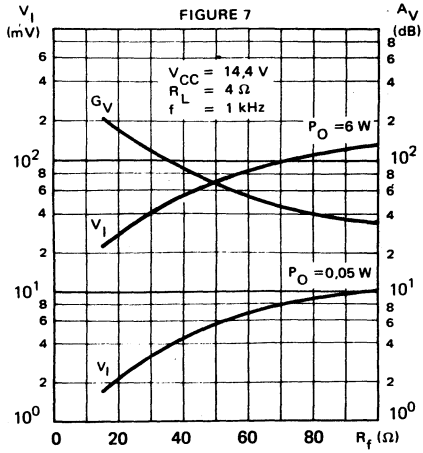
TYPICAL VALUE OF C3 VERSUS R_f FOR VARIOUS VALUES OF B
VALEUR TYPIQUE DE C3 EN FONCTION DE R_f POUR DIFFERENTES BANDES PASSANTES

FIGURE 6



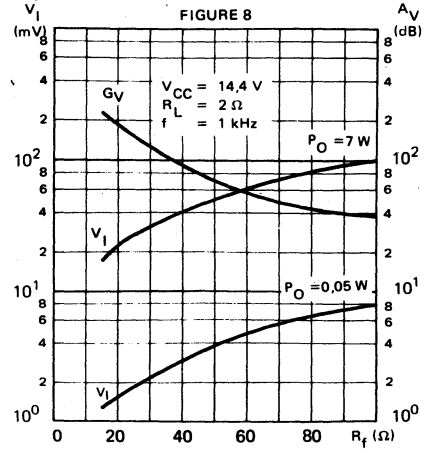
TYPICAL RELATIVE VOLTAGE GAIN (CLOSED LOOP) AND TYPICAL INPUT VOLTAGE VERSUS FEEDBACK RESISTANCE (R_f)
GAIN EN TENSION TYPIQUE (EN BOUCLE FERMEE) ET TENSION D'ENTREE TYPIQUE EN FONCTION DE LA RESISTANCE DE CONTRE REACTION (R_f)

FIGURE 7



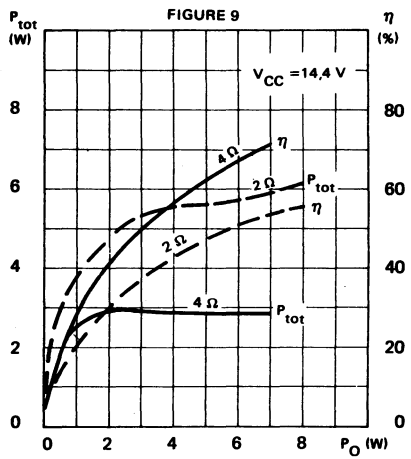
TYPICAL RELATIVE VOLTAGE GAIN (CLOSED LOOP) AND TYPICAL INPUT VOLTAGE VERSUS FEEDBACK RESISTANCE (R_f)
GAIN EN TENSION TYPIQUE (EN BOUCLE FERMEE) ET TENSION D'ENTREE TYPIQUE EN FONCTION DE LA RESISTANCE DE CONTRE REACTION (R_f)

FIGURE 8



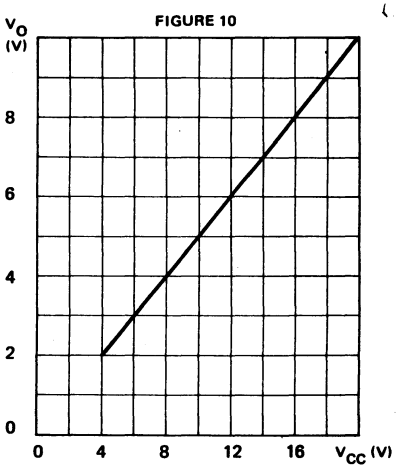
TYPICAL POWER DISSIPATION AND EFFICIENCY OUTPUT POWER
PUISSANCE DISSIPEE TYPIQUE ET EFFICACITE EN FONCTION DE LA PUISSANCE DE SORTIE

FIGURE 9



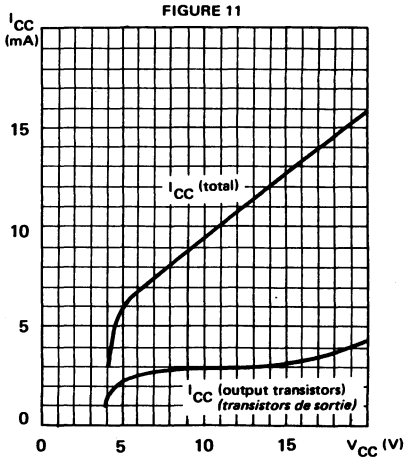
TYPICAL QUIESCENT OUTPUT VOLTAGE (Pin 12) VERSUS SUPPLY VOLTAGE
TENSION DE SORTIE TYPIQUE AU REPOS (Broche 12) EN FONCTION DE LA TENSION D'ALIMENTATION

FIGURE 10



TYPICAL QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE
COURANT DE REPOS TYPIQUE EN FONCTION DE LA TENSION D'ALIMENTATION

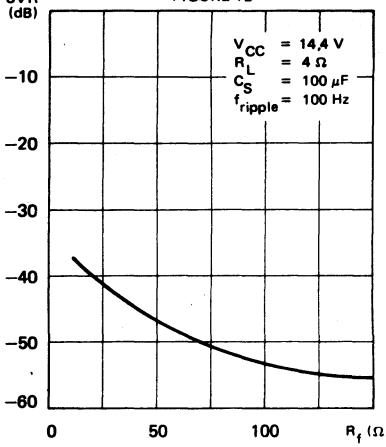
FIGURE 11



4

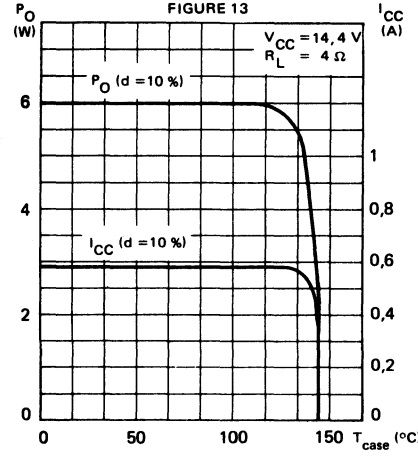
TYPICAL SUPPLY VOLTAGE REJECTION VERSUS FEEDBACK RESISTANCE
REJECTION DE L'ONDULATION D'ALIMENTATION EN FONCTION DE LA RESISTANCE DE CONTRE REACTION

FIGURE 12



OUTPUT POWER AND SUPPLY CURRENT VERSUS PACKAGE TEMPERATURE
PUISSANCE DE SORTIE ET COURANT D'ALIMENTATION EN FONCTION DE LA TEMPERATURE DE BOITIER

FIGURE 13



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages :

1 – An overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily supported.

2 – The heat-sink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of too high a junction temperature : all that happens is that P_O (and therefore P_{tot}) are reduced.

PROTECTION THERMIQUE

La présence d'un circuit de protection thermique présente les avantages suivants :

1 – Une surcharge des sorties (même permanente) ou une température ambiante dépassant les limites absolues est subie sans dommage.

2 – Le radiateur peut présenter un facteur de sécurité plus faible que pour un circuit conventionnel. Le circuit n'est pas endommagé si la température de jonction est trop élevée. Tout ce qui se produit est une diminution de P_O et par suite P_{tot}.

TEST AND APPLICATION CIRCUIT
CIRCUIT DE MESURE ET D'APPLICATION

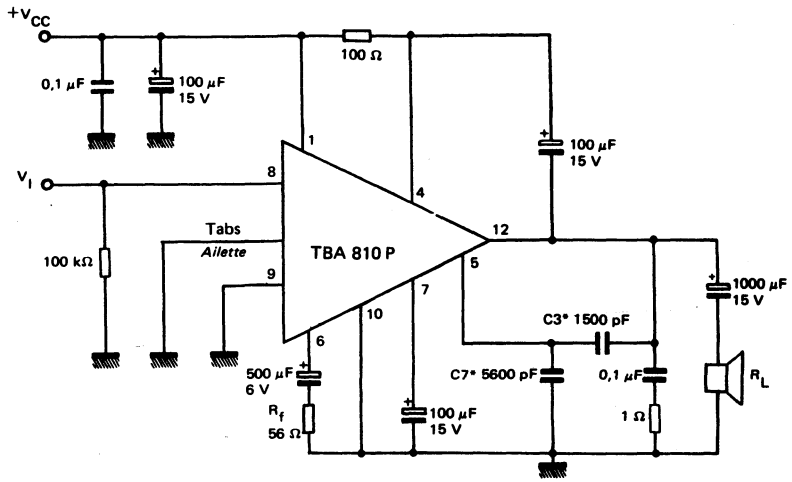
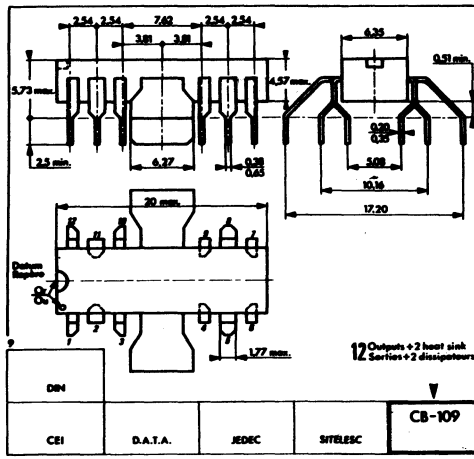
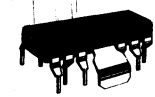


Figure 14
* C3, C7 see Fig. 6
voir Fig. 6

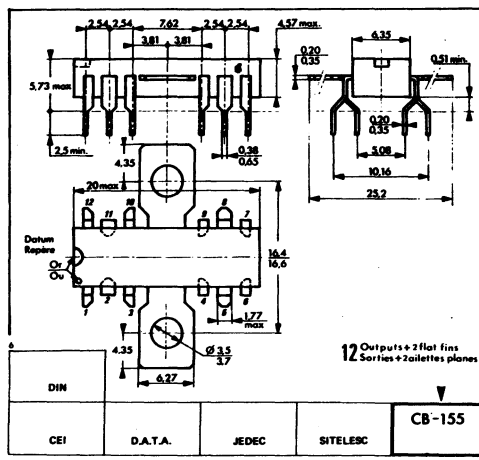
4



CASE / BOITIER
CB-109



PLASTIC PACKAGE
BOITIER PLASTIQUE



CASE / BOITIER
CB-155

PLASTIC PACKAGE
BOITIER PLASTIQUE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TBA810 S
TBA810 AS

AF AMPLIFIER
AMPLIFICATEUR BF

The TBA810 S is a monolithic integrated circuit designed for classe B audio amplification, with up to 7 W output power; It is internally protected against overheating.
It provides the advantages following:
- **The high idling current stability obtained from a built-in temperature and voltage-compensating network makes thermal runaway impossible.**
- **Open-loop gain is high enough to allow a great amount of feedback (low distortion) and keep a sufficient closed loop-gain (high sensitivity).**
- **The use of PNP transistors in the preamplifier allows D.C. input voltage to be zero.**
- **The exceptional D.C. output voltage stability and minimized potential loss, give to the output voltage high power capability.**
- **The special Split - DIP case makes it possible to use a part of the printed circuit board as a heat sink (TBA810 S).**
- **Other highlights include: few external components and not any adjustment.**

Le TBA810 S est un circuit intégré monolithique destiné à l'amplification BF classe B: sa puissance de sortie peut atteindre 7 W. Il est protégé intérieurement contre les températures excessives.
Il présente les avantages suivants:
- Régulation du courant de repos en fonction de la tension d'alimentation et de la température, donc suppression du risque d'emballement thermique.
- Gain de boucle ouverte élevé, donc possibilité d'appliquer un taux de contre-réaction important (distorsion réduite) tout en conservant une sensibilité correcte.
- Etage d'entrée à transistors PNP, ce qui permet d'appliquer le signal en un point dont le potentiel continu de référence est à la masse.
- Régulation de la tension continue de sortie, avec une faible dispersion, ce qui garantit le fonctionnement symétrique de l'étage de puissance.
- Possibilité d'utiliser une portion du circuit imprimé comme dissipateur de chaleur grâce à son boîtier Split - DIP à ailette (TBA810 S).
- Absence de réglage et nombre de composants extérieurs réduit.

AF AMPLIFIER
AMPLIFICATEUR BF

CASES / BOITIERS

CB-109

TBA 810 S

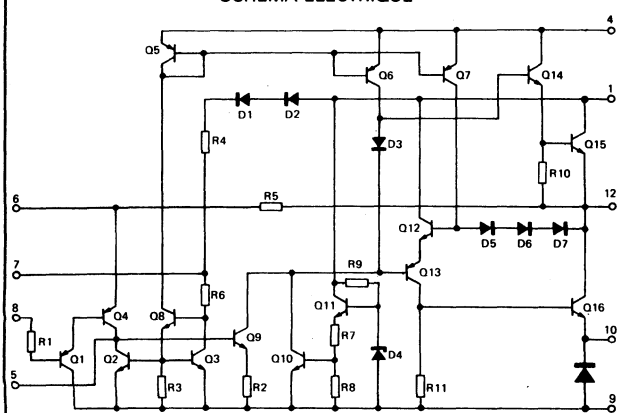
CB-155

TBA 810 AS

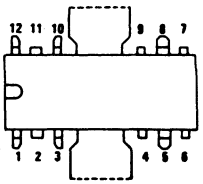
PLASTIC PACKAGES
BOITIERS PLASTIQUE

4

BLOCK DIAGRAM
SCHEMA ELECTRIQUE



PIN CONFIGURATION
BROCHAGE



Tab must be grounded
L'ailette doit être réunie à la masse

1 V_{CC}
2 **Not to use**
Ne pas utiliser
3 **Not to use**
Ne pas utiliser
4 **Bootstrap**
Bootstrap
5 **Compensation**
Compensation
6 **Feed-back network**
Réseau de contre-réaction
7 **Preamplifier decoupling**
Découplage du préamplificateur
8 **Input** / Entrée
9 **Substrate and preamplifier ground**
Substrat et masse du préamplificateur
10 **Output stage ground**
Masse de l'étage de sortie
11 **Not to use**
Ne pas utiliser
12 **Output** / Sortie

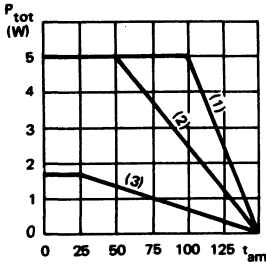
NT7510

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

Maximum power dissipation
Dissipation de puissance maximale

TBA 810 S

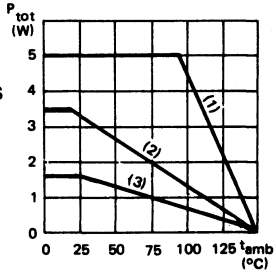


(1) With infinite heat sink
Avec radiateur infini

(2) With a 10°C/W heat sink - TBA 810 AS
With a 25°C/W heat sink - TBA 810 S
Avec radiateur de 10°C - TBA 810 AS
Avec radiateur de 25°C - TBA 810 S

(3) Without heat sink
Sans radiateur

TBA 810 AS



LIMITING VALUES
VALEURS LIMITES ABSOLUES

Supply voltage *Tension d'alimentation*	V_{CC}	20	V
Peak output current (non repetitive) *Courant crête en sortie non répétitif*	I_O	3,5	A
Peak output current (repetitive) *Courant crête en sortie répétitif*	I_O	2,5	A
Junction temperature *Température de jonction*	T_j	−40 +150	°C °C
Storage temperature *Température de stockage*	T_{stg}	−40 +150	°C °C

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C (Note 1)

(Unless otherwise stated)
(Sauf indications contraires)

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Supply voltage *Tension d'alimentation*		V_{CC}		4		20	V
Quiescent output voltage (pin 12) *Tension de repos (broche 12)*	V_{CC} = 14,4 V	V_O		6,4	7,2	8	V
Quiescent current *Courant de repos*	V_{CC} = 14,4 V	I_{CC}			12	20	mA
Bias current (pin 8) *Courant d'entrée (broche 8)*	V_{CC} = 14,4 V	I_B			0,4		µA
Output power *Puissance de sortie*	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 16 V	P_O			7		W
	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 14,4 V	P_O		5,5	6		W
	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 9 V	P_O			2,5		W
	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 6 V	P_O			1		W
Maximum input voltage peak *Tension d'entrée de crête maximale*		V_I			310		mV
Sensitivity *Sensibilité*	P_O = 6 W V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz R_f = 56 Ω	S			80		mV
	P_O = 6 W V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz R_f = 22 Ω	S			35		mV
Input resistance (pin 8) *Impédance d'entrée (broche 8)*		Z_I			5		MΩ

Note 1 : The characteristics above were obtained using the circuit shown in figure
Mesuré dans les conditions de la figure 1

4

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C

(Unless otherwise stated)
(Sauf indications contraires)

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Frequency response (−3 dB) *Bande passante (−3 dB)*	V_{CC} = 14,4 V R_f = 56 Ω C3 = 820 pF C3 = 1500 pF	B			40 - 20.000 40 - 10.000		Hz Hz
Distortion *Distorsion*	V_{CC} = 14,4 V P_O = 50 mW → 3 W R_L = 4 Ω R_f = 56 Ω f = 1 kHz	d			0,3		%
Voltage gain (open loop) *Gain de tension en boucle ouverte*	V_{CC} = 14,4 V R_L = 4 Ω f = 1 kHz	A_V			80		dB
Voltage gain (closed loop) *Gain de tension en boucle fermée*	V_{CC} = 14,4 V R_L = 4 Ω R_f = 56 Ω f = 1 kHz	A_V		34	37	40	dB
Input noise voltage *Tension de bruit à l'entrée*	V_{CC} = 14,4 V R_G = 0 B (−3 dB) = 20-20 000 Hz	V_n			2		μV
Input noise current *Courant de bruit à l'entrée*	V_{CC} = 14,4 V B (−3 dB) = 20 - 20 000 Hz	I_n			0,1		nA
Efficiency *Rendement*	V_{CC} = 14,4 V P_O = 5 W R_L = 4 Ω f = 1 kHz				70		%
Supply voltage rejection *Réjection de l'ondulation d'alimentation*	V_{CC} = 14,4 V R_L = 4 Ω f_{ripple} = 100 Hz	SVR			38		dB

THERMAL CHARACTERISTICS
CARACTERISTIQUES THERMIQUES

*With tabs soldered to printed circuit with minimized copper area
Dissipateur soudé à une surface réduite de circuit imprimé

Junction-case thermal resistance *Résistance thermique (jonction-boîtier)*		$R_{th(j-c)}$	max	12 (TBA 810 S) 10 (TBA 810 AS)	°C/W
Junction-ambient thermal resistance *Résistance thermique (jonction-ambiante)*		$R_{th(j-a)}$	max	70* (TBA 810 S) 80 (TBA 810 AS)	°C/W

MEASUREMENT DIAGRAM
SCHEMA DE MESURE

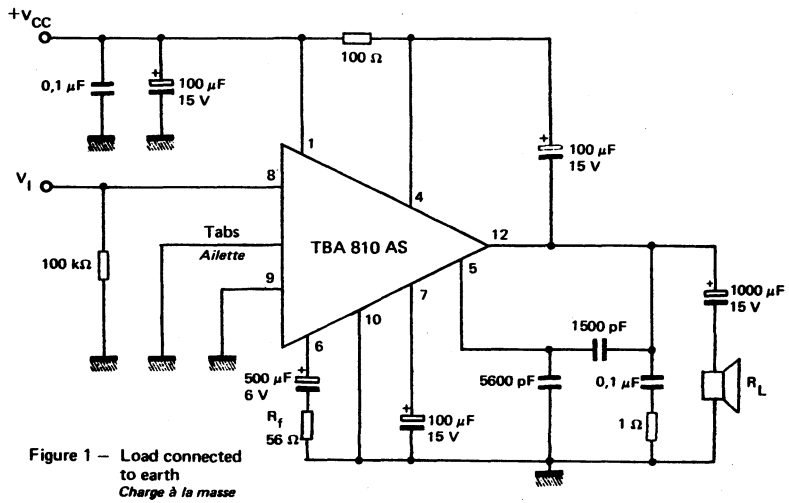
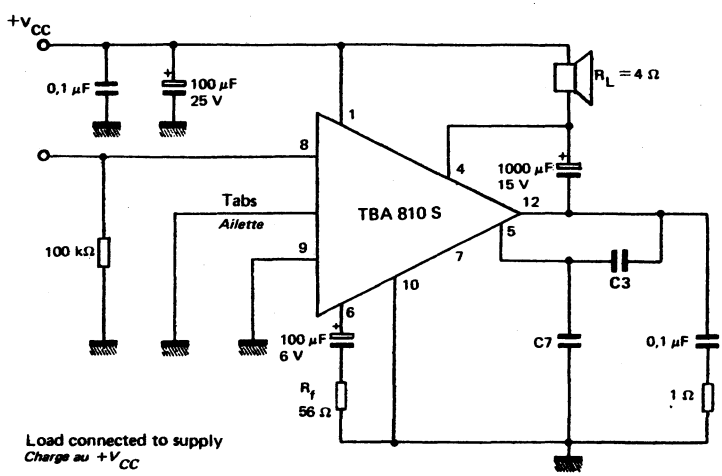


Figure 1 – Load connected to earth
Charge à la masse

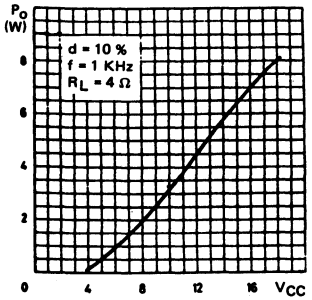
APPLICATION DIAGRAM WITH LOAD CONNECTED TO $+V_{CC}$
SCHEMA D'APPLICATION AVEC CHARGE AU $+V_{CC}$



Load connected to supply
Charge au $+V_{CC}$

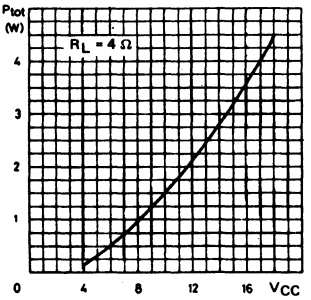
Power output versus supply voltage.

Puissance de sortie en fonction de la tension d'alimentation.



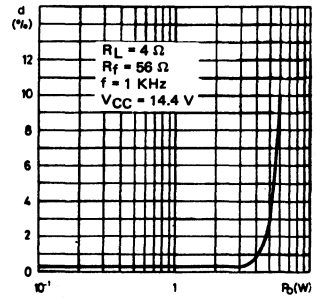
Maximum power dissipation, versus supply voltage (sine wave operation).

Puissance dissipée maximale en fonction de la tension d'alimentation.



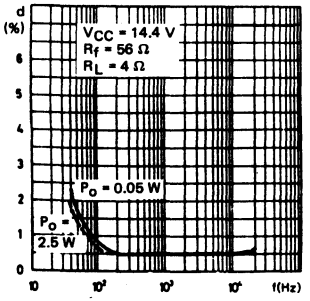
Distorsion versus output power.

Distorsion en fonction de la puissance de sortie.



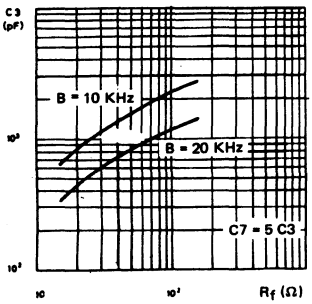
Distorsion versus frequency.

Distorsion en fonction de la fréquence.



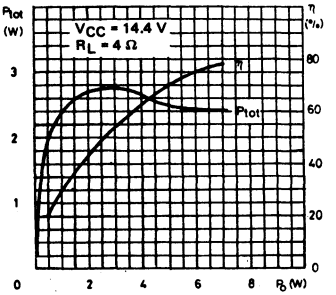
Value of C3 versus R_f for various values of B.

Valeur de C3 en fonction de R_f pour différentes bandes passantes.



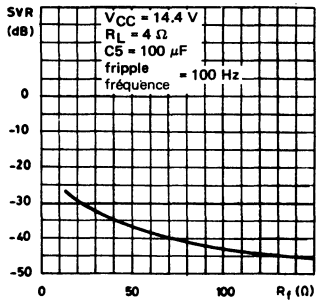
Power dissipation and efficiency versus output power.

Puissance dissipée et rendement en fonction de la puissance de sortie.



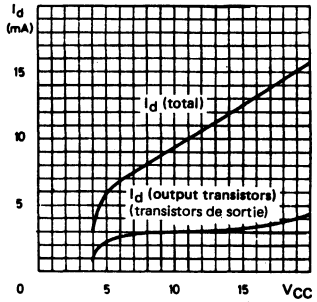
Supply voltage rejection.

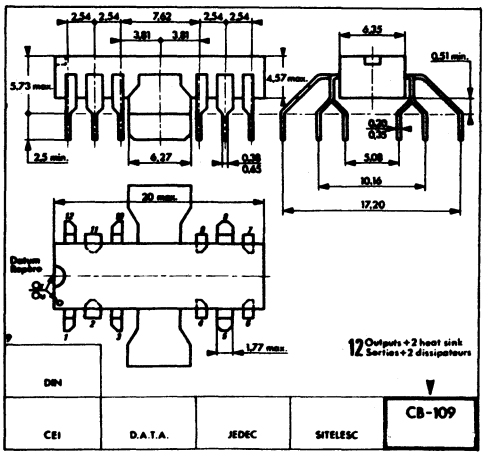
Réjection de l'ondulation d'alimentation.



Quiescent current versus supply voltage.

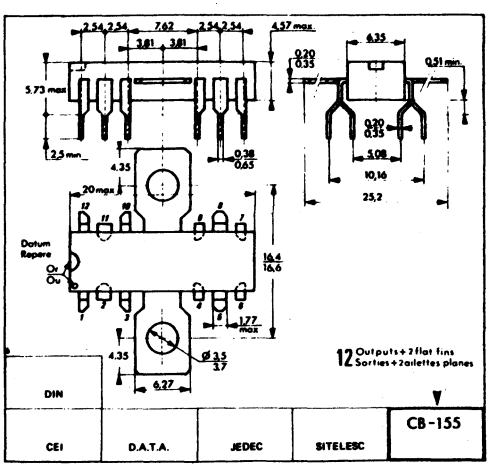
Courant de repos en fonction de la tension d'alimentation.





CASE / BOITIER
CB-109

PLASTIC PACKAGE
BOITIER PLASTIQUE



CASE / BOITIER
CB-155

PLASTIC PACKAGE
BOITIER PLASTIQUE

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Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TBA820

AF AMPLIFIER

The TBA820 is a monolithic integrated audio power amplifier.
Its main features:

- working with supply voltages from 3 to 16 volts,
- low idle current (4 mA typ.),
- high efficiency,

make it especially suitable for mobile, battery operated equipments.
Other features include:

- output power up to 2W without any external heat sink,
- high input impedance, low bias current,
- high ripple rejection,
- no thermal runaway,
- no cross-over distortion,
- few external components required.

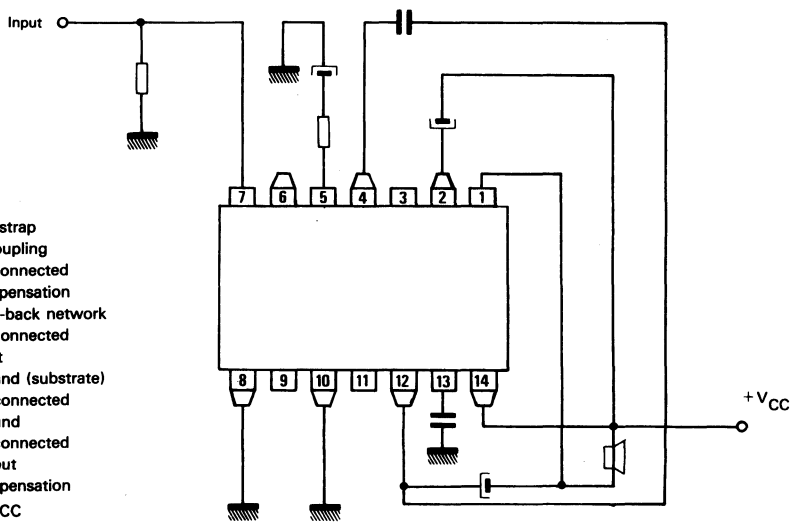
The TBA820 is supplied in a quad-in-line, 14 leads package.

AF AMPLIFIER

CASE CB-21

PLASTIC-PACKAGE

PIN CONFIGURATION



1 Bootstrap
2 Decoupling
3 No connected
4 Compensation
5 Feed-back network
6 No connected
7 Input
8 Ground (substrate)
9 No connected
10 Ground
11 No connected
12 Output
13 Compensation
14 ± V_{CC}

NT7905-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

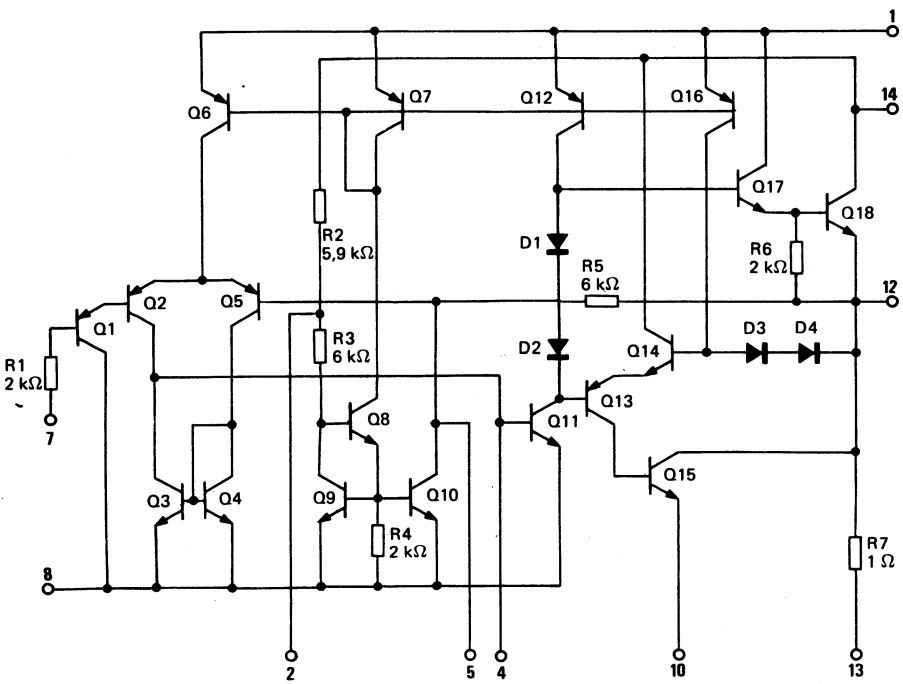
ABSOLUTE RATINGS (LIMITING VALUES)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	16	V
Output peak current	I_O	1.5	A
Storage temperature	T_{stg}	− 40, + 150	°C
Junction temperature	Tj	+ 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C (note 1) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3	–	16	V
Quiescent output voltage Pin 12 V_{CC} = 9 V	V_O	4	4.5	5	V
Quiescent drain current V_{CC} = 9 V	I_{CC}	–	4		mA
Bias current Pin 7 V_{CC} = 9 V	I	–	0.1	–	μA
Output power V_{CC} = 12 V ; R_L = 8 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz V_{CC} = 9 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz V_{CC} = 6 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz V_{CC} = 3.5 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz	P_O	– – – – –	2 1.6 1.2 0.75 0.22	– – – – –	W
Input sensitivity V_{CC} = 9 V ; P_O = 1.2 W ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz V_{CC} = 9 V ; P_O = 1.2 W ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz V_{CC} = 9 V ; P_O = 50 mW ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz V_{CC} = 9 V ; P_O = 50 mW ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz	S	– – – –	16 60 3.5 12	– – – –	mV
Input resistance	R_I	–	5	–	MΩ
Frequency response (– 3 dB) V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C_B = 680 pF V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C_B = 220 pF	B		25 to 7.000 25 to 20.000		Hz
Distortion V_{CC} = 9 V ; P_O = 500 mW ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz V_{CC} = 9 V ; P_O = 500 mW ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz	d	– –	0.8 0.4	– –	%
Voltage gain (open loop) V_{CC} = 9 V ; R_L = 8 Ω ; f = 1 kHz	A_V	–	75	–	dB
Voltage gain (closed loop) V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz	A_V	– –	45 34	– –	dB
Input noise voltage V_{CC} = 9 V ; B (– 3 dB) = 25 to 20.000 Hz	V_n	–	3	–	μV_{eff}
Input noise current V_{CC} = 9 V ; B (– 3 dB) = 25 to 20.000 Hz	I_n	–	0.4	–	
Signal to noise ratio V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; R1 = 100 kΩ P_O = 1.2 W ; B (– 3 dB) = 25 to 20.000 Hz		–	70	–	dB
Supply voltage rejection (see fig. 2) V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C6 = 50 μF f (ripple) = 100 Hz	SVR	–	42	–	dB

Note 1 : The characteristics above were obtained using the circuit shown in fig. 1.

TEST AND APPLICATION CIRCUITS

FIGURE 1 – LOAD CONNECTED TO THE SUPPLY VOLTAGE

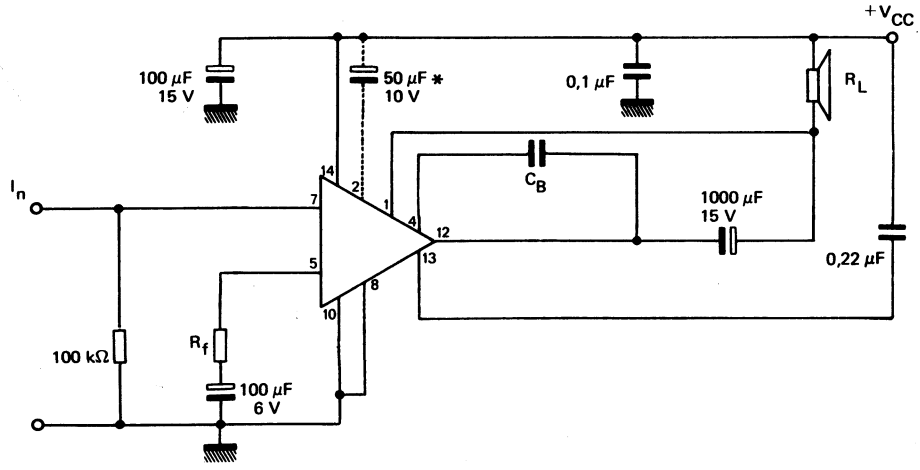
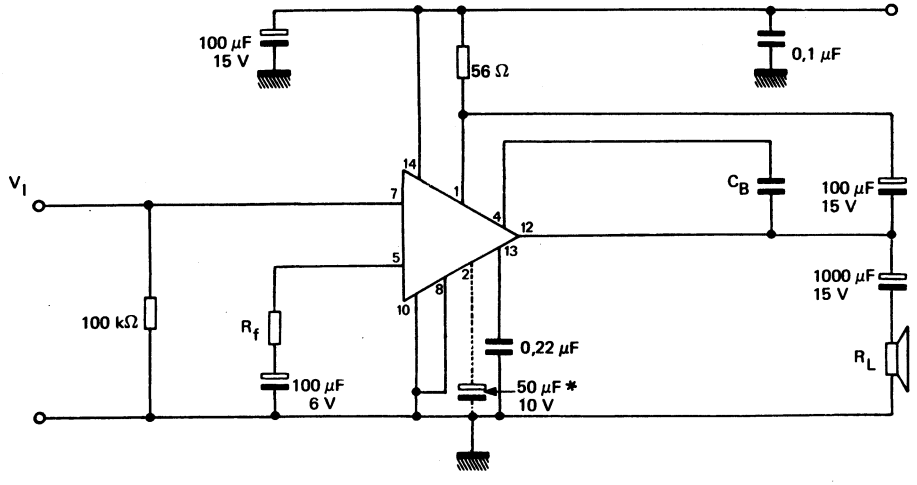


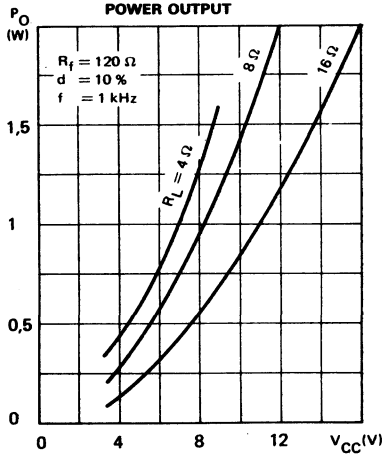
FIGURE 2 – LOAD CONNECTED TO GROUND



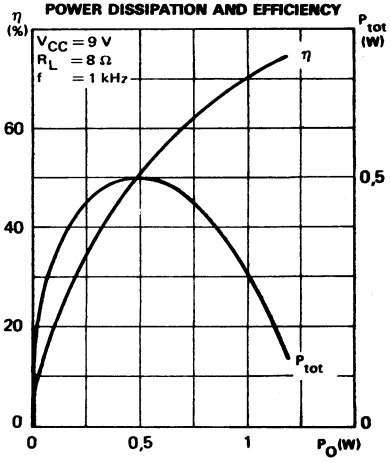
*Must be used when high ripple rejection is requested.

TYPICAL CHARACTERISTICS

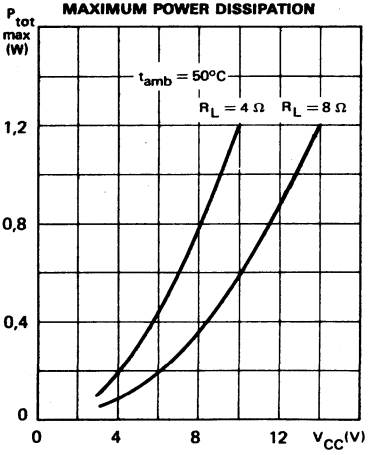
POWER OUTPUT



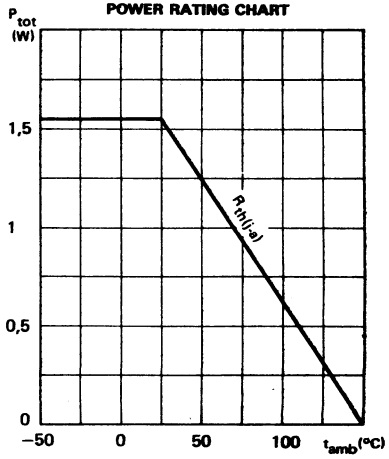
POWER DISSIPATION AND EFFICIENCY



MAXIMUM POWER DISSIPATION

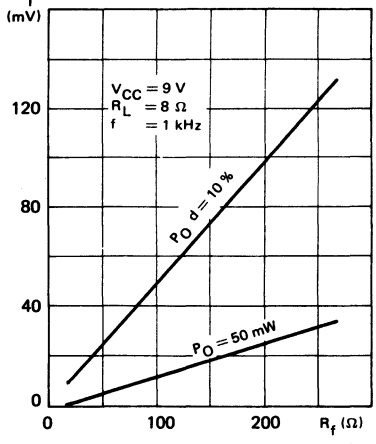


POWER RATING CHART

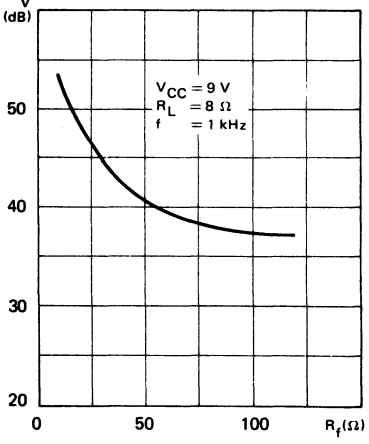


TYPICAL CHARACTERISTICS

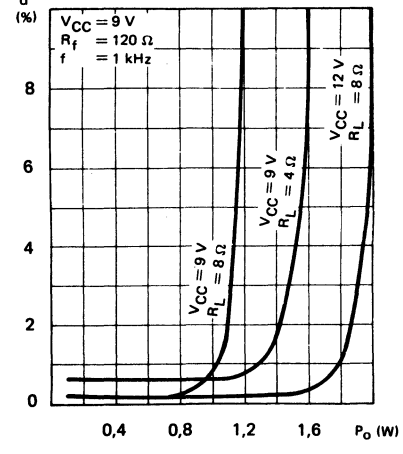
SENSITIVITY



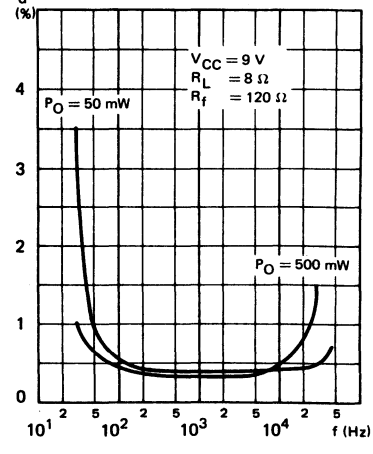
VOLTAGE GAIN (CLOSED LOOP)



DISTORTION

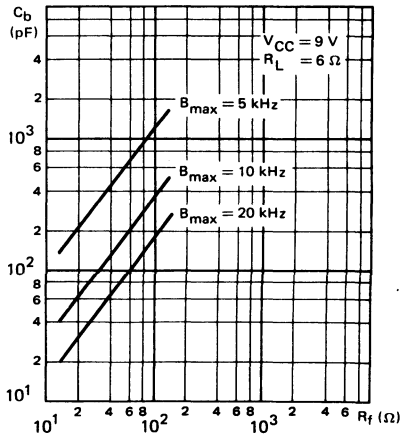


DISTORTION

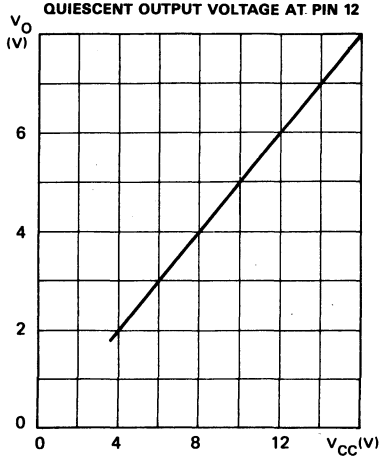


TYPICAL CHARACTERISTICS

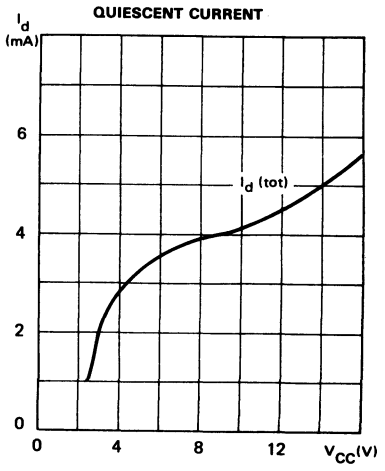
TYPICAL VALUE OF C_B VERSUS R_f AND B



QUIESCENT OUTPUT VOLTAGE AT PIN 12

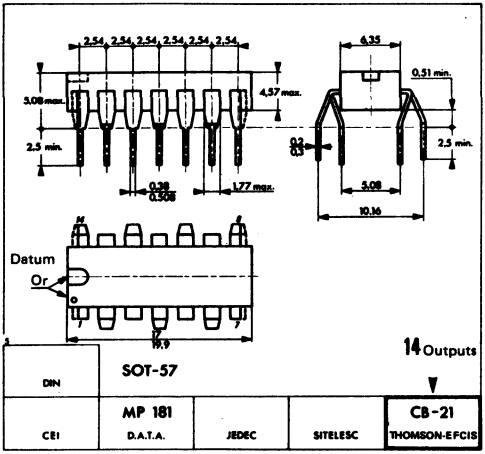


QUIESCENT CURRENT



CASE CB-21

PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TBA820 M

AF AMPLIFIER

The TBA 820 M is a monolithic integrated audio power amplifier.
Its main features:

- working with supply voltages from 3 to 16 volts,
- low idle current (4 mA typ.),
- high efficiency,

make it especially suitable for mobile, battery operated equipments.
Other features include:

- output power up to 2 W without any external heat sink,
- high input impedance, low bias current,
- high ripple rejection,
- no thermal runaway,
- no cross-over distortion,
- few external components required.

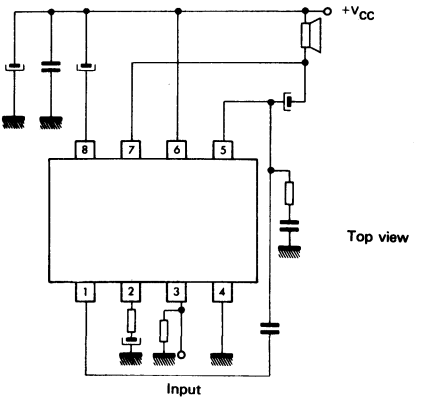
The TBA 820 M is supplied in a dual-in-line, 8 leads package.

AF AMPLIFIER

CASE CB-98

DP SUFFIX
PLASTIC PACKAGE

PIN CONFIGURATION



Top view

1 Compensation
2 Feedback
3 Input
4 Ground
5 Output
6 Supply
7 Bootstrap
8 Filtering

NT7913-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

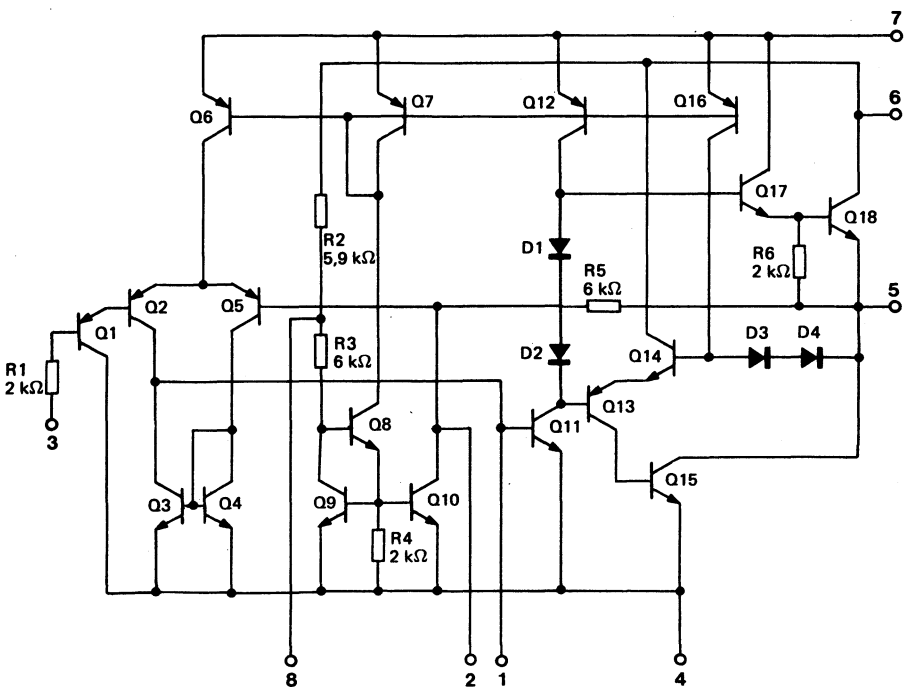
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	16	V
Output peak current	I_O	1.5	A
Storage temperature	T_{stg}	− 40 , + 150	°C
Junction temperature	Tj	+ 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C (note 1) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3	–	16	V
Quiescent output voltage Pin 5	V_O				V
V_{CC} = 9 V		4	4.5	5	
Quiescent drain current	I_{CC}				mA
V_{CC} = 9 V		–	4	12	
Bias current Pin 3	I				µA
V_{CC} = 9 V		–	0.1	–	
Output power measured at pin 5	P_O				W
V_{CC} = 12 V ; R_L = 8 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		–	2	–	
V_{CC} = 9 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		–	1.6	–	
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		0.9	1.2	–	
V_{CC} = 3.5 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		–	0.75	–	
V_{CC} = 3.5 V ; R_L = 4 Ω ; R_f = 120 Ω ; d = 10 % ; f = 1 kHz		–	0.25	–	
Input sensitivity	S				mV
V_{CC} = 9 V ; P_O = 1.2 W ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz		–	16	–	
V_{CC} = 9 V ; P_O = 1.2 W ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz		–	60	–	
V_{CC} = 9 V ; P_O = 50 mW ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz		–	3.5	–	
V_{CC} = 9 V ; P_O = 50 mW ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz		–	12	–	
Input resistance	R_I	–	5	–	MΩ
Frequency response (– 3 dB)	B				Hz
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C_B = 680 pF			25 to 7.000		
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C_B = 220 pF			25 to 20.000		
Distortion	d				%
V_{CC} = 9 V ; P_O = 500 mW ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz		–	0.8	–	
V_{CC} = 9 V ; P_O = 500 mW ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz		–	0.4	–	
Voltage gain (open loop)	A_V				dB
V_{CC} = 9 V ; R_L = 8 Ω ; f = 1 kHz		–	75	–	
Voltage gain (closed loop)	A_V				dB
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 33 Ω ; f = 1 kHz		–	45	–	
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; f = 1 kHz		–	34	–	
Input noise voltage	V_n				μV_{eff}
V_{CC} = 9 V ; B (– 3 dB) = 25 to 20.000 Hz		–	3	–	
Input noise current	I_n				nA
V_{CC} = 9 V ; B (– 3 dB) = 25 to 20.000 Hz		–	0.4	–	
Signal to noise ratio					dB
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; R1 = 100 kΩ P_O = 1.2 W ; B (– 3 dB) = 25 to 20.000 Hz		–	70	–	
Supply voltage rejection fig. 2	SVR				db
V_{CC} = 9 V ; R_L = 8 Ω ; R_f = 120 Ω ; C6 = 50 µF f (ripple) = 100 Hz		–	42	–	

Note 1 : The characteristics above were obtained using the circuit shown in fig. 1.

TEST AND APPLICATION CIRCUITS

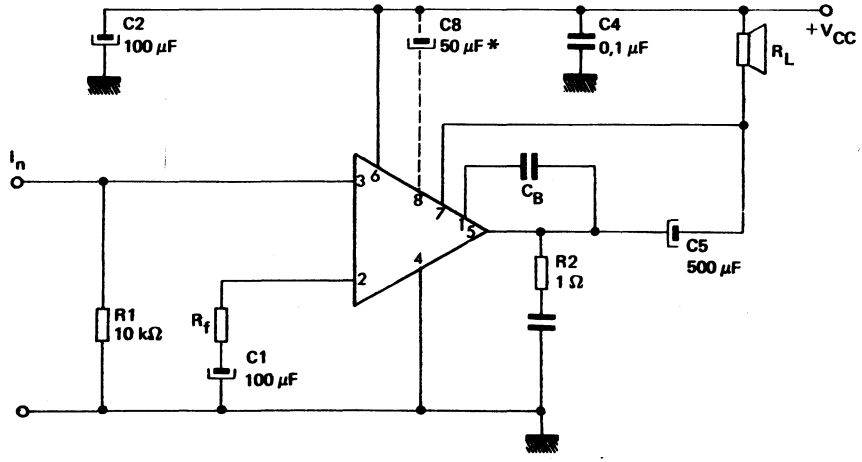


FIGURE 1 – LOAD CONNECTED TO THE SUPPLY VOLTAGE

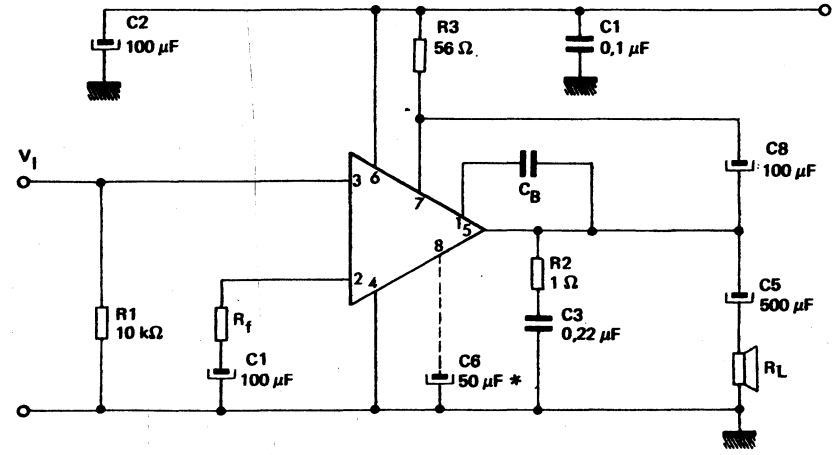


FIGURE 2 – LOAD CONNECTED TO GROUND

*Must be used when high ripple rejection is requested.

TYPICAL CHARACTERISTICS

FIGURE 3 – POWER OUTPUT

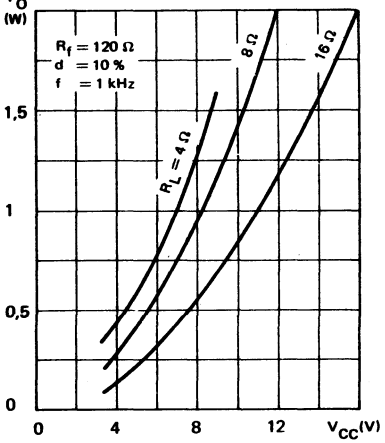


FIGURE 4 – DISTORTION

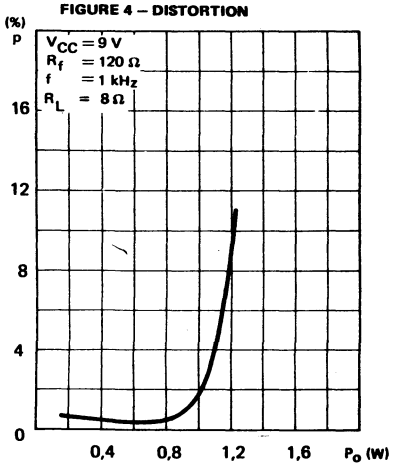


FIGURE 5 – POWER DISSIPATION AND EFFICIENCY

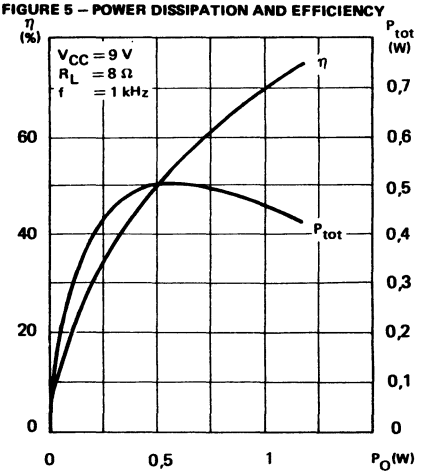
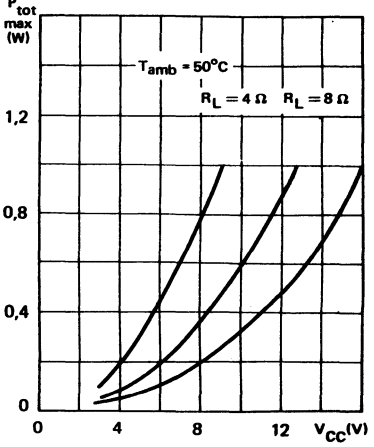


FIGURE 6 – MAXIMUM POWER DISSIPATION



TYPICAL CHARACTERISTICS

FIGURE 7 – TYPICAL VALUE OF C_B VERSUS R_f AND B

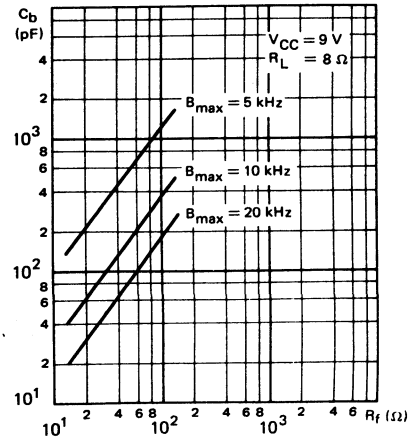


FIGURE 8 – RELATIVE FREQUENCY RESPONSE

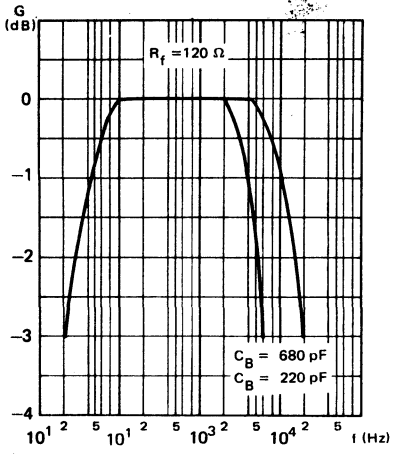


FIGURE 9 – SENSITIVITY

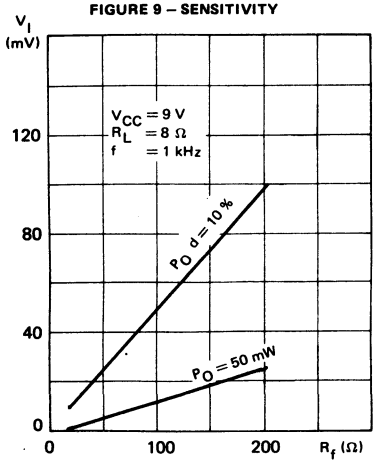
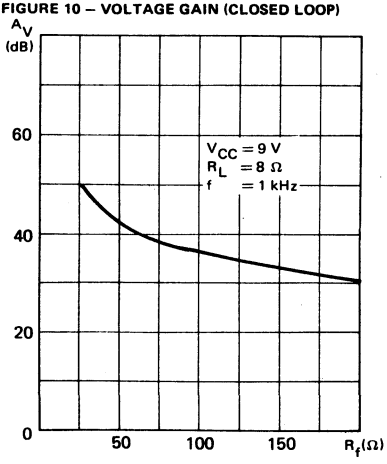


FIGURE 10 – VOLTAGE GAIN (CLOSED LOOP)



TYPICAL CHARACTERISTICS

FIGURE 11 – DISTORTION

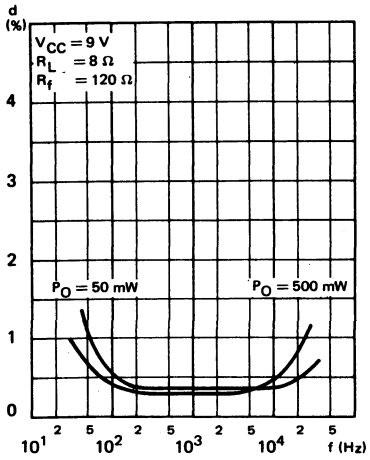


FIGURE 12 – SUPPLY VOLTAGE REJECTION

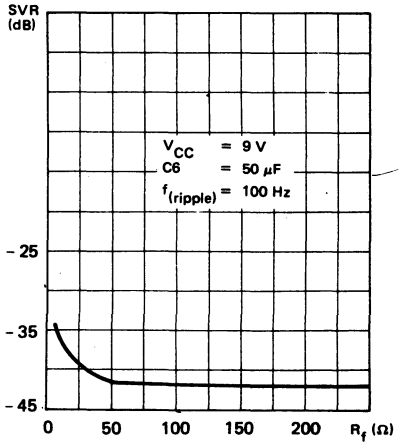
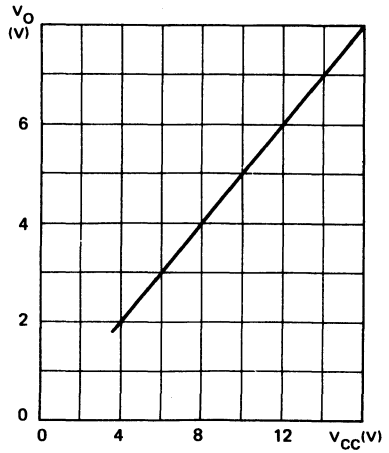


FIGURE 13 – QUIESCENT OUTPUT VOLTAGE AT PIN 5



TYPICAL CHARACTERISTICS

FIGURE 14 – QUIESCENT CURRENT

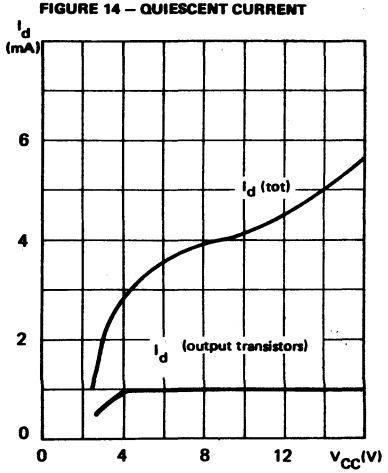


FIGURE 15 – POWER RATING CHART

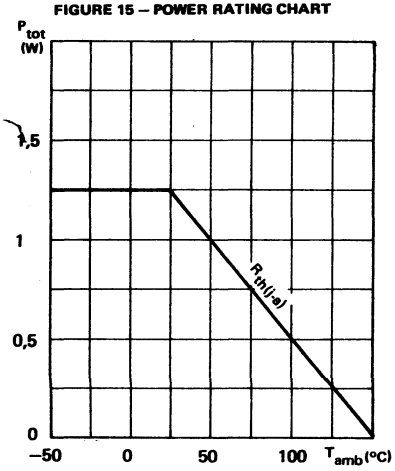
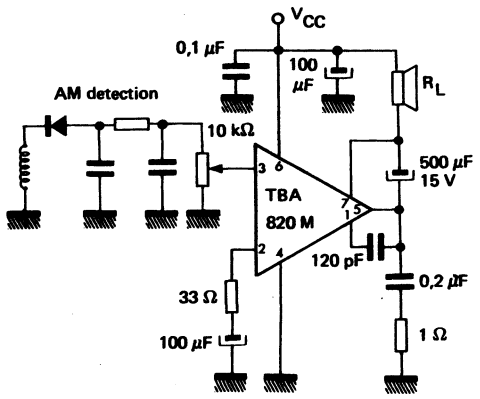
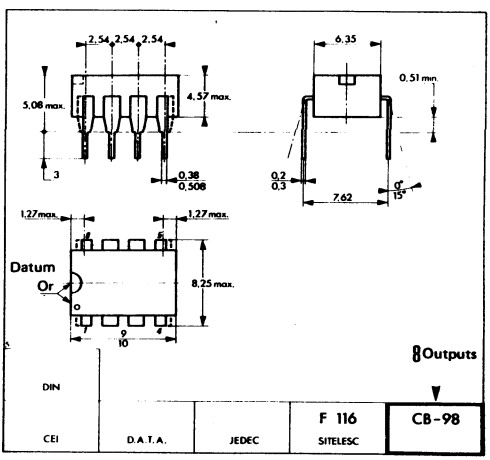


FIGURE 16 – LOW COST APPLICATION FOR



CASE CB-98

DP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TCA830 SM

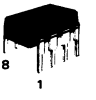
AF AMPLIFIER

The TCA 830SM is a monolithic integrated circuit designed for class B audio amplification, with up to 2.3 W output power ; it is internally protected against overheating.
It provides the advantages following :

- The high idling current stability obtained from a built-in temperature and voltage-compensating network makes thermal runaway impossible.
- Open-loop gain is high enough to allow a great amount of feedback (low distortion) and keep a sufficient closed loop-gain (high sensitivity).
- The use of PNP transistors in the preamplifier allows D.C. input voltage to be zero.
- The exceptional D.C. output voltage stability and minimized potential loss, give to the output voltage high power capability.
- The minidip package makes it easy to use where limited space is available.
- Others highlights include : few external components and not any adjustment.

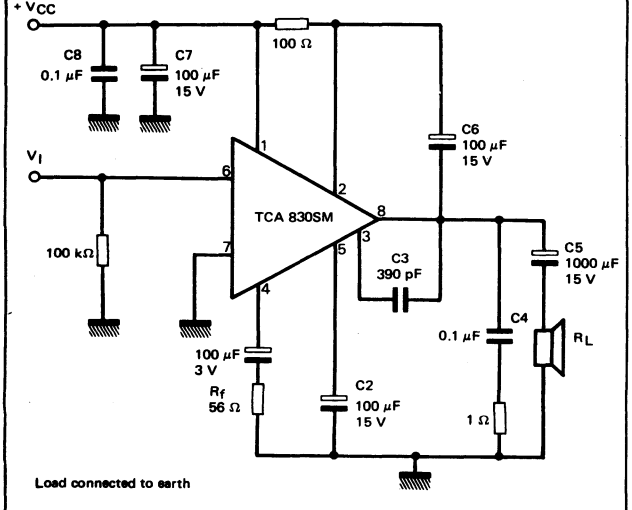
AF AMPLIFIER

CASE CB-98

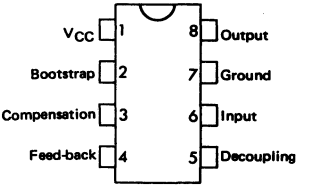


PLASTIC PACKAGE

TYPICAL APPLICATION



PIN ASSIGNMENT

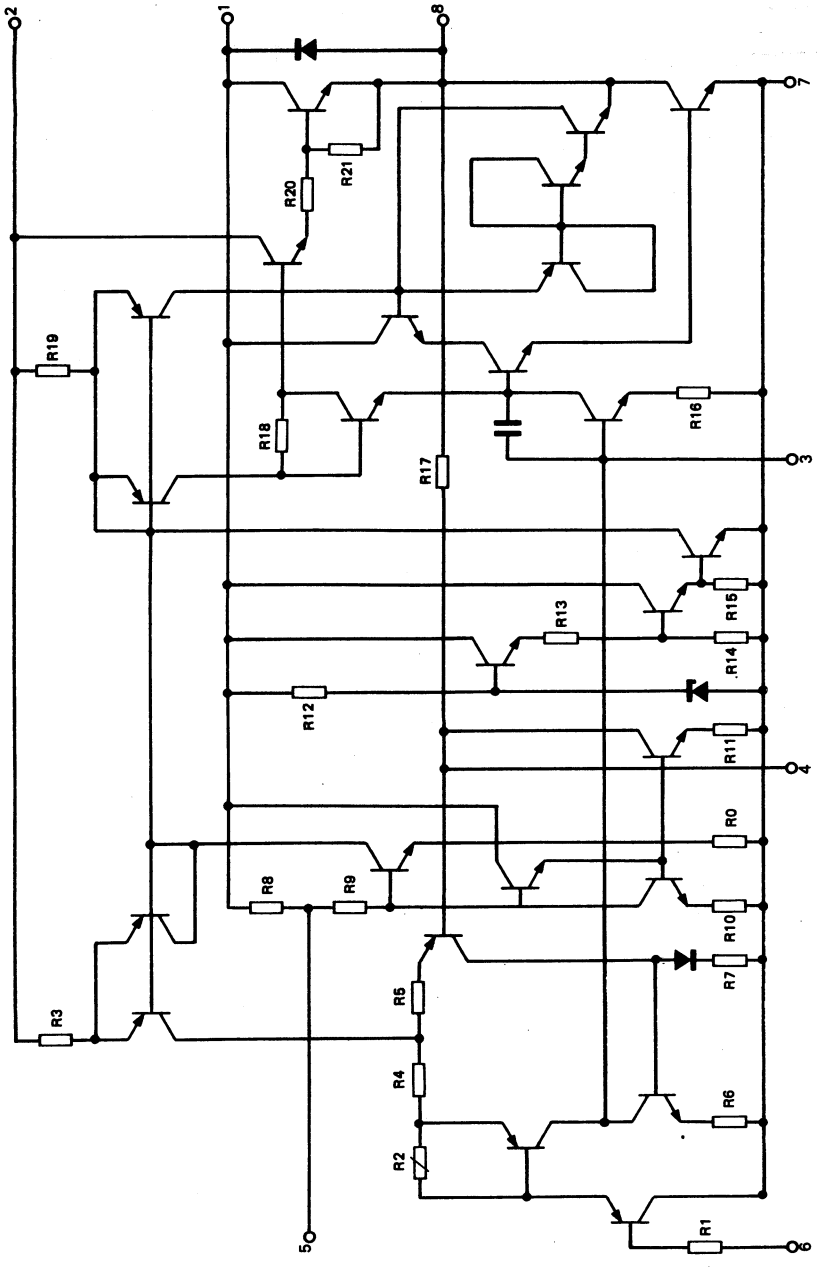


NT8235-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

SCHEMATIC DIAGRAM



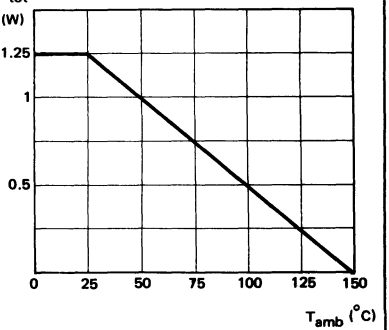
ABSOLUTE MAXIMUM RATING

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	20	V
Peak output current (no repetitive)	I_O	2.5	A
Peak output current (repetitive)	I_O	2	A
Junction temperature	T_j	+ 150	°C
Storage temperature	T_{stg}	- 40, + 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	85	°C/W

MAXIMUM POWER DISSIPATION



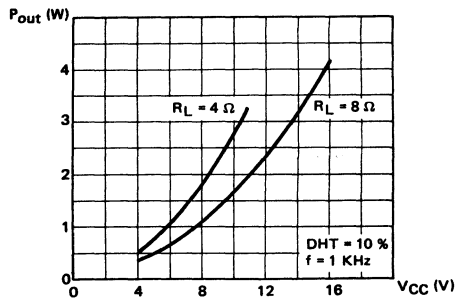
STATIC CHARACTERISTICS

T_{amb} = 25°C (Unless otherwise noted) (Note 1)

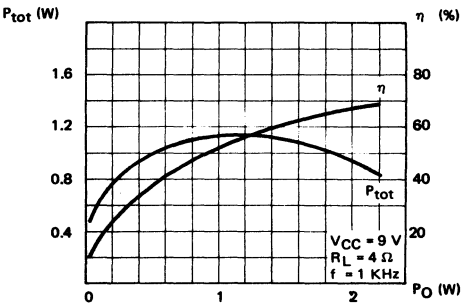
Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4	–	20	V
Quiescent output voltage (V_{CC} = 12 V)	Pin 8	V_O	5.3	6	6.7	V
Quiescent current (V_{CC} = 9 V)	Pin 1	I_{CC}	–	8.5	16	mA
Bias current (V_{CC} = 12 V)	Pin 6	I_B	–	0.2	–	µA
Output power (d = 10 % ; f = 1 KHz)		P_O				W
R_L = 4 Ω ; V_{CC} = 9 V			1.6	2	–	
R_L = 4 Ω ; V_{CC} = 6 V			0.75	1.0	–	
R_L = 8 Ω ; V_{CC} = 12 V			–	2.3	–	
Maximum input voltage peak		V_I	–	–	310	mV
Input resistance	Pin 6	Z_I	–	5	–	MΩ
Frequency response (- 3 dB)						
V_{CC} = 9 V ; R_f = 56 Ω ; C3 = 390 pF ; R_L = 4 Ω				40 - 10.000		Hz
Distortion						
V_{CC} = 9 V ; P_O = 50 mW to 1 W ; R_L = 4 Ω ; R_f = 56 Ω ; f = 1 KHz		d	–	0.3	1	%
Voltage gain (V_{CC} = 9 V ; R_L = 4 Ω ; f = 1 KHz)		A_V				dB
Open loop			60	75	–	
Closed loop (R_f = 56 Ω)			34	37	40	
Input noise voltage (V_{CC} = 9 V ; R_G = 0 ; B (- 3dB) = 40-10.000 Hz)		V_n	–	2	–	µV
Input noise current (V_{CC} = 9 V ; B (- 3 dB)= 40 - 10.000 Hz)		I_n	–	0.1	–	nA
Efficiency (V_{CC} = 9 V ; P_O= 1.6 W ; R_L = 4 Ω ; f = 1 KHz)		η	–	62	–	%
Supply voltage rejection		SVR				dB
(V_{CC} = 9 V ; R_L = 4 Ω ; f_{ripple} = 100 Hz ; R_f = 56 Ω)						
C2 = 100 µF			40	45	–	
C2 = 25 µF			–	38	–	

Note 1 : The above characteristics were obtained using the circuit shown in figure 1. (See page 6/7).

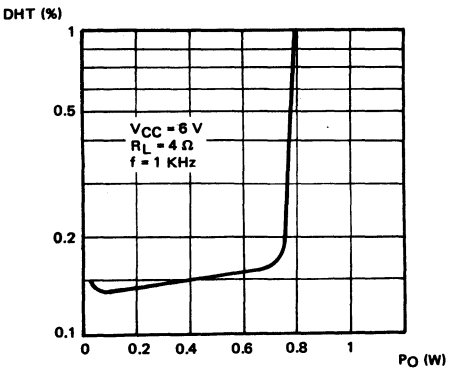
OUTPUT POWER VS SUPPLY VOLTAGE



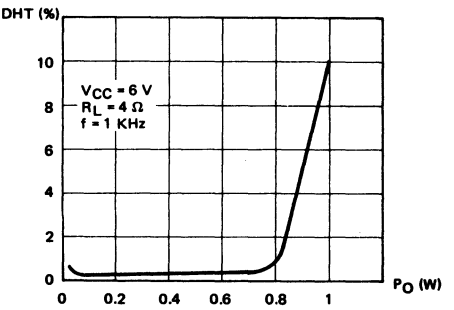
TOTAL DISSIPATED POWER VS OUTPUT POWER



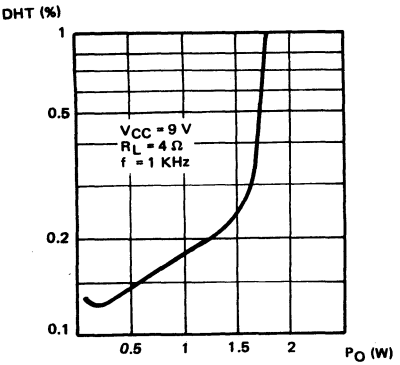
DISTORTION VS OUTPUT POWER



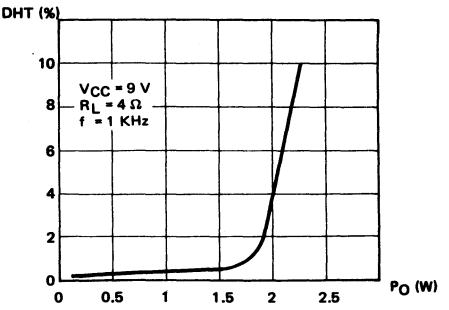
DISTORTION VS OUTPUT POWER



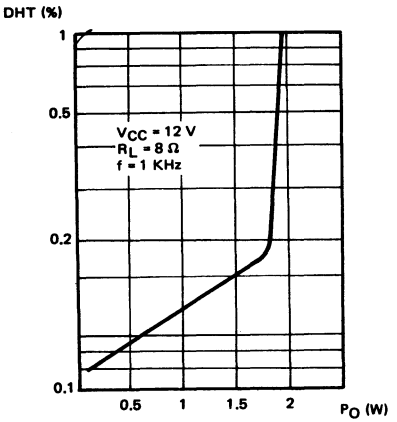
DISTORTION VS OUTPUT POWER



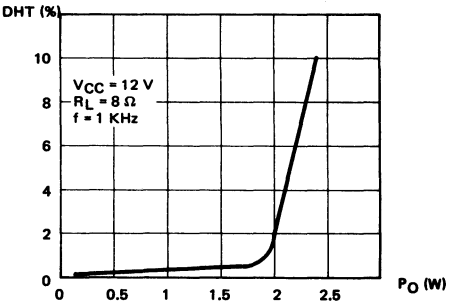
DISTORTION VS OUTPUT POWER



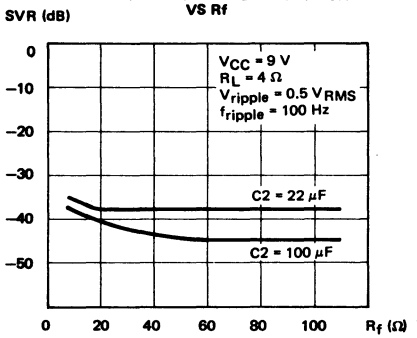
DISTORTION VS OUTPUT POWER



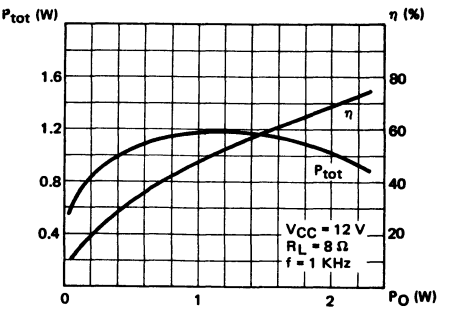
DISTORTION VS OUTPUT POWER



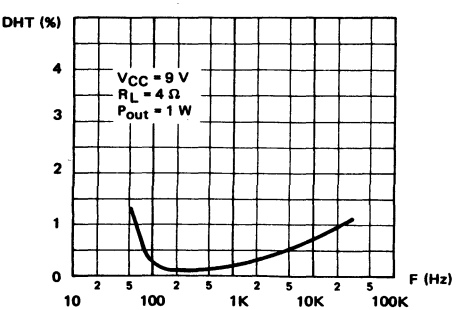
SUPPLY VOLTAGE RIPPLE REJECTION VS Rf



TOTAL DISSIPATED POWER VS OUTPUT POWER



DISTORTION VS FREQUENCY



DISTORTION VS FREQUENCY

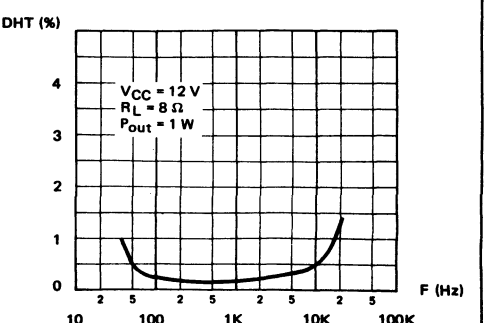


FIGURE 1 – MEASUREMENT DIAGRAM

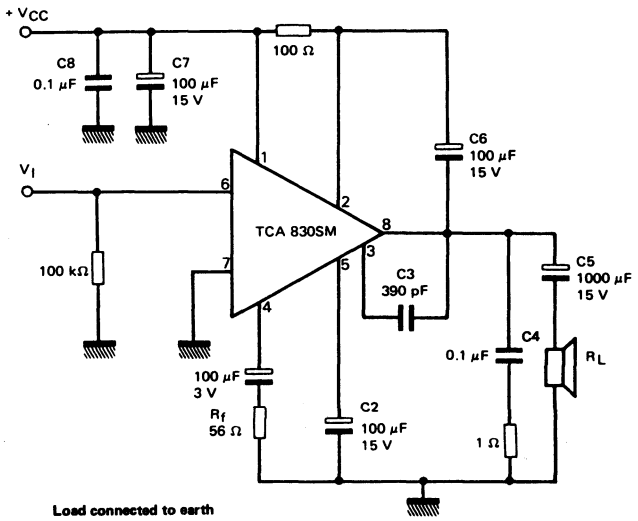
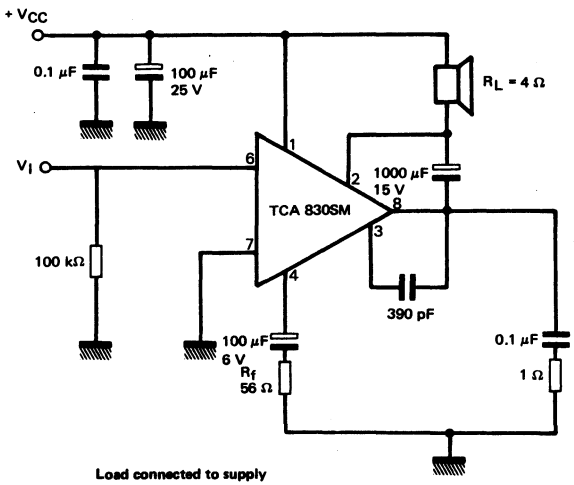
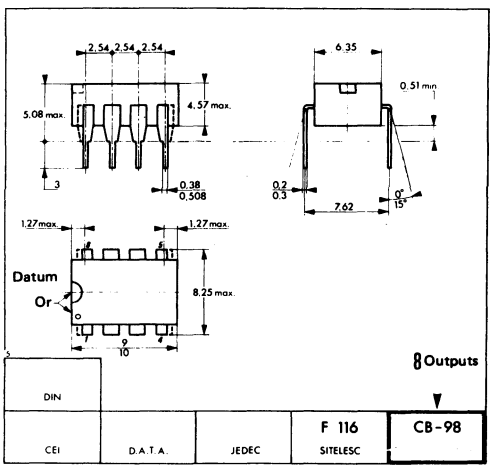


FIGURE 2 – APPLICATION DIAGRAM WITH LOAD CONNECTED TO + VCC



CASE CB-98

PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TCA830 SR

AF AMPLIFIER
AMPLIFICATEUR BF

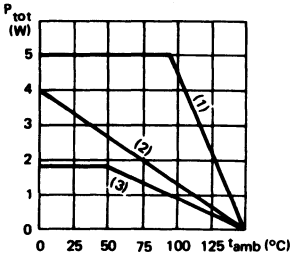
The TCA 830 SR is a monolithic integrated circuit designed for class B audio amplification, with up to 4.2 W output power; It is internally protected against overheating.
It provides the advantages following:

- **The high idling current stability obtained from a built-in temperature and voltage-compensating network makes thermal runaway impossible.**
- **Open-loop gain is high enough to allow a great amount of feedback (low distortion) and keep a sufficient closed loop-gain (high sensitivity).**
- **The use of PNP transistors in the preamplifier allows D.C. input voltage to be zero.**
- **The exceptionnal D.C. output voltage stability and minimized potential loss, give to the output voltage high power capability.**
- **The special Split - DIP case makes it possible to use a part of the printed circuit board as a heat sink.**
- **Others highlights include: few external components and not any adjustment.**

Le TCA 830 SR est un circuit intégré monolithique destiné à l'amplification BF classe B : sa puissance de sortie peut atteindre 4,2 W. Il est protégé intérieurement contre les températures excessives.
Il présente les avantages suivants :

- Régulation du courant de repos en fonction de la tension d'alimentation et de la température, donc suppression du risque d'emballement thermique.
- Gain de boucle ouverte élevé, donc possibilité d'appliquer un taux de contre-réaction important (distorsion réduite) tout en conservant une sensibilité correcte.
- Etage d'entrée à transistors PNP, ce qui permet d'appliquer le signal en un point dont le potentiel continu de référence est à la masse.
- Régulation de la tension continue de sortie, avec une faible dispersion, ce qui garantit le fonctionnement symétrique de l'étage de puissance.
- Possibilité d'utiliser une portion de circuit imprimé comme dissipateur de chaleur grâce à son boîtier Split - DIP à ailette.
- Absence de réglage et nombre de composants extérieurs réduit.

Maximum power dissipation
Dissipation de puissance maximale



(1) With infinite heat sink
Avec radiateur infini

(2) With a 25°C/W heat sink
Avec radiateur de 25°C

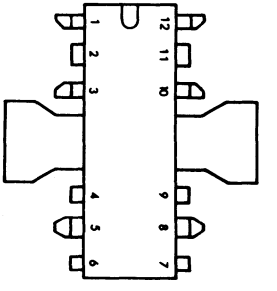
(3) Without heat sink
Sans radiateur

AF AMPLIFIER
AMPLIFICATEUR BF

CASE / BOITIER **CB-109**

PLASTIC PACKAGE
BOITIER PLASTIQUE

PIN CONFIGURATION
BROCHAGE



1 **V_{CC}**
2 **Not to use**
Ne pas utiliser
3 **Not to use**
Ne pas utiliser
4 **Bootstrap**
Bootstrap
5 **Compensation**
Compensation
6 **Feed-back network**
Réseau de contre-réaction
7 **Preamplifier decoupling**
Découplage du préamplificateur
8 **Input**
Entrée
9 **Substrate and preamplifier ground**
Substrat et masse du préamplificateur
10 **Output stage ground**
Masse de l'étage de sortie
11 **Not to use**
Ne pas utiliser
12 **Output**
Sortie

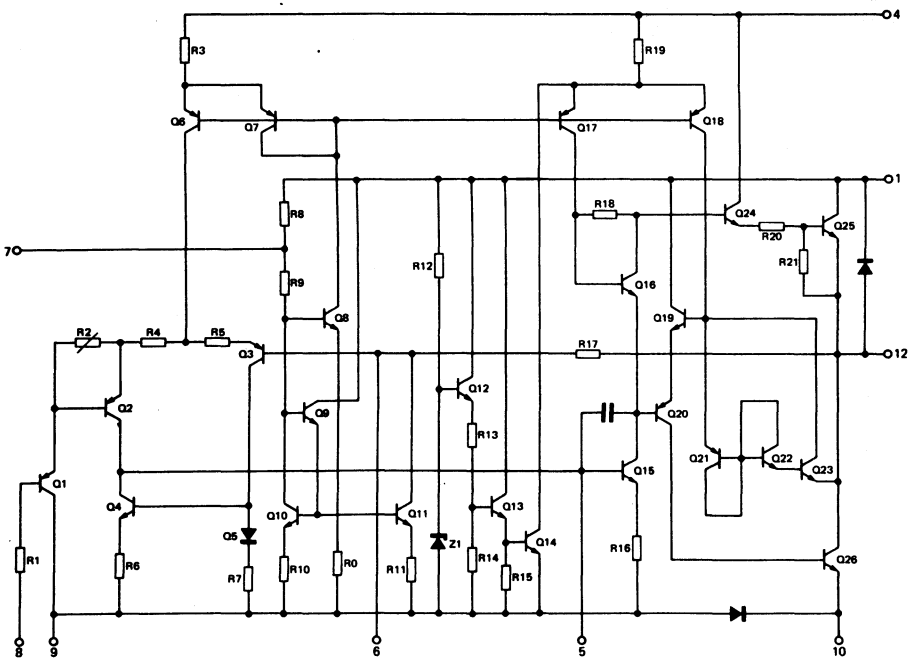
Tab must be grounded
L'ailette doit être réunie à la masse

NT7643

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

BLOCK DIAGRAM
SCHEMA ELECTRIQUE



LIMITING VALUES
VALEURS LIMITES ABSOLUES

Supply voltage *Tension d'alimentation*	V_{CC}	20	V
Peak output current (non repetitive) *Courant crête en sortie non répétitif*	I_O	2,5	A
Peak output current (repetitive) *Courant crête en sortie répétitif*	I_O	2	A
Junction temperature *Température de jonction*	T_j	−40 + 150	°C °C
Storage temperature *Température de stockage*	T_{stg}	−40 + 150	°C °C

STATIC CHARACTERISTICS
CARACTERISTIQUES STATIQUES

T_{amb} = 25 °C (Note 1) (Unless otherwise stated) *(Seuf indications contraires)*

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Supply voltage *Tension d'alimentation*		V_{CC}		4		20	V
Quiescent output voltage (pin 12) *Tension de repos (broche 12)*	V_{CC} = 12 V	V_O		5,3	6	6,7	V
Quiescent current *Courant de repos*	V_{CC} = 9 V	I_{CC}			8,5	16	mA
Bias current (pin 8) *Courant d'entrée (broche 8)*	V_{CC} = 12 V	I_B			0,2		µA
Output power *Puissance de sortie*	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 14 V	P_O			4,2		W
	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 12 V	P_O		2,5	3,4		W
	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 9 V	P_O			2		W
	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 6 V	P_O			0,8		W
	d = 10 % R_L = 8 Ω f = 1 kHz V_{CC} = 16 V	P_O			3,7		W
	d = 10 % R_L = 8 Ω f = 1 kHz V_{CC} = 12 V	P_O			2,3		W
Maximum input voltage RMS *Tension d'entrée de RMS maximale*		V_I				310	mV
Sensitivity *Sensibilité*	P_O = 3,4 W V_{CC} = 12 V R_L = 4 Ω f = 1 kHz R_f = 56 Ω	S			50		mV

Note 1 : The characteristics above were obtained using the circuit shown in figure 1
Mesuré dans les conditions de la figure 1

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C

(Unless otherwise stated)
(Sauf indications contraires)

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Input resistance (pin 8) *Impédance d'entrée (broche 8)*		Z_I			5		MΩ
Frequency response (−3 dB) *Bande passante (−3 dB)*	V_{CC} = 12 V R_f = 56 Ω C3 = 390 pF R_L = 4 Ω				40 - 10.000		Hz
Distortion *Distorsion*	V_{CC} = 12 V P_O = 50 mW ÷ 2 W R_L = 4 Ω R_f = 56 Ω f = 1 kHz	d			0,3		%
Voltage gain (open loop) *Gain de tension en boucle ouverte*	V_{CC} = 12 V R_L = 4 Ω f = 1 kHz	A_V			75		dB
Voltage gain (closed loop) *Gain de tension en boucle fermée*	V_{CC} = 12 V R_L = 4 Ω R_f = 56 Ω f = 1 kHz	A_V		34	37	40	dB
Input noise voltage *Tension de bruit à l'entrée*	V_{CC} = 12 V R_G = 0 B (−3 dB) = 40-10.000 Hz	V_n			2		μV
Input noise current *Courant de bruit à l'entrée*	V_{CC} = 12 V B (−3 dB) = 40 - 10 000 Hz	I_n			0,1		nA
Efficiency *Rendement*	V_{CC} = 12 V P_O = 3,4 W R_L = 4 Ω f = 1 kHz	η			62		%
Supply voltage rejection *Réjection de l'ondulation d'alimentation*	V_{CC} = 12 V R_L = 4 Ω f_{ripple} = 100 Hz R_f = 56 Ω	SVR	C2=100μF C2= 25μF		45 38		dB dB

THERMAL CHARACTERISTICS
CARACTERISTIQUES THERMIQUES

*With tabs soldered to printed circuit with minimized copper area
Dissipateur soudé à une surface réduite de circuit imprimé

Junction-case thermal resistance *Résistance thermique (jonction-boîtier)*		$R_{th(j-c)}$		12	°C/W
Junction-ambient thermal resistance *Résistance thermique (jonction-ambiante)*		$R_{th(j-a)}$		70*	°C/W

MEASUREMENT DIAGRAM
SCHEMA DE MESURE

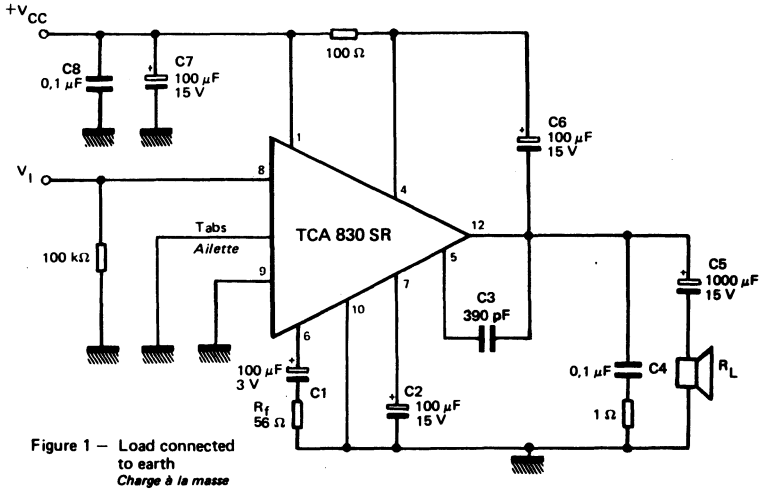
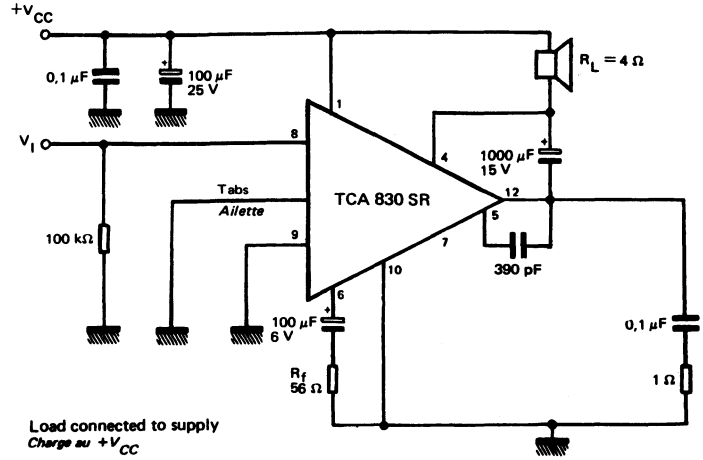


Figure 1 – Load connected to earth
Charge à la masse

APPLICATION DIAGRAM WITH LOAD CONNECTED TO $+V_{CC}$
SCHEMA D'APPLICATION AVEC CHARGE AU $+V_{CC}$

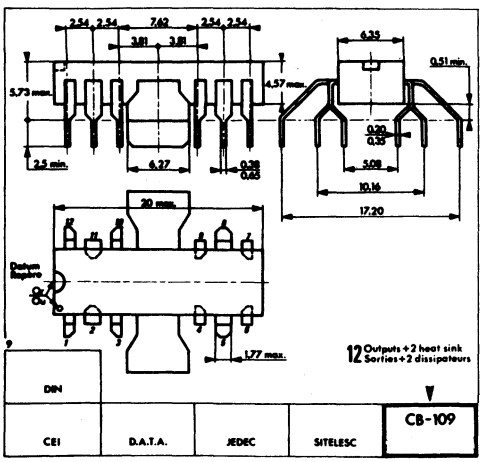


Load connected to supply
Charge au $+V_{CC}$

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

CASE / BOITIER CB-109

PLASTIC PACKAGE
BOITIER PLASTIQUE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TCA940
TCA940 E

AF AMPLIFIER
AMPLIFICATEUR BF

The TCA 940,E is a monolithic integrated circuit designed for class B audio amplification, with up to 10 W output power.
It provides all the advantages of integrated AF amplifiers: constant idling current and voltage, high efficiency, low distortion; furthermore, an internal circuit protects it against overheating, supply overvoltage and load short-circuit.
The TCA 940, E is pin-to-pin compatible with TBA 810 AS.

Le TCA 940, E est un circuit monolithique destiné à l'amplification BF classe B; sa puissance de sortie peut atteindre 10 W.
Il présente tous les avantages des amplificateurs BF intégrés: stabilité du courant et de la tension de repos, rendement élevé, faible distorsion; en outre, un dispositif intérieur le protège contre l'échauffement excessif, les surtensions d'alimentation et le court-circuit de la charge.
Le TCA 940, E est interchangeable broche à broche avec le TBA 810 AS.

AF AMPLIFIER
AMPLIFICATEUR BF

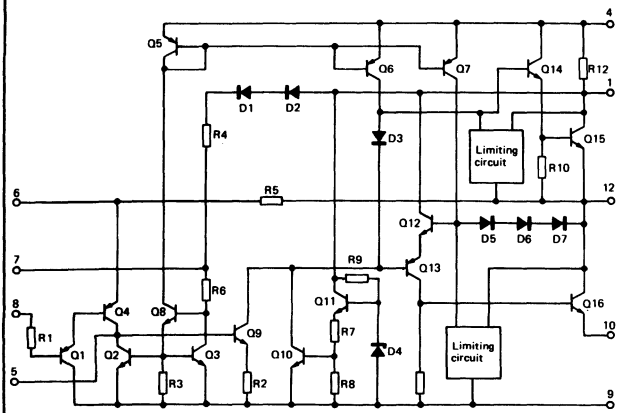
CASES / BOITIERS

CB-155
TCA 940

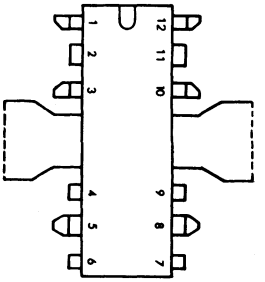
CB-109
TCA 940 E

PLASTIC PACKAGES
BOITIERS PLASTIQUE

BLOCK DIAGRAM
SCHEMA ELECTRIQUE



PIN CONFIGURATION
BROCHAGE



1 V_{CC}
2 **Not to use**
Ne pas utiliser
3 **Not to use**
Ne pas utiliser
4 **Bootstrap**
Bootstrap
5 **Compensation**
Compensation
6 **Feed-back network**
Réseau de contre-réaction
7 **Preamplifier decoupling**
Découplage du préamplificateur
8 **Input** / Entrée
9 **Substrate and preamplifier ground**
Substrat et masse du préamplificateur
10 **Output stage ground**
Masse de l'étage de sortie
11 **Not to use**
Ne pas utiliser
12 **Output** / Sortie

Tab must be grounded
L'ailette doit être réunie à la masse

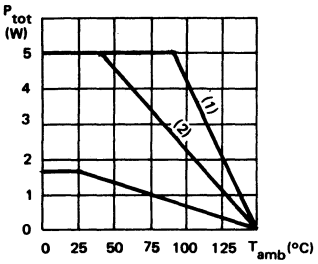
NT7741

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

Maximum power dissipation
Dissipation de puissance maximale

TCA 940

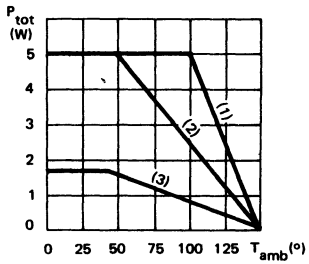


(1) With infinite heat sink
Avec radiateur infini

(2) With a 10°C/W heat sink
Avec radiateur de 10°C/W

(3) Without heat sink
Sans radiateur

TCA 940 E



LIMITING VALUES
VALEURS LIMITES ABSOLUES

Supply voltage *Tension d'alimentation*	V_{CC}	24	V
Peak output current (non repetitive) *Courant crête en sortie non répétitif*	I_O	3,5	A
Peak output current (repetitive) *Courant crête en sortie répétitif*	I_O	3	A
Junction temperature *Température de jonction*	T_j	−40 +150	°C °C
Storage temperature *Température de stockage*	T_{stg}	−40 +150	°C °C

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C (Note 1) (Unless otherwise stated) *(Sauf indications contraires)*

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Supply voltage *Tension d'alimentation*		V_{CC}		6		24	V
Quiescent output voltage (pin 12) *Tension de repos (broche 12)*	V_{CC} = 18 V	V_O		8,2	9	9,8	V
Quiescent current *Courant de repos*	V_{CC} = 18 V	I_{CC}			20	42	mA
Bias current (pin 8) *Courant d'entrée (broche 8)*	V_{CC} = 18 V	I_B			0,5	3	µA
Output power *Puissance de sortie*	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 20 V	P_O			10		W
	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 18 V	P_O		7	9		W
	d = 10 % R_L = 4 Ω f = 1 kHz V_{CC} = 16 V	P_O			7		W
	d = 10 % R_L = 8 Ω f = 1 kHz V_{CC} = 20 V	P_O			6,5		W
	d = 10 % R_L = 8 Ω f = 1 kHz V_{CC} = 18 V	P_O			5		W
Voltage for input saturation (peak) *Tension saturant l'entrée (crête)*		V_I		250			mV
Sensitivity *Sensibilité*	P_O = 9 W V_{CC} = 18 V R_L = 4 Ω f = 1 kHz R_f = 56 Ω	S			90		mV
Input impedance (pin 8) *Impédance d'entrée (broche 8)*		Z_I			5		MΩ

Note 1 : The characteristics above were obtained using the circuit shown in figure 1
Mesuré dans les conditions de la figure 1

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C

(Unless otherwise stated)
(Sauf indications contraires)

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Frequency response (−3 dB) *Bande passante (−3 dB)*	V_{CC} = 18 V C3 = 1000 pF	B			40 - 20 000		Hz
Distortion *Distorsion*	V_{CC} = 18 V P_O = 50 mW → 5 W R_L = 4 Ω R_f = 56 Ω f = 1 kHz	d			0,3		%
Voltage gain (open loop) *Gain de tension en boucle ouverte*	V_{CC} = 18 V R_L = 4 Ω f = 1 kHz	A_V			75		dB
Voltage gain (closed loop) *Gain de tension en boucle fermée*	V_{CC} = 18 V R_L = 4 Ω R_f = 56 Ω f = 1 kHz	A_V		34	37	40	dB
Input noise voltage *Tension de bruit à l'entrée*	V_{CC} = 18 V B(−3 dB) = 40 - 20 000 Hz	V_n			3		μV
Input noise current *Courant de bruit à l'entrée*	V_{CC} = 18 V B (−3 dB) = 40 - 20 000 Hz	I_n			0,15		nA
Efficiency *Rendement*	V_{CC} = 18 V P_O = 9 W R_L = 4 Ω f = 1 kHz	η			65		%
Supply voltage rejection *Réjection de l'ondulation d'alimentation*	V_{CC} = 18 V R_L = 4 Ω f_{ripple} = 100 Hz	SVR			43		dB

THERMAL CHARACTERISTICS
CARACTERISTIQUES THERMIQUES

Junction-case thermal resistance *Résistance thermique (jonction-boîtier)*		$R_{th(j-c)}$			10	°C/W
Junction-ambient thermal resistance *Résistance thermique (jonction-ambiante)*		$R_{th(j-a)}$			80	°C/W

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C (Note 1) (Unless otherwise stated) *(Sauf indications contraires)*

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Supply voltage *Tension d'alimentation*		V_{CC}		6		24	V
Quiescent output voltage (pin 12) *Tension de repos (broche 12)*	V_{CC} = 18 V	V_O		8,2	9	9,8	V
Quiescent current (pin 1) *Courant de repos (broche 1)*	V_{CC} = 18 V	I_{CC}			20	42	mA
Bias current (pin 8) *Courant d'entrée (broche 8)*	V_{CC} = 18 V	I_B			0,5	3	µA
Output power *Puissance de sortie*	d = 10 % R_L = 8 Ω f = 1 kHz V_{CC} = 20 V	P_O			6,5		W
	d = 10 % R_L = 8 Ω f = 1 kHz V_{CC} = 18 V	P_O		5	5,4		W
Voltage for input saturation (peak) *Tension saturant l'entrée (crête)*		V_I		250			mV
Sensitivity *Sensibilité*	P_O = 5,4 W V_{CC} = 18 V R_L = 8 Ω f = 1 kHz R_f = 56 Ω	S			90		mV
Input impedance (pin 8) *Impédance d'entrée (broche 8)*		Z_I			5		MΩ
Frequency response (−3 dB) *Bande passante (−3 dB)*	V_{CC} = 18 V C3 = 1000 pF	B		40 - 20 000			Hz

Note 1 : The characteristics above were obtained using the circuit shown in figure 1
Mesuré dans les conditions de la Figure 1

ELECTRICAL CHARACTERISTICS
CARACTERISTIQUES ELECTRIQUES

T_{amb} = 25°C

(Unless otherwise stated)
(Sauf indications contraires)

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Distorsion *Distorsion*	V_{CC} = 18 V P_O = 50 mW → 3,5 W R_L = 8 Ω R_f = 56 Ω f = 1 kHz	d			0,2		%
Voltage gain (open loop) *Gain de tension en boucle ouverte*	V_{CC} = 18 V R_L = 8 Ω f = 1 kHz	A_V			75		dB
Voltage gain (closed loop) *Gain de tension en boucle fermée*	V_{CC} = 18 V R_L = 8 Ω R_f = 56 Ω f = 1 kHz	A_V		34	37	40	dB
Input noise voltage *Tension de bruit à l'entrée*	V_{CC} = 18 V B(−3 dB) = 40 - 20 000 Hz	V_n			3		μV
Input noise current *Courant de bruit à l'entrée*	V_{CC} = 18 V B(−3 dB) = 40 - 20 000 Hz	I_n			0,15		nA
Efficiency *Rendement*	V_{CC} = 18 V P_O = 5,4 W R_L = 8 Ω f = 1 kHz	η			70		%
Supply voltage rejection *Réjection de l'ondulation d'alimentation*	V_{CC} = 18 V R_L = 8 Ω f_{ripple} = 100 Hz	SVR			43		dB

THERMAL CHARACTERISTICS
CARACTERISTIQUES THERMIQUES

Junction-case thermal resistance *Résistance thermique (jonction-boîtier)*		$R_{th(j-c)}$				12	°C/W
Junction-ambient thermal resistance *Résistance thermique (jonction-ambiante)*		$R_{th(j-a)}$				70*	°C/W

* Tabs soldered to printed circuit with minimized copper area
Ailettes soudées au circuit imprimé avec une surface de cuivre réduite

MEASUREMENT AND APPLICATION DIAGRAM
SCHEMA D'APPLICATION ET DE MESURE

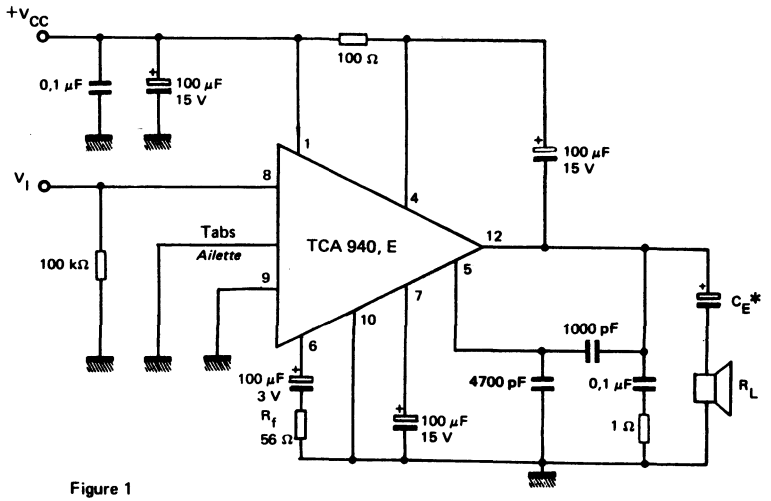


Figure 1

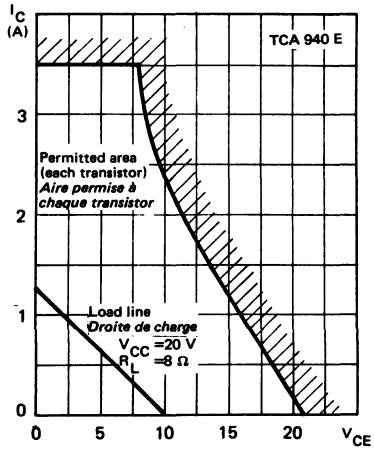
*C_E = 500 µF – 15 volts pour $R_L = 8\ \Omega$
C_E 1000 µF – 15 volts pour $R_L = 4\ \Omega$

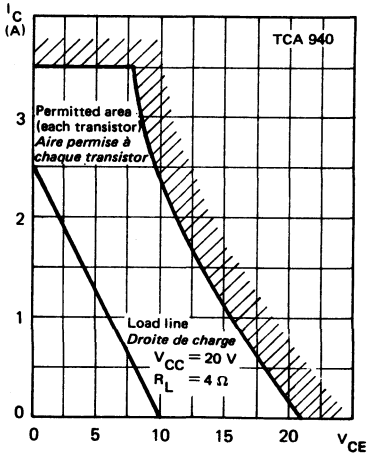
OVERLOAD AND OVERVOLTAGE PROTECTION

PROTECTION CONTRE LES SURCHARGES ET LES SURTENSIONS

Each power transistor is protected by a special, entirely integrated circuit which prevents it from working in dangerous conditions. The permitted area will not shrink with increased junction temperature.

Chaque transistor de puissance est protégé par un circuit spécial, entièrement intégré, qui l'empêche de fonctionner dans des conditions dangereuses. L'aire permise ne retrécit pas quand la température de jonction augmente.



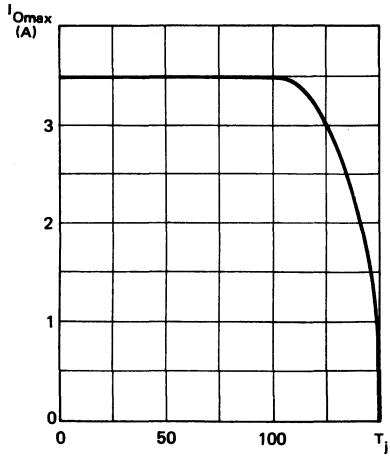


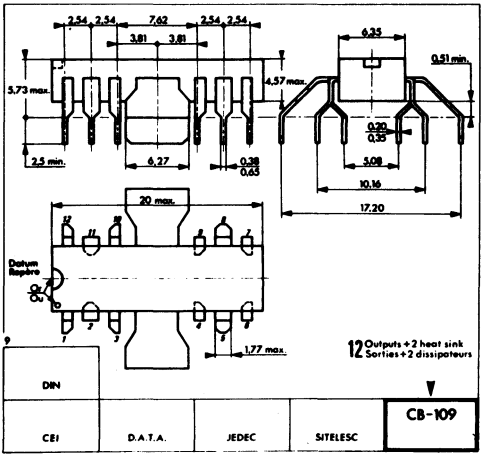
THERMAL PROTECTION

SECURITE THERMIQUE

When the die is overheated, available output current progressively falls down to 0.

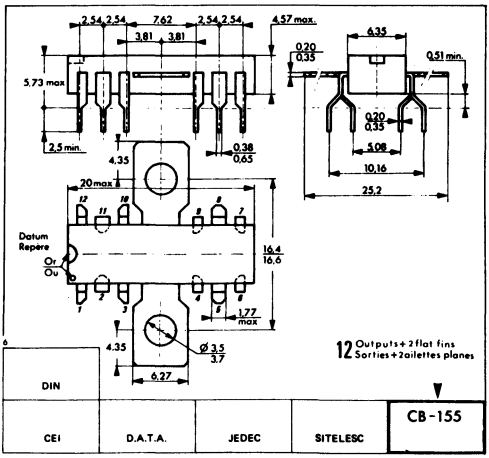
Quand la pastille intégrée s'échauffe trop, le courant disponible en sortie tombe progressivement à 0.





CASE / BOITIER CB-109

PLASTIC PACKAGE
BOITIER PLASTIQUE



CASE / BOITIER CB-155

PLASTIC PACKAGE
BOITIER PLASTIQUE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TDA1102

20 W HI FI AUDIO POWER AMPLIFIER WITH SHORT-CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

AMPLIFICATEUR BF 20 W AVEC PROTECTION CONTRE LES COURTS-CIRCUITS ET LIMITATION THERMIQUE

The TDA 1102 is a monolithic power amplifier with differential inputs specially intended for use as audio high fidelity amplifier. Typically it provides 20 W output power (d = 1 %) at V_{CC} = 28 V, or ± 14 V, R_L = 4Ω. It is supplied in a special case featuring very low thermal resistance. An internal circuitry protects it against overheating, load and DC short-circuit. Each power transistor is protected by an original (and patented) circuit which prevents it from working in dangerous conditions. The permitted area doesn't shrink with increased junction temperature.
The TDA 1102 has the same pin configuration as TDA 1111

Le TDA 1102 est un amplificateur BF intégré à entrées différentielles, spécialement développé pour les applications haute-fidélité. Il fournit 20 W dans une charge de 4 ohms avec une tension d'alimentation de 28 V ou ± 14 V (d = 1 %).
Il est monté dans un boîtier de puissance à très faible résistance thermique. Un dispositif interne le protège contre un échauffement excessif et contre les courts-circuits sur la charge et directement sur la sortie. Chaque transistor de puissance en sortie est protégé par un dispositif original (et breveté) qui l'empêche de travailler dans des conditions dangereuses. L'aire permise ne retrécit pas quand la température de jonction augmente.
Le TDA 1102 a le même brochage que le TDA 1111

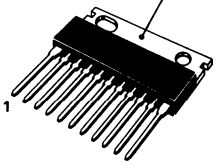
- **Output power to** / Puissance de sortie à **28 V, R_L = 4Ω**
  d = 1 % to / à **20 W**
  d = 10 % to / à **25 W**
- **Protected against overheating** / Protection contre surcharges thermiques
- **Load and DC short-circuit protection** / Protection court-circuit charge et sortie
- **Protected against inductive loads** / Protection contre charges inductives.

20 W HI FI AUDIO POWER AMPLIFIER WITH SHORT-CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

AMPLIFICATEUR BF 20 W AVEC PROTECTION CONTRE LES COURTS-CIRCUITS ET LIMITATION THERMIQUE

CASE / BOITIER **CB-173**

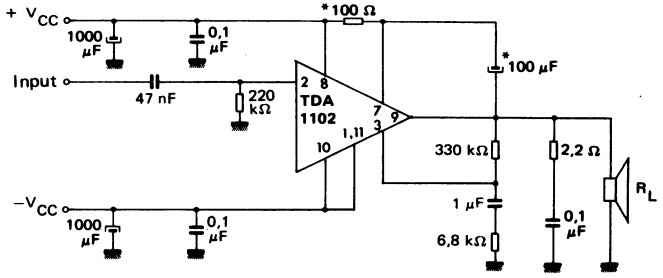
Tab connected to substrate
Ailette connectée au substrat



SP SUFFIX
PLASTIC PACKAGE
SUFFIXE SP
BOITIER PLASTIQUE

TYPICAL APPLICATION CIRCUIT

SCHEMA D'APPLICATION TYPIQUE

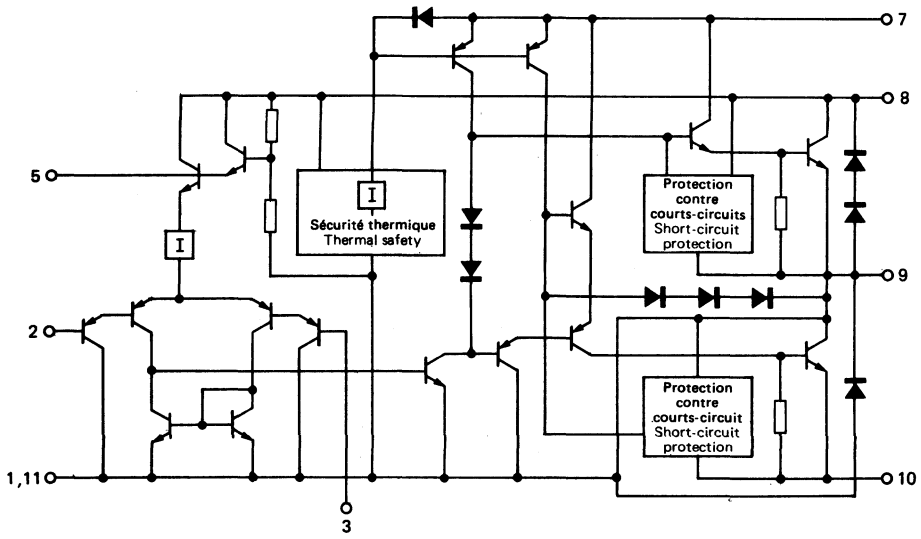


* **Optional, see p. 8**
* Facultatif, voir p. 8

A_V = 34 dB

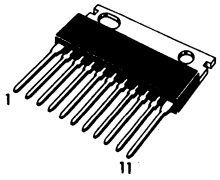
NT8026

SCHEMA INTERNE
INTERNAL DIAGRAM



BROCHAGE
PIN CONFIGURATION

BOITIER **CB-173**
Case



Les broches 1 et 11 sont réunies intérieurement et solidaires de l'ailette.

Pins 1 and 11 are internally connected and joined to the tab.

1 **Substrat** Substrate $-V_{CC}$
2 **Entrée non inverseuse** Non inverting input
3 **Entrée inverseuse** Inverting input
4 **Ne pas utiliser** Not to be used
5 **Filtrage** Ripple rejection
6 **Ne pas utiliser** Not to be used
7 **Bootstrap** Bootstrap
8 $+V_{CC}$
9 **Sortie** Output
10 $-V_{CC}$
11 **Substrat** Substrate $-V_{CC}$

VALEURS LIMITES ABSOLUES
ABSOLUTE MAXIMUM RATINGS

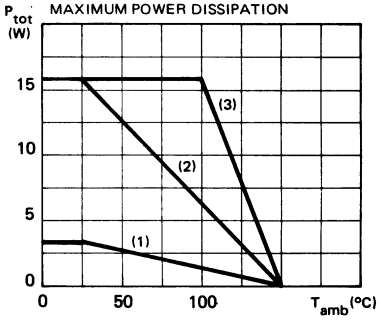
Tension d'alimentation Supply voltage	max.	V_{CC}	36	V
Température de jonction Junction temperature (1)	max.	T_j	150	°C
Température de stockage Storage temperature	min. max.	T_{stg}	− 40 + 150	°C °C

(1) **Valeur limite assurée par le dispositif de protection interne**
This limit value is automatically achieved by internal protection

CARACTERISTIQUES THERMIQUES
THERMAL CHARACTERISTICS

		MIN.	TYP.	MAX.	
Résistance thermique (jonction ambiante) (Junction ambient) thermal resistance	$R_{th(j-a)}$		30	35	°C/W
Résistance thermique (jonction boîtier) (Junction case) thermal resistance	$R_{th(j-c)}$		2,5	3	°C/W

DISSIPATION DE PUISSANCE MAXIMALE
MAXIMUM POWER DISSIPATION



(1) Sans radiateur
Without heatsink

(2) Avec radiateur 5°C/W
With heatsink 5°C/W

(3) Radiateur infini
Infinite heatsink

CARACTERISTIQUES GENERALES
GENERAL CHARACTERISTICS

T_{amb} = 25°C

(Voir schéma test page 5)
(Refer to the test circuit page 5)

PARAMETRES PARAMETERS	CONDITIONS DE MESURE TEST CONDITIONS	SYMBOLES SYMBOLS	MIN.	TYP.	MAX.	UNITES UNITS
Gamme de V_{CC} en fonctionnement V_{CC} operating range		V_{CC}	12		32	V
Courant de polarisation Input bias current	V_{CC} = 28 V	I_B		100	400	nA
Tension de décalage à l'entrée Input offset voltage		V_{IO}		± 3		mV
Courant de décalage à l'entrée Input offset current		I_{IO}		± 25		nA
Courant d'alimentation au repos Quiescent supply current	V_{CC} = 14 V	I_{CC}		20		mA
	V_{CC} = 28 V	I_{CC}		25		mA
Courant crête en sortie Peak output current	(Voir courbe page 14) (See curve page 14)	I_O		±3,5		A
Bande passante (−3 dB) Frequency response		B		30 → 120 000		Hz
Distorsion Distortion	R_L = 4 Ω V_{CC} = 28 V P_O = 15 W	d				
	f = 1 kHz			0,3	1	%
	f = 40 Hz → 15 kHz			0,5		%
	R_L = 4 Ω V_{CC} = 28 V P_O = 150mW → 10 W	d				
	f = 1 kHz			0,1	0,5	%
	f = 40 Hz → 15 kHz			0,2		%

CARACTERISTIQUES GENERALES (suite)
GENERAL CHARACTERISTICS (continued)

T_{amb} = 25°C

(Voir schéma test page 5)
(Refer to the test circuit page 5)

PARAMETRES PARAMETERS	CONDITIONS DE MESURE TEST CONDITIONS	SYMBOLES SYMBOLS	MIN.	TYP.	MAX.	UNITES UNITS
Puissance de sortie Output power	V_{CC} = 28 V V_{CC} = 24 V R_L = 4 Ω d = 1 % f = 1 kHz	P_O	15	20 15		W W
	V_{CC} = 28 V R_L = 8 Ω d = 1 % f = 1 kHz	P_O		10,4		W
	V_{CC} = 28 V R_L = 4 Ω d = 10 % f = 1 kHz	P_O	19	25		W
	V_{CC} = 28 V R_L = 8 Ω d = 10 % f = 1 kHz	P_O		13		W
Réjection de l'ondulation d'alimentation Supply voltage rejection ratio	V_{CC} = 28 V R_L = 4 Ω ΔV_{CC} = 1 Vpp f_{ripple} = 100 Hz A_V = 34 dB C_D = 100 µF	SVR		57		dB
Gain de tension (boucle ouverte) Voltage gain (open loop)	f = 1 kHz	A_V		90		dB
Gain de tension (boucle fermée) (Note 1) Voltage gain (closed loop)	f = 1 kHz	A_V	30		60	dB
Résistance d'entrée Input resistance		R_I		5		MΩ
Température de la protection thermique Thermal shut down temperature				155		°C
Tension de bruit ramenée à l'entrée Input noise voltage	R_G = 10 kΩ B = 40 Hz...20 kHz	v_n		3		µV
Tension à vide borne 5 (Note 2) Voltage pin 5 (when unconnected)	V_{CC} = 28 V			20		V

Note 1 — **Plage de gain pour laquelle la compensation interne assure une bonne stabilité.**
Voltage gain range giving good stability with the internal compensation.

Note 2 — **La borne 5 fournit, à la mise sous tension, le courant nécessaire à la charge du condensateur de découplage. En régime établi, le pont de polarisation extérieur lui impose un potentiel supérieur, bloquant ainsi le transistor de charge rapide.**
When switching on, pin 5 will provide sufficient current to rapidly charge decoupling capacitor.
At steady state, external biasing bridge will set on pin 5 a greater voltage ; thus, charging transistor gets OFF.

CIRCUIT DE MESURE (alimentation simple)
TEST CIRCUIT (single supply)

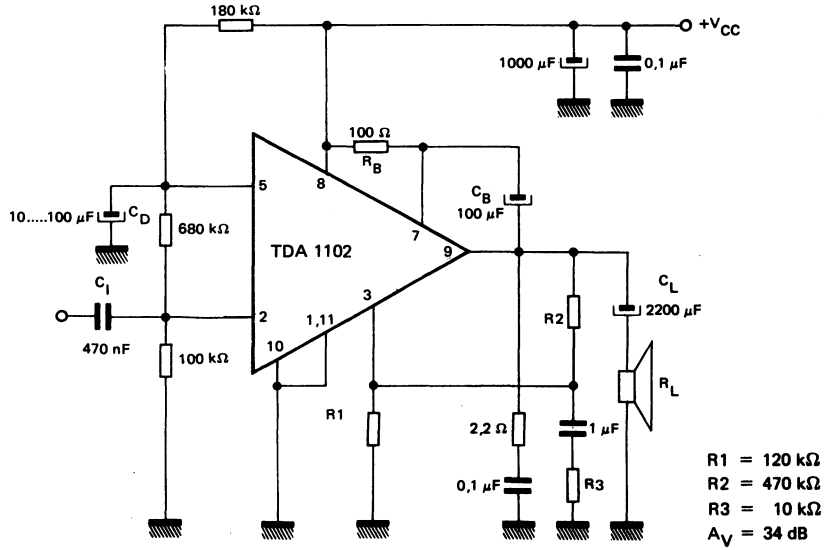


Fig. 1 – PUISSANCE DE SORTIE TYPIQUE EN FONCTION DE LA TENSION D'ALIMENTATION
TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

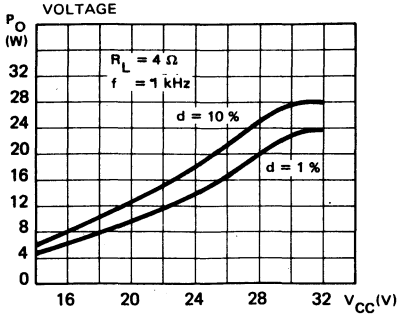


Fig. 2 – PUISSANCE DE SORTIE TYPIQUE EN FONCTION DE LA TENSION D'ALIMENTATION
TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

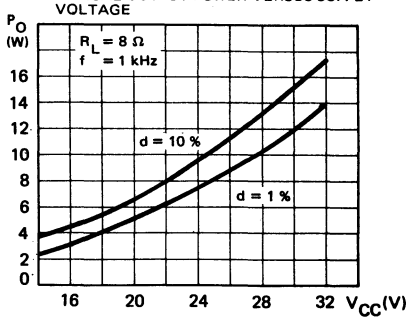


Fig. 3 – DISTORSION TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE
TYPICAL DISTORTION VERSUS OUTPUT POWER

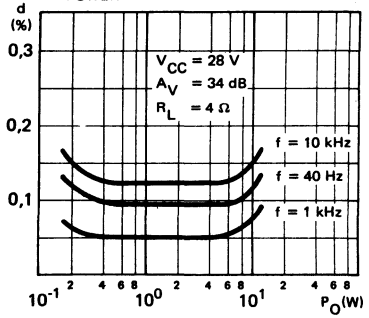


Fig. 4 – DISTORSION TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE
TYPICAL DISTORTION VERSUS OUTPUT POWER

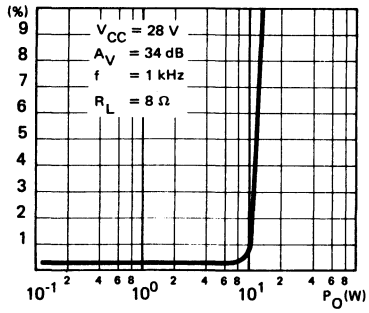


Fig. 5 – DISTORSION TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE
TYPICAL DISTORTION VERSUS OUTPUT POWER

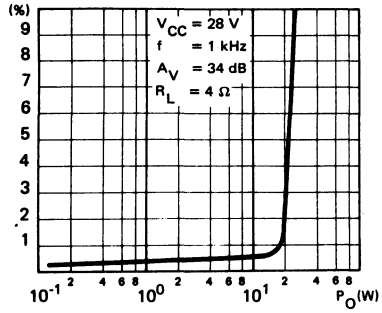


Fig. 6 – DISTORSION TYPIQUE EN FONCTION DE LA FREQUENCE
TYPICAL DISTORTION VERSUS FREQUENCY

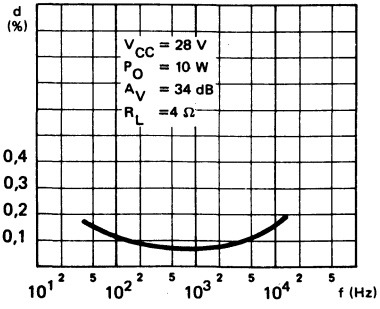


Fig. 7 – DISTORSION TYPIQUE EN FONCTION DE LA FREQUENCE
TYPICAL DISTORTION VERSUS FREQUENCY

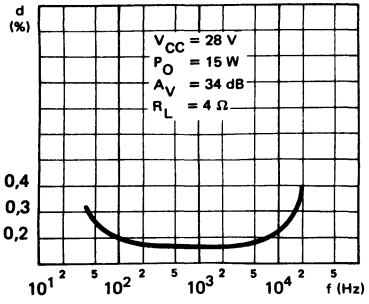


Fig. 8 – SENSIBILITE TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE
TYPICAL SENSITIVITY VERSUS OUTPUT POWER

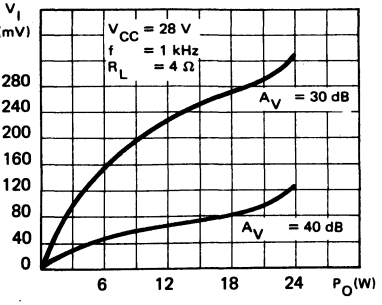


Fig. 9 – SENSIBILITE TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE
TYPICAL SENSITIVITY VERSUS OUTPUT POWER

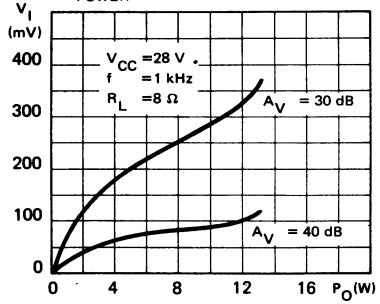


Fig. 10 – FREQUENCE DE REPONSE EN BOUCLE OUVERTE
OPEN LOOP FREQUENCY RESPONSE

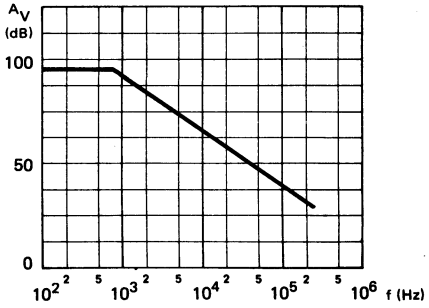


Fig. 11 – COURANT DE REPOS TYPIQUE EN FONCTION DE LA TENSION D'ALIMENTATION
TYPICAL QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE

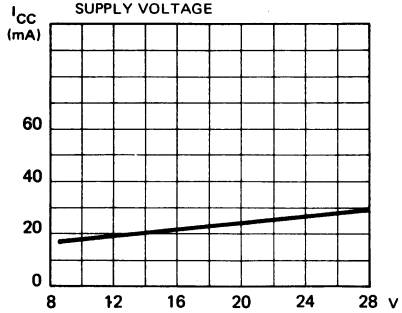


Fig. 12 – PUISSANCE DISSIPEE TYPIQUE ET RENDEMENT EN FONCTION DE LA PUISSANCE DE SORTIE
TYPICAL POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

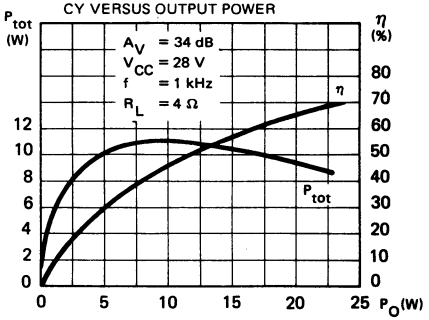


Fig. 13 – PUISSANCE DISSIPEE TYPIQUE ET RENDEMENT EN FONCTION DE LA PUISSANCE DE SORTIE
TYPICAL POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

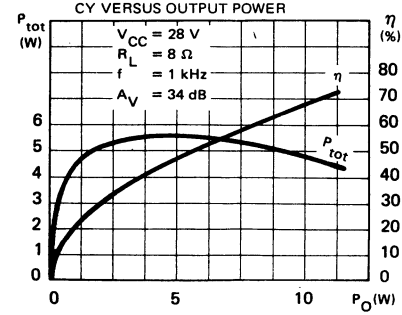
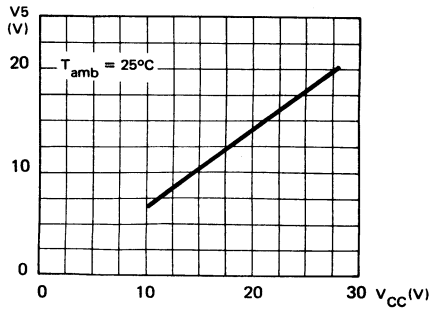
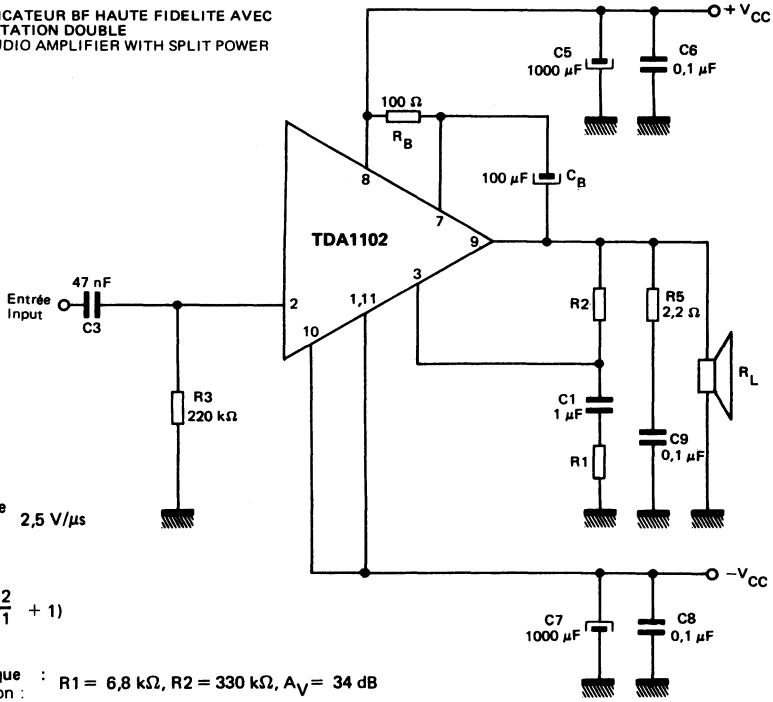


Fig. 14 – TENSION BORNE 5 EN FONCTION DE V_{CC}
PIN 5 VOLTAGE VERSUS V_{CC}



SCHEMAS D'APPLICATION
APPLICATION CIRCUITS

Fig.15 – AMPLIFICATEUR BF HAUTE FIDELITE AVEC ALIMENTATION DOUBLE
HI-FI AUDIO AMPLIFIER WITH SPLIT POWER SUPPLY



Vitesse de montée
Slew rate 2,5 V/µs

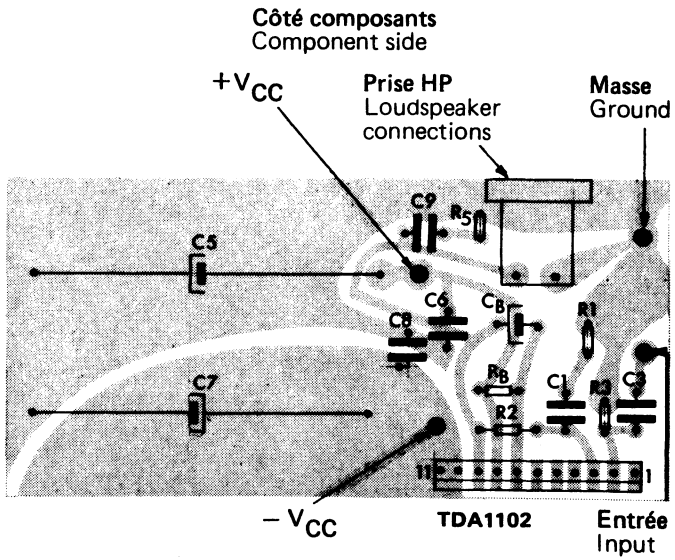
Gain

$A_V = 20 \log. \left(\frac{R2}{R1} + 1\right)$

Application typique : R1 = 6,8 kΩ, R2 = 330 kΩ, A_V = 34 dB
Typical application :

Quand le circuit "Bootstrap" n'est pas utilisé (R_B et C_B supprimés, les broches 7 et 8 reliées à $+V_{CC}$), la tension de déchet vers le haut augmente d'environ 1 V, ce qui réduit la puissance disponible.
When the bootstrap circuit is not used (R_B and C_B removed, pins 7 and 8 tied to $+V_{CC}$), upper voltage loss becomes approximately 1 volt greater, consequently output power is reduced.

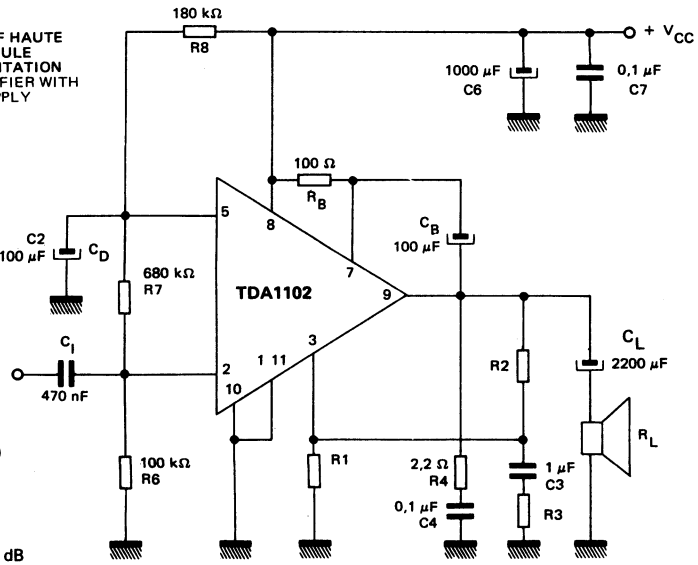
Circuit imprimé et disposition des composants
P.C board and component layout



Echelle : 1
Scale :

Côté cuivre
Copper side

Fig.16 – AMPLIFICATEUR BF HAUTE FIDELITE A UNE SEULE TENSION D'ALIMENTATION
HI-FI AUDIO AMPLIFIER WITH SINGLE POWER SUPPLY



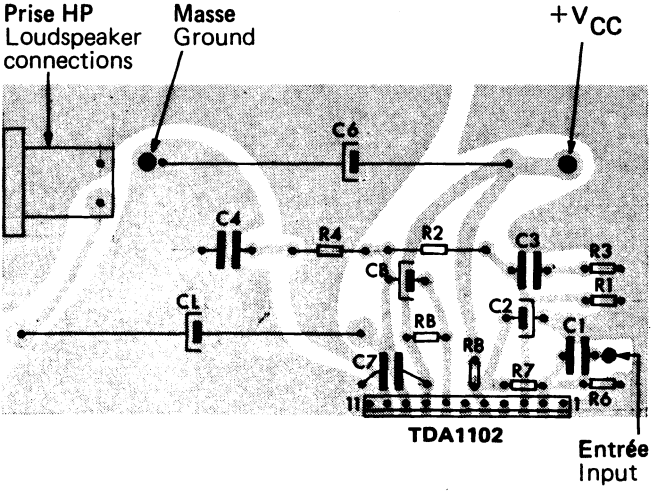
$$A_V = 20 \text{ Log.}\left(\frac{R2}{R1//R3} + 1\right)$$

R1 = 120 kΩ
R2 = 470 kΩ
R3 = 10 kΩ, A_v = 34 dB

Quand le circuit "Bootstrap" n'est pas utilisé (R_B et C_B supprimés, les broches 7 et 8 reliées à $+V_{CC}$), la tension de déchet vers le haut augmente d'environ 1 V, ce qui réduit la puissance disponible.
When the bootstrap circuit is not used (R_B and C_B removed, pins 7 and 8 tied to $+V_{CC}$), upper voltage loss becomes approximately 1 volt greater, consequently output power is reduced.

Circuit imprimé et disposition des composants
P.C board and component layout

Côté composants
Component side



Echelle : 1
Scale :

Côté cuivre
Copper side

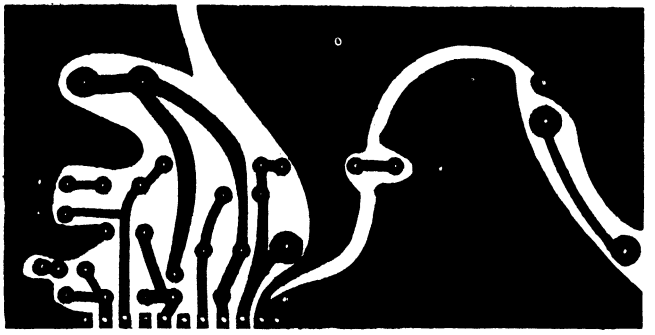
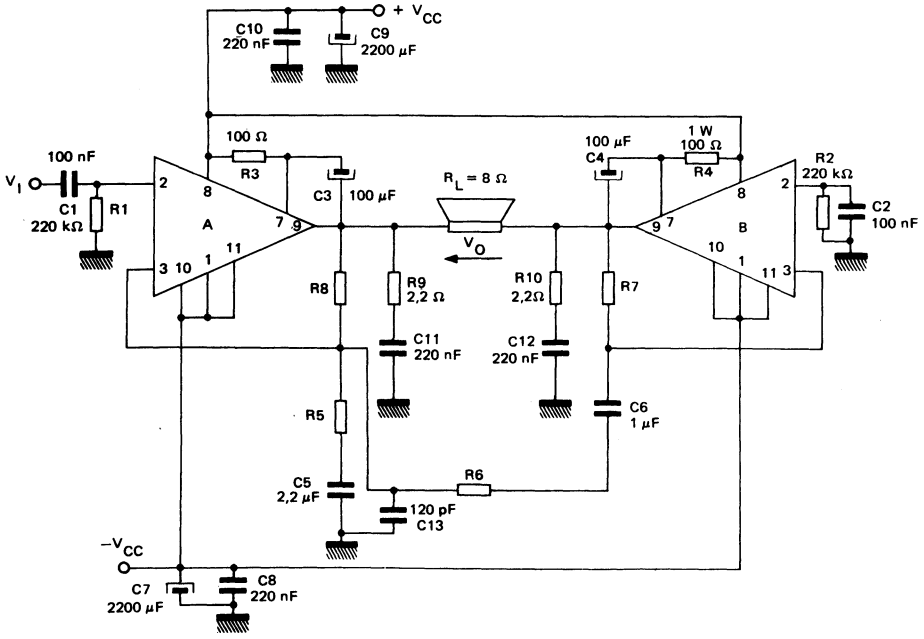


Fig.17 – APPLICATION TYPIQUE EN PONT AVEC ALIMENTATION DOUBLE
TYPICAL BRIDGE AMPLIFIER CONFIGURATION WITH SPLIT POWER SUPPLY



Gain en tension de l'amplificateur A
Voltage gain A amplifier

$$A_V(A) = 20 \text{ Log.}\left(\frac{R8}{R5//R6} + 1\right)$$

Gain total
Total gain

$$20 \text{ Log.} \left|\frac{V_O}{V_I}\right| = 46 \text{ dB}$$

Gain en tension de l'amplificateur B
Voltage gain B amplifier

$$A_V(B) = 20 \text{ Log.}\left|-\frac{R7}{R6}\right|$$

Avec
With $R7 = 470\ k\Omega$, $R8 = 220\ k\Omega$, $R5 = 4{,}7\ k\Omega$, $R6 = 4{,}7\ k\Omega$, $A_V(A) = A_V(B) = 40$ dB

PARAMETRES PARAMETERS	CONDITIONS DE MESURE TEST CONDITIONS		MIN. TYP. MAX.	UNITES UNITS
Puissance de sortie Output power	$V_{CC} = \pm 14$ V $R_L = 8\ \Omega$ f = 1 kHz $A_V(A) = A_V(B) = 40$ dB d = 1 % d = 10 %	P_O	 36 44	 W W
Tension de décalage en sortie Output offset voltage	R7 = 470 kΩ, R8 = 220 kΩ R5 = 4,7 kΩ, R6 = 4,7 kΩ $A_V(A) = A_V(B) = 40$ dB	V_O(off)	5	mV

Amplificateur typique en pont avec alimentation double (pour le circuit de la figure 17)
Typical bridge amplifier configuration with split power supply (for the circuit of figure 17)

Fig.18 – **DISTORSION TYPIQUE EN FONCTION DE LA FREQUENCE**
TYPICAL DISTORTION VERSUS FREQUENCY

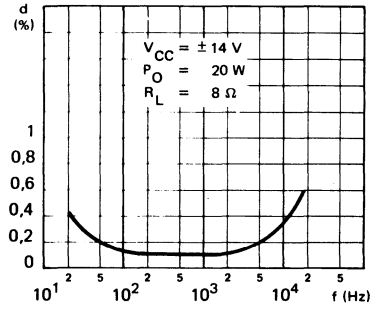
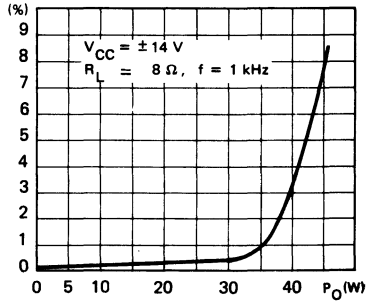
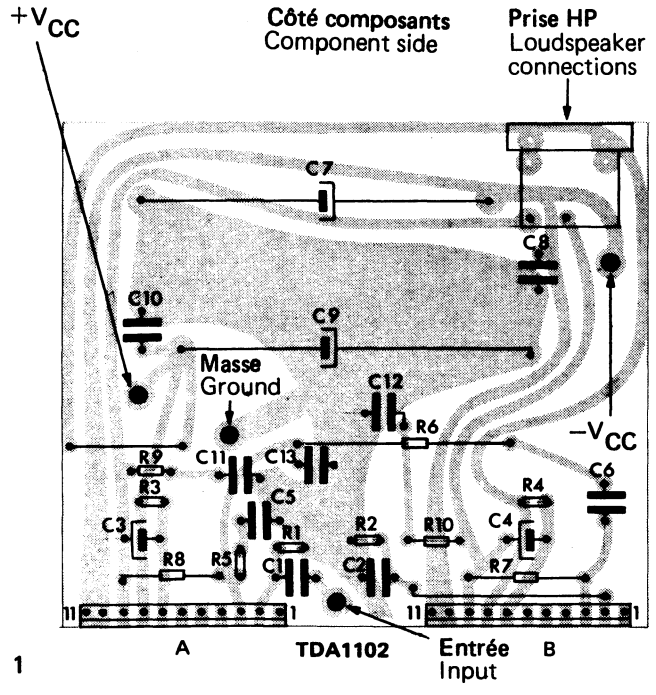


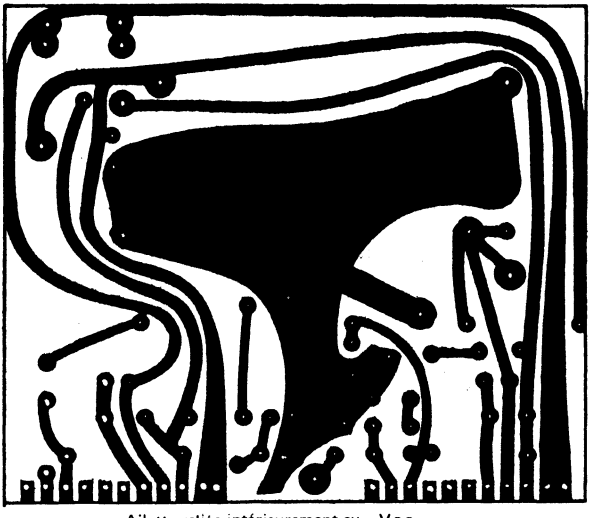
Fig.19 – **DISTORSION TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE**
TYPICAL DISTORTION VERSUS OUTPUT POWER



Circuit imprimé et disposition des composants pour le circuit de la figure 17
P.C board and component layout for the circuit of figure 17



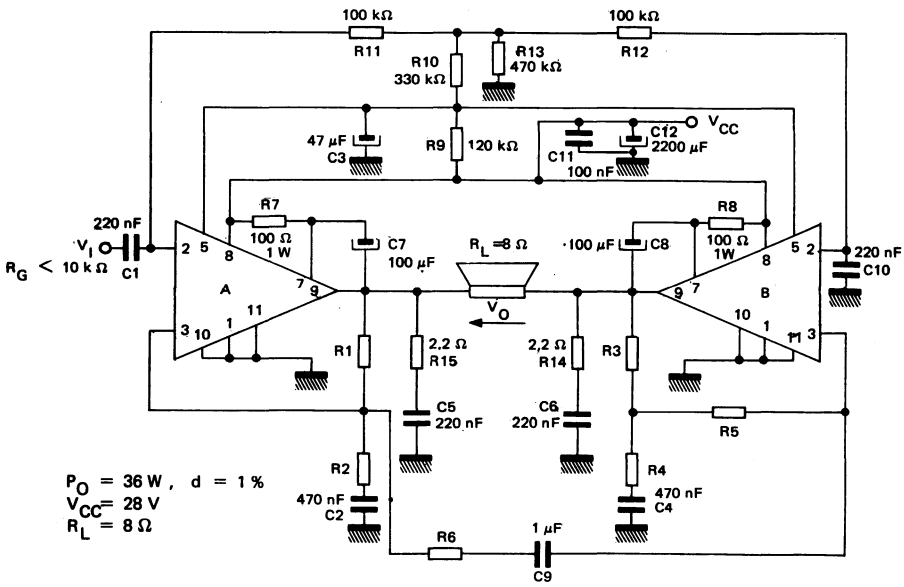
Echelle : 1
Scale :



Côté cuivre
Copper side

Ailette reliée intérieurement au - V_{CC}
The tab is internally connected to - V_{CC}

Fig.20 – APPLICATION TYPIQUE EN PONT AVEC ALIMENTATION SIMPLE
TYPICAL BRIDGE AMPLIFIER CONFIGURATION WITH SINGLE POWER SUPPLY



Gain en tension des amplificateurs A et B
Voltage gain A and B amplifiers

$$A_V(A) = 20 \text{ Log.}\left(\frac{R1}{R2//R6} + 1\right) \qquad A_V(B) = 20 \text{ Log.}\left|\left(\frac{R3}{R4} + 1\right)\left(-\frac{R5}{R6}\right)\right|$$

avec / with $R1 = R3 = 470\ k\Omega$, $R2 = R4 = 15\ k\Omega$, $R5 = R6 = 100\ k\Omega$, $A_V(A) = A_V(B) = 30\ dB$

Gain total / Total gain $20 \text{ Log. } \left(\frac{V_O}{V_I}\right) = 36\ dB$

Amplificateur typique en pont avec alimentation simple (pour le circuit de la figure 20)
Typical bridge amplifier configuration with single power supply (for the circuit of the figure 20)

Fig.21 – DISTORSION TYPIQUE EN FONCTION DE LA FREQUENCE
TYPICAL DISTORTION VERSUS FREQUENCY

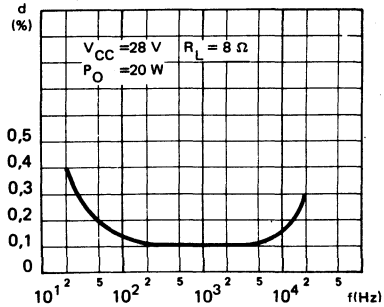
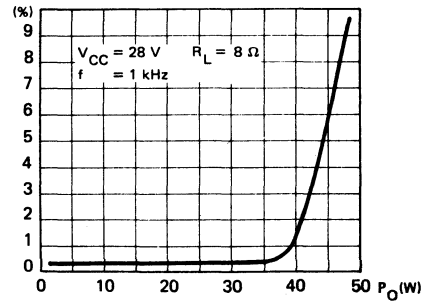
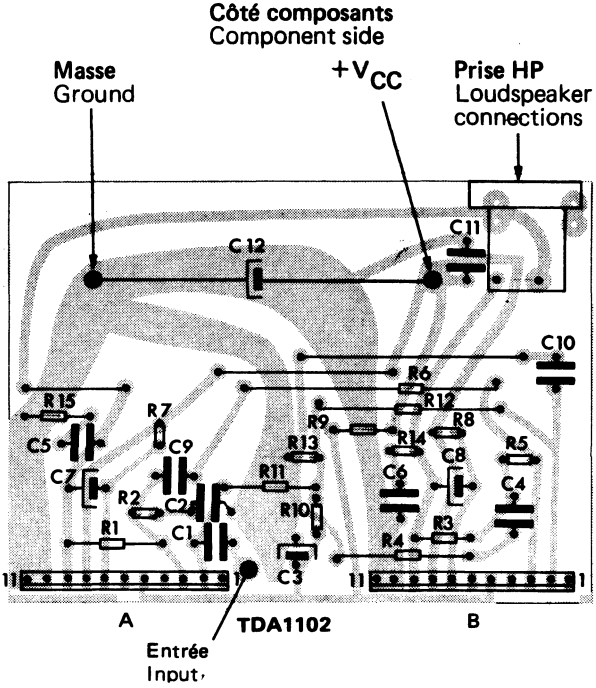


Fig.22 – DISTORSION TYPIQUE EN FONCTION DE LA PUISSANCE DE SORTIE
TYPICAL DISTORTION VERSUS OUTPUT POWER

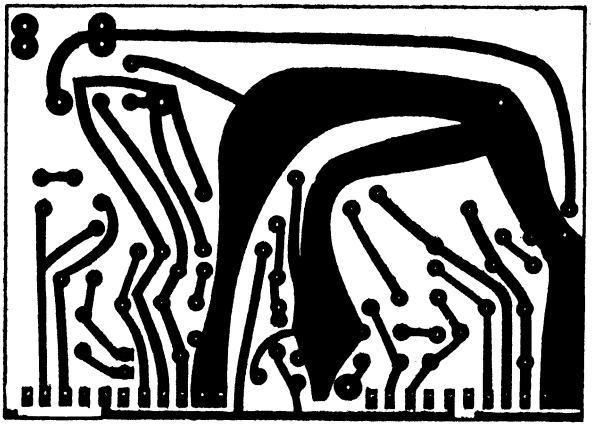


Circuit imprimé et disposition des composants (pour le circuit de la figure 20)
P.C board and component layout (for the circuit of the figure 20)



Echelle : 1
Scale :

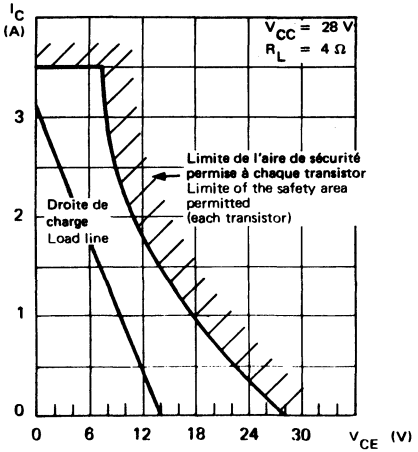
Côté cuivre
Copper side

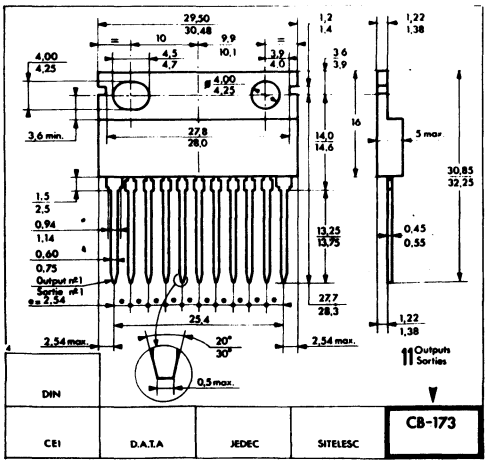


PROTECTION CONTRE LES SURCHARGES ET LES SURTENSIONS
OVERLOAD AND OVERVOLTAGE PROTECTION

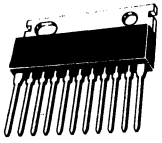
Chaque transistor de puissance est protégé par un circuit spécial, entièrement intégré, qui l'empêche de fonctionner dans des conditions dangereuses. L'aire permise ne retrécit pas quand la température de jonction augmente.

Each power transistor is protected by a special, entirely integrated circuit, which prevents it from working in dangerous conditions. The permitted area will not shrink with increased junction temperature.





CASE / BOITIER CB-173



SP SUFFIX
PLASTIC PACKAGE
SUFFIXE SP
BOITIER PLASTIQUE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TDA1111

POWER AUDIO AMPLIFIERS 8 TO 20 W
AMPLIFICATEURS BASSE FREQUENCE 8 A 20 W

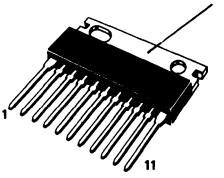
The TDA1111 is a power amplifier, specially intended for use audio high fidelity amplifier.
It is supplied in special case featuring very low thermal resistance.
The junction temperature is limited by an internal protection circuit.

Le circuit intégré monolithique TDA1111 est un amplificateur de puissance, particulièrement destiné aux applications amplificateur basse fréquence haute fidélité.
Il est présenté en boîtier spécial à très faible résistance thermique.
La température de jonction est limitée par un circuit de protection interne.

POWER AUDIO AMPLIFIERS 8 TO 20 W
AMPLIFICATEURS BASSE FREQUENCE 8 A 20 W

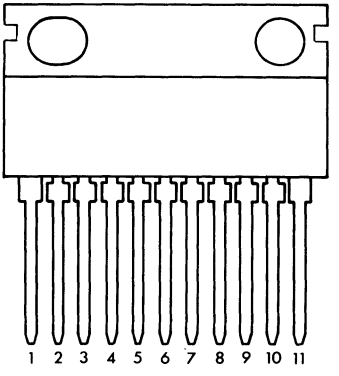
CASE / BOITIER **CB-173**

Tab is connected to substrat
Ailette reliée au substrat



SP SUFFIX
PLASTIC PACKAGE
SUFFIXE SP
BOITIER PLASTIQUE

PIN CONFIGURATION
BROCHAGE



1 **Substrat** $-V_{CC}$
Substrat
2 **Non inverting input**
Entrée non inverseuse
3 **Inverting input**
Entrée inverseuse
4 **Frequency compensation**
Compensation en fréquence
5 **No connected**
Ne pas connecter
6 **Not to be used**
Ne pas utiliser
7 **Boostrap**
Bootstrap
8 $+V_{CC}$
9 **Output**
Sortie
10 $-V_{CC}$
11 **Substrate** $-V_{CC}$
Substrat

NT7905

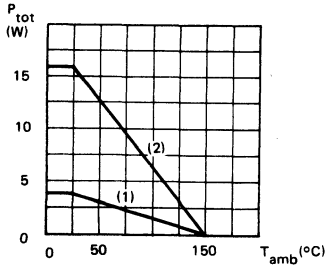
THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

THERMAL CHARACTERISTICS
CARACTERISTIQUES THERMIQUES

Junction-ambient thermal resistance *Résistance thermique (jonction-ambiante)*	(max)	$R_{th(j-a)}$		35	°C/W
Junction-case thermal resistance *Résistance thermique (jonction-boîtier)*	(max)	$R_{th(j-c)}$		3	°C/W

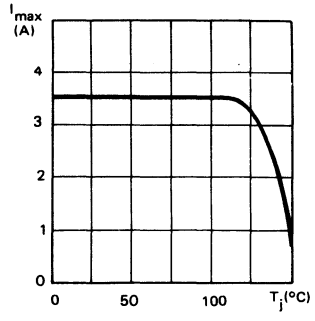
Maximum power dissipation
Dissipation de puissance maximale



(1) Without heatsink
Sans radiateur

(2) With heatsink 5°C/W
Avec radiateur 5°C/W

TYPICAL THERMAL PROTECTION CHARACTERISTICS
CARACTERISTIQUES TYPIQUES DE PROTECTION THERMIQUE



ABSOLUTE RATINGS (LIMITING VALUES)
VALEURS LIMITES ABSOLUES D'UTILISATION

T_{amb} = 25°C (Unless otherwise stated) *(Sauf indications contraires)*

Supply voltage *Tension d'alimentation*		V_{CC}		30	V
Operating supply voltage *Tension d'alimentation en charge*				28	V
Junction temperature *Température de jonction*	(1) max.	T_j		150	°C
Storage temperature *Température de stockage*	min. max.	T_{stg}		−25 +150	°C °C

(1) This limit value is automatically achieved by internal protection
Valeur limite assurée par le dispositif de protection interne

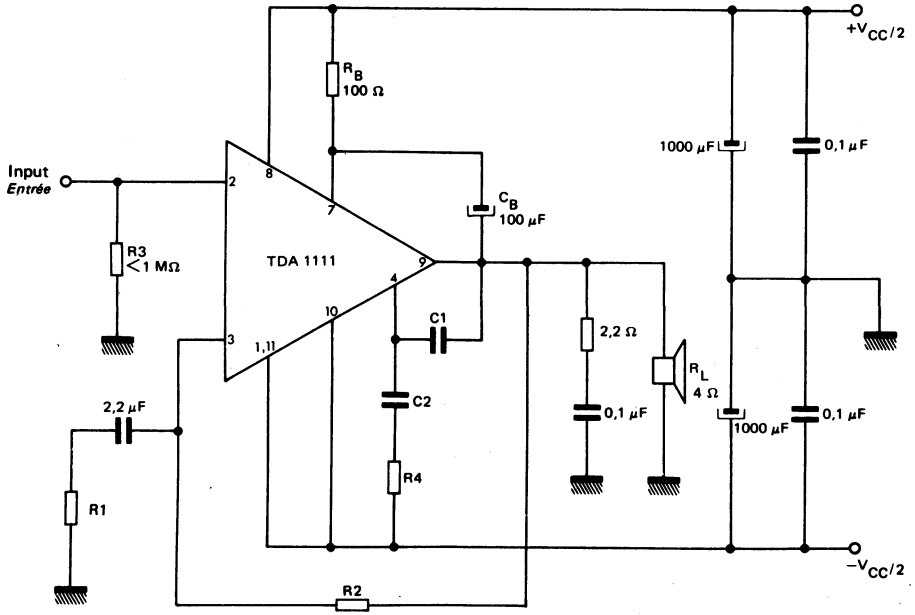
GENERAL CHARACTERISTICS
CARACTERISTIQUES GENERALES

T_{amb} = 25°C (Unless otherwise stated) *(Sauf indications contraires)*

	Test conditions *Conditions de mesure*			Min.	Typ.	Max.	
Input bias current *Courant d'entrée*		I_I			200		nA
Input noise voltage *Tension de bruit ramenée à l'entrée*	R_G = 10 kΩ B = 20 kHz	v_n			4		μV
Quiescent supply current *Courant d'alimentation au repos*	V_{CC} = 14 V	I_{CC}			20		mA
	V_{CC} = 28 V	I_{CC}			25		mA
Peak output current *Courant crête en sortie*					±3,5		A
Output power *Puissance de sortie* (See application diagram) *(Voir schéma d'application)*	V_{CC} = 28 V R_L = 4 Ω d = 1 % f = 1 kHz	P_O		15	20		W
Supply voltage rejection *Réjection de l'ondulation d'alimentation*	V_{CC} = 28 V ΔV_{CC} = 2 V p.p f = 100 Hz A_V = 33 dB A_V = 28 dB	SVR		40 45	53 58		dB

APPLICATION CIRCUITS
CIRCUITS D'APPLICATION

HI - FI AUDIO AMPLIFIER WITH SPLIT POWER SUPPLY
AMPLIFICATEUR BF HAUTE FIDELITE, ALIMENTATIONS SYMETRIQUES



Gain *Gain* $A_V = \frac{R2}{R1} + 1$

Bandwidth *Bande passante* $B = \frac{R1}{R2} \frac{Y}{C1}$ (small signal) *(petit signal)*

Slew-rate *Vitesse de montée* 1 V/µs

$Y = 2,7 \cdot 10^{-4}$ S typ.

Typical application
Application typique

R1 = 6,8 kΩ, R2 = R3 = 220 kΩ, C1 = 68 pF, C2 = 1 nF, R4 = 270 Ω

A_V = 33

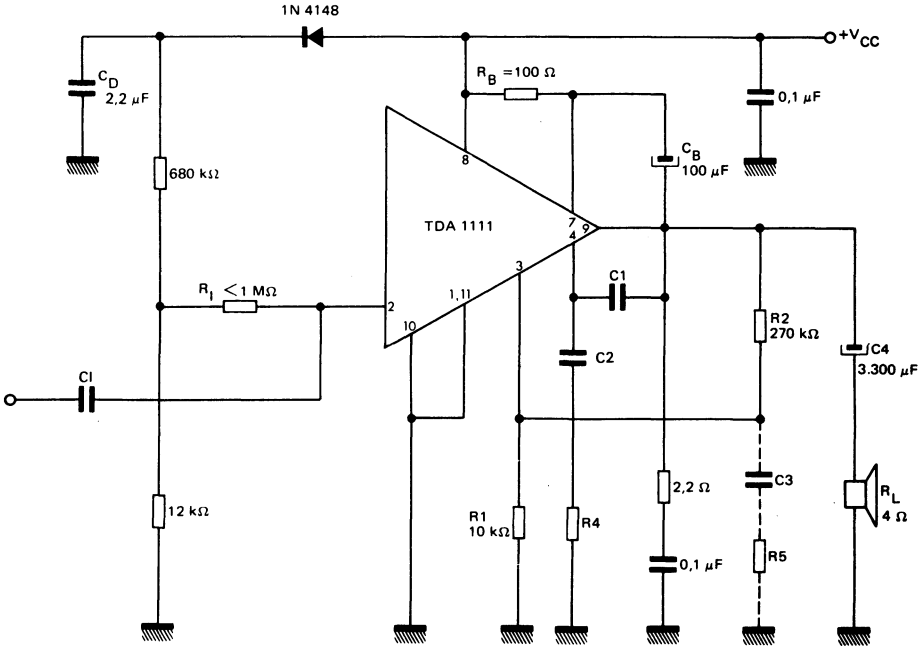
B = 40 Hz - 120 kHz

When the bootstrap circuit is not used (R_B and C_B removed, pins 7 and 8 tied to $+V_{CC}$), upper voltage loss becomes approximately 1 volt greater ; consequently output power is reduced.

Quand le circuit "Bootstrap" n'est pas utilisé (R_B et C_B supprimés, les broches 14 et 1 reliées à $+V_{CC}$), la tension de déchet vers le haut augmente d'environ 1 V, ce qui réduit la puissance disponible.

APPLICATION CIRCUITS
CIRCUITS D'APPLICATION

HI - FI AUDIO AMPLIFIER WITH SINGLE POWER SUPPLY
AMPLIFICATEUR BF HAUTE FIDELITE, A UNE SEULE TENSION D'ALIMENTATION



The output power is the same as in previous case
La puissance de sortie est la même que dans le montage précédent

Voltage gain : $A_V = \frac{R2}{R1} + 1 = 28$
Gain en tension

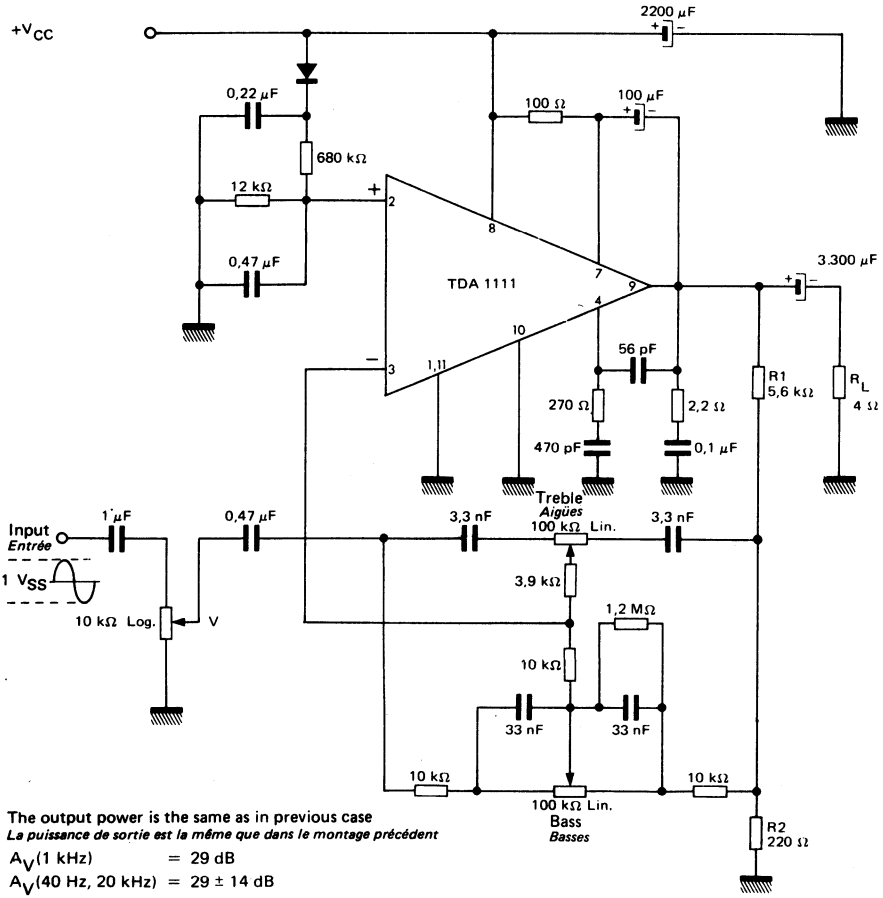
Bandwidth : B = 12 Hz - 140 kHz
Bande passante

For higher voltage gain, C3 and R5 should be used. C3 . R5 should be kept lower than C4 . R_L and C_I . R_I lower than 10 mS for better transient overloading protection.

Si on désire un gain en tension plus élevé, il faut employer C3 et R5. Pour une meilleure résistance aux surcharges transitoires, la constante de temps C3 . R5 doit rester inférieure à C4 . R_L et C_I . R_I inférieur à 10 mS.

APPLICATION CIRCUITS
CIRCUITS D'APPLICATION

AF AMPLIFIER WITH TONE CONTROLS
AMPLIFICATEUR DE PUISSANCE AVEC REGLAGES DE TONALITE

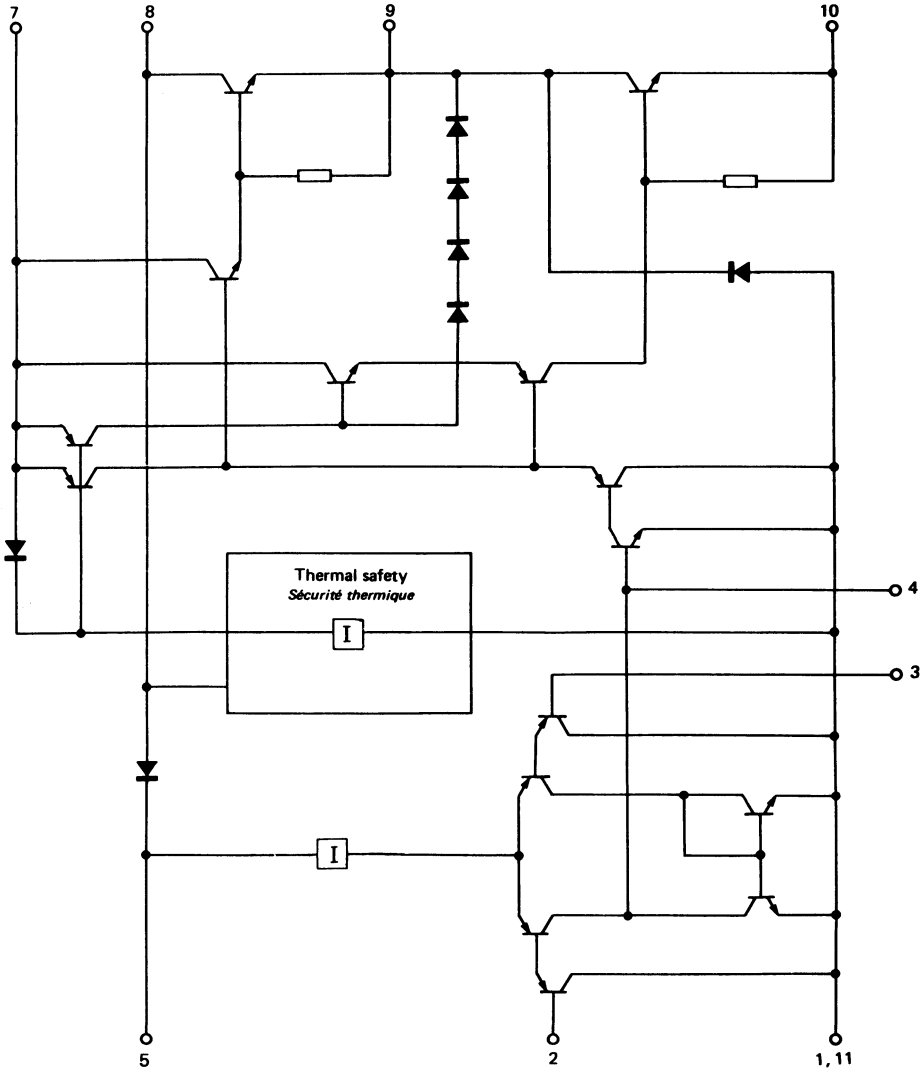


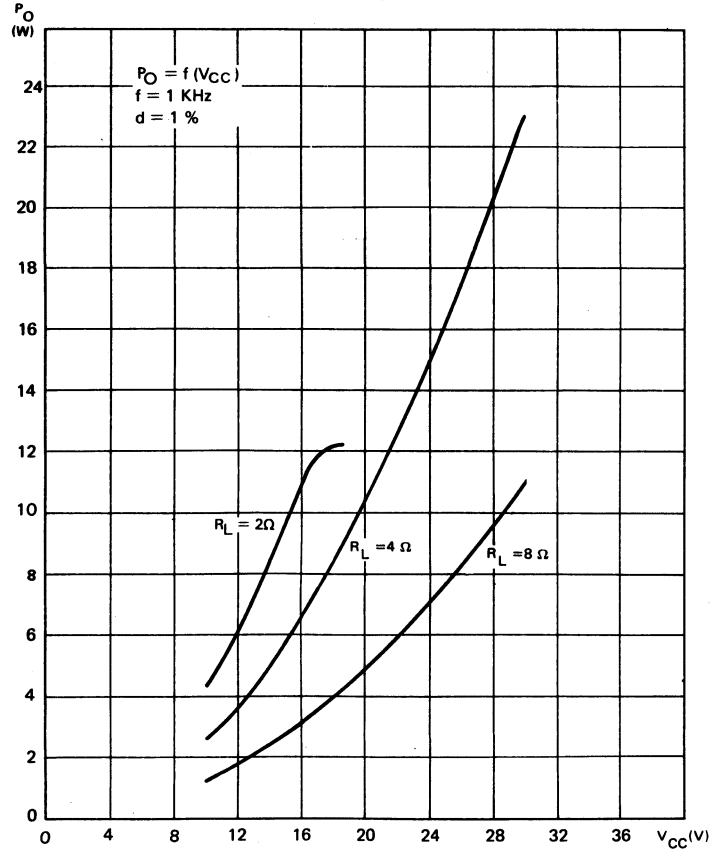
The output power is the same as in previous case
La puissance de sortie est la même que dans le montage précédent

A_V(1 kHz) = 29 dB

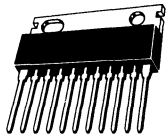
A_V(40 Hz, 20 kHz) = 29 ± 14 dB

INTERNAL DIAGRAM
SCHEMA INTERNE

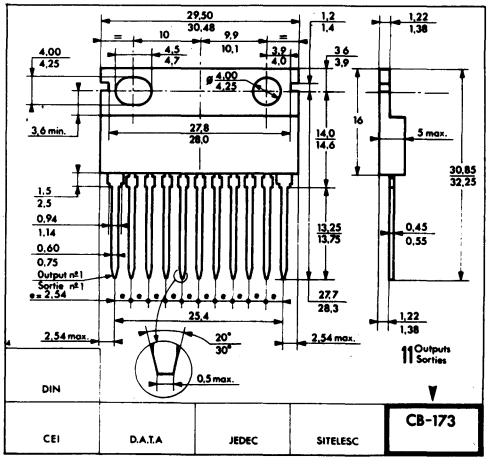



P_O (W)
$P_O = f(V_{CC})$
f = 1 KHz
d = 1 %
24
22
20
18
16
14
12
10
8
6
4
2
0
0
4
8
12
16
20
24
28
32
36
V_{CC}(V)
R_L = 2Ω
R_L = 4 Ω
R_L = 8 Ω

CASE / BOITIER **CB-173**



SP SUFFIX
PLASTIC PACKAGE
SUFFIXE SP
BOITIER PLASTIQUE



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NOTES

THOMSON SEMICONDUCTORS

TDA2003

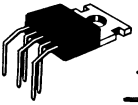
10 W CAR RADIO AUDIO AMPLIFIER

The TDA 2003 has improved performance with the same pin configuration as the TDA 2002. The additional features of TDA 2002; very low number of external components, ease of assembly, space and cost saving, are maintained. The device provides a high output current capability (up to 3.5 A) very low harmonic and cross-over distortion.
Completely safe operation is guaranteed due to protection against DC and AC short circuit between all pins and ground, thermal over-range, load dump voltage surge up to 40 V, polarity inversion and fortuitous open ground.

10 W CAR RADIO AUDIO AMPLIFIER

CASE

CB-367



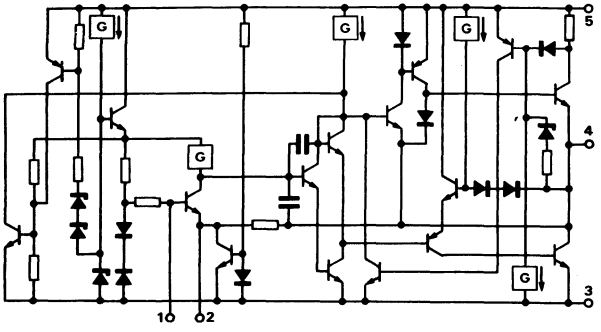
TDA2003 H

CB-360

TDA2003V

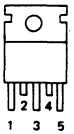
SP SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM

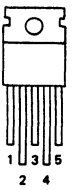


PIN CONFIGURATIONS

CB 367
Top view



CB-360
Top view



1 Non inverting input
2 Inverting input
3 Ground
4 Output
5 Supply voltage

Tab is connected to pin 3

NT8024-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak supply voltage (50 ms)	V_{CC}	40	V
DC supply voltage	V_{CC}	28	V
Operating supply voltage	V_{CC}	18	V
Output peak current (repetitive)	I_O	3.5	A
Output peak current (no repetitive)	I_O	4.5	A
Power dissipation (T_{case} = 90 °C)	P_{tot}	20	W
Storage and junction temperature	$T_j - T_{stg}$	− 40 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-case thermal resistance	$R_{th(j-c)}$	3 max.	°C/W

STATIC CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 14.4 V; (see figure 1) (Unless otherwise stated)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{CC}	8		18	V
Quiescent output voltage	Pin 4	V_O	6.1	6.9	7.7	V
Quiescent drain current	Pin 5	I_{CC}		44	50	mA

DYNAMIC CHARACTERISTICS

T_{amb} = 25 °C; V_{CC} = 14.4 V; A_V = 40 dB; (see figure 2) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Output power (d = 10 %; f = 1kHz)	P_O				V
R_L = 4 Ω		5.5	6	–	
R_L = 2 Ω		9	10	–	
R_L = 3.2 Ω		–	7.5	–	
R_L = 1.6 Ω		–	12	–	
Input saturation voltage	V_I	300	–	–	mV

FIG. 1 – DC TEST CIRCUIT

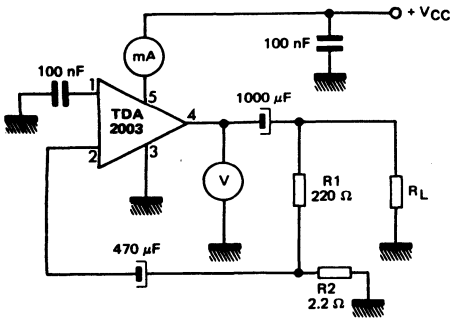
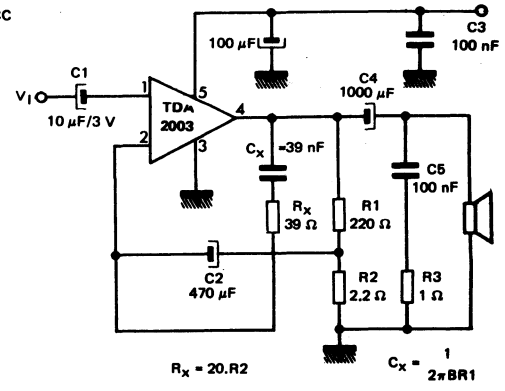


FIG. 2 – AC TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input sensitivity	S				mV
f = 1 kHz; P_O = 0.5 W; R_L = 4 Ω		–	14	–	
P_O = 6 W; R_L = 4 Ω		–	55	–	
P_O = 0.5 W; R_L = 2 Ω		–	10	–	
P_O = 10 W; R_L = 2 Ω		–	50	–	
Bandwidth (– 3 dB)	B				Hz
P_O = 1 W; R_L = 4 Ω			40 to 15.000		
Harmonic distortion	d				%
0.05 W ⩽ P_O ⩽ 4.5 W; R_L = 4 Ω; f = 1 kHz		–	0.15	–	
0.05 W ⩽ P_O ⩽ 7.5 W; R_L = 2 Ω; f = 1 kHz		–	0.15	–	
Input resistance (f = 1 kHz) Pin 1	R_I	70	150	–	kΩ
Voltage gain (R_L = 4 Ω; f = 1 kHz)	A_V				dB
Open loop		–	80	–	
Closed loop		39.5	40	40.5	
Input noise voltage	V_n				μV
B (– 3 dB) = 10 to 25.000 Hz; B (– 20 dB) = 4 to 27.000 Hz		–	1	5	
Input noise current	i_n				pA
B (– 3 dB) = 10 to 25.000 Hz; B (– 20 dB) = 4 to 27.000 Hz		–	60	200	
Efficiency	η				%
f = 1 kHz; P_O = 6 W; R_L = 4 Ω		–	69	–	
P_O = 10 W; R_L = 2 Ω		–	65	–	
Supply voltage rejection	SVR				dB
f = 100 Hz; V_{ripple} = 0.5 V; R_G = 10 kΩ; R_L = 4 Ω		30	36	–	

TYPICAL CHARACTERISTICS

FIG. 3 – QUIESCENT OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE

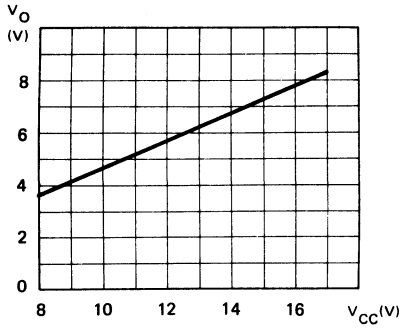


FIG. 4 – QUIESCENT DRAIN CURRENT VERSUS SUPPLY VOLTAGE

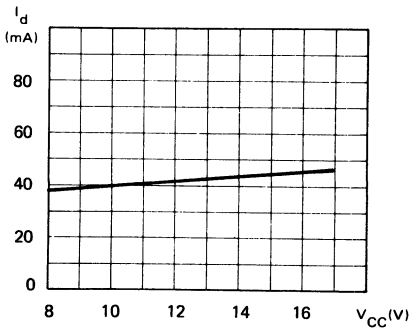


FIG. 5 – OUTPUT POWER VERSUS SUPPLY VOLTAGE

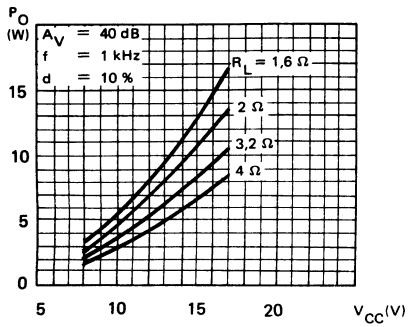
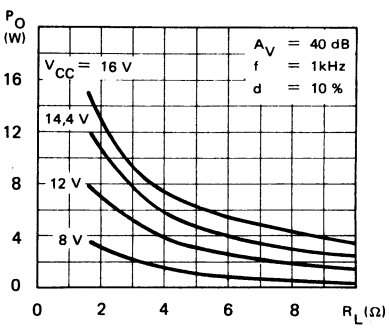


FIG. 6 – OUTPUT POWER VERSUS R_L



TYPICAL CHARACTERISTICS (continued)

FIG. 7 – GAIN VERSUS INPUT SENSITIVITY

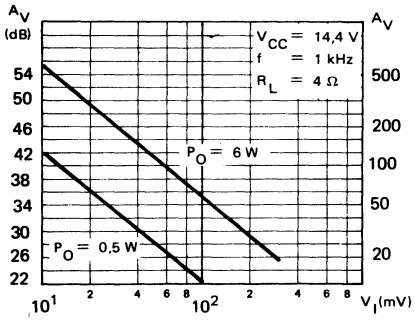


FIG. 8 – GAIN VERSUS INPUT SENSITIVITY

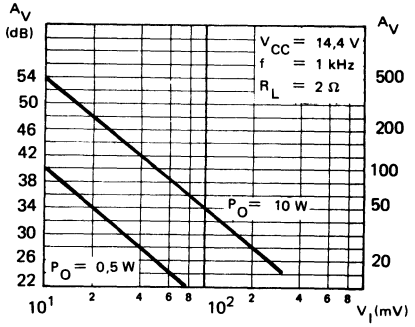


FIG. 9 – DISTORTION VERSUS OUTPUT POWER

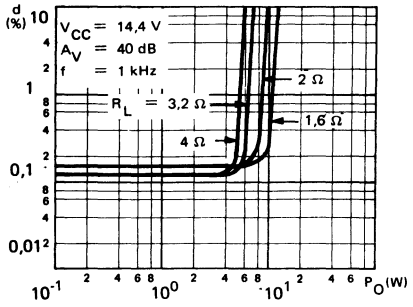


FIG. 10 – DISTORTION VERSUS FREQUENCY

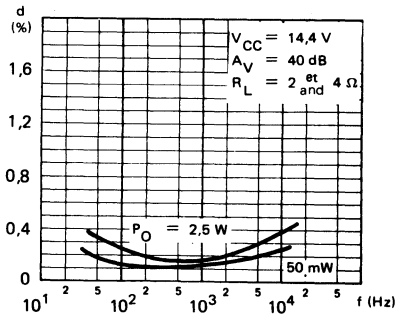


FIG. 11 – SUPPLY VOLTAGE REJECTION VERSUS VOLTAGE GAIN

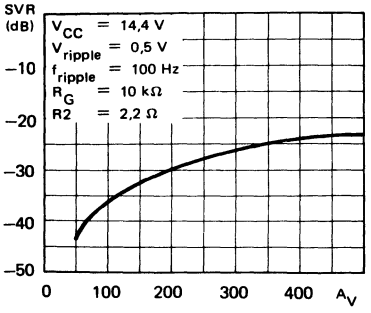
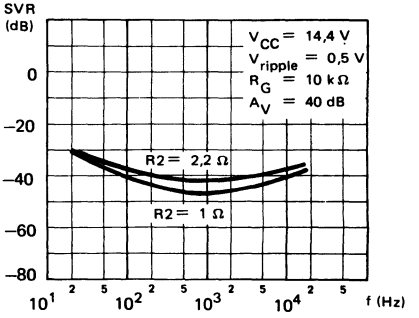


FIG. 12 – SUPPLY VOLTAGE REJECTION VERSUS FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIG. 13 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER (R_L = 4 Ω)

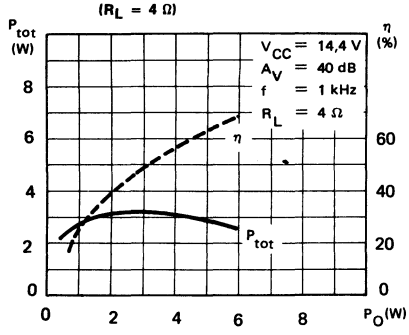


FIG. 14 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER (R_L = 2 Ω)

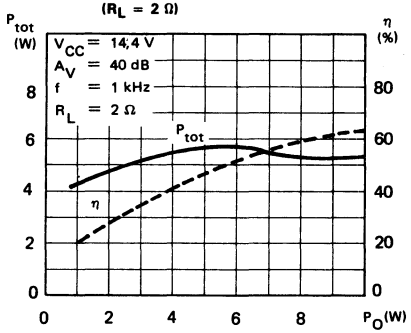


FIG. 15 – MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (SINE WAVE OPERATION)

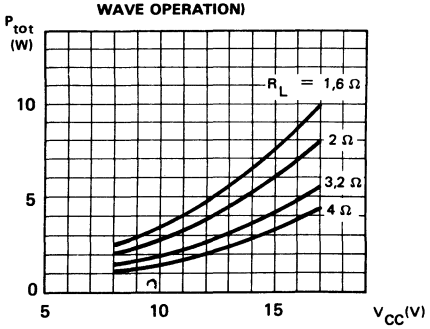


FIG. 16 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

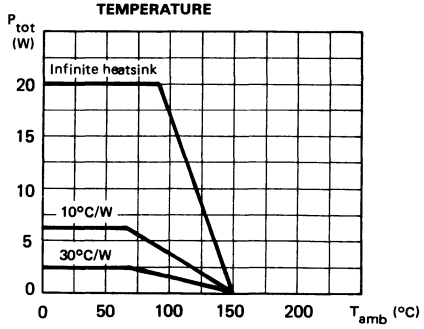


FIG. 17 – TYPICAL VALUES OF CAPACITOR (C_x) FOR DIFFERENT VALUES OF FREQUENCY RESPONSE (B)

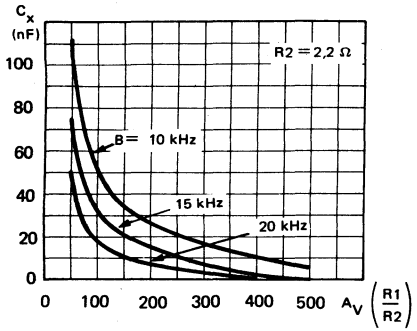
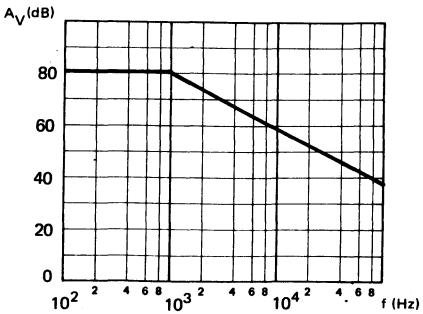


FIG. 18 – OPEN LOOP VOLTAGE GAIN VERSUS FREQUENCY



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APPLICATION INFORMATION

FIG. 19 – TYPICAL APPLICATION CIRCUIT

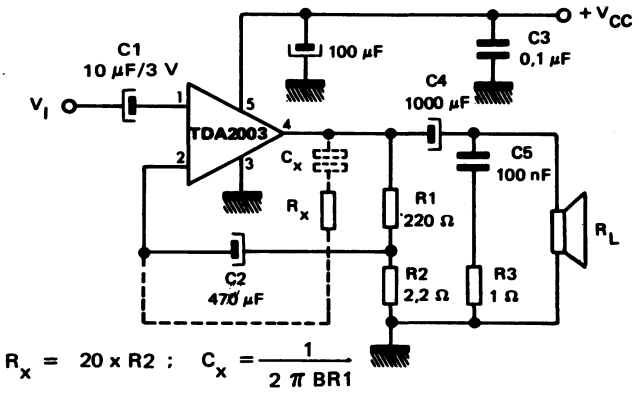
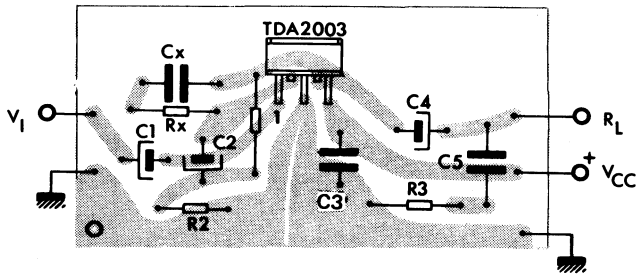
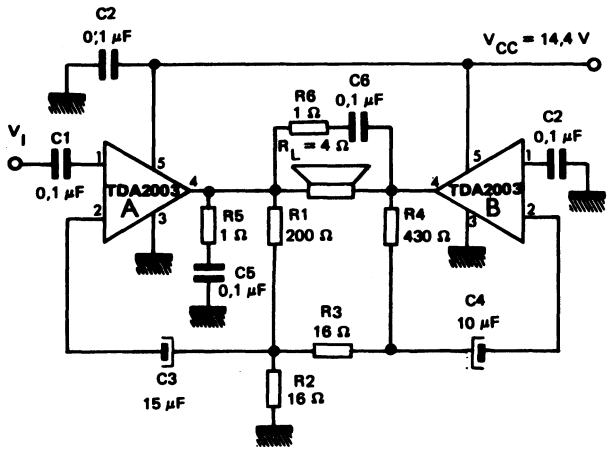


FIG. 20 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 19 (1/1 SCALE)



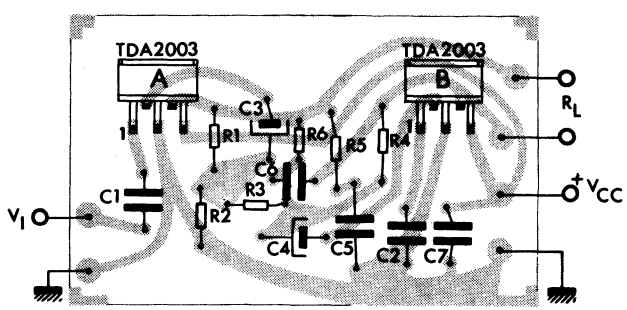
APPLICATION INFORMATION (continued)

FIG. 21 – 20 W BRIDGE CONFIGURATION APPLICATION CIRCUIT*



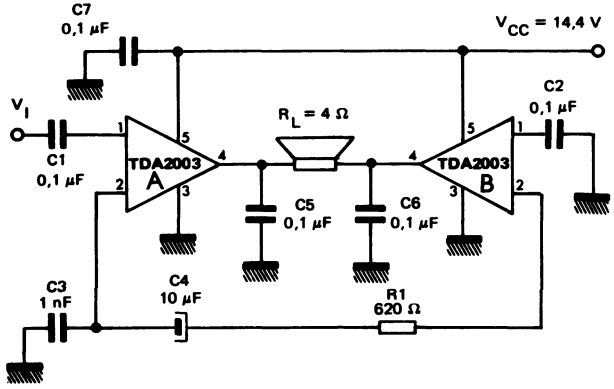
The values of the capacitors C3 and C4 are different to optimize the SVR (Typ. 40 dB)

FIG. 22 – PC BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 21 (1/1 SCALE)



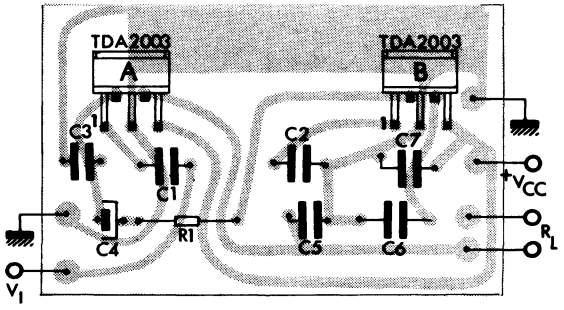
APPLICATION INFORMATION (continued)

FIG. 23 – LOW COST BRIDGE CONFIGURATION CIRCUIT (P_O = 18 W)*



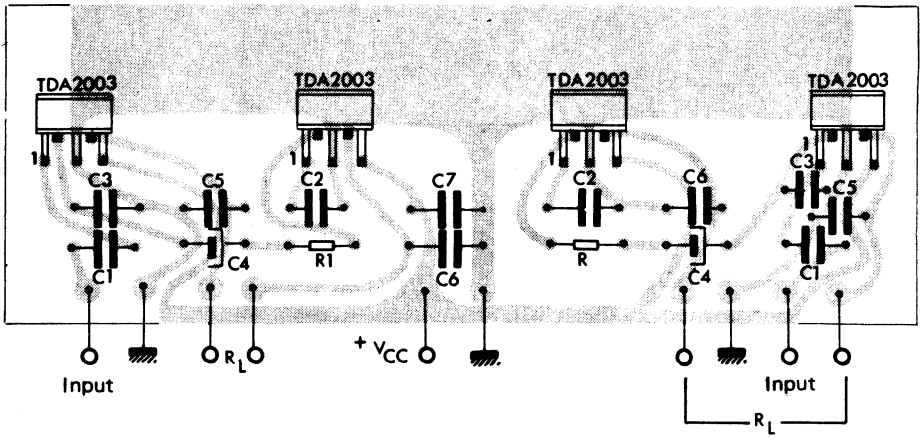
In this application the devices can support a short-circuit between every side of the loudspeaker and ground.

FIG. 24 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 23 (1/1 SCALE)



APPLICATION INFORMATION (continued)

FIG. 25 – P.C. BOARD AND COMPONENT LAYOUT FOR THE LOW-COST BRIDGE AMPLIFIER OF FIG. 23 STEREO VERSION (1/1 SCALE)



BUILT-IN PROTECTION SYSTEMS

LOAD DUMP VOLTAGE SURGE

The TDA2003 has a circuit which enables is to withstand a voltage pulse train, on pin 5, of the type shown in fig. 26.

If the supply voltage peaks to more than 40 V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig. 26.

A suggested LC network is shown in fig. 27. With this network, a train of pulses with amplitude up to 120 V and width 2 ms can be applied at point A.

Figure 26

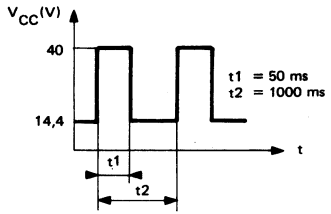
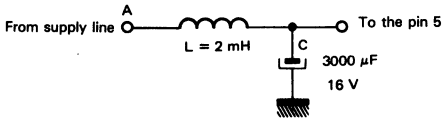


Figure 27



SHORT-CIRCUIT (AC AND DC CONDITIONS)

The TDA2003 can withstand a permanent short-circuit on the output for a supply voltage up to 16 V.

BUILT-IN PROTECTION SYSTEMS (continued)

POLARITY INVERSION

High current (up to 5 A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1 A fuse (normally connected in series with the supply). This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

OPEN GROUND

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA2003 protection diodes are included to avoid any damage.

INDUCTIVE LOAD

A protection diode is provided between pin 4 and 5 (see the internal schematic diagram) to allow use of the TDA2003 with inductive loads. In particular, the TDA2003 can drive a coupling transformer for audio modulation.

DC VOLTAGE

The maximum operating DC voltage on the TDA2003 is 18 V. However the device can withstand a DC voltage up to 28 V with to damage. This could occur during winter if two batteries are series connected to crank the engine.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1 — An overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2 — The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_O (and therefore P_{tot}) and I_d are reduced (figs. 28 and 29).

FIG. 28 — OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE

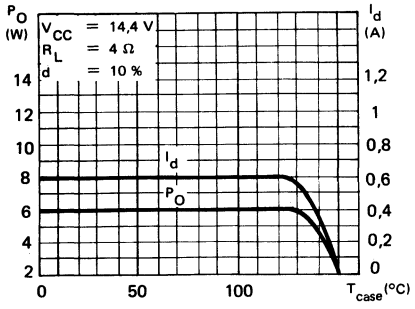
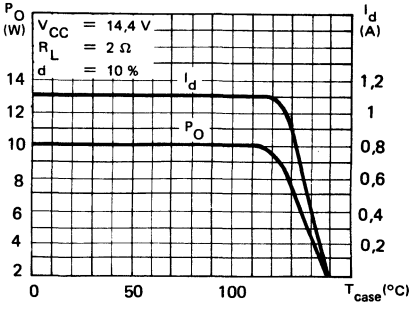


FIG. 29 — OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE



PRATICAL CONSIDERATIONS

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	10 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of SVR
C3	0,1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0,1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
C_x	$\cong \frac{1}{2\pi\ BR1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(A_V - 1) \bullet R2$	Setting of gain		Increase of drain current
R2	2,2 Ω	Setting of gain and SVR	Degradation of SVR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_x	$\cong$ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

PRINTED CIRCUIT BOARD

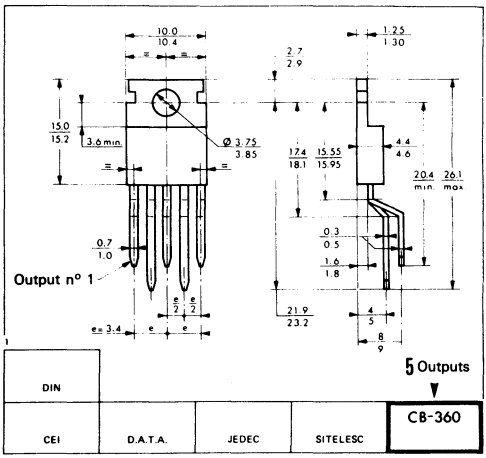
The layout shown in figure 20 is recommended. If different layours are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

ASSEMBLY SUGGESTION

The device does not require insulation between the package and the heatsink. Pin lenght should be as short as possible. The soldering temperature must not exceed 260 °C for 12 seconds.

APPLICATION SUGGESTION

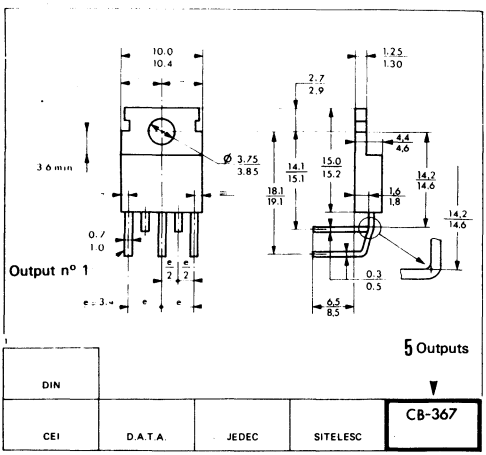
The recommended component values are those shown in the application circuits of fig. 19. Different values can be used. The following table is intended to aid the car-radio designer.



CASE

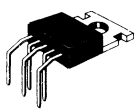
CB-360

SP SUFFIX
PLASTIC PACKAGE



CASE

CB-367



SP SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TDA2006

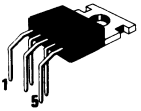
10 W AUDIO POWER AMPLIFIER WITH SHORT-CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

The TDA 2006 is a monolithic integrated circuit in CB-360 or CB-367 package intended for use as a low frequency class "B" amplifier.
Typically it provides 12 W ouput power (d = 10 %) at ± 12 V on a 4 Ω load, and 8 W on a 8 Ω.
The TDA 2006 provides high output (up to 2,5 A) and has very low harmonic and cross over distortion.
The device incorporates a short-circuit protection which automatically limits the dissipated power so as to keep the working point of the output transistors within their safe operating area.
A conventional thermal shut down system is also included.

10 W AUDIO POWER AMPLIFIER WITH SHORT-CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

CASES

CB-367



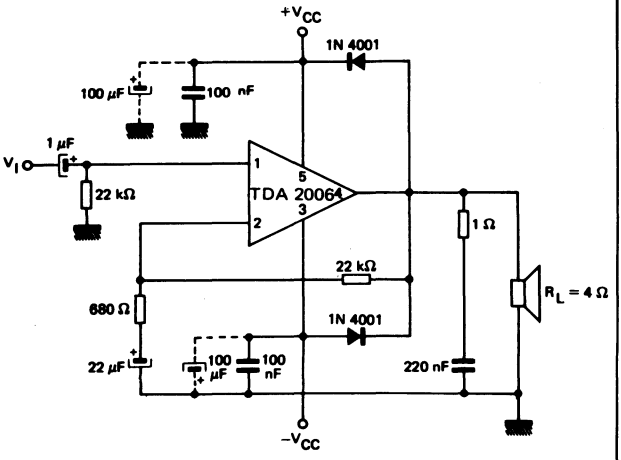
TDA2006 H

CB-360

TDA2006 V

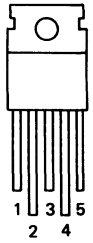
SP SUFFIX
PLASTIC PACKAGE

TEST AND APPLICATION CIRCUIT



PIN CONFIGURATION

Top view



1 Non inverting input
2 Inverting input
3 – V_{CC}
4 Output
5 + V_{CC}

Tab is connected to pin 3

NT8026-A

THOMSON SEMICONDUCTORS
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THOMSON COMPONENTS

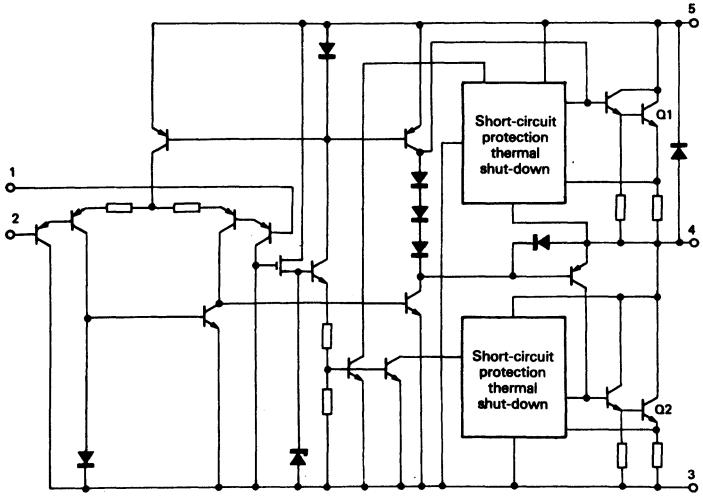
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	± 15	V
Input voltage	V_I	V_{CC}	
Differential input voltage	V_{ID}	± 12	V
Output peak current (internally limited)	I_O	3	A
Power dissipation (T_{case} = 90 °C)	P_{tot}	20	W
Junction temperature	T_j	− 40 to + 150	°C
Storage temperature	T_{stg}	− 40 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-case thermal resistance	$R_{th(j-c)}$	3 max.	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{CC} = ± 12 V; T_{amb} = 25 °C (refer to the test circuit) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	± G	–	± 15	V
Quiescent drain current (V_{CC} = ± 15 V)	I_{CC}	–	40	80	mA
Bias current (V_{CC} = ± 15 V)	I_B	–	0.2	3	μA
Input offset voltage (V_{CC} = ± 15 V)	V_{IO}	± 8	± 2	–	mV
Input offset current (V_{CC} = ± 15 V)	I_{IO}	± 80	–	–	nA
Output offset voltage (V_{CC} = ± 15 V)	V_O	–	± 10	± 100	mV
Output power (d = 10 %; Av = 30 dB; f = 1 kHz)	P_O				W
R_L = 4 Ω		–	12	–	
R_L = 8 Ω		6	8	–	
Harmonic distortion	d				%
0.1 W ≤ P_O ≤ 8 W; R_L = 4 Ω; A_V = 30 dB; f = 1 kHz		–	0.2	–	
0.1 W ≤ P_O ≤ 4 W; R_L = 8 Ω; A_V = 30 dB; f = 1 kHz		–	0.1	–	
Input sensitivity (A_V = 30 dB; f = 1 kHz)	S				mV
P_O = 10 W; R_L = 4 Ω		–	200	–	
P_O = 6 W; R_L = 8 Ω		–	220	–	
Bandwidth (– 3 dB)	B				Hz
A_V = 30 dB; P_O = 8 W; R_L = 4 Ω			10 to 140.000		
Input resistance Pin 1	R_I	0.5	5	–	MΩ
Voltage gain (f = 1 kHz)	A_V				dB
Open loop		–	75	–	
Closed loop		29.5	30	30.5	
Input noise voltage (R_L = 4 Ω)	V_n				μV
Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz		–	3	10	
Input noise current (R_L = 4 Ω)	i_n				pA
Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz		–	80	200	
Supply voltage rejection ratio	SVR				dB
R_L = 4 Ω; A_V = 30 dB; R_G = 22 kΩ; V_{ripple} = 0.5 V_{eff} f_{ripple} = 100 Hz		40	50	–	
Drain current	I_{CC}				mA
P_O = 12 W; R_L = 4 Ω		–	845	–	
P_O = 8 W; R_L = 8 Ω		–	490	–	
Thermal shut-down case temperature (P_{tot} = 9 W)	T_{case}	110	–	–	°C

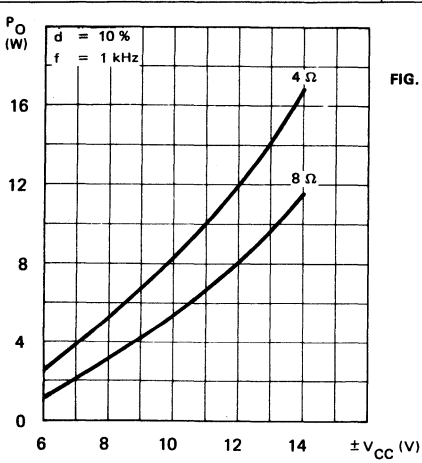


FIG. 1 – TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

FIG. 2 – DISTORTION VERSUS OUTPUT POWER

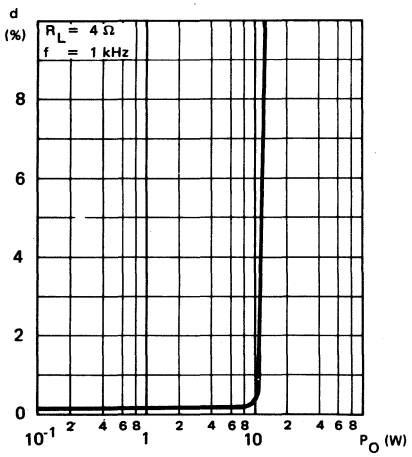


FIG. 3 – TYPICAL DISTORTION VERSUS OUTPUT POWER

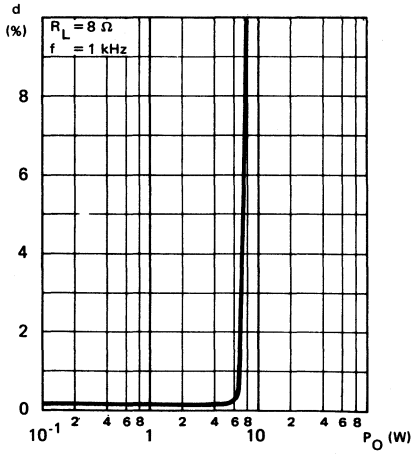


FIG. 4 – TYPICAL DISTORTION VERSUS FREQUENCY

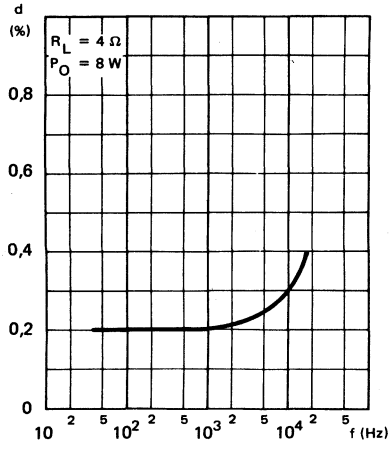


FIG. 5 – TYPICAL DISTORTION VERSUS FREQUENCY

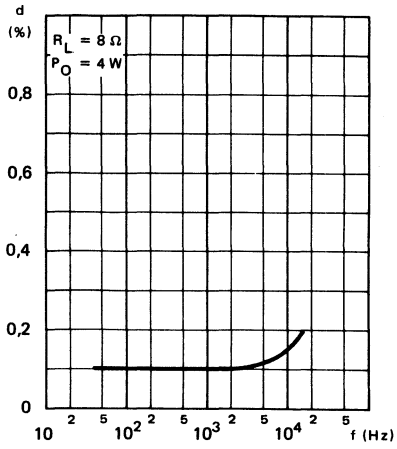


FIG. 6 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

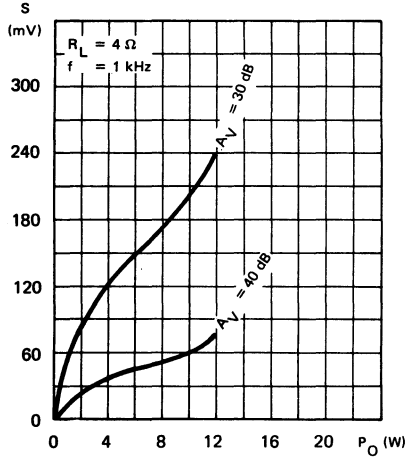


FIG. 7 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

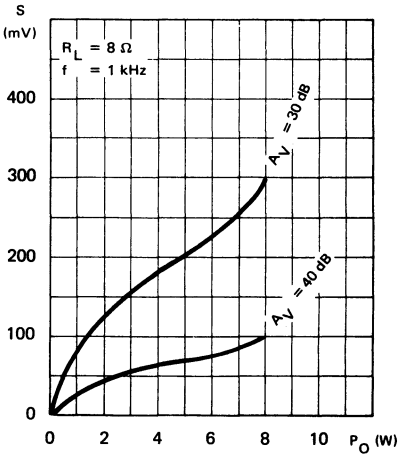


FIG. 8 – FREQUENCY RESPONSE WITH DIFFERENT VALUES OF THE ROLLOFF CAPACITOR C8 (see Fig. 14)

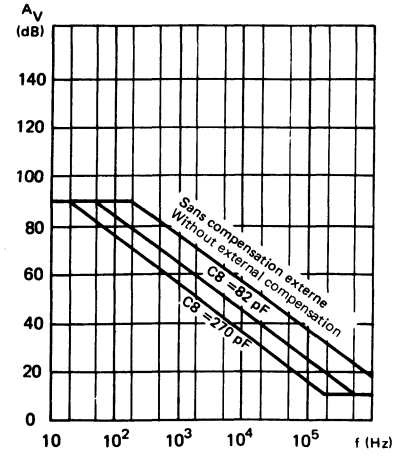


FIG. 9 – TYPICAL VALUE OF C8 VERSUS VOLTAGE GAIN FOR DIFFERENT BANDWIDTHS (see Fig. 14)

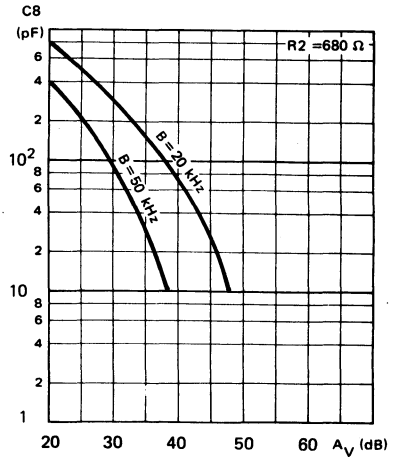


FIG. 10 – QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE

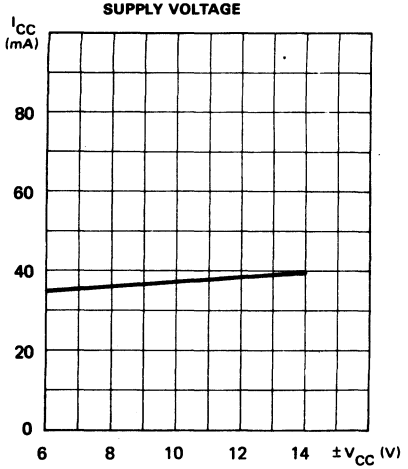


FIG. 11 – SUPPLY VOLTAGE REJECTION RATIO VERSUS VOLTAGE GAIN

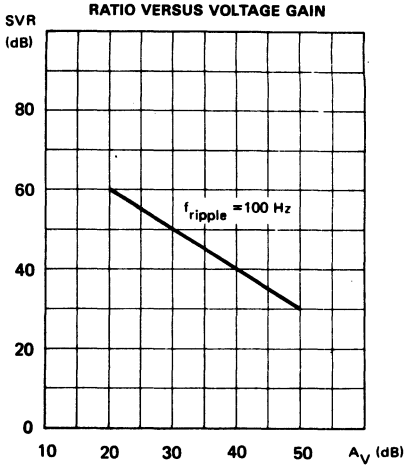


FIG. 12 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

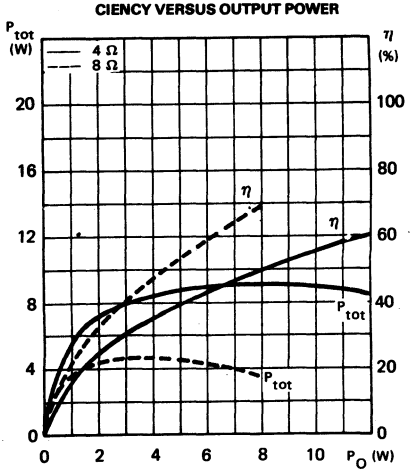


FIG. 13 – MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (sine wave operation)

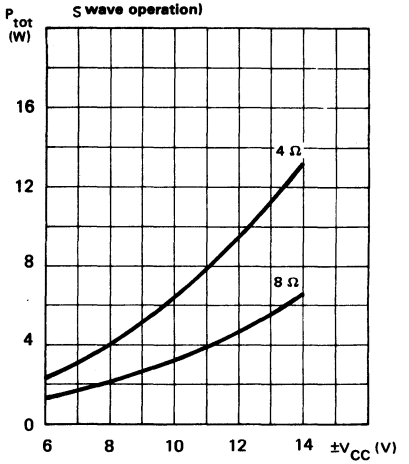
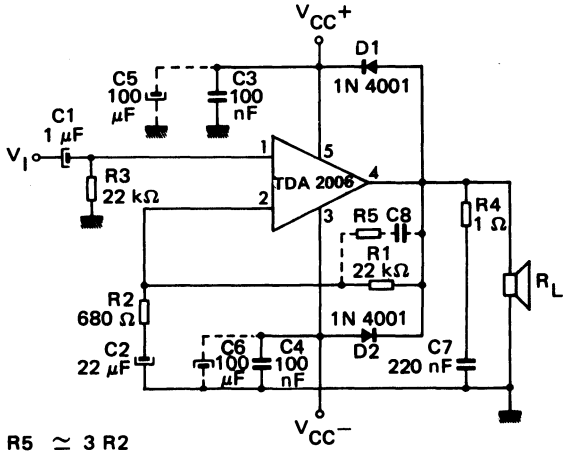


FIG. 14 – TYPICAL AMPLIFIER WITH SPLIT POWER SUPPLY



R5 ≃ 3 R2
C8 = See Figure 9

FIG. 15 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 14

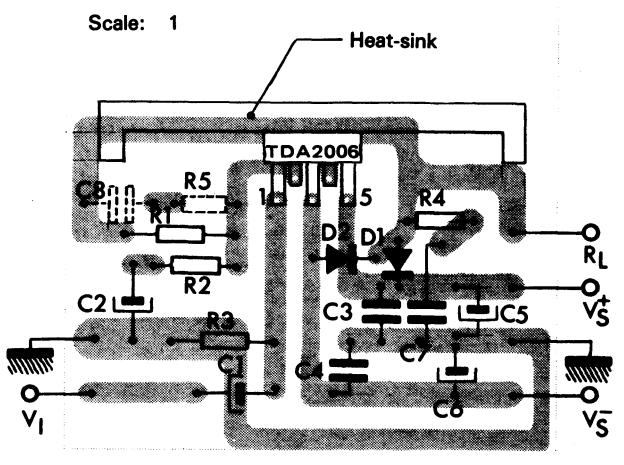


FIG. 16 – TYPICAL AMPLIFIER WITH SINGLE POWER SUPPLY

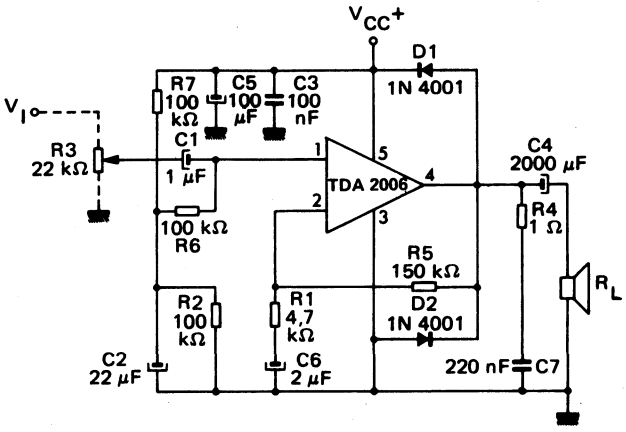


FIG. 17 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 15

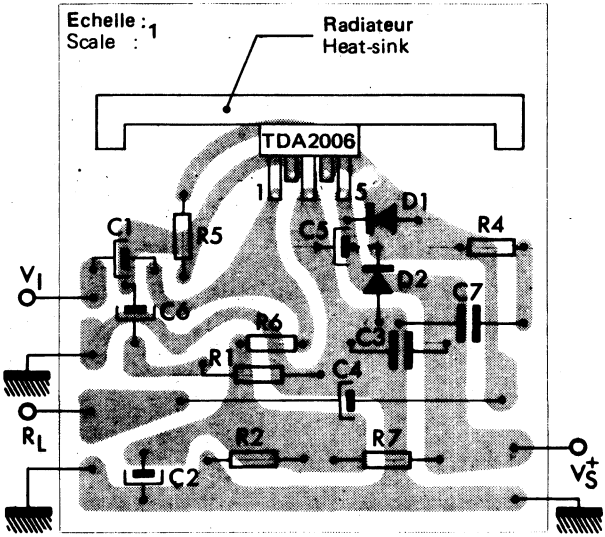
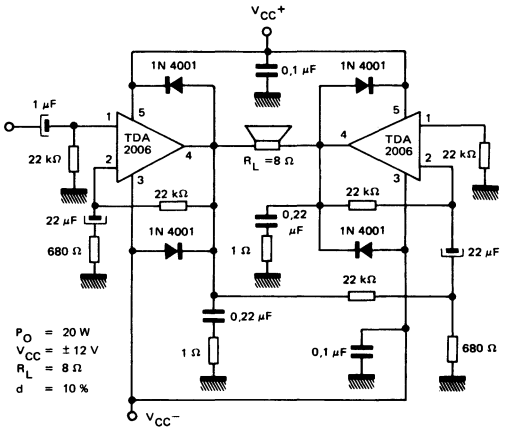


FIG. 18 – TYPICAL BRIDGE AMPLIFIER CONFIGURATION WITH SPLIT POWER SUPPLY



SHORT-CIRCUIT PROTECTION

The TDA 2006 has an internal circuit which limits the currents of the output transistors.

Figure 19 shows that the maximum output current is a function of the collector emitter voltage.

Hence, the output transistors work within their safe operating area (figure 20).

This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2006 is thus protected against temporary over-loads or short-circuit. Should the short-circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

FIG. 19 – MAXIMUM OUTPUT CURRENT VERSUS VOLTAGE (V_{CE}) ACROSS EACH OUTPUT TRANSISTOR

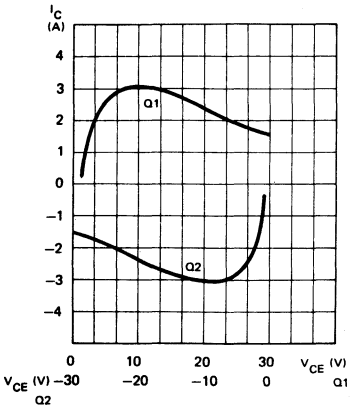
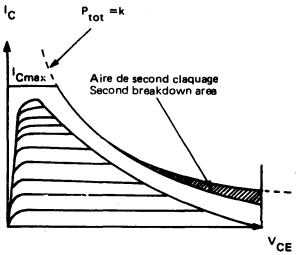


FIG. 20 – SAFE OPERATIONS AREA AND COLLECTOR CHARACTERISTIC OF THE PROTECTED POWER TRANSISTOR



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1 – An overload on the output, even if it is permanent, or an above limit ambient temperature can be easily supported since the junction temperature cannot be higher than 150 °C.

2 – The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply reduces the power dissipation and the current consumption.

FIG. 21 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE (R_L = 4 Ω)

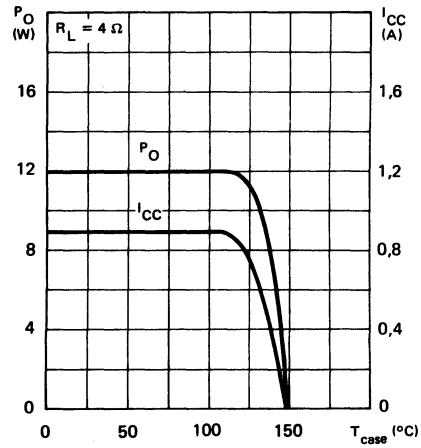
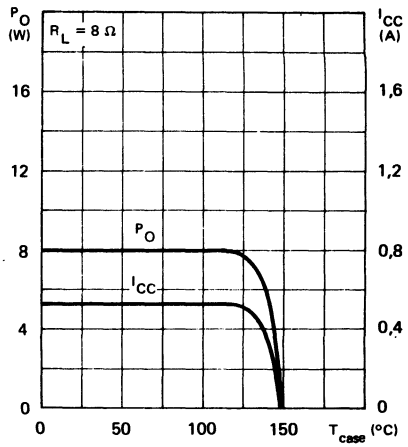


FIG. 22 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE (R_L = 8 Ω)



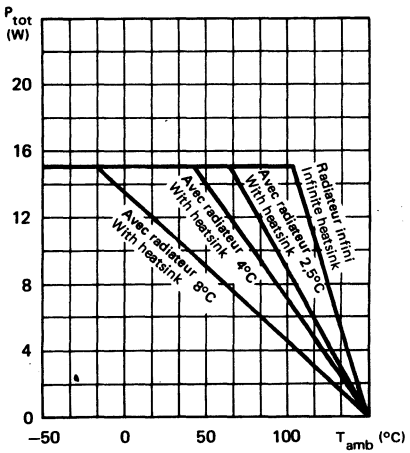


FIG. 23 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); figure 23 shows this dissipable power as a function of ambient temperature for different thermal resistances.

PRACTICAL CONSIDERATIONS

PRINTED CIRCUIT BOARD

The layout in figure 16 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

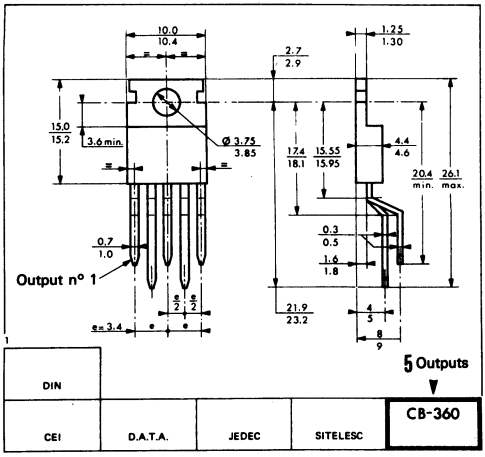
ASSEMBLY SUGGESTION

No electrical isolation needs be used between the package and the heatsink with single supply voltage configuration.

EXTERNAL COMPONENTS

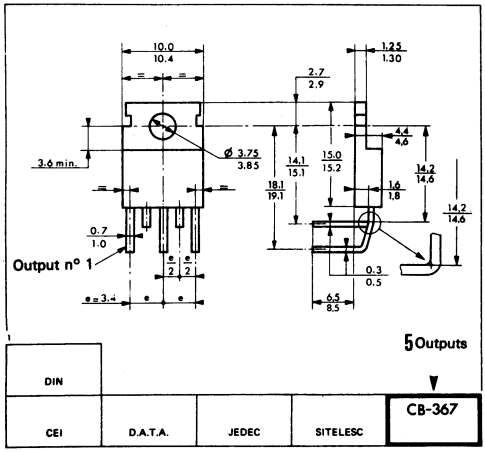
The recommended values of the external components are those shown on application circuit of figure 16. Different values can be used. The following table can help the designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain
R2	680 Ω	Closed loop gain setting	Decrease of gain	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R5	≅ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 μF	Inverting DC decoupling		Increase of low frequencies cutoff
C3, C4	0,1 μF	Supply voltage bypass		Danger of oscillation
C5, C6	100 μF	Supply voltage bypass		Danger of oscillation
C7	0,22 μF	Frequency stability		Danger of oscillation
C8	$\cong \frac{1}{2\pi\ BR1}$	Upper frequency cutoff	Small bandwidth	Larger bandwidth
D1, D2	1N 4001 t_{fr} = 1 μs / V_F = 1,1 V − I_F = 1 A		To protect the device against output voltage spikes	

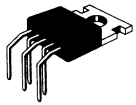


CASE CB-360

SP SUFFIX
PLASTIC PACKAGE



CASE CB-367



SP SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

12/12

THOMSON SEMICONDUCTORS

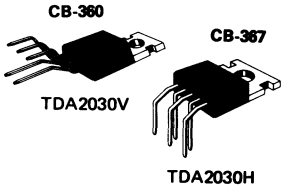
TDA2030V
TDA2030H

12 W HI-FI AUDIO POWER AMPLIFIER WITH SHORT-CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

The TDA 2030 is a monolithic integrated circuit in CB-360 and/or CB-367 packages intended for use as a low frequency class "B" amplifier.
Typically it provides 14 W ouput power (d = 0.5 %) at ± 14 V/4 Ω; at ± 14 V the guaranteed output power is 12 W on a 4 Ω load and 8 W on a 8 Ω (DIN 45500).
The TDA 2030 provides high output current (up to 3 A) and has very low harmonic and cross over distortion.
This device incorporates a short-circuit protection which automatically limits the dissipated power so as to keep, the working point of the output transistors within their safe operating area.
A conventional thermal shut down system is also included.

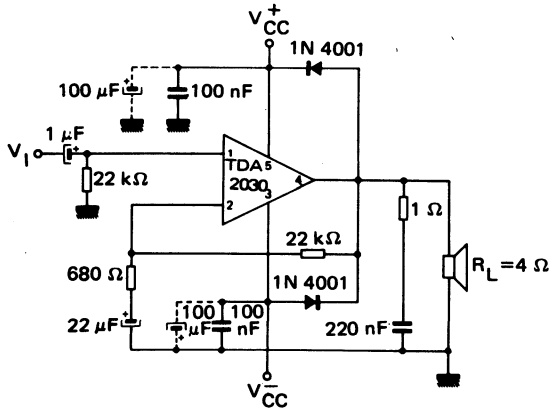
12 W HI-FI AUDIO POWER AMPLIFIER WITH SHORT-CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

CASES



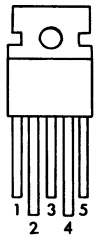
SP SUFFIX
PLASTIC PACKAGE

TEST AND APPLICATION CIRCUIT



PIN CONFIGURATION

Top view



1 Non inverting input
2 Inverting input
3 − V_{CC}
4 Output
5 + V_{CC}

NT8108-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

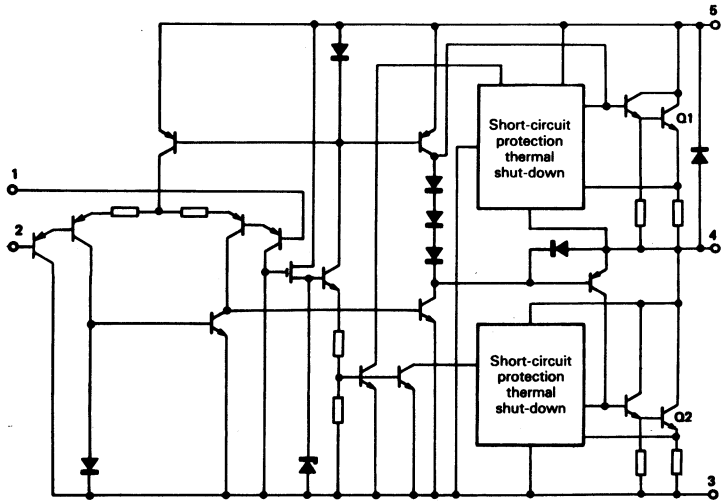
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	± 18	V
Input voltage	V_I	V_{CC}	
Differential input voltage	V_{ID}	± 15	V
Output peak current (internally limited)	I_O	3.5	A
Power dissipation T_{case} = 90 °C	P_{tot}	20	W
Junction temperature	Tj	− 40 °C, + 150	°C
Storage temperature	T_{stg}	− 40 °C, + 150	°C

THERMAL CHARACTERISTICS

Test conditions	Symbol	Value	Unit
Junction-case thermal resistance	$R_{th(j-c)}$	3	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{CC} = ± 14 V; T_{amb} = 25 °C (refer to the test circuit) (Unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	± 6	–	± 18	V
Quiescent drain current (V_{CC} = ± 18 V)	I_{CC}	–	40	60	mA
Bias current (V_{CC} = ± 18 V)	I_B	–	0.2	2	μA
Input offset voltage (V_{CC} = ± 18 V)	V_{IO}	–	± 2	± 20	mV
Input offset current (V_{CC} = ± 18 V)	I_{IO}	–	± 20	± 200	nA
Output offset voltage (V_{CC} = ± 18 V)	V_O	–	± 2.5	± 22	mV
Output power	P_O				W
d = 0.5 %; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz					
R_L = 4 Ω		12	14	–	
R_L = 8 Ω		8	9	–	
d = 10 %; A_V = 30 dB; f = 1 kHz					
R_L = 4 Ω		–	18	–	
R_L = 8 Ω		–	11	–	
Harmonic distortion	d				%
0.1 W ⩽ P_O ⩽ 12 W; R_L = 4 Ω; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz		–	0.2	0.5	
0.1 W ⩽ P_O ⩽ 8 W; R_L = 8 Ω; A_V = 30 dB; 40 Hz ⩽ f ⩽ 15 kHz		–	0.1	0.5	
Input sensitivity (A_V = 30 dB; f = 1 kHz)	S				mV
P_O = 12 W; R_L = 4 Ω		–	215	–	
P_O = 8 W; R_L = 8 Ω		–	250	–	
Bandwidth (– 3 dB)	B				Hz
A_V = 30 dB; P_O = 12 W: R_L = 4 Ω			10 to 140.000		
Input resistance Pin 1	R_I	0.5	5	–	MΩ
Voltage gain (f = 1 kHz)	A_V				dB
Open loop		–	90	–	
Closed loop		29.5	30	30.5	
Input noise voltage (R_L = 4 Ω)	V_n				μV
Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz		–	3	10	
Input noise current (R_L = 4 Ω)	i_n				pA
Test equipment bandwith (– 3 dB) = 10 to 25.000 Hz		–	80	200	
Supply voltage rejection ratio	SVR				dB
R_L = 4 Ω; A_V = 30 dB; R_G = 22 kΩ; V_{ripple} = 0.5 V_{eff} f_{ripple} = 100 Hz		40	50	–	
Drain current	I_{CC}				mA
P_O = 14 W; R_L = 4 Ω		–	900	–	
P_O = 9 W; R_L = 8 Ω		–	515	–	
Thermal shut-down case temperature (P_{tot} = 12 W)	T_{case}	110	–	–	°C

FIG. 1 – TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

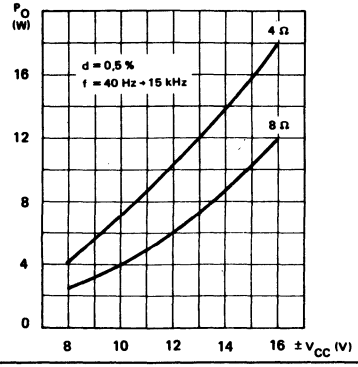


FIG. 2 – TYPICAL OUTPUT POWER VERSUS SUPPLY VOLTAGE

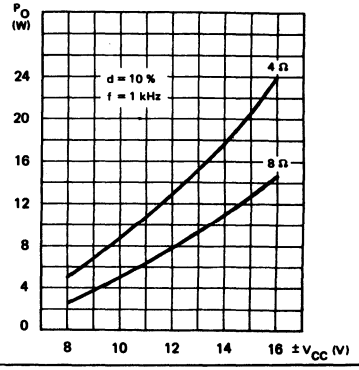


FIG. 3 – TYPICAL DISTORTION VERSUS OUTPUT POWER

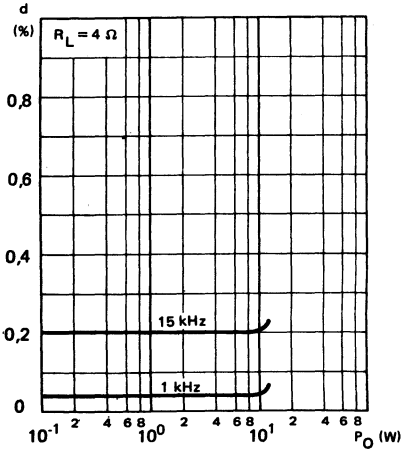


FIG. 4 – TYPICAL DISTORTION VERSUS OUTPUT POWER

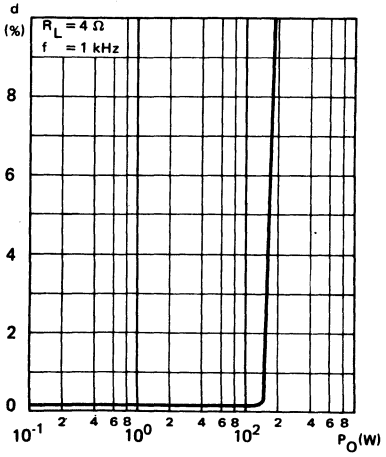


FIG. 5 – TYPICAL DISTORTION VERSUS OUTPUT POWER

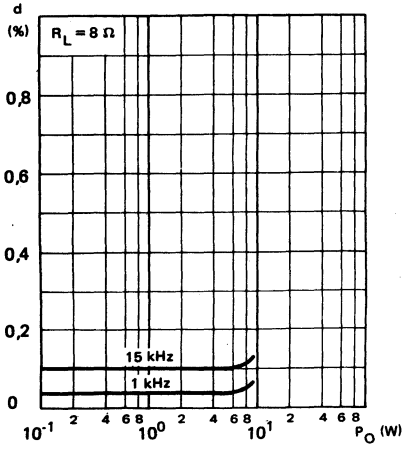


FIG. 6 – TYPICAL DISTORTION VERSUS OUTPUT POWER

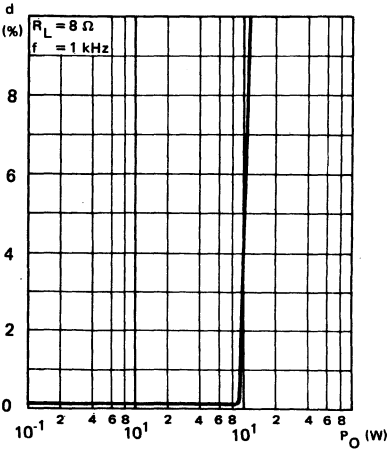


FIG. 7 – TYPICAL DISTORTION VERSUS FREQUENCY

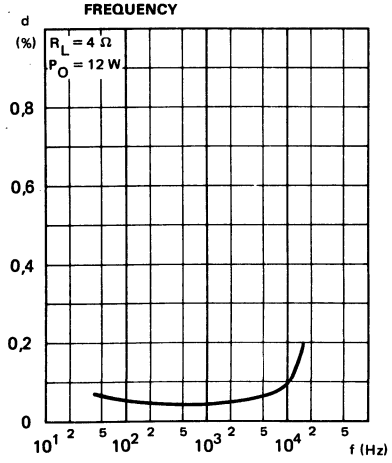


FIG. 8 – TYPICAL DISTORTION VERSUS FREQUENCY

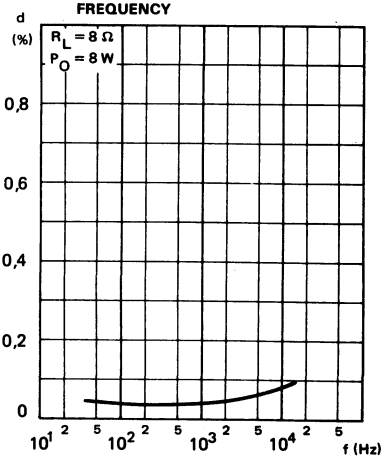


FIG. 9 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

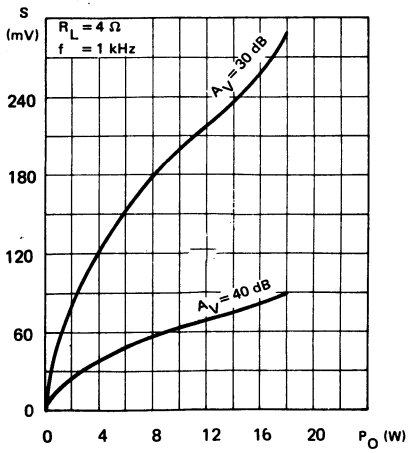


FIG. 10 – TYPICAL SENSITIVITY VERSUS OUTPUT POWER

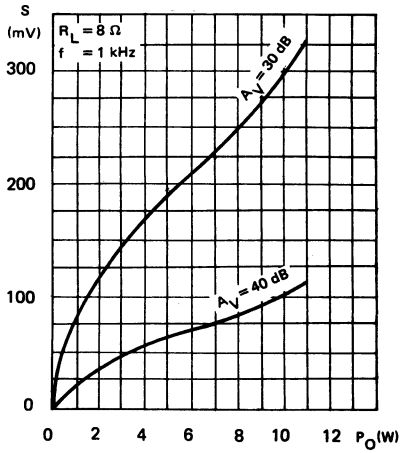


FIG. 11 – FREQUENCY RESPONSE WITH DIFFERENT VALUES OF THE ROLLOFF CAPACITOR C8 (SEE FIG. 17)

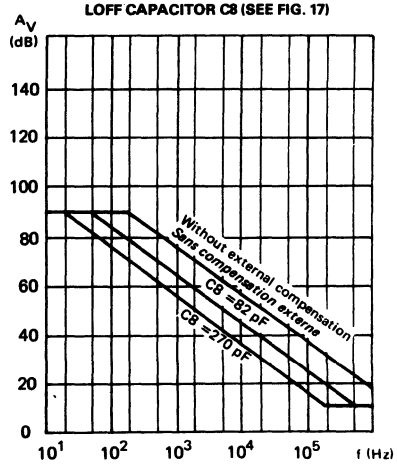


FIG. 12 – TYPICAL VALUE OF C8 VERSUS VOLTAGE GAIN FOR DIFFERENT BANDWIDTHS (SEE FIG. 17)

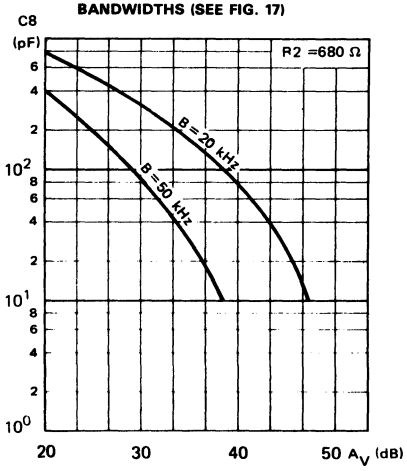


FIG. 13 – QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE

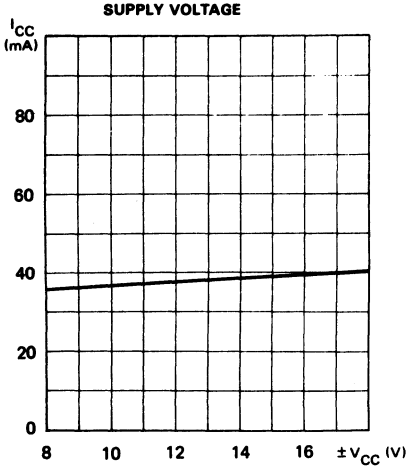


FIG. 14 – SUPPLY VOLTAGE REJECTION RATIO VERSUS VOLTAGE GAIN

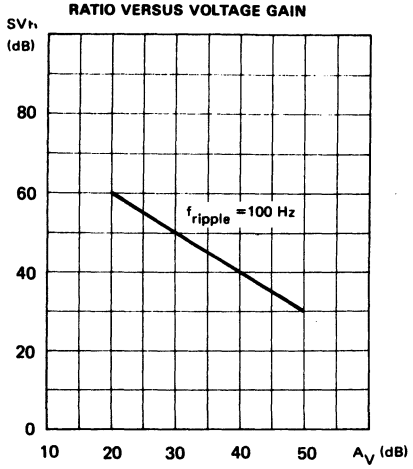


FIG. 15 – POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

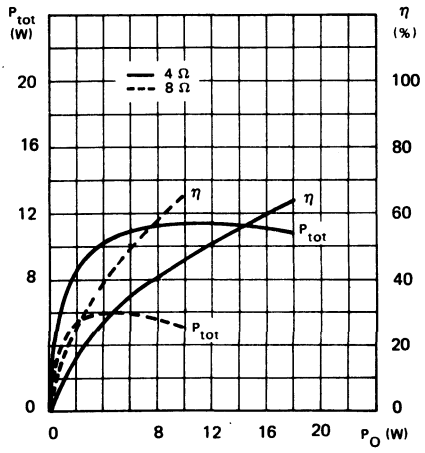


FIG. 16 – MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (SINE WAVE OPERATION)

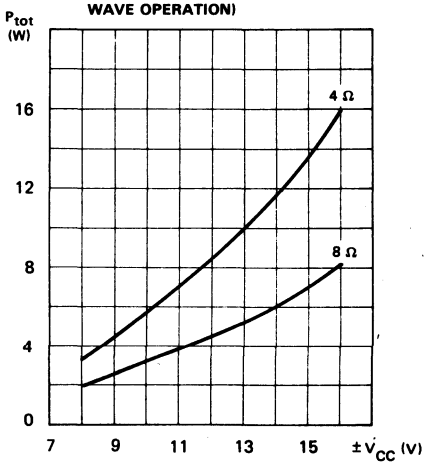
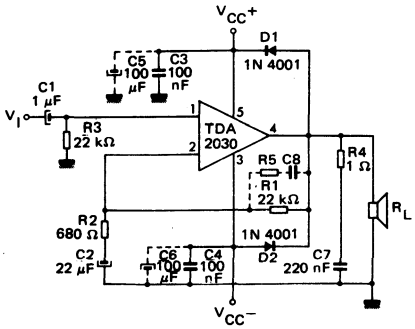


FIG. 17 – TYPICAL AMPLIFIER WITH SPLIT POWER SUPPLY



R5 ≃ 3 R2
C8 = See figure 12

FIG. 18 – TYPICAL AMPLIFIER WITH SINGLE POWER SUPPLY

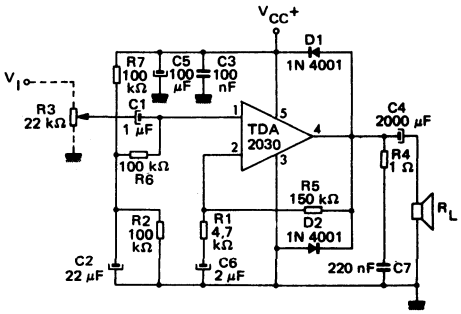


FIG. 19 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 17

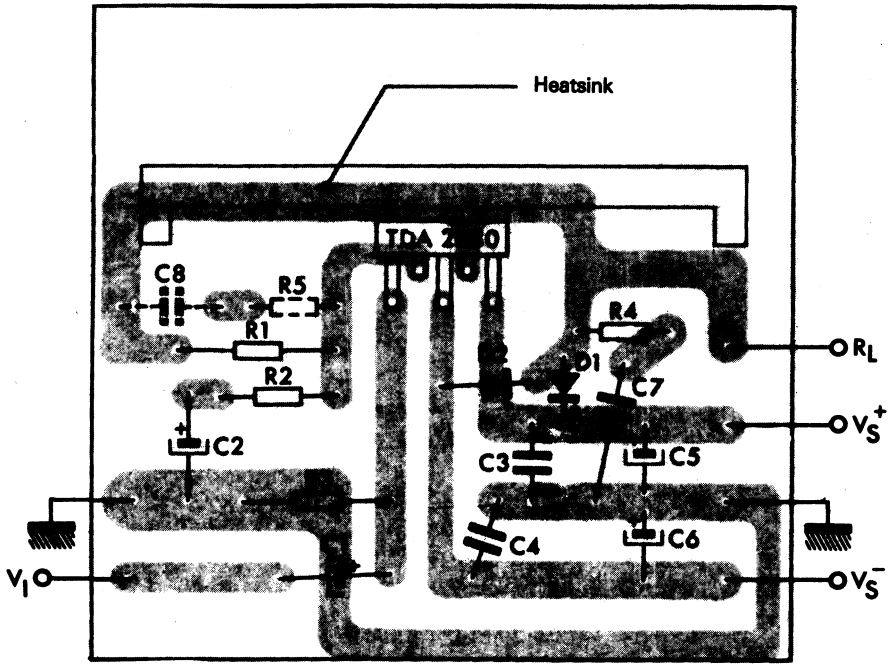


FIG. 20 – P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 18

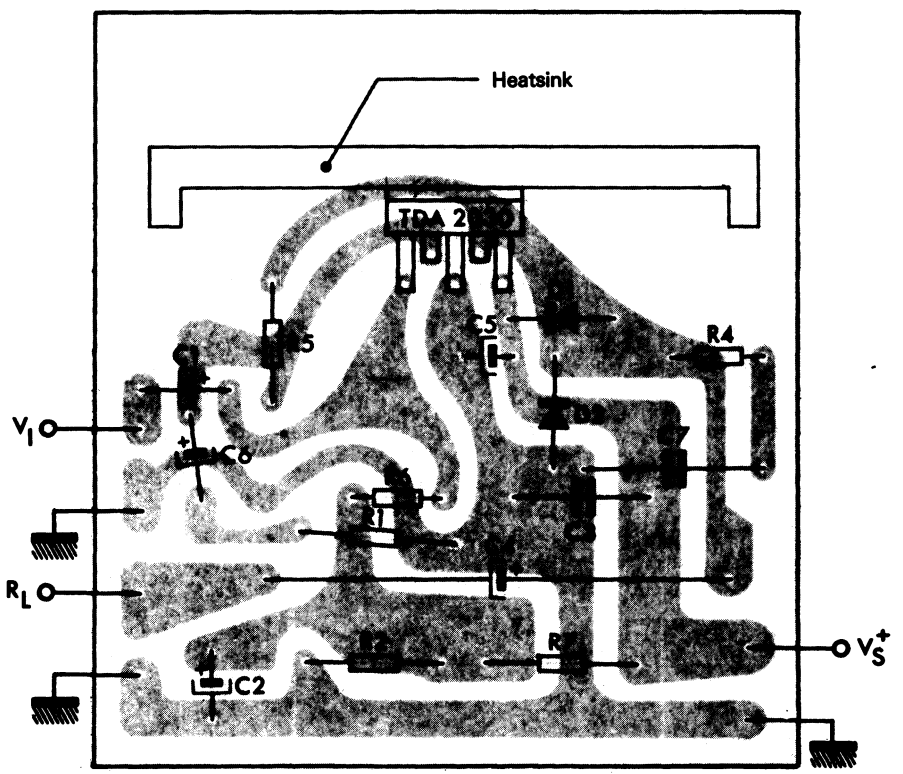
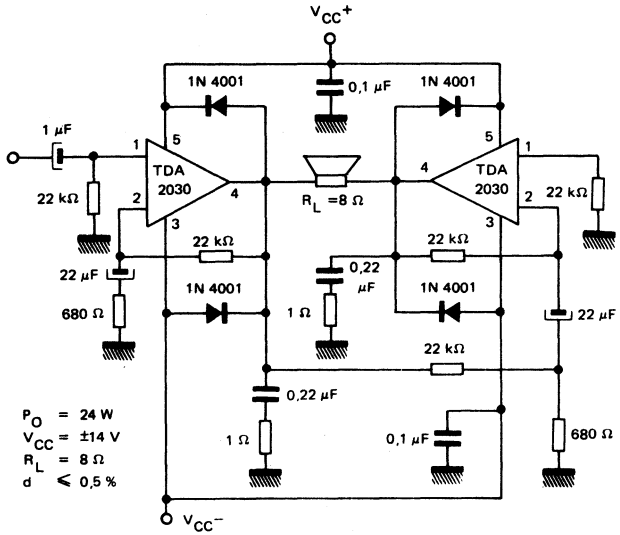


FIG. 21 – TYPICAL BRIDGE AMPLIFIER CONFIGURATION WITH SPLIT POWER SUPPLY



SHORT-CIRCUIT PROTECTION

The TDA 2030 has an internal circuit which limits the currents of the output transistors.

Figure 22 shows that the maximum output current is a function of the collector emitter voltage.

Hence, the output transistors work within their safe operating area (figure 23).

This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2030 is thus protected against temporary over-loads or short-circuit. Should the short-circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

FIG. 22 – MAXIMUM OUTPUT CURRENT VERSUS VOLTAGE (V_{CE}) ACROSS EACH OUTPUT TRANSISTOR

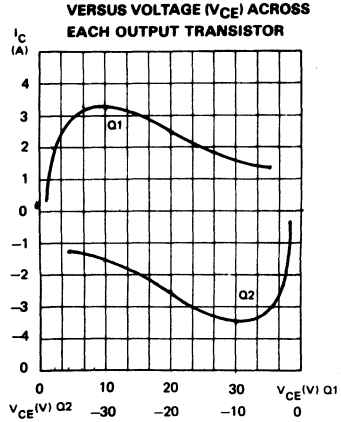
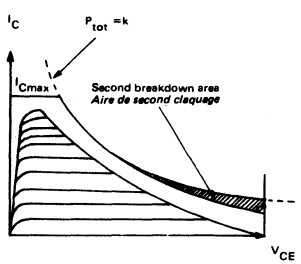


FIG. 23 – SAFE OPERATIONS AREA AND COLLECTOR CHARACTERISTICS OF THE PROTECTED POWER TRANSISTOR



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1 – An overload on the output (even if it is permanent) or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150 °C.

2 – The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply reduces the power dissipation and the current consumption.

FIG. 24 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE (R_L = 4 Ω)

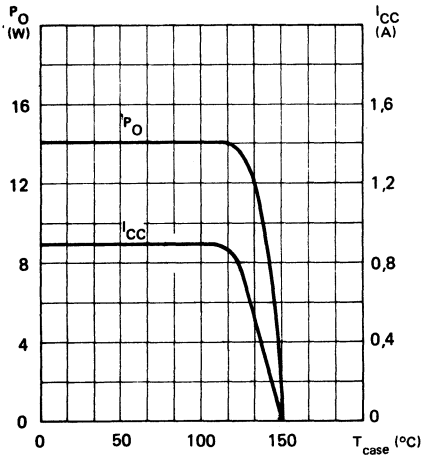


FIG. 25 – OUTPUT POWER AND DRAIN CURRENT VERSUS CASE TEMPERATURE (R_L = 8 Ω)

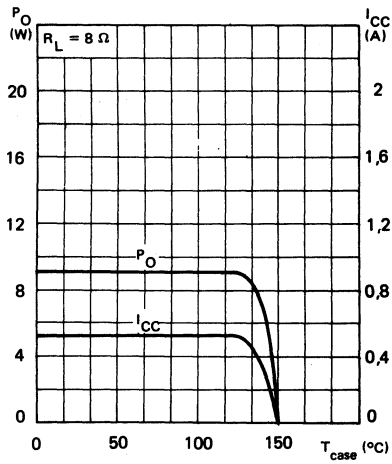
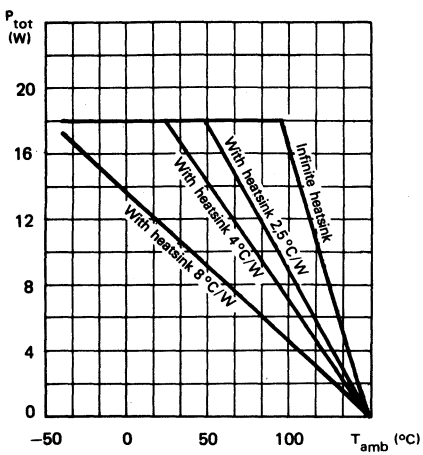


FIG. 26 – MAXIMUM ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); figure 26 shows this dissipable power as a function of ambient temperature for different thermal resistance.

PRACTICAL CONSIDERATIONS

PRINTED CIRCUIT BOARD

The layout in figure 19 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

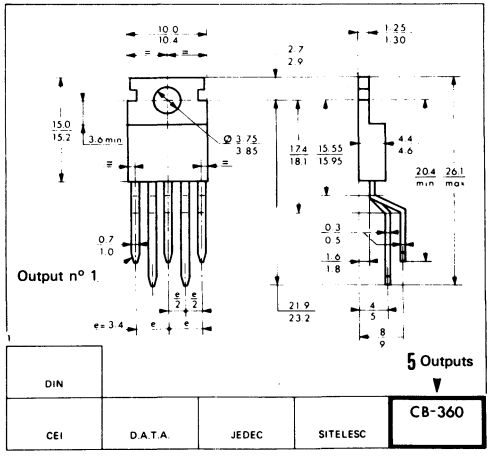
ASSEMBLY SUGGESTION

No electrical isolation needs be used between the package and the heatsink with single supply voltage configuration.

EXTERNAL COMPONENTS

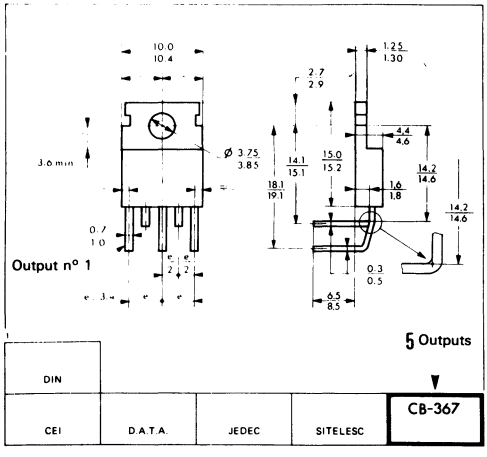
The recommended values of the external components are those shown on application circuit of figure 17. Different values can be used. The following table can help the designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain
R2	680 Ω	Closed loop gain setting	Decrease of gain	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R5	≅ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 μF	Inverting DC decoupling		Increase of low frequencies cutoff
C3, C4	0,1 μF	Supply voltage bypass		Danger of oscillation
C5, C6	100 μF	Supply voltage bypass		Danger of oscillation
C7	0,22 μF	Frequency stability		Danger of oscillation
C8	$\cong \frac{1}{2\pi\ BR1}$	Upper frequency cutoff	Small bandwidth	Larger bandwidth
D1, D2	1N 4001 t_{fr} = 1 μs / V_F = 1,1 V − I_F = 1 A		To protect the device against output voltage spikes	

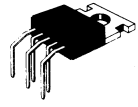


CASE CB-360

SP SUFFIX
PLASTIC PACKAGE



CASE CB-367



SP SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TEA2021

7 W AUDIO AMPLIFIER

The TEA2021 is a monolithic integrated circuit designed for classe B audio amplification, with up to 7 W output power : it is internally protected against overheating.
It provides the advantages following :

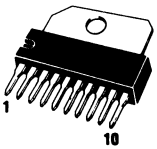
- The idling current stability obtained from a built-in temperature and voltage-compensating network makes thermal runaway impossible
- High open-loop gain.
- The use of PNP transistors in the preamplifier allows DC input voltage to be zero.
- Others highlights include : few external components
  . simple heatsinking
  . space and cost saving.

- High output power : 7 W at $V_{CC} = 16$ V, $R_L = 4\ \Omega$
- Low noise
- High supply voltage ripple rejection
- Load dump protection up to 40 V

The circuit is protected against overheating, output short-circuits ($V_{CC} = 15$ V), polarity inversion and fortuitous open ground.

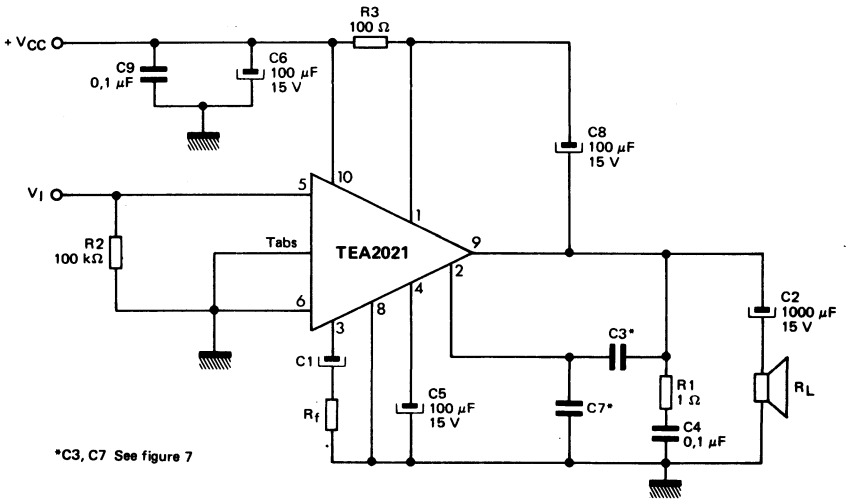
7 W AUDIO AMPLIFIER

CASE CB-313



SP SUFFIX
PLASTIC PACKAGE

SCHEMATIC



*C3, C7 See figure 7

NT8318-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

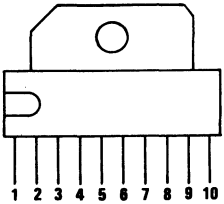
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak supply voltage (50 ms)	V_{CC}	40	V
DC supply voltage	V_{CC}	28	V
Supply voltage	V_{CC}	20	V
Peak output current (non repetitive)	I_O	4	A
Peak output current (repetitive)	I_O	3	A
Junction temperature	T_j	- 40,+ 150	°C
Storage temperature	T_{stg}	- 40,+ 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-case thermal resistance	$R_{th(j-c)}$	10	°C/W
Junction ambient thermal resistance	$R_{th(j-a)}$	55	°C/W

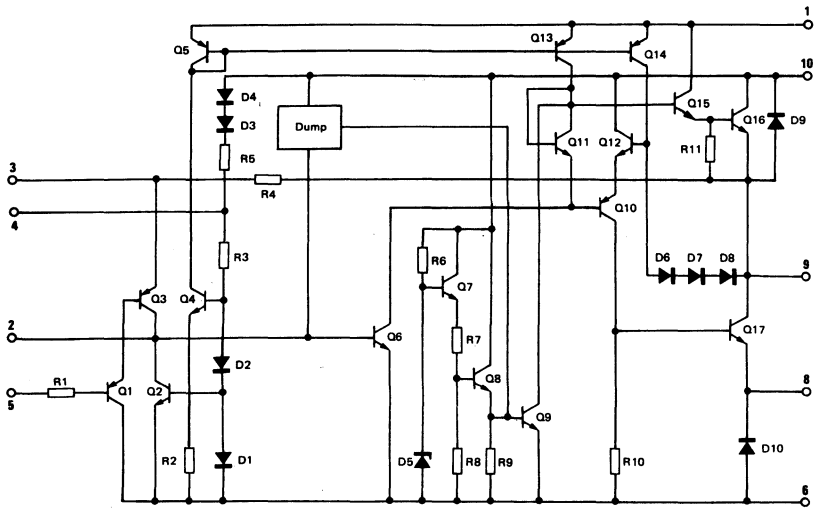
PIN CONFIGURATION



1	Bootstrap
2	Compensation
3	Feed-back network
4	Ripple rejection
5	Input

6	Preamplifier ground and substrate
7	No to be used
8	Output stage ground
9	Output
10	Supply voltage V_{CC}

ELECTRICAL DIAGRAM



ELECTRICAL CHARACTERISTICS

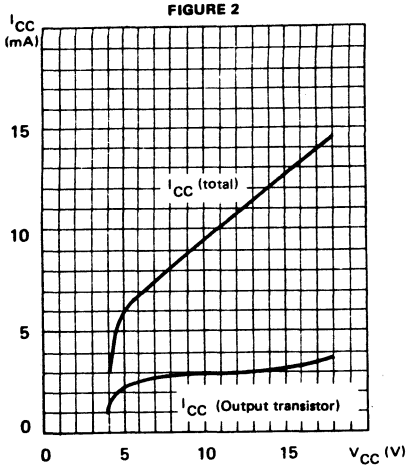
$T_{amb} = +25°C$ Note 1 $V_{CC} = 14.4$ V (Unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply voltage	Pin 10	V_{CC}	4	–	20	V
Quiescent output voltage (V_{CC} = 14.4 V)	Pin 9	V_O	6.4	7.2	8	V
Quiescent current (V_{CC} = 14.4 V)	Pin 10	I_{CC}	–	12	20	mA
Bias current (V_{CC} = 14.4 V)	Pin 5	I_B	–	0.4	–	µA
Output power (d = 10 % ; f = 1 KHz)		P_O				W
V_{CC} = 14.4 V ; R_L = 4 Ω			5.5	6	–	
V_{CC} = 13.2 V ; R_L = 3.2 Ω			–	5.8	–	
Input voltage saturation (sine wave)		V_{Irms}	220	–	–	mV
Sensitivity (f = 1 KHz)		S				mV
P_O = 6 W ; V_{CC} = 14.4 V ; R_L = 4 Ω ; R_f = 56 Ω			–	75	–	
P_O = 6 W ; V_{CC} = 14.4 V ; R_L = 4 Ω ; R_f = 22 Ω			–	30	–	
P_O = 5.8 W ; V_{CC} = 13.2 V ; R_L = 3.2 Ω ; R_f = 56 Ω			–	60	–	
P_O = 5.8 W ; V_{CC} = 13.2 V ; R_L = 3.2 Ω ; R_f = 10 Ω			–	12	–	
Input resistance	Pin 5	Z_I	–	5	–	MΩ
Frequency response (–3 dB), (V_{CC} = 14.4 V ; R_L = 4 Ω ; R_f = 56 Ω)		B				Hz
C3 = 820 pF				40 - 20 000		
C3 = 1500 pF				40 - 10 000		
Distortion (V_{CC} = 14.4 V ; P_O = 50 mW⇒2.5 W ; R_L = 4 Ω ; f = 1 KHz)		d	–	0.3	–	%
Voltage gain (open loop) (V_{CC} = 14.4 V ; R_L = 4 Ω ; f = 1 KHz)		A_V	–	80	–	dB
Voltage gain (closed loop)		A_V				dB
V_{CC} = 14.4 V ; R_L = 4 Ω ; f = 1 KHz ; R_f = 56 Ω			34	37	40	
Input noise voltage (V_{CC} = 16 V ; B(–3 dB) = 40 - 15 000 Hz)		v_n	–	2	–	µV
Input noise current (V_{CC} = 16 V ; B(–3 dB) = 40 - 15 000 Hz)		i_n	–	80	–	pA
Efficiency (V_{CC} = 14.4 V ; P_O = 6 W ; R_L = 4 Ω ; f = 1 KHz)		η	–	67	–	%
Supply voltage rejection		SVR				dB
V_{CC} = 14.4 V ; R_L = 4 Ω ; V_{ripple} = 1 Vrms ; f = 100 Hz ; A_V = 37 dB ; C5 = 100 µF			40	48	–	

Note 1 : The characteristics above were obtained using the circuit shown in figure 1.

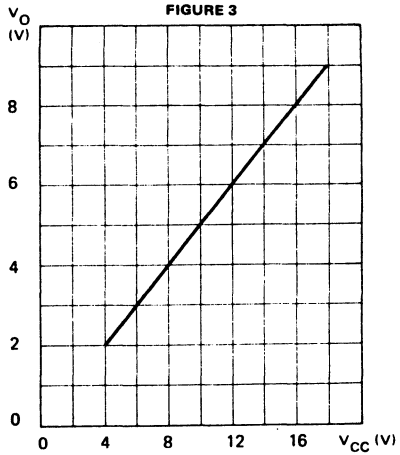
TYPICAL QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE

FIGURE 2



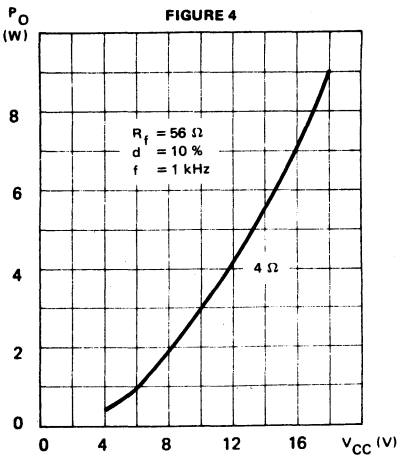
TYPICAL QUIESCENT OUTPUT VOLTAGE (pin 8) VERSUS SUPPLY VOLTAGE

FIGURE 3



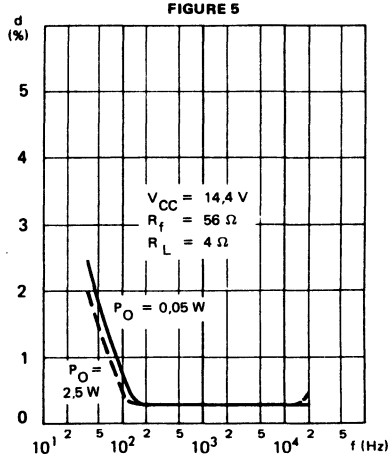
TYPICAL POWER OUTPUT VERSUS SUPPLY VOLTAGE

FIGURE 4



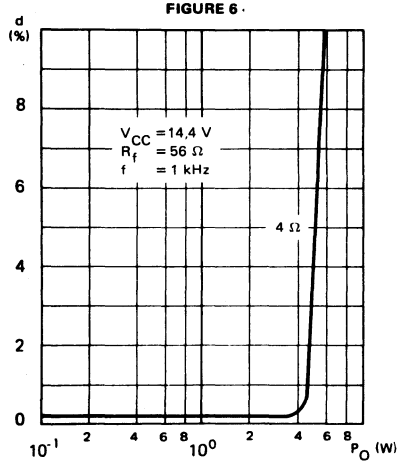
TYPICAL DISTORTION VERSUS FREQUENCY

FIGURE 5



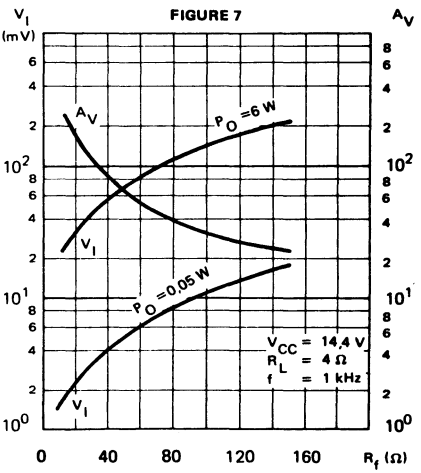
TYPICAL DISTORTION VERSUS OUTPUT POWER

FIGURE 6 -



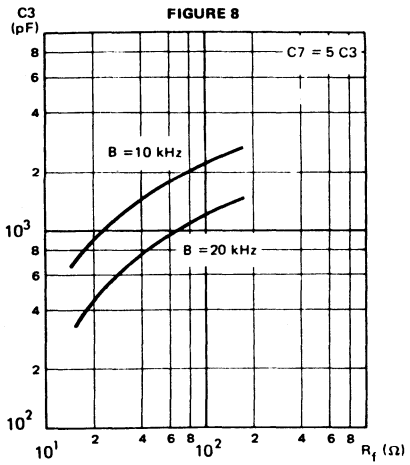
TYPICAL RELATIVE VOLTAGE GAIN (CLOSED LOOP) AND TYPICAL INPUT VOLTAGE VERSUS FEEDBACK RESISTANCE (R_f)

FIGURE 7



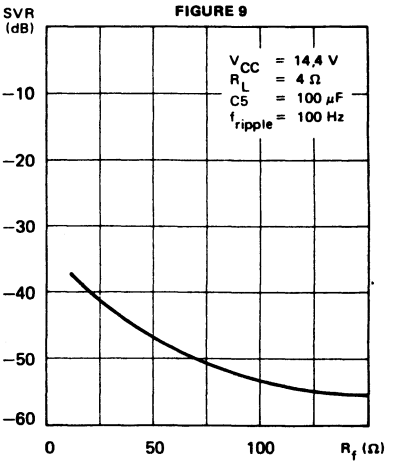
TYPICAL VALUES OF C3 VERSUS R_f FOR VARIOUS VALUES OF B

FIGURE 8



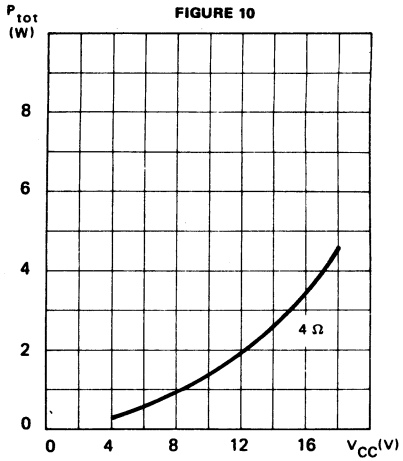
TYPICAL SUPPLY VOLTAGE REJECTION RATIO VERSUS FEEDBACK RESISTANCE

FIGURE 9



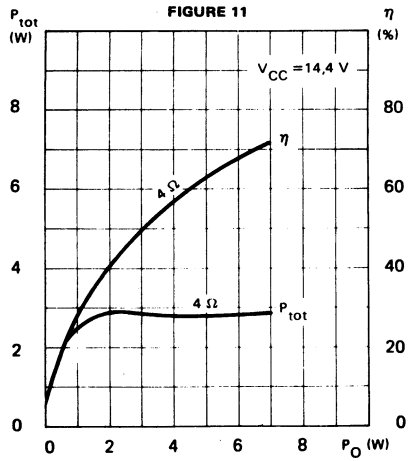
MAXIMUM POWER DISSIPATION VERSUS SUPPLY VOLTAGE (Sine wave operation)

FIGURE 10

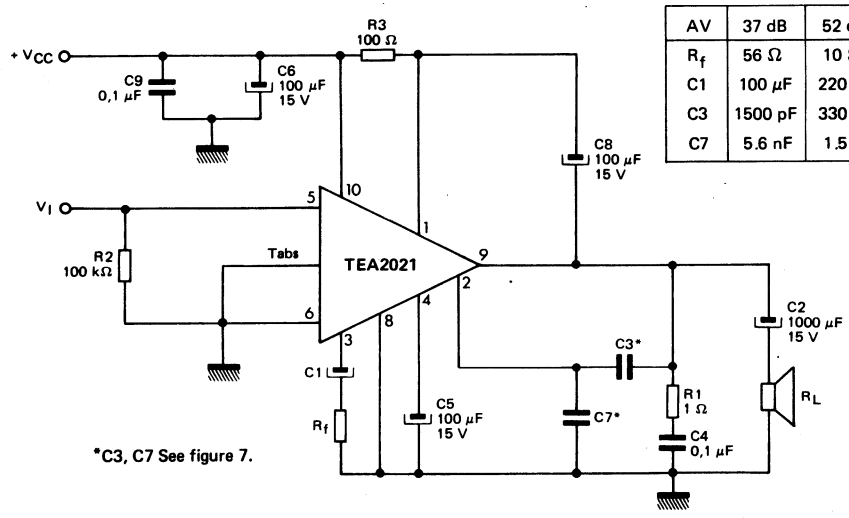


TYPICAL POWER DISSIPATION AND EFFICIENCY VERSUS OUTPUT POWER

FIGURE 11



TEST AND APPLICATION CIRCUIT



AV	37 dB	52 dB
R_f	56 Ω	10 Ω
C1	100 μF	220 μF
C3	1500 pF	330 pF
C7	5.6 nF	1.5 nF

BUILT-IN PROTECTION SYSTEMS

Load dump protection

The load dump case occurs in a car when the engine is running and the battery is disconnected : voltage spikes on the power line are supplied by the alternator since there is no clampling effect due to battery capacitance.

The TEA2021 was designed to withstand a pulse train on pin 10, of the type shown in fig. 12. Providing an LC filter is included, as shown in fig. 13, a much higher pulse train amplitude (up to 100 V peak) in allowed on the supply line with no damage to the device.

Short-circuit protection

The TEA2021 can withstand a permanent short-circuit accross the load for a supply voltage up to 15 V.

Polarity inversion protection

High current (up to 5 A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1 A fuse (normally connected in series with the supply). This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

Open ground protection

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TEA2021, protection diodes are included to avoid any damage.

Inductive load protection

A protection diode is provided between pins 9 and 10 (see the internal schematic diagram) the allow used of the TEA 2021 with inductive loads.

In particular, the TEA2021 can drive the coupling transformer for audio modulation in CB transmitters.

DC voltage protection

The maximum operating DC voltage on the TEA2021 is 20 V.

However the device can withstand a DC voltage up to 28 V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

FIGURE 12

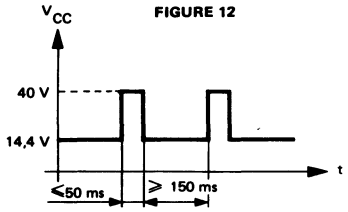
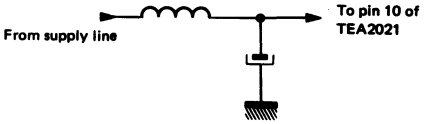
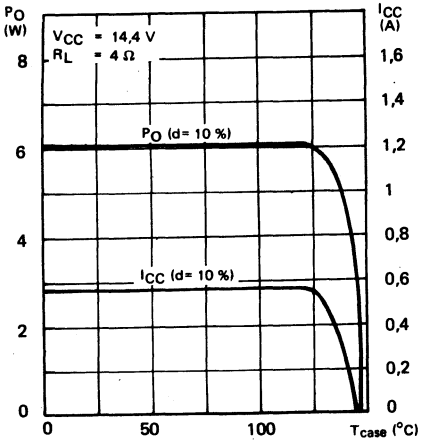


FIGURE 13



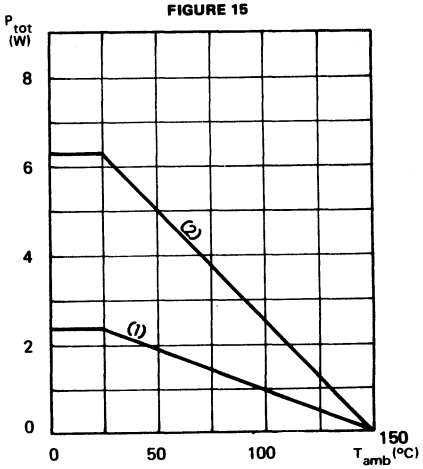
OUTPUT POWER AND SUPPLY CURRENT VERSUS PACKAGE TEMPERATURE

FIGURE 14



MAXIMUM POWER DISSIPATION

FIGURE 15



(1) Without heatsink
(2) With heatsink 10°C/W

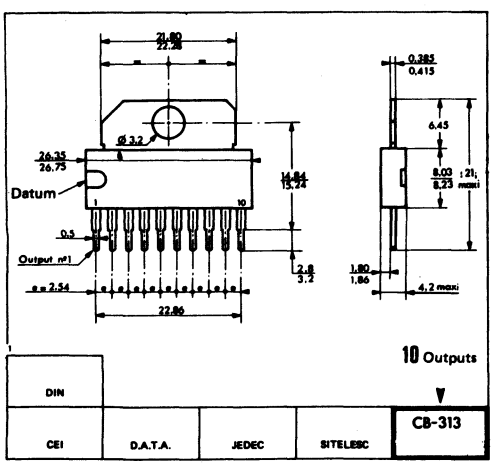
THERMAL PROTECTION

A thermal limiting circuit is internally provided on TEA 2021 to prevent chip temperature exceeding 150°C. This protection offers the following advantages :

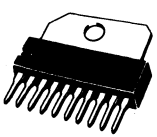
1 - An overload on the output (even of permanent), or an above-limit ambient temperature can be withstood.

2 - The heatsink can be designed with smaller safety margins compared with that of a conventional power audio amplifier.

The TEA2021 will remain undamaged in the event of excessive junction temperature : all that happens is that P_O (and therefore P_{tot}) are reduced (fig. 14).



CASE CB-313



SP SUFFIX
PLASTIC PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

TEA2024

ADVANCE INFORMATION

STEREO AF AMPLIFIER

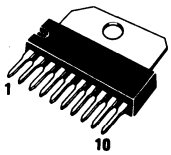
The TEA2024 is an A.F. stereo amplifier in plastic package of 10 passages which is especially adapted for use in radio-cassette and low cost car-radio.

It has the capacity to supply an output power of 3.5 W per channel in the following conditions : $V_{CC} = 12$ V, THD = 10 %, $R_L = 4\ \Omega$.

- Low idle current
- Internal thermal protection
- Protection against short-circuit
- Single-in-line package
- Very few external components
- Excellent ripple rejection.

STEREO AF AMPLIFIER

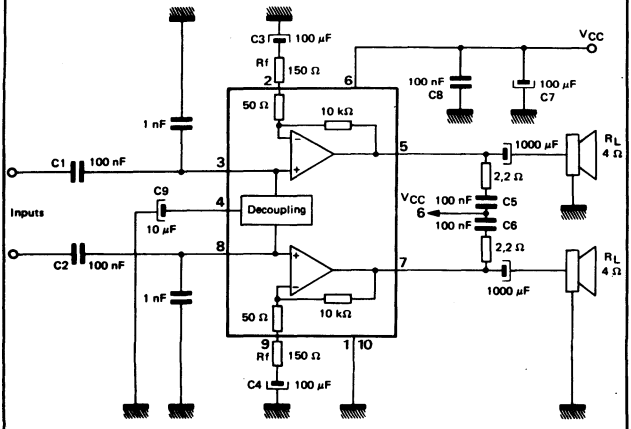
CASE CB-313



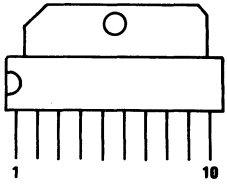
SP SUFFIX
PLASTIC PACKAGE

TYPICAL APPLICATION

DUAL MODE



PIN ASSIGNMENT



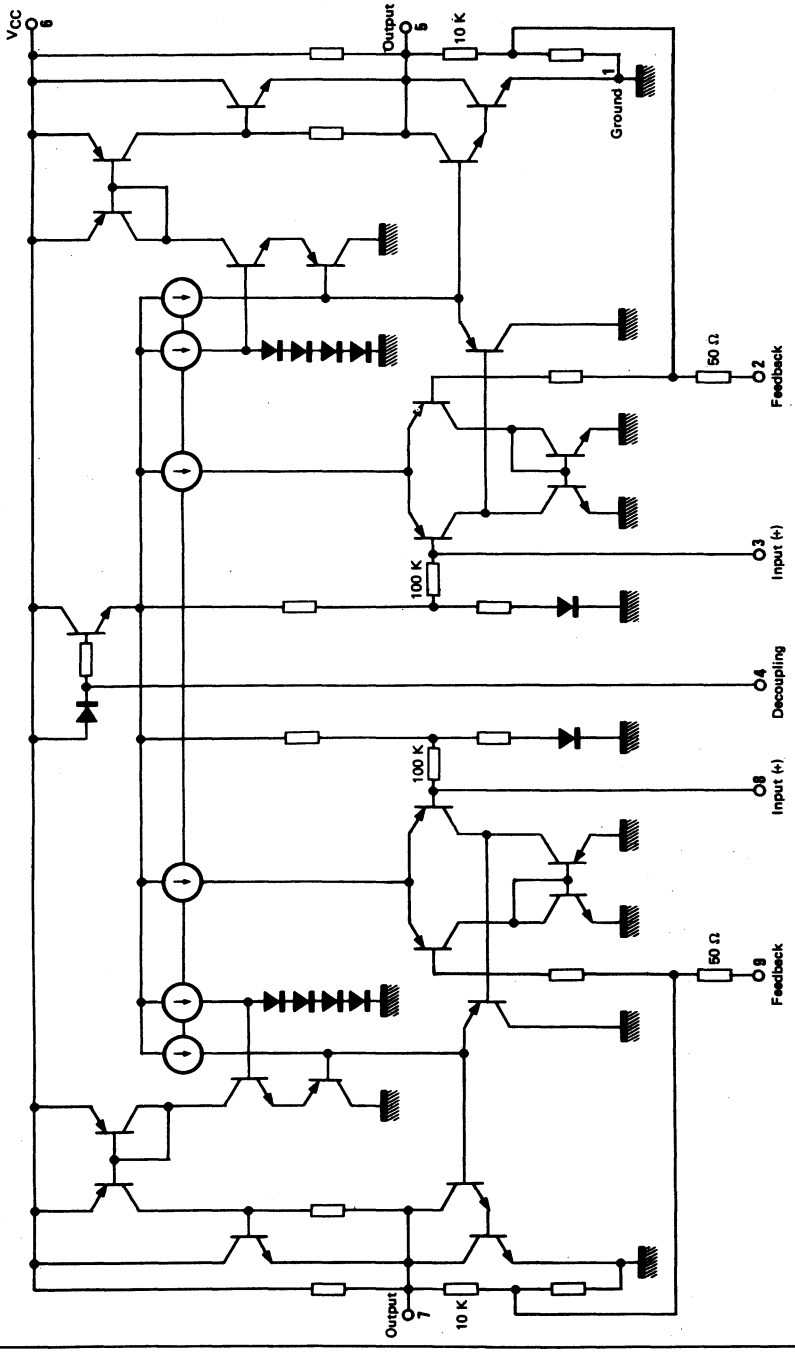
1. Ground (1)
2. Feedback (1)
3. Positive Input (1)
4. Decoupling
5. Output (1)
6. V_{CC} (1)
7. Output (2)
8. Positive Input (2)
9. Feedback (2)
10. Ground (2)

SP8236-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

ELECTRICAL DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	20	V
Operating supply voltage	V_{CC}	18	V
Power dissipation	P_{tot}	See graphs	
Maximum output current	I_O	2.5	A
Storage or junction temperature	T_{stg}, T_j	- 40, + 150	°C

THERMAL CHARACTERISTICS

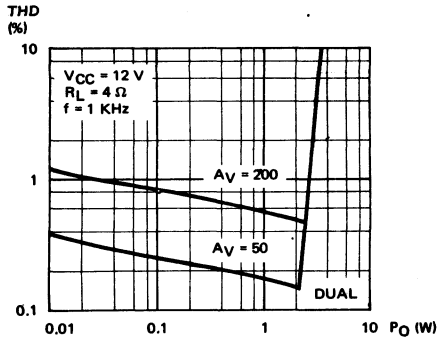
Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	60	°C/W
Junction-case thermal resistance	$R_{th(j-c)}$	9	°C/W

ELECTRICAL CHARACTERISTICS

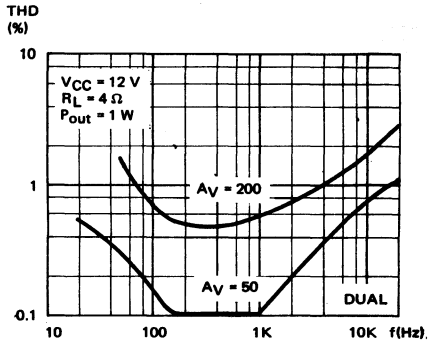
V_{CC} = 12 V, T_{amb} = + 25°C, R_L = 4 Ω, A_V = 46 dB, Dual mode (unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage range	V_{CC}	6	–	18	V
Supply current (V_E = 0)	I_{CC}	–	35	60	mA
D.C. output voltage (V_{CC} = 12 V)	V_{out}	5.4	6.0	6.6	V
Output power (f = 1 KHz ; d = 10 % ; R_L = 4 Ω)	P_{out}				W
Dual mode - per channel					
V_{CC} = 12 V		3	3.5	–	
V_{CC} = 9 V		–	1.75	–	
V_{CC} = 6 V		–	0.60	–	
V_{CC} = 14.4 V		–	5	–	
BTL mode - V_{CC} = 12 V		–	10	–	
Voltage gain without external resistance					dB
R_f = 150 Ω	A_{V1}	31	34	37	
R_f = 0 Ω	A_{V2}	–	46	–	
Distortion (f = 1 KHz ; V_{CC} = 12 V ; R_L = 4 Ω ; P_{out} 0.5 to 2 W)	d	–	0.3	1.5	%
Input noise voltage (R_G = 0 ; B = 20 KHz)		–	2	–	μV
Supply voltage ripple rejection	SVR		-		dB
Fripple= 100 Hz ; Vripple= 0.5 V_{RMS} ; R_G= 0		40	50	–	
Crosstalk (f = 1 KHz ; R_G = 10 K)	C_T	40	52	–	dB
Frequency response (3 dB) - (P_{out} = 1 W ; R_L = 4 Ω)	B	–	0.015 - 40	–	KHz
Open loop gain		–	80	–	dB

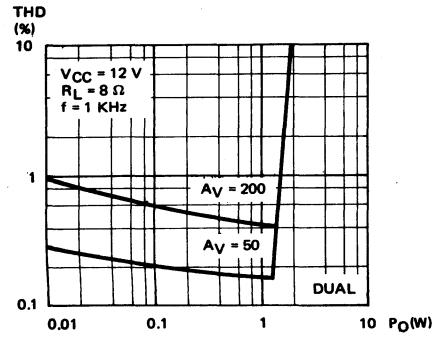
DISTORTION VS OUTPUT POWER



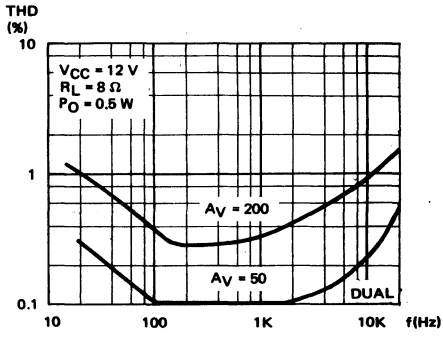
DISTORTION VS FREQUENCY



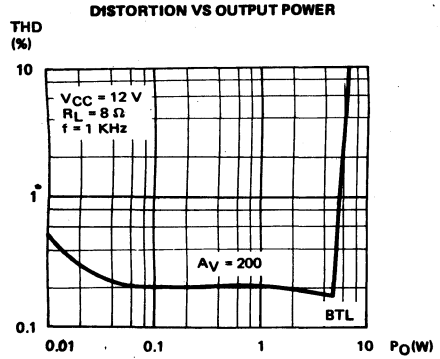
DISTORTION VS OUTPUT POWER



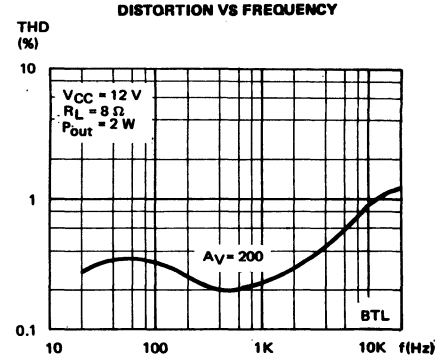
DISTORTION VS FREQUENCY



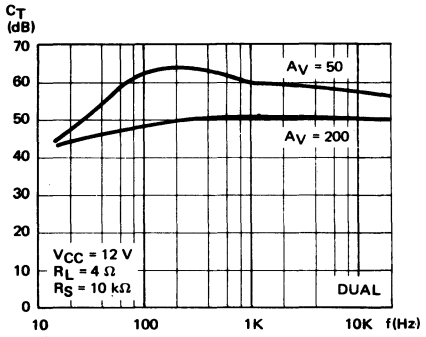
DISTORTION VS OUTPUT POWER



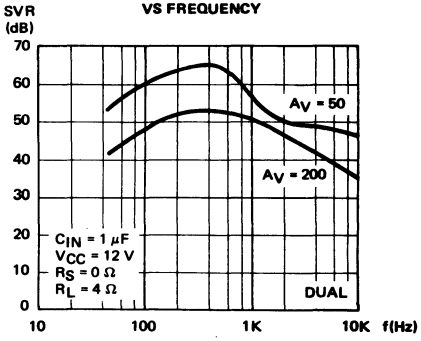
DISTORTION VS FREQUENCY



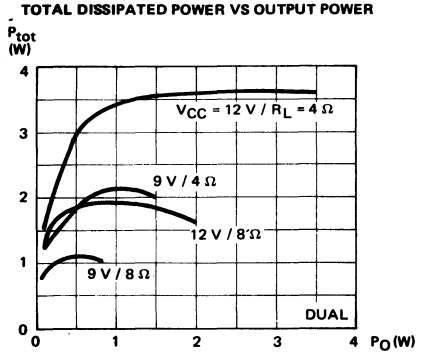
CROSSTALK VS FREQUENCY



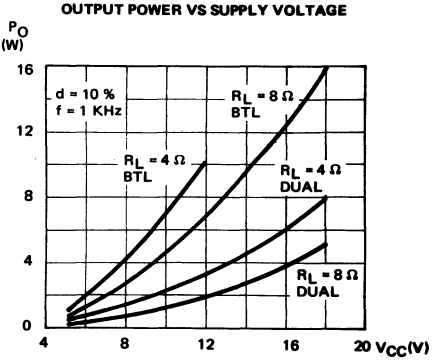
SUPPLY VOLTAGE RIPPLE REJECTION VS FREQUENCY



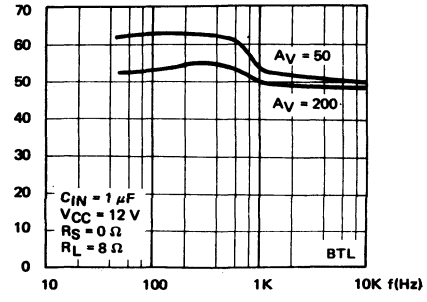
TOTAL DISSIPATED POWER VS OUTPUT POWER



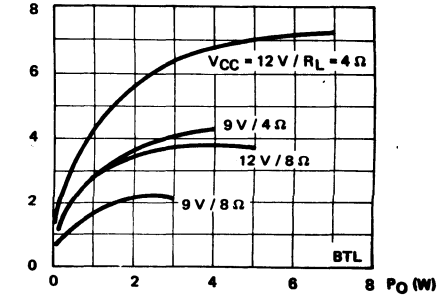
OUTPUT POWER VS SUPPLY VOLTAGE



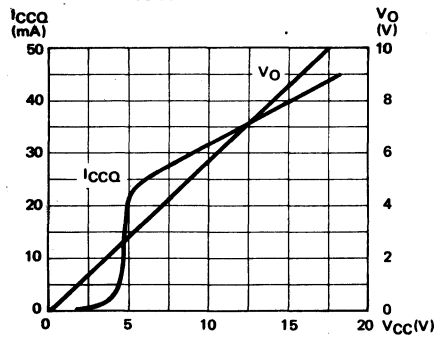
SUPPLY VOLTAGE RIPPLE REJECTION VS FREQUENCY



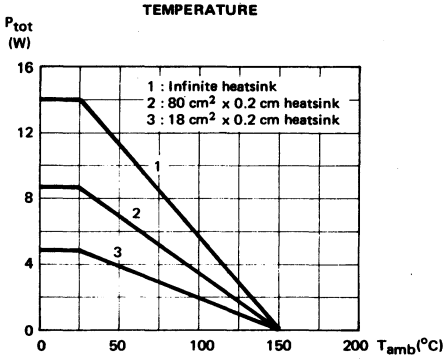
TOTAL DISSIPATED POWER VS OUTPUT POWER



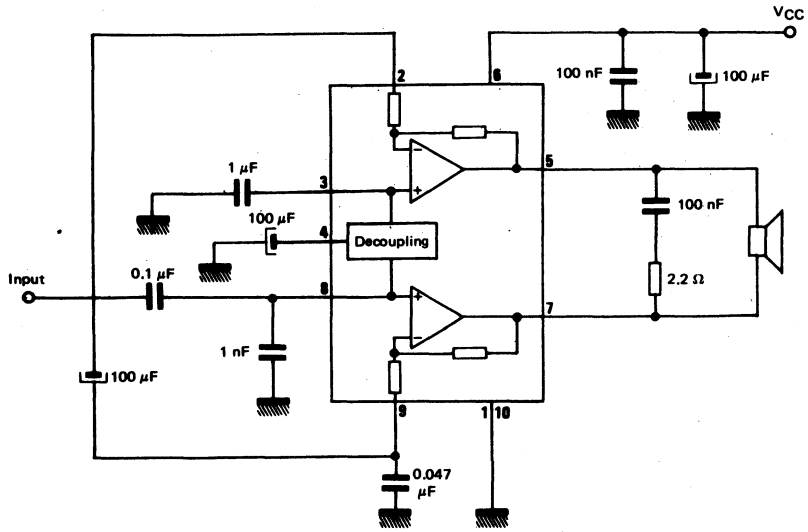
QUIESCENT CURRENT/D.C. OUTPUT VOLTAGE VS SUPPLY VOLTAGE



MAX DISSIPATED POWER VS AMBIENT TEMPERATURE



BRIDGE MODE



APPLICATION INFORMATION

GROUND CONNECTION

Two ground pins are provided and must be connected together on the PC board. The GND connections for power - return from the load and negative supply - must be kept separated from the signal and feed-back ground. Inappropriate ground connections will cause parasitic oscillation, distortion and cross-talk.

VOLTAGE GAIN

The voltage gain is determined by the ratio of internal feedback resistors and external resistor R_f.

$G_V = 34$ dB for $R_f = 150\ \Omega$

$G_V = 46$ dB for $R_f = 0\ \Omega$

CAPACITORS C5 AND C6

These capacitors must be connected close to the I.C. connections. Low temp-coefficient type will give the best results to prevent oscillations.

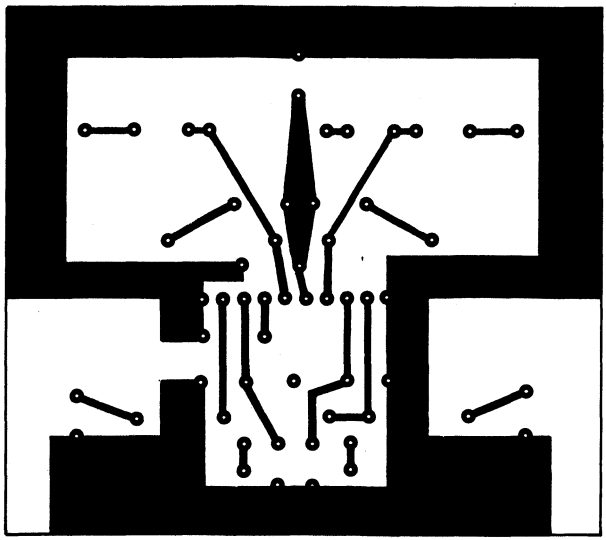
1 nF ceramic capacitors bypassing inputs to ground will help prevent high oscillations or radio interference.

OUTPUT POWER TABLE (TYPICAL VALUE)
THD = 10 % ; f = 1 KHz ; $T_{amb} = +25°C$

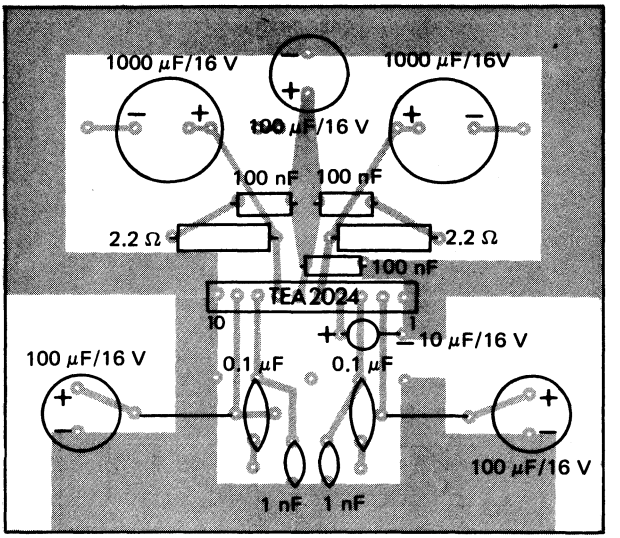
LOAD \ V_{CC}		6 V	9 V	12 V	14.4 V
DUAL	8 Ω	–	1 W/ch	1.8 W/ch	3.0 W/ch
	4 Ω	0.6 W/ch	1.8 W/ch	3.5 W/ch	5 W/ch
BTL	8 Ω	1.2 W	3.5 W	6.7 W	10.5 W
	4 Ω	2.0 W	6.3 W	10 W	–

DUAL and BTL MODES

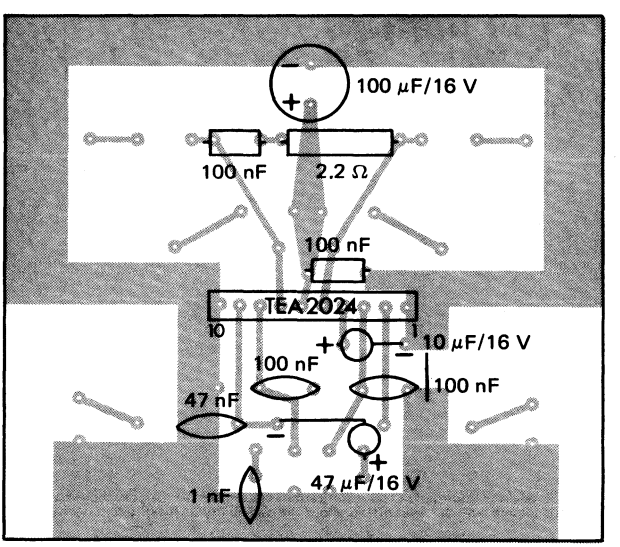
PRINTED CIRCUIT BOARD



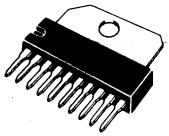
COMPONENT LAYOUT (DUAL MODE)



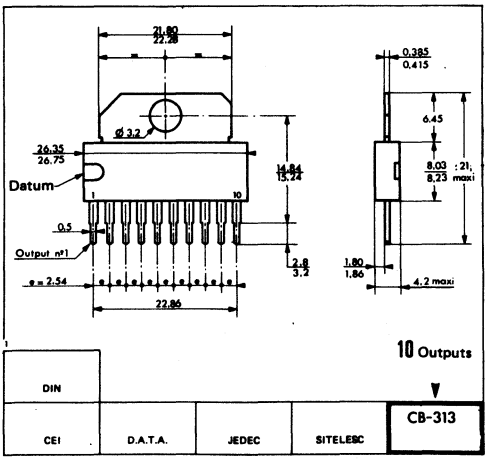
COMPONENT LAYOUT (BRIDGE MODE)



CASE CB-313



SP SUFFIX
PLASTIC PACKAGE



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THOMSON SEMICONDUCTORS

TEA2025

ADVANCE INFORMATION

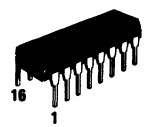
STEREO AUDIO AMPLIFIER

Dual or BTL connection modes.
Few external components.
Works with low supply voltage : 3 V.
High channel separation.
No schock noise when switch on or off.
Maximum voltage gain of 45 dB (adjustable with external resistor).
Soft clipping.

- $3\ V \leqslant V_{CC} \leqslant 12\ V$
- $P = 2 \times 1\ W$, $V_{CC} = 6\ V$, $R_L = 2\ \Omega$
- $P = 2 \times 2.3\ W$, $V_{CC} = 9\ V$, $R_L = 4\ \Omega$
- $P = 2 \times 0.1\ W$, $V_{CC} = 3\ V$, $R_L = 4\ \Omega$

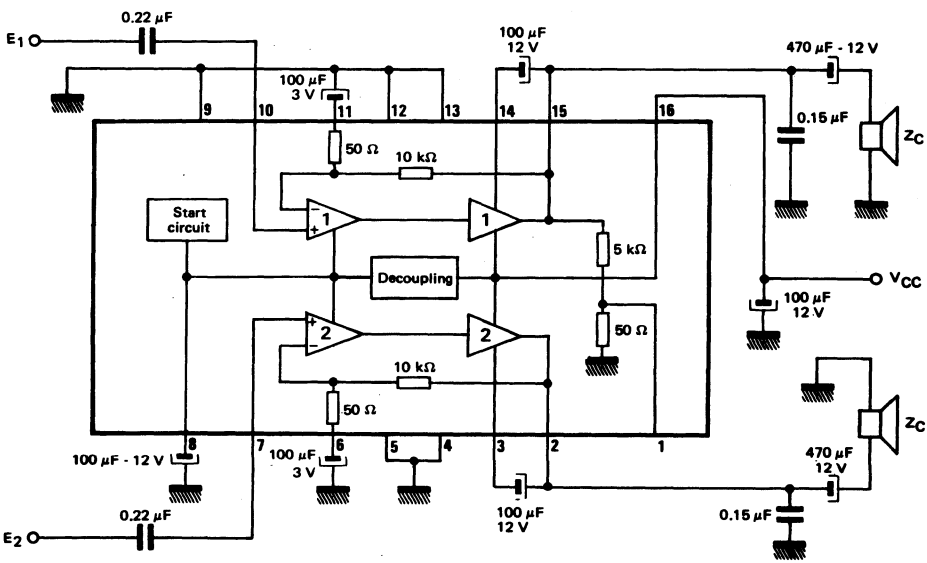
STEREO AUDIO AMPLIFIER

CASE CB-79



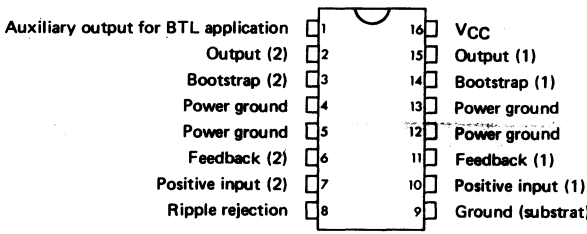
DP SUFFIX
PLASTIC PACKAGE

APPLICATION AND TEST CIRCUIT (DUAL MODE)

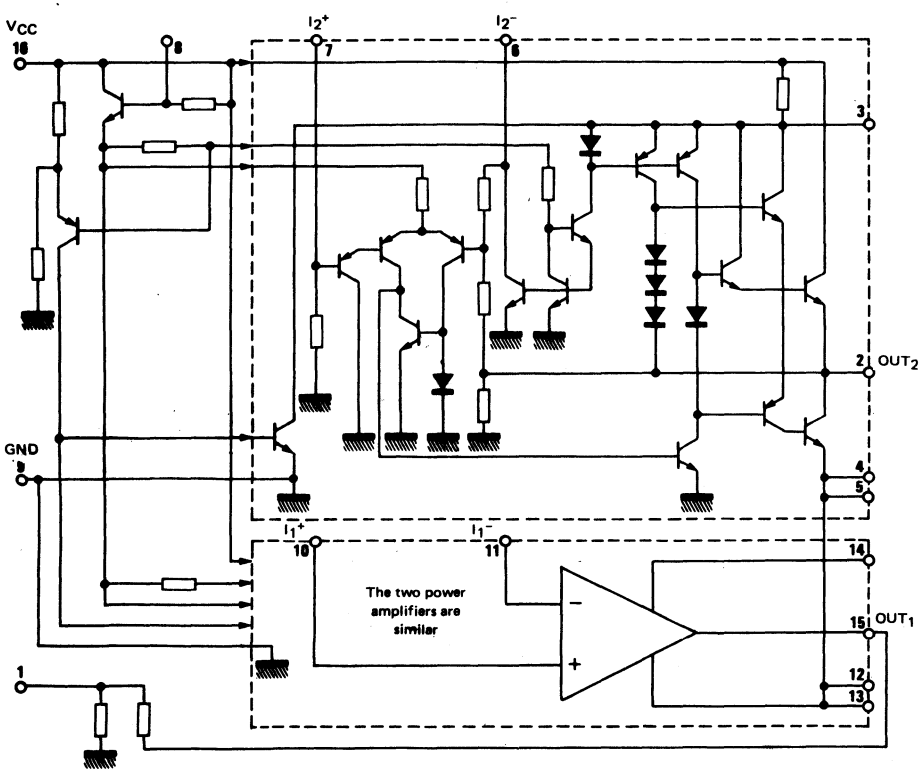


SP8237-A

PIN CONFIGURATION



ELECTRICAL DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	15	V
Output peak current	I_O	1.5	A
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	- 40, + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-case thermal resistance	$R_{th(j-c)}$	15	°C/W
Junction-ambient thermal resistance (See note)	$R_{th(j-a)}$	60	°C/W

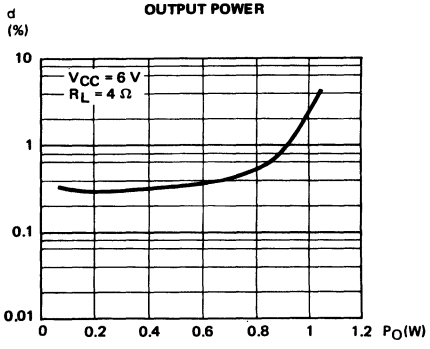
Note : The $R_{th(j-a)}$ is measured on devices bonded on a 10 x 5 x 0.15 cm glass-epoxy substrate with a 35 µm thick copper surface of 5 cm^2.

ELECTRICAL CHARACTERISTICS

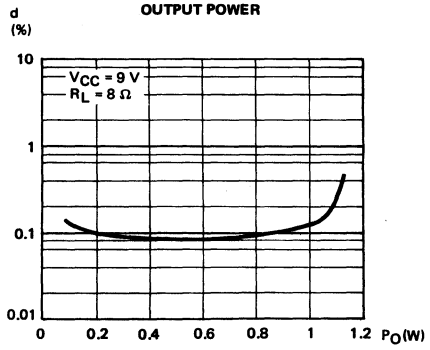
$T_{amb} = 25°C$, $V_{CC} = 9$ V, dual mode (unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3	–	12	V
Quiescent current		–	40	50	mA
Quiescent output voltage		–	4.5	–	V
Voltage gain	A_V				dB
Dual mode		43	45	47	
BTL mode		49	51	53	
Voltage gain difference		–	–	± 1	dB
Input impedance		–	30	–	kΩ
Output power (f = 1 KHz ; d = 10 %)					
Dual mode - per channel					W
V_{CC} = 9 V : R_L = 4 Ω		1.7	2.3	–	
R_L = 8 Ω		–	1.3	–	
V_{CC} = 6 V : R_L = 4 Ω		0.7	1	–	
R_L = 8 Ω		–	0.6	–	
V_{CC} = 3 V : R_L = 4 Ω		–	0.1	–	
BTL mode					
V_{CC} = 9 V : R_L = 8 Ω		–	4.7	–	
V_{CC} = 6 V : R_L = 4 Ω		–	2.8	–	
Distortion (V_{CC} = 9 V ; R_L = 4 Ω ; f = 1 KHz ; P_o = 250 mW)					%
Dual mode		–	0.3	1.5	%
BTL mode		–	0.5	–	
Supply voltage rejection (R_G = 0, A_V = 45 dB, V_{ripple} = 150 mV RMS, f_{ripple} = 100 Hz)	SVR	40	46	–	dB
Input noise voltage (A_V = 200, Bandwidth : 20 Hz to 20 KHz)					µV
R_G = 0		–	1.5	3	
R_G = 10 kΩ		–	3	6	
Cross-talk (R_G = 10 kΩ ; f = 1 KHz ; R_L = 4 Ω ; P_o = 1 W)		40	55	–	dB

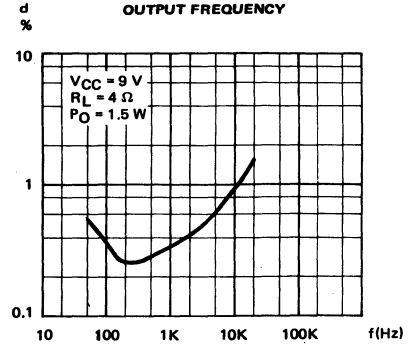
TYPICAL DISTORTION VERSUS OUTPUT POWER



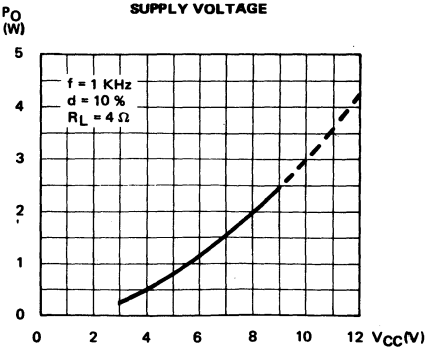
TYPICAL DISTORTION VERSUS OUTPUT POWER



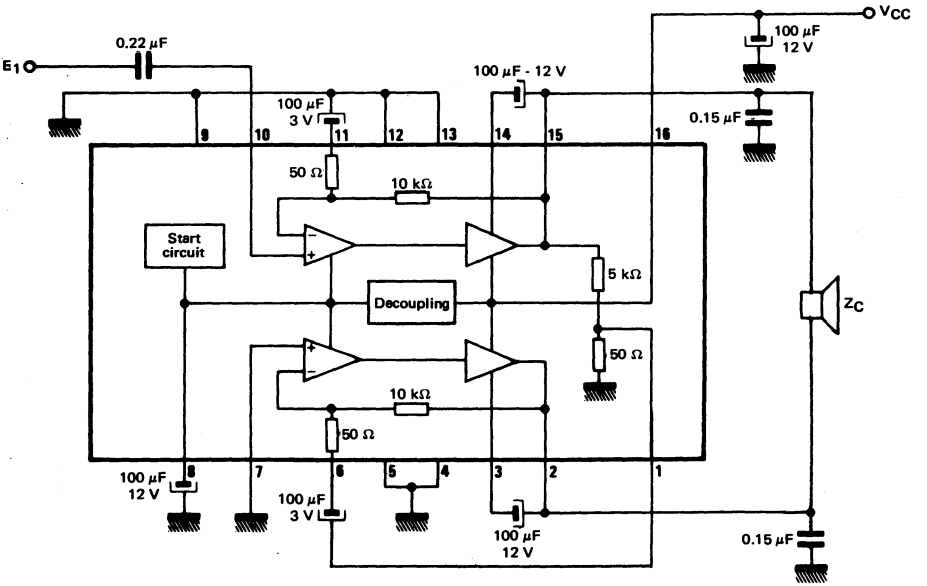
TYPICAL DISTORTION VERSUS OUTPUT FREQUENCY



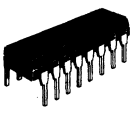
DUAL MODE OUTPUT POWER/VERSUS SUPPLY VOLTAGE



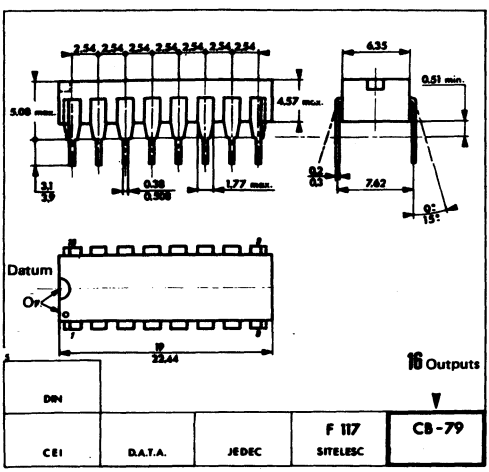
BRIDGE APPLICATION



CASE CB-79



DP SUFFIX
PLASTIC PACKAGE



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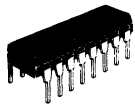
SWITCH MODE POWER SUPPLIES

5

SWITCH MODE POWER SUPPLIES

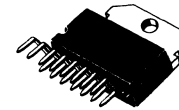
DIL14 (CB-2)



DIL16 (CB-79)

DIL8 (CB-98)

SIL17 (CB-215)



SIL15 (CB-501)

SWITCH MODE POWER SUPPLIES (FLYBACK MODE)

Rating	TEA1001	UAA4001	UAA4006	TEA2018	TEA2019
Maximum output current (A)	± 3.0	± 1.0	± 1.5	± 0.5	± 0.5
Base current regulation $I_B = f(I_C)$	Automatic	Automatic	Automatic	$I_B = KI_C$	$I_B = KI_C$
Protection against desaturation	–	–	●	–	●
Secondary current supervision	●	●	●	●	●
t_{on} min (μs)	2.0	2.0	Adjustable from 1.0 to 10.0	Adjustable from 1.0 to 10.0	2.0
t_{on} max	Adjustable	Adjustable	Adjustable	80 %	50 %
Start supply current (mA)	15.0	15.0	0.3	1.0	1.0
Soft-start	●	●	●	–	–
Oscillator sync.	● PLL	–	●Without PLL	–	● PLL
Typical supply output power (W)	100 to 300	< 100	< 100 DIL16 100 to 200 SIL15	< 60	< 60
Package	SIL17 (CB-215)	DIL16 (CB-79)	SIL15(CB-501) DIL16(CB-79)	DIL8 (CB-98)	DIL14 (CB-2)
Page	565	587	599	577	581

THOMSON SEMICONDUCTORS

TEA1001

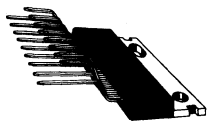
SWITCH MODE POWER SUPPLY CONTROLLER

The TEA1001-SP is a monolithic IC intended for power transistor control in single transistor DC-DC converters (Fly Back type).

- Direct drive of the switching transistor
- Complete PWM power control circuitry
- Up to ± 3 A base current output
- Output transistor V_{CEsat} sensing
- Output transistor current limitation
- Under and over voltage lockout
- Programmable soft start
- Thermal overload protection
- Regulation better than 0.2 %
- On-chip low drift 2.5 V reference
- 50 kHz operation with PLL circuit for external synchronization.

SWITCH MODE POWER SUPPLY CONTROLLER

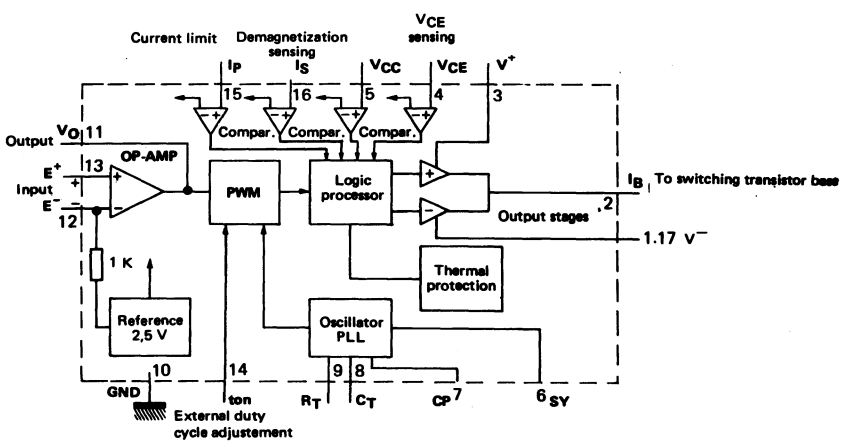
CASE CB-215



SP SUFFIX
PLASTIC PACKAGE

5

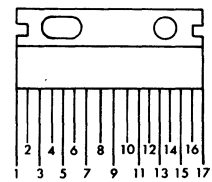
BLOCK DIAGRAM



NT8234R1-A

PIN CONFIGURATION

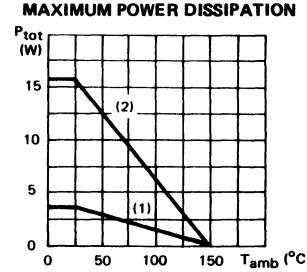
1, 17	V^-	Negative output stage supply
2	I_B	Output
3	V^+	Positive output stage supply
4	V_{CE}	V_{CEsat} sensing
5	V_{CC}	V_{CC}
6	SY	Synchronization input
7	C_P	Phase comparator output
8	C_T	C_T oscillator external capacitor
9	R_T	R_T oscillator external resistor
10	GND	Ground
11	V_O	Op-Amp. output
12	E^-	Op-Amp. inverting input - V_{ref}
13	E^+	Op-Amp. non inverting input
14	t_{on} M	$t_{on\ max}$ external adjustment and softstart
15	I_P	Primary current limit input
16	I_S	Secondary current monitoring input



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage V_{CC}/ground	V_{CC} – GND	+ 15	V
Positive supply for the output stage	V^+ – GND	+ 15	V
Negative supply for the output state : Substrate/Ground	V^- – GND	- 7	V
Voltage between pins 5 and 1	$V_{CC} - V^-$	+ 20	V
Output current pulsed	I_B	± 3	A
Pin 4 current	I_{CE}	10	mA
Pin Ip max input current	I_P	± 5	mA
Pin I_S max input current	I_S	± 5	mA
Junction temperature	T_j	- 40, + 150	°C
Storage temperature	T_{stg}	- 40, + 150	°C

MAXIMUM POWER DISSIPATION



(1) Without heat-sink
(2) With heat-sink 5°C/W

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Junction-case thermal resistance	$R_{th(j-c)}$	3	°C/W
Junction-ambient thermal resistance	$R_{th(j-a)}$	35	°C/W

ELECTRICAL CHARACTERISTICS

$T_{amb} = 25°C$; $V_{CC} = 10$ V ; $V^- = -5$ V ; $V^+ = +4$ V (Unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	–	10	14	V
Supply quiescent current	I_{CC}	–	18	25	mA
Positive output stage supply voltage	V^+	–	4	V_{CC}	V
Negative output stage supply voltage	V^-	-6	-5	–	V
V_{CC} threshold to insure operation (V_{CC} increasing)	V_{CCL}	6	6.5	7	V
Hysteresis on V_{CC} threshold	ΔV_{CC}	–	0.6	–	V
Primary current limit input threshold	V_{IP}	–	± 0.2	–	V
Pin 15 input current ($V_{IN} = 0$ V)	I_P	–	4	20	µA
Output transistor saturation voltage (Pin 4 voltage must be 3 V above ground)					
Positive stage ($I_B = 3$ A)	V^+_{CE}	–	2.2	3	V
Negative stage ($I_B = 3$ A)	V^-_{CE}	–	2.8	–	V
Secondary current monitoring input threshold	I_S	–	100	–	mV
Pin 16 input current ($V_{IN} = 0$ V)	I_S	–	2	+10	µA
V_{CE} input threshold	V_{CE}	–	5	–	V
Op-amp. open loop gain	A_{VOL}		100.000		
Op-amp. external feed back resistor	R_f	50	–	–	kΩ
Op-amp. input current	I_B	–	50	250	nA
Op-amp. offset voltage	V_{IO}	–	2	7	mV
Op-amp. inverting input resistance to V_{ref}	R_{IN}	–	1	–	kΩ
Internal reference voltage	V_{ref}	2.4	2.55	2.7	V
Ref. voltage variation with temperature $-25°C < T_a < +85°C$	ΔV_{ref}	–	± 1	–	%
R_T optimal current	R_T	–	0.5	–	mA
Oscillator operating frequency range		5	–	50	kHz
Oscillator frequency temperature coefficient		–	100	–	ppm/°C
Oscillator free running frequency equation ($I_{R_T} = 0.5$ mA)			$f = \frac{1.85}{R_T \cdot C_T}$		Hz
Synchronization pulse voltage	V_{SY}	1.5	–	V_{CC}	V
Phase comparator output current ($V_{SY} > 1.5$ V)	V_{CP}				
$V_{CP} > V_{CC}/2$		–	+1.8	–	mA
$V_{CP} < V_{CC}/2$		–	−1.8	–	mA
Synchronization input impedance	R_{SY}	–	1.000	–	Ω
Maximum limit of conduction time (Pin 14 open)					
$V_{CC} < V_{CCL}$		–	0	–	% of
$V_{CCL} < V_{CC} < 14$ V		–	50	–	oscillator
$V_{CC} > 14$ V		–	0	–	period
Maximum duty cycle (set externally)					
$0.2\ V < V_{t_{on}} < 0.375\ V_{CC}$		–	90	–	% of
$0.375\ V_{CC} < V_{t_{on}} < 0.625\ V_{CC}$		–	according	–	oscillator
$0.625\ V_{CC} < V_{t_{on}}$		–	to V_{ton} 0	–	period

5

CIRCUIT DESCRIPTION

OSCILLATOR

This is a sawtooth generator which free-running frequency is set externally by resistor R_T and capacitor C_T.
The charge current of the capacitor is $I = V_{CC}/2\ R_T$, the peak and valley voltages of the sawtooth are respectively 0.625 V_{CC} and 0.375 V_{CC}. The discharge current is about 12 times greater than the charge current.

The oscillator free-running frequency is $f_o = \frac{1.85}{R_T . C_T}$.

Synchronization

The phase comparator becomes active when a positive pulse is applied on synchronization input SY.
In this case, the output S of the comparator supplies a positive current when the sawtooth is lower than its average value $V_{CC}/2$, and negative when it is greater than $V_{CC}/2$.

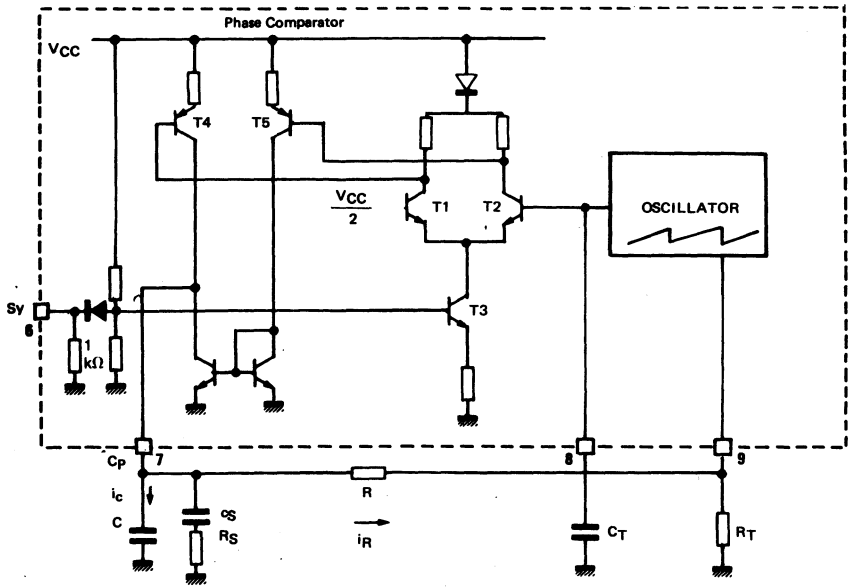
If t_s is the width of the synchro pulse, the optimal value for C is $C = 1.70\ t_s$.
(nF) (μs)

The value of R must be so that $R < 3\ \frac{t_o}{t_s}$ with $t_o = \frac{1}{f_o}$
(kΩ)

The elements R_S and C_S are necessary to stabilize the loop.

Example :

$f_o = 15$ KHz	$R = 10\ k\Omega$
$R_T = 12\ k\Omega$	$C = 10$ nF
$C_T = 10$ nF	$R_S = 2.2\ k\Omega$
$\frac{t_o}{t_s} = 12 \Rightarrow t_s = 5.5\ \mu s$	$C_S = 0.2\ \mu F$



PULSE - WIDTH MODULATOR (PWM)

Main modulator

This modulator produces a square wave whose duty cycle results from a comparison between the sawtooth and the output of the operational amplifier. The output is OFF during the return of the sawtooth.

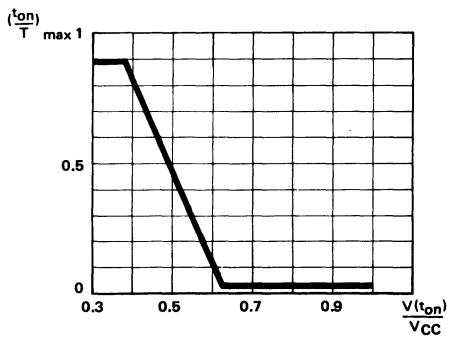
Auxiliary modulator

The voltage V (t_{on}) applied to pin 14 sets the maximum duty cycle.

An internal voltage divider between V_{CC} and ground presets the maximum ON time to 50 % of the period. This limit can be externally altered by paralleling two external resistors across the internal divider ones. These resistors should be lower than the 30 kΩ internal resistors.

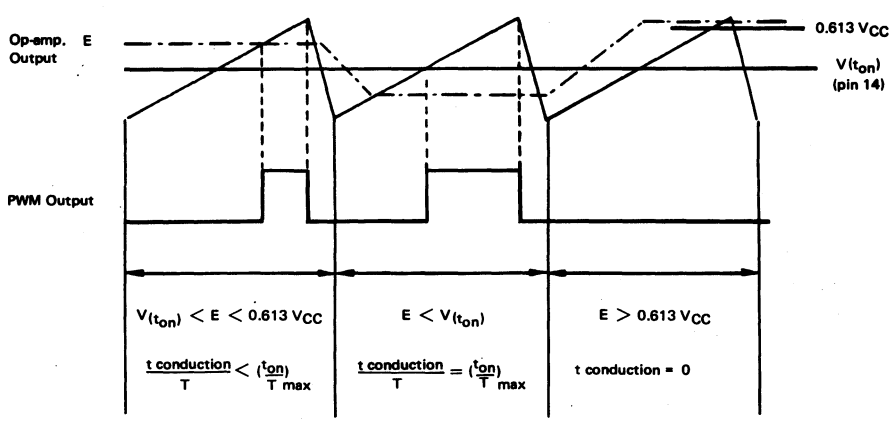
Minimum conduction time

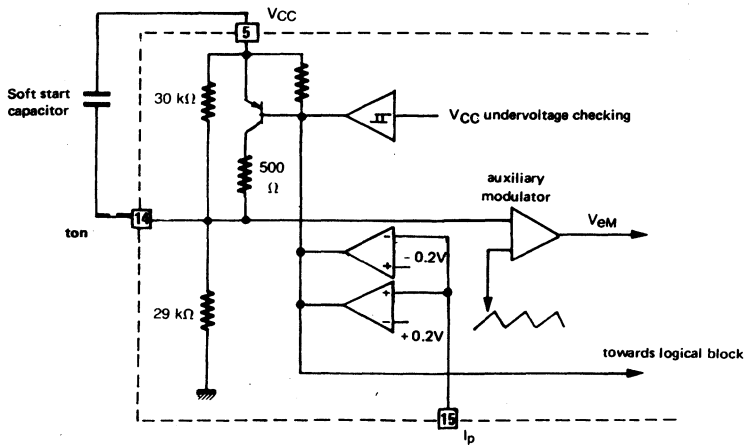
In order to allow the discharge of the snubber network, a minimum on-time is set at about 5 % of the period. Any attempt to set a lower value results in a no-conduction state.



Maximum duty cycle as a function of voltage on pin 14 normalised to V_{CC}.

Operation of the PWM duty cycle limitations :





INTERNAL CIRCUIT CONFIGURATION RELATED TO PIN 14

PROTECTION ELEMENTS

V_{CC} supply check

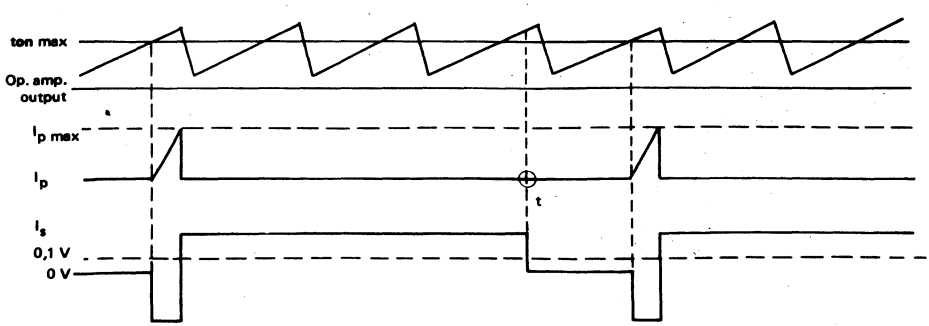
A comparator pulls pin 14 up to V_{CC} as long as V_{CC} has not reached 6.5 V, or if V_{CC} exceeds 14 V. A soft start can be achieved by connecting a capacitor between pin 14 and ground or V_{CC} (see figure above).

Primary current limitation

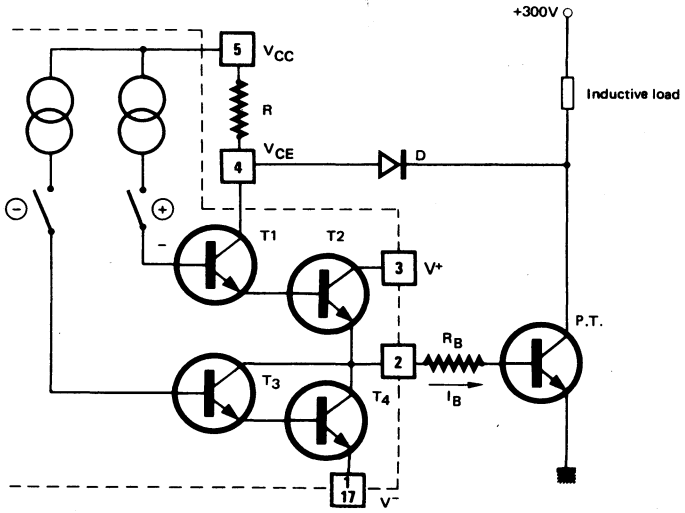
The primary current is measured across a shunt, and compared to reference voltage of + 0.2 V and −0.2 V respectively. When the detector senses an over-current, the output is turned off. The information coming from the comparators is also transmitted to pin 14, so that, during a permanent overload, the external capacitor integrates the oversteps, thus reducing the duty cycle.

Secondary current

An internal comparator whose threshold is 0.1 volt checks after each oscillator period that the secondary current has been completely drained to zero before storing energy again in the primary inductance, thus avoiding excess of core magnetization. When a secondary winding is continuously short-circuited, the total flow of current I_s spreads over several periods, during which the output is inhibited.



POWER STAGE



Positive stage

A feed-back loop provides an output current matched to the instantaneous requirement of the switching transistor. The higher the level of saturation of this transistor, the greater proportion of the current flowing through resistor R is shunted by diode D. Thus the base current of T_2, and consequently the output current of the IC, decreases.

Transistor T_1 remains saturated. The voltage V_{CE} of the power transistor (P.T.) is given approximately by :

$$(V_{CE})\ P.T. = (V_{BE})\ P.T. + R_B.I_B$$

Resistor R_B stabilizes the feed-back loop. Its value must be as low as possible, generally around 1 0hm.

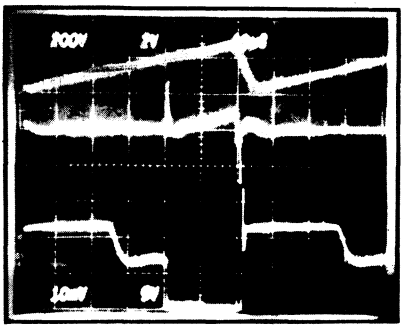
Negative stage

As the voltage V_{CE} of the switching transistor rises above 5 V, the negative stage of the TEA1001 is set into conduction. Transistors T_3 and T_4, in a darlington configuration, apply a high reverse base current to the switching transistor, which results in a very fast turn-off.

For further information concerning the TEA1001 internal structure, please refer to application note NA-011 A edited by THOMSON SEMICONDUCTORS

5

TYPICAL WAVEFORMS

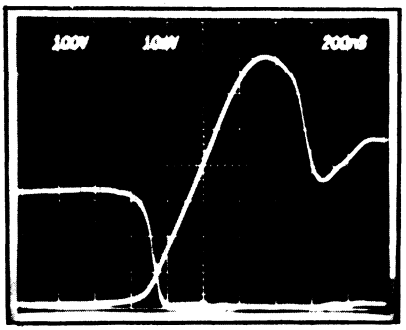


Oscillator V_8
2 V/div

Base current
1 A/div

Collector
voltage
200 V/div

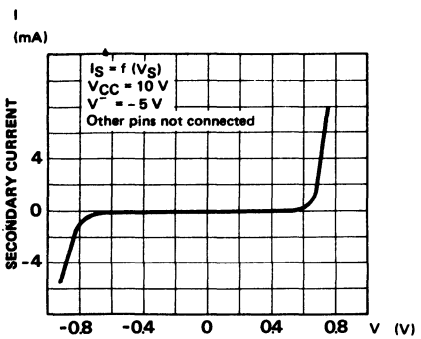
SWITCHING TRANSISTOR BASE CURRENT AND COLLECTOR VOLTAGE DURING ONE OSCILLATOR PERIOD



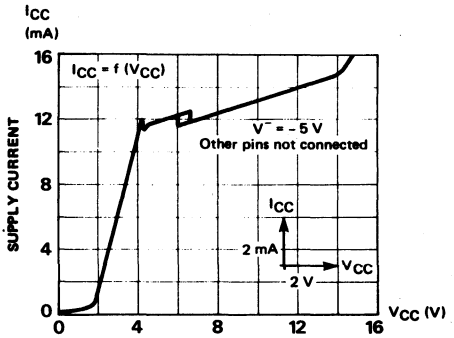
VCE : Collector voltage 100 V/div

I_C : Collector current 1 A/div

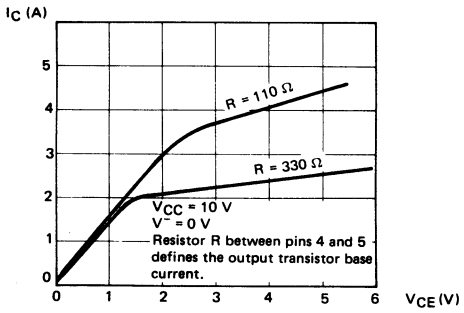
SWITCHING TRANSISTOR COLLECTOR VOLTAGE AND CURRENT



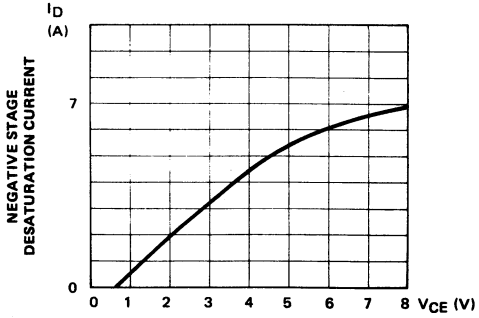
PIN 15 AND 16 CURRENT-VOLTAGE CHARACTERISTICS



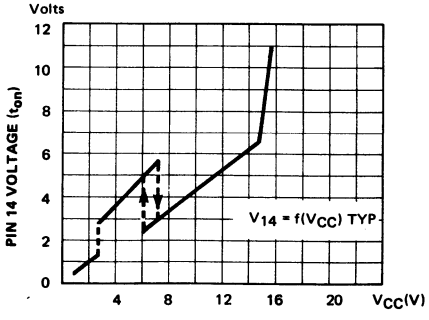
SUPPLY CURRENT I_{CC} AS A FUNCTION OF SUPPLY VOLTAGE



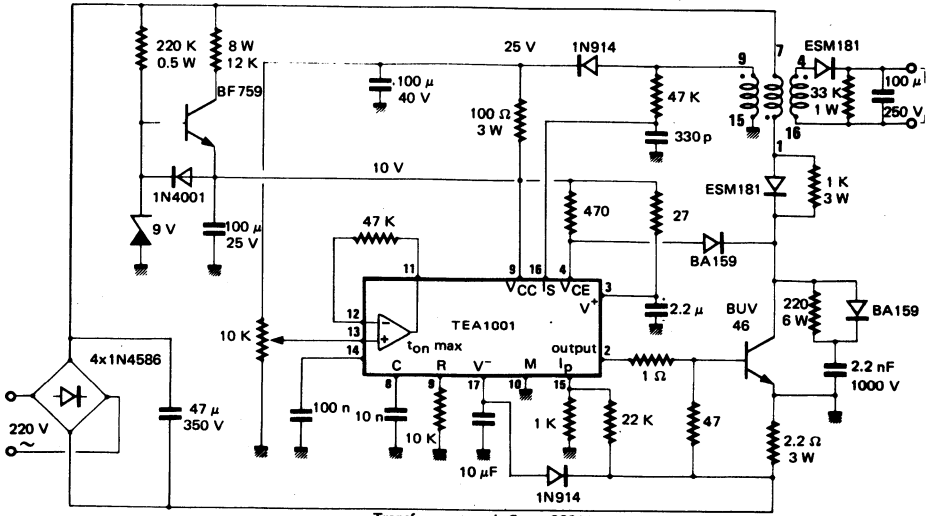
POSITIVE STAGE OUTPUT TRANSISTOR COLLECTOR CHARACTERISTICS



NEGATIVE STAGE OUTPUT TRANSISTOR COLLECTOR CHARACTERISTICS

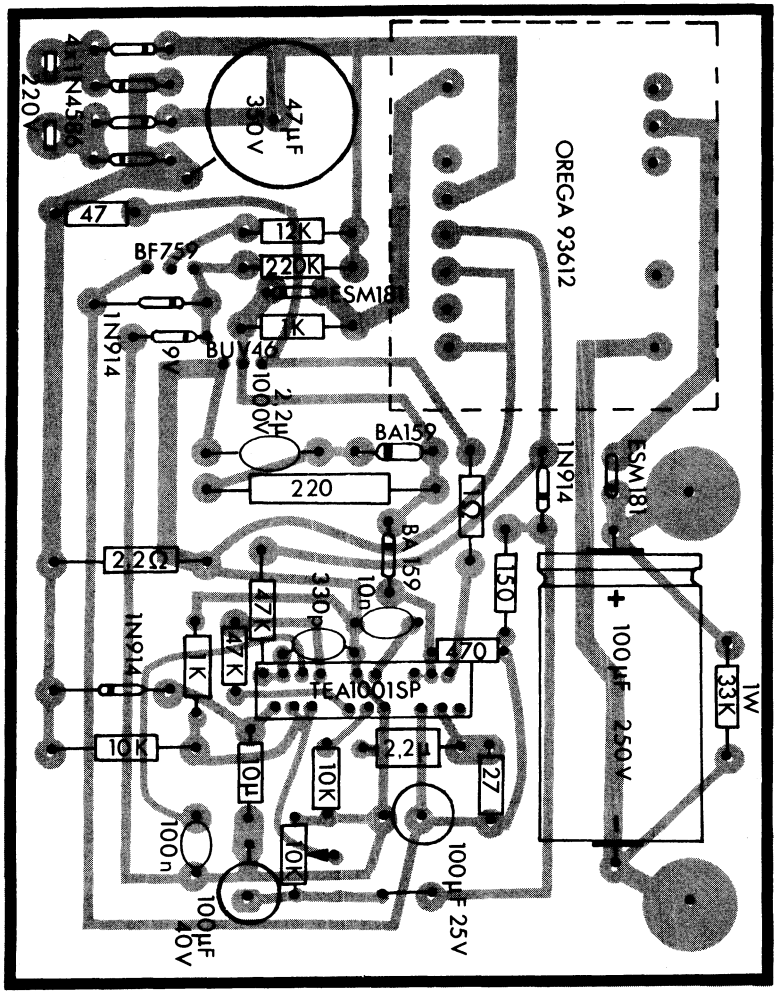


TYPICAL APPLICATION 100 W FLY-BACK CONVERTER

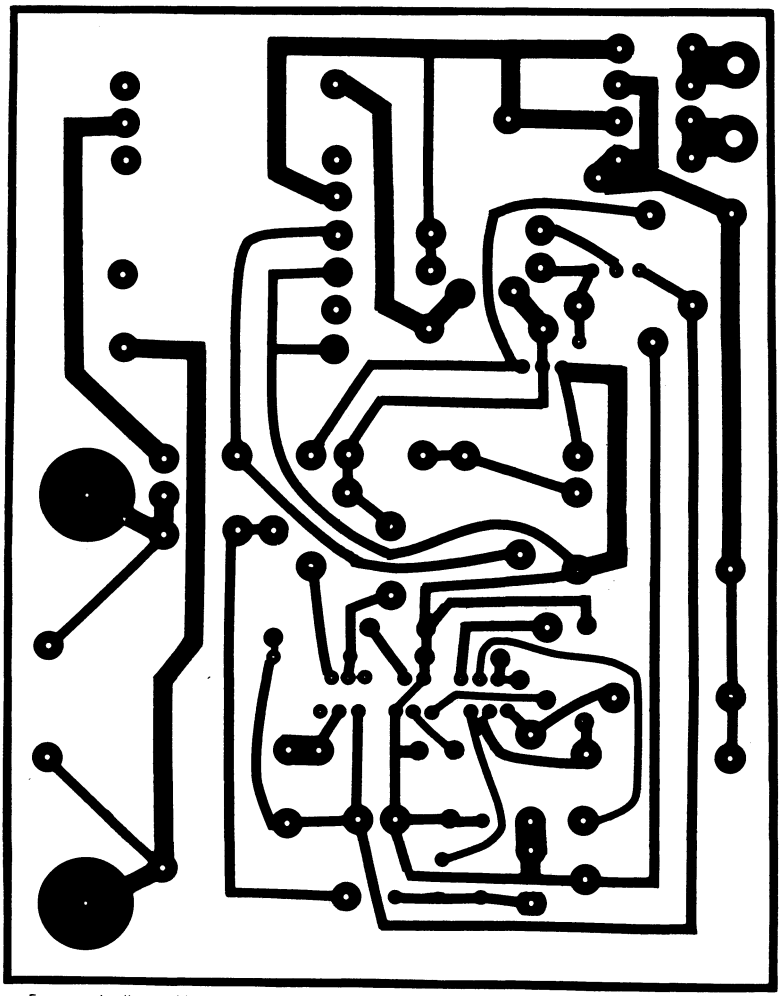


Transformer type is Orega 93612.

COMPONENT SIDE



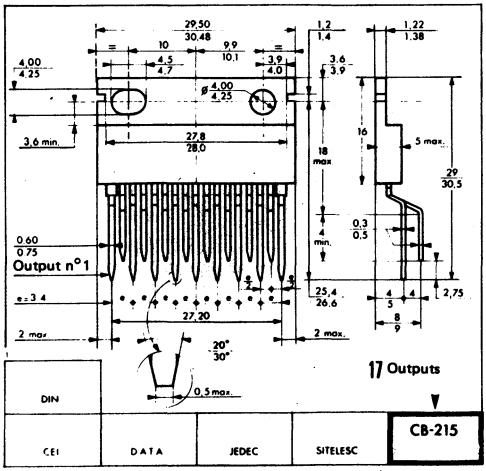
COPPER SIDE



For more details one this application and on the TEA1001, report to application notes NA-011 and NA-014.

CASE CB-215

SP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

Printed in France

THOMSON SEMICONDUCTORS

TEA2018

PRODUCT PREVIEW

SWITCH-MODE POWER SUPPLY CONTROL CIRCUIT

The TEA2018 is a large diffusion, low cost integrated circuit, packaged in an 8 pin mini-dip CB-98, for the control of switch-mode power supplies in fly-back discontinuous mode.
It can be used each time the output current and power dissipated in the I.C. are compatible with the present datas : (useful power under 90 W).
The application range is very wide : Video display units - Video games black-and-white T.V. set, even 90° colour - Hi-fi amplifiers - Function generator...
When synchronization is necessary, use the circuit TEA2019.

MAIN FEATURES

- Direct drive of the switch-transistor
- Positive and negative output current up to 0.5 A.
- Current limitation
- Demagnetization sensing
- Total protection from over-load or short-circuit
- Output current is a function of the switch transistor collector current : $I_C = kI_B$ externally programmed
- Low rest current before starting
- 2 μs t_{on} min
- Thermal protection.

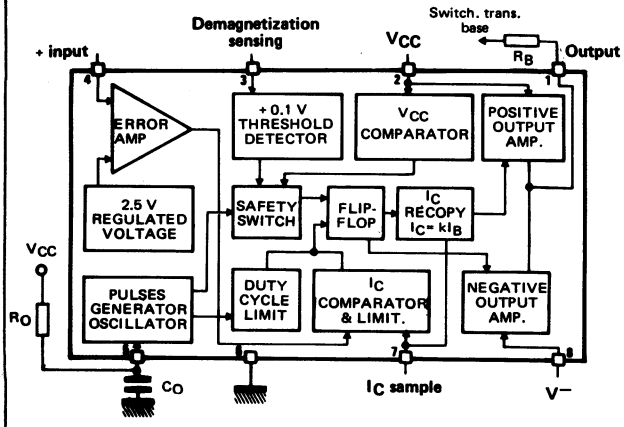
SWITCH-MODE POWER SUPPLY CONTROL CIRCUIT

CASE CB-98

DP SUFFIX
PLASTIC PACKAGE

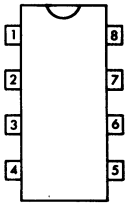
5

BLOCK DIAGRAM



The present pin configuration can be subject to modification.

PIN ASSIGNMENT



1. Output
2. Positive supply voltage
3. Demagnetisation sensing
4. Error amplifier non inverting input
5. Oscillator capacitor and resistor
6. Ground
7. I_C sample (negative)
8. Negative supply.

PP8205R1-A

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THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	$V_{(2-6)}$	15	V
Negative supply	$V_{(8-6)}$	-6	V
Total voltage	$V_{(2-8)}$	20	V
Output current	I_1	±0.5	A
Pin 3 input current	I_3	±5	mA
Junction temperature	T_j	+150	°C
Operating ambient temperature	T_{oper}	-20 to+ 70	°C
Storage temperature	T_{stg}	-40 to+150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance*	$R_{th(j-a)}$	80	°C/W

*Ex : 0.7 Watt in the I.C. makes its junction temperature grow 56°C over the ambient temperature.
To keep a good reliability a 100°C maximum junction working temperature is recommended.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{(2-6)}$	6	8	15	V
Negative auxiliary voltage	$V_{(8-6)}$	-1	-3	-6	V
Release voltage of the supply voltage (V_{CC} increasing)	$V_{(2-6)}$	–	5.8	–	V
Stop voltage of the supply voltage (V_{CC} decreasing)	$V_{(2-6)}$	–	4.8	–	V
Rest supply current before starting ($V_{(2-6)} < 5.5$ V)	$I_{(2-6)}$	–	1	–	mA
Current limitation threshold	$V_{(7-6)}$	–	-1	–	V
Current sample input resistance	R_7	–	1000	–	Ω
Demagnetization sensing threshold	$V_{(3-6)}$	–	0.1	–	V
Demagnetization sensing input current ($V_{(3-6)}$ = 0)	I_3	–	1	–	μA
Maximum conducting duty cycle	–	–	80	–	% T_o
Op. amplifier internally adjusted gain	–	–	50	–	–
Op. amplifier input current	I_4	–	-0.5	–	μA
Internal reference voltage	–	–	2.4	–	V
Reference voltage temperature drift	–	–	10^{-4}	–	V/°C
Oscillator frequency drift V/temp (V_{CC} = 8 V)	–	–	0.005	–	%/°C
Oscillator frequency drift V/V_{CC} (6 V < V_{CC} < 15 V)	–	–	0.05	–	%/V

GENERAL DESCRIPTION

The switch-mode principle is the fly-back discontinuous system working at fixed frequency when regulating. However a large lake of periods can occur, by the action of an over-load or a short-circuit of the load through the demagnetisation sensing that forbids any new period before the end of the secondary current.

Corresponding to each oscillator fly-back, a 2 μs pulse sets the flip-flop on starting the output current with a large positive pulse that allows a quick saturation of the switching transistor and a minimum t_{on} to discharge the R.D.C. network capacitor.

In normal regulating conditions, the output current is stopped (reset of the flip-flop) by the comparison between the switching power transistor current sampled on an emitter shunt resistor, and the error amplifier output. The sampling peak negative voltage at pin 7 is less than 1 volt. If it reaches 1 volt, it automatically resets the flip-flop, assuming a current limitation.

By no regulation condition, and if the current limitation is not reached, the flip-flop can be stopped before the end of the period by the duty-cycle limitation.

In order to save power, the positive base current, after the starting pulse, is an instantaneous function of the collector current sampled accross the shunt resistor. The ratio I_C / I_B can be programmed :

$$\frac{I_C}{I_B} = \frac{R_B}{R_e}$$

R_e must be first calculated to obtain the limitation current at 1 V.

R_B can be then taken to have a forced ratio I_C/I_B desired.

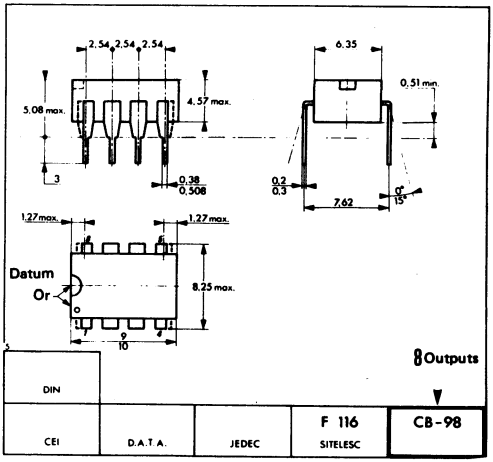
After the positive base current is stopped, the negative sink base current will occur after a fixed delay of about one microsecond. That allows the collector current a fast decreasing. 2 to 3 V negative voltage is necessary at pin 8. For low power units, it is easy to supply it from the shunt resistor.

Starting process :

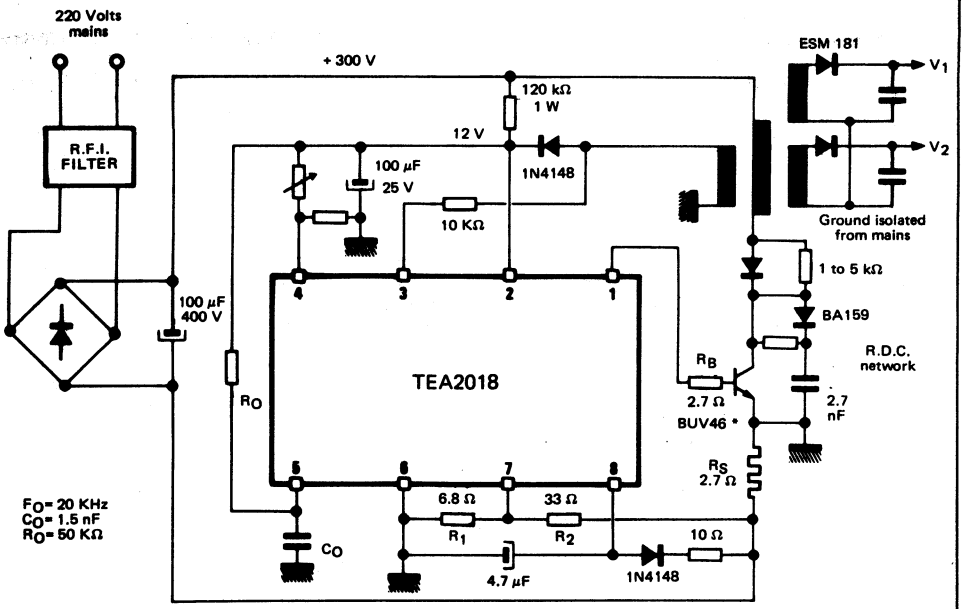
Before the voltage accross the V_{CC} capacitor reaches 5.8 V, no output pulse is delivered. The rest current is then about 1 mA. So that V_{CC} can be first supplied from the 300 V high voltage through a small power resistor. When the capacitor voltage reaches 5.8 V, it begins to supply pulses, and base current periods begin to occur. It makes the capacitor voltage decreasing. It can go down to 4.8 V without stop. But the auxiliary winding of the transformer comes then supplying V_{CC} giving it the wanted power.

CASE CB-98

DP SUFFIX
PLASTIC PACKAGE



60 WATT TYPICAL APPLICATION



I_C limit : 2.5 A - I_C normal working : 1.5 ⟶ 2.2 A.

Resistance calculation :

$$R_e = \frac{1\ V}{2.5A} = 0.4\ \Omega$$

To get a ratio $\frac{I_C}{I_B} = 7$, R_B must be : $7 \times R_e$

$$R_B = 2.8\ \Omega$$

values to be taken if the negative voltage is not supplied as following.

On this paper, R_{shunt} is taken largely higher than the R_e value calculated to supply a negative voltage at pin 8. The limit value of 1 volt at pin 7 is got from a low impedance parallel bridge to R_S (R_1 and R_2).
But the negative current rectified to pin 8 modifies about 12 % the R_S value with a 10 Ω series resistor used to smooth the rectified current.

*Switching transistor : BUV46 or other equivalent device.

The calculation of the bridge must also take in account the parallel resistance of the bridge. So after calculation, the 2.7 Ω resistor has an effective value of 2.2 Ω.

Bridge calculation : to get 2.5 A current limit :
2.5 A across 2.2 Ω ⟶ 5.5 V. To get 1 V at pin 7, the ratio $\frac{R_1}{R_1 + R_2}$ is $\frac{1}{5.5} = 0.17$

With $R_1 + R_2 = 40\ \Omega$:

$$R_1 = 6.8\ \Omega\ ;\ R_2 = 33\ \Omega$$

With these values, the negative voltage at pin 8 is about 2 to 2.5 volts at 2A peak collector current. The average power in R_S is less than 1 watt.
This is an example. Other values can be calculated in the same way.
V_{CC} at pin 2 has to be taken as low as possible (over 6 V) to decrease the I.C. dissipated power.

THOMSON SEMICONDUCTORS

TEA2019

PRODUCT PREVIEW

SWITCH-MODE POWER SUPPLY - CONTROL CIRCUIT

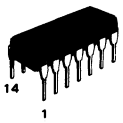
This circuit is a large diffusion, low cost integrated circuit, packaged in a 14 pin DIP case CB2, for the control of switch-mode power supplies in fly-back discontinuous mode.
It can be used, when the oscillator must be synchronized each time the power dissipated in the I.C. are compatible with the present data (useful power under 90 W).
The application range is very wide : Video display units - Video games black-and-white T.V. set, even 90° colour - Hi-fi amplifiers - Function generator...
The difference with the TEA2018 is the synchronous capability with internal PLL.

MAIN FEATURES

- Direct drive of the switch-transistor
- Positive and negative output current up to 0.5 A.
- Current limitation
- Demagnetization sensing
- Total protection from over-load or short-circuit
- Output current is a function of the switch transistor collector current : $I_C = kI_B$ externally programmed
- Low rest current before starting
- 2 μs t_{on} min
- Synchronization capability with internal PLL
- Saturation testing
- Thermal protection.

SWITCH-MODE POWER SUPPLY CONTROL CIRCUIT

CASE CB-2 (TO-116)



DP SUFFIX
PLASTIC PACKAGE

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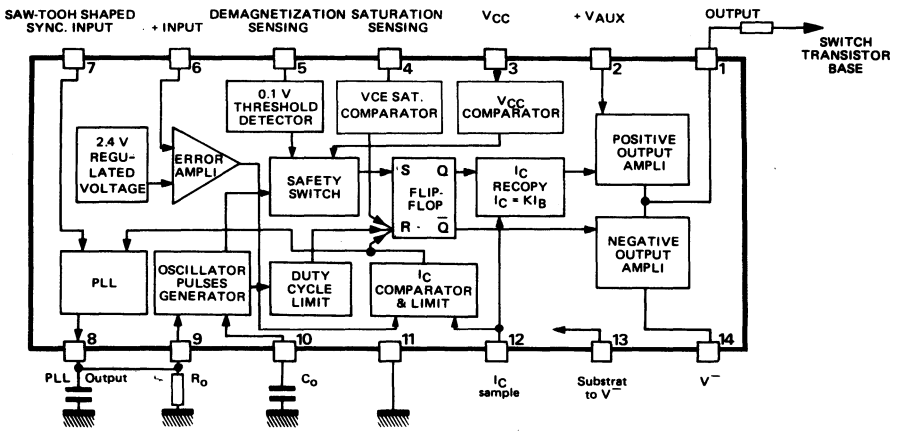
BLOCK DIAGRAM



PP8233R1-A 1/6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage V_{CC}	$V_{(3-1)}$	15	V
Auxiliary output supply voltage	$V_{(2-11)}$	15	V
Negative supply	$V_{(13\&14-11)}$	-6	V
Total voltage	$V_{(2\&3-13\&14)}$	20	V
Output current	I_1	±0.5	A
Pin 5 input current	I_5	5	mA
Pin 4 input current	I_4	5	mA
Junction temperature	T_j	+150	°C
Operating ambient temperature	T_{oper}	-20 to+ 70	°C
Storage temperature	T_{stg}	-40 to+ 150	°C

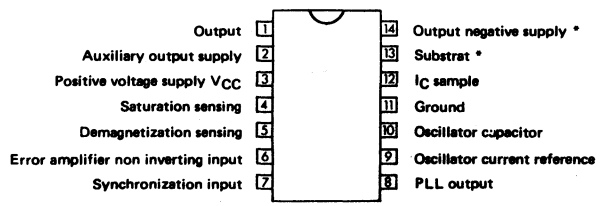
THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance*	$R_{th(j-a)}$	70	°C/W

*Ex : 0.8 Watt in the I.C. makes its junction temperature grow 56°C over the ambient temperature.

To keep a good reliability a 100°C maximum junction working temperature is recommended.

PIN CONFIGURATION



*Pin 13 and 14 have to be externally connected together.

ELECTRICAL CHARACTERISTICS

$T_{amb} = 25°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{(2\&3-11)}$	6	8	15	V
Negative auxiliary voltage	$V_{(13\&14-11)}$	-1	-3	-6	V
Release voltage of the supply voltage (V_{CC} increasing)	$V_{(3-11)}$	–	5.8	–	V
Stop voltage of the supply voltage (V_{CC} decreasing)	$V_{(3-11)}$	–	4.8	–	V
Rest supply current before starting ($V_{(3-11)} < 5.8$ V)	$I_{(3-11)}$	–	1	–	mA
Current limitation threshold	$V_{(12-11)}$	–	-1	–	V
Current sample input resistance	R_{12}	–	1000	–	Ω
Demagnetization sensing threshold	$V_{(5-11)}$	–	0.1	–	V
Demagnetization sensing input current ($V_{(5-11)} = 0$ V)	I_5	–	1	–	μA
Maximum conducting duty cycle	–	–	80	–	% T_o
Op amplifier internally adjusted gain	–	–	50	–	–
Op amplifier input current	I_6	–	–0.5	–	μA
Internal reference voltage	–	–	2.4	–	V
Reference voltage temperature drift	–	–	10^{-4}	–	V/°C
Oscillator frequency drift V/temp ($V_{CC} = 8$ V)	–	–	0.005	–	%/°C
Oscillator frequency drift V/V_{CC} ($6 V < V_{CC} < 15$ V)	–	–	0.05	–	%/V
SYNCHRONIZATION INPUT (PIN 7)					
Peak to peak saw-tooth voltage	V_{7PP}	–	2.5	–	V
Input impedance	R_7	–	60	–	kΩ
OSCILLATOR CURRENT REFERENCE (PIN 9) - $C_o = 1.5$ nF - $R_o = 68$ kΩ - $R_{8-9} = 50$ kΩ					
Frequency sensitivity		–	100	–	Hz/μA
Capture range	ΔF	–	±2.5	–	KHz
SATURATION SENSING (PIN 4)					
Input threshold	V_4	–	3.2	–	V
Input current ($V_4 > 3.2$ V)	I_4	50	–	–	μA
Input internal resistance		–	1	–	kΩ

5

GENERAL DESCRIPTION

The switch-mode principle is the fly-back discontinuous system working at fixed frequency when regulating. However a large lake of periods can occur, by the action of an over-load or a short-circuit of the load through the demagnetization sensing that forbids any new period before the end of the secondary current.

Corresponding to each oscillator fly-back, a 2 μs pulse sets the flip-flop on starting the output current with a large positive pulse that allows a quick saturation of the switching transistor and a minimum t_{on} to discharge the R.D.C. network capacitor.

In normal regulating conditions, the output current is stopped (reset of the flip-flop) by the comparison between the switching power transistor current sampled on an emitter shunt resistor, and the error amplifier output. The sampling peak negative voltage at pin 12 is less than 1 volt. If it reaches 1 volt, it automatically resets the flip-flop, assuming a current limitation.

By no regulation condition, and if the current limitation is not reached, the flip-flop can be stopped before the end of the period by the duty-cycle limitation.

In order to save power, the positive base current, after the starting pulse, is an instantaneous function of the collector current sampled accross the shunt resistor. The ratio I_C / I_B can be programmed :

$$\frac{I_C}{I_B} = \frac{R_B}{R_e}$$

R_e must be first calculated to obtain the limitation current at 1 V.
R_B can be then taken to have a forced I_C/I_B desired ratio.

After the positive base current is stopped, the negative sink base current will occur after a fixed delay of about one microsecond. That allows the collector current a fast decreasing. 2 to 3 V negative voltage is necessary at pin 14. For low power units, it is easy to supply it from the shunt resistor.

Starting process :

Before the voltage across the V_{CC} capacitor reaches 5.8 V, no output pulse is delivered. The rest current is then about 1 mA. So that V_{CC} can be first supplied from the 300 V high voltage through a small power resistor. When the capacitor voltage reaches 5.8 V, it begins to supply pulses, and base current periods begin to occur. It makes the capacitor voltage decreasing. It can go down to 4.8 V without stop. But the auxiliary winding of the transformer comes then supplying V_{CC} giving it the wanted power.

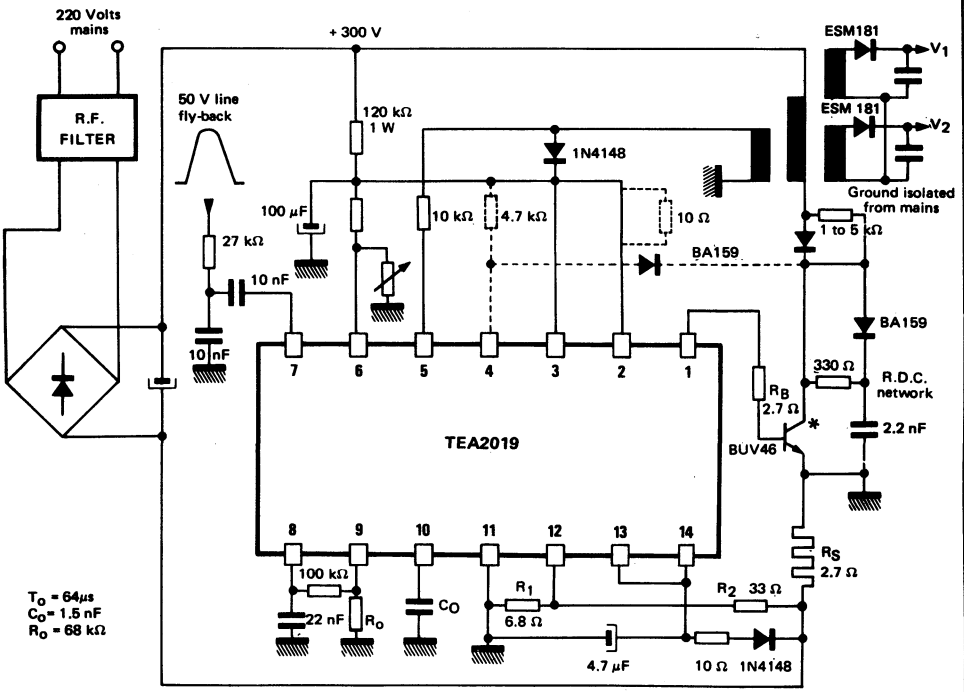
The TEA2019 has some additional capabilities as regards to the TEA2018.

- The oscillator charge current is made through an internal current generator, programmed externally instead of an external charge resistor. The saw-tooth so provided is linear.
- The oscillator can be synchronized through an internal PLL circuitry, that makes the end of the switching transistor current synchronous with the external synchro pulse.
This synchro pulse can be, for example, the fly-back pulse of a T.V. horizontal sweep circuit. It must be integrated in a R.C. network to make a low voltage saw-tooth that must be introduced at pin 7, as indicated on the application sheet.
The PLL output voltage - pin 8 - supplies a correction current to pin 9 through an external resistor, to keep the oscillator at the right frequency.
The synchronization operates only when regulating.
- In the TEA2019, the positive output power supply is separated from the low signal general supply, so that it can be supplied from a lower voltage, in order to decrease the IC dissipated power.
For low power units, the IC can be normally supplied by connecting pins 2 and 3 together.
- In order to protect the substrat, pin 13, from the parasitic voltage peaks due to the negative peak output current at pin 14, the substrat, (pin 13) is separated from the negative supply (pin 14). They must be externally connected.
- The switching transistor saturation voltage can be watched over at pin 4. Then a high voltage diode must be connected between the collector of the switching transistor, pin 4, and a resistor to V_{CC} (see application diagram page 5).
If a too low base current value has been choosen the saturation voltage can be too high, so, with this network, when V_{CEsat} goes over 2.5 V, the base current is then stopped before the normal end of the period.

REMARK : The TEA2019 can work without this protection.

60 WATT TYPICAL APPLICATION

LINE SYNCHRONIZED



*Switching transistor : BUV46 or other equivalent device.

I_C limit : 2.5 A - I_C normal working : 1.5 ⟶ 2.2 A.

Resistance calculation :

$$R_e = \frac{1\ V}{2.5A} = 0.4\ \Omega$$

To get a ratio $\frac{I_C}{I_B} = 7$, R_B must be : 7 x R_e

$$R_B = 2.8\ \Omega$$

values to be taken if the negative voltage is not supplied as following.

On this paper, R_{shunt} is taken largely higher than the R_e value calculated to supply a negative voltage at pins 13 &14. The limit value of 1 volt at pin 12 is got from a low impedance parallel bridge to R_S (R_1 and R_2).
But the negative current rectified to pins 13 & 14 modifies about 12 % the R_S value with a 10 Ω series resistor used to smooth the rectified current.

The calculation of the bridge must also take in account the parallel resistance of the bridge. So after calculation, the 2.7 Ω resistor has an effective value of 2.2 Ω.

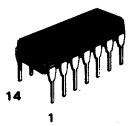
Bridge calculation : to get 2.5 A current limit :
2.5 A across 2.2 Ω ⟶ 5.5 V. To get 1 V at pin 12, the ratio $\frac{R_1}{R_1 + R_2}$ is $\frac{1}{5.5} = 0.17$

With $R_1 + R_2 = 40\ \Omega$:

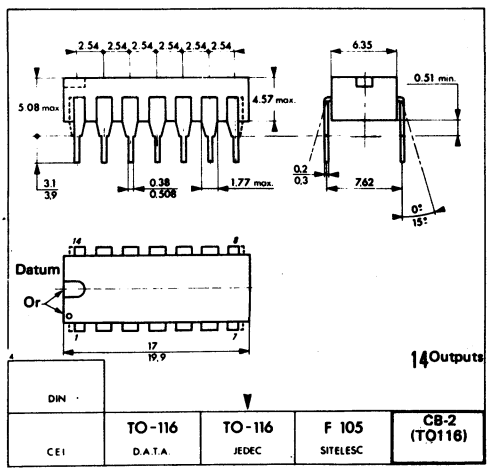
$$R_1 = 6.8\ \Omega\ ;\ R_2 = 33\ \Omega$$

With these values, the negative voltage at pins 13 & 14 is about 2 to 2.5 volts at 2A peak collector current. The average power in R_S is less than 1 watt.
This is an example. Other values can be calculated in the same way.
V_{CC} at pin 2 has to be taken as low as possible (over 3 V) to decrease the I.C. dissipated power.

CASE CB-2 (TO-116)



DP SUFFIX
PLASTIC PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

UAA4001

SWITCH MODE POWER SUPPLY CONTROLLER

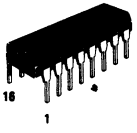
The UAA4001 is a monolithic IC intended for power transistor control in single transistor DC-DC converters (Fly back type).

- Direct drive of the switching transistor
- Complete PWM power control circuitry
- Up to ± 1 A peak base current output
- Output transistor V_{CEsat} sensing
- Output transistor current limitation
- Under and over voltage lockout
- Programmable soft-start
- Thermal overload protection
- Regulation better than 0.2 %
- On-chip low drift 2.5 V reference
- 50 kHz max operating frequency

*The average current is limited by the package power dissipation.

SWITCH MODE POWER SUPPLY CONTROLLER

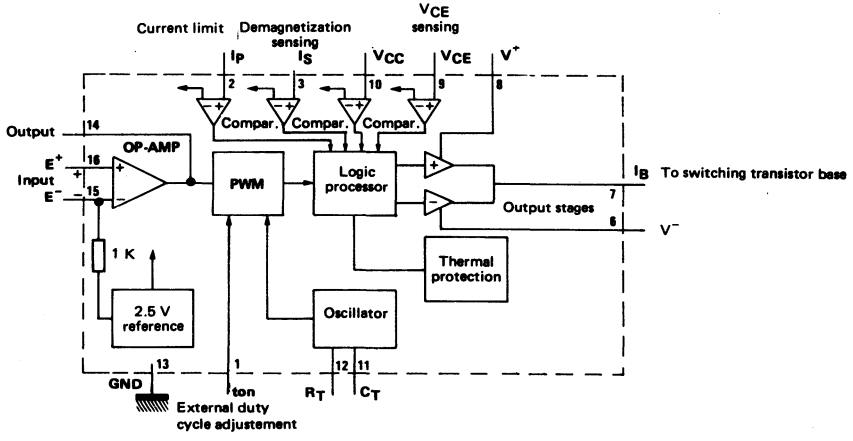
CASE CB-79



DP SUFFIX
PLASTIC PACKAGE

5

BLOCK DIAGRAM

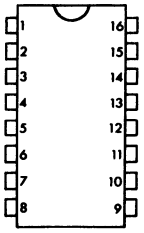


NT8109R1-A

PIN CONFIGURATION

1	$t_{on\ max}$	$t_{on\ max}$ external adjustment and soft-start
2	I_P	Primary current limit input
3	I_S	Secondary current monitoring input
4	N.C.	
5	N.C.	
6	V^-	Negative output stage supply
7	I_B	Output
8	V^+	Positive output stage supply
9	V_{CE}	V_{CEsat} sensing
10	V_{CC}	V_{CC}
11	C_T	C_T oscillator external capacitor
12	R_T	R_T oscillator external resistor
13	GND	Ground
14	V_O	Op-amp. output
15	E^-	Op-amp. inverting input - V_{ref}
16	E^+	Op-amp. non inverting input.

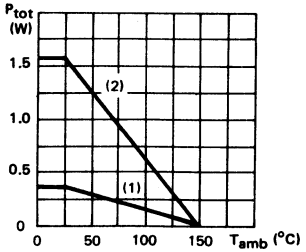
CASE CB-79



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage V_{CC}/ground	$V_{CC} - GND$	+ 15	V
Positive supply for the output stage	$V^+ - GND$	+ 15	V
Negative supply for the output state : Substrate/Ground	$V^- - GND$	- 7	V
Voltage between pins 10 and 6	$V_{CC} - V^-$	+ 20	V
Output current pulsed	I_B	± 1.5	A
Pin 9 current	I_{CE}	10	mA
Pin I_P max input current	I_P	± 5	mA
Pin I_S max input current	I_S	± 5	mA
Junction temperature	T_j	- 40, + 150	°C
Storage temperature	T_{stg}	- 40, + 150	°C

MAXIMUM POWER DISSIPATION



$T_j < 150°C$

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C ; V_{CC} = 10 V ; V^- = - 5 V ; V^+ = + 4 V (Unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	–	10	14	V
Supply quiescent current	I_{CC}	–	18	25	mA
Positive output stage supply voltage	V^+	–	4	V_{CC}	V
Negative output stage supply voltage	V^-	- 6	- 5	–	V
V_{CC} threshold to insure operation (V_{CC} increasing)	V_{CCL}	6	6.5	7	V
Hysteresis on V_{CC} threshold	ΔV_{CC}	–	0.6	–	V
Primary current limit input threshold	V_{IP}	–	± 0.2	–	V
Pin 2 input current (V_{IN} = 0 V)	I_P	–	4	20	µA
Output transistor saturation voltage (Pin 9 voltage must be 3 V above ground)					
Positive stage (I_B = 1 A)	V^+_{CE}	–	1	1.5	V
Negative stage (I_B = 1 A)	V^-_{CE}	–	1	–	V
Secondary current monitoring input threshold	V_{IS}	–	100	–	mV
Pin 3 input current (V_{IN} = 0 V)	I_S	–	2	+ 10	µA
V_{CE} input threshold	V_{CE}	–	5	–	V
Op-amp. open loop gain	A_{VOL}		100.000		
Op-amp. external feed back resistor	R_f	50	–	–	kΩ
Op-amp. input current	I_B	–	50	250	nA
Op-amp. offset voltage	V_{IO}	–	2	7	mV
Op-amp. inverting input resistance to V_{ref}	R_{IN}	–	1	–	kΩ
Internal reference voltage	V_{ref}	2.4	2.55	2.7	V
Ref. voltage variation with temperature - 25°C < T_a < + 85°C	ΔV_{ref}	–	± 1	–	%
R_T optimal current	I_{RT}	–	0.5	–	mA
Oscillator operating frequency range		5	–	50	kHz
Oscillator frequency temperature coefficient		–	100	–	ppm/°C
Oscillator free running frequency equation (I_{R_T} = 0.5 mA)			$f = \frac{1.85}{R_T \cdot C_T}$		Hz
Maximum limit of conduction time (Pin 1 open)					
$V_{CC} < V_{CCL}$		–	0	–	% of
$V_{CCL} < V_{CC} < 14$ V		–	50	–	oscillator
$V_{CC} > 14$ V		–	0	–	period
Maximum duty cycle (set externally)					
0.2 V < $V_{t_{on}}$ < 0.375 V_{CC}		–	90	–	% of
0.375 V_{CC} < $V_{t_{on}}$ < 0.625 V_{CC}		–	according	–	oscillator
0.625 V_{CC} < $V_{t_{on}}$		–	to $V_{t_{on}}$ 0	–	period

CIRCUIT DESCRIPTION

OSCILLATOR

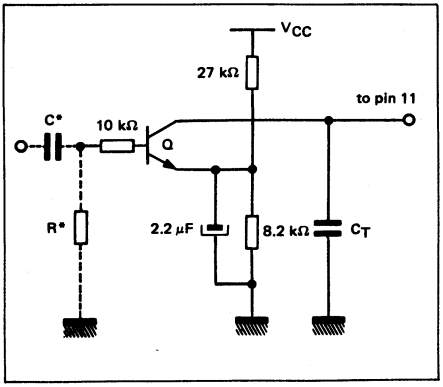
This is a sawtooth generator which free-running frequency is set externally by resistor R_T and capacitor C_T.
The charge current of the capacitor is $I = V_{CC}/2\ R_T$, the peak and valley voltages of the sawtooth are respectively 0.625 V_{CC} and 0.375 V_{CC}. The discharge current is about 12 times greater than the charge current.

The oscillator free-running frequency is $f_O = \frac{1.85}{R_T . C_T}$

Synchronization

For some applications, it may be desirable to synchronize the internal oscillator of the UAA4001 with an external oscillator.

The following typical diagram illustrates this arrangement:



- Synchronization pulses must have the following characteristics :

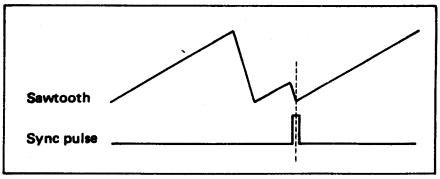
$$\frac{V_{CC}}{2} < \text{amplitude} < V_{CC}\ ,\ 5\ \% < \frac{t}{T} < 20\ \%$$

where $\frac{t}{T}$ is the duty cycle.

*If the duty cycle is higher than 10 %, an RC differentiator network will be added. Its time constant τ should be related to the oscillator period so that $10\ \% < \frac{\tau}{T} < 20\ \%$.

- The transistor Q is driven into conduction by the synchronization pulse. It discharges capacitor C_T below the oscillator low threshold. That way, C_T charging time increases which in turn lowers the oscillator frequency. A frequency of $F_{free} > F_{sync}$ has to be selected.
The proposed arrangement allows, in a frequency range from 5 kHz to 50 kHz, the synchronizing frequency to deviate from the oscillator frequency by an amount of up to 20 %.

However it is necessary not to exceed this amount in order to avoid secondary sawtooth as shown on the following diagram.



This phenomenon may also happen if the synchronization pulse is too short.

PULSE - WIDTH MODULATOR (PWM)

Main modulator

This modulator produces a square wave whose duty cycle results from a comparison between the sawtooth and the output of the operational amplifier. The output is set OFF during the return of the sawtooth.

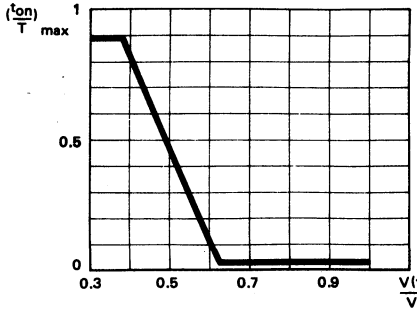
Auxiliary modulator

The voltage V (t_{on}) applied to pin 1 sets the maximum duty cycle.

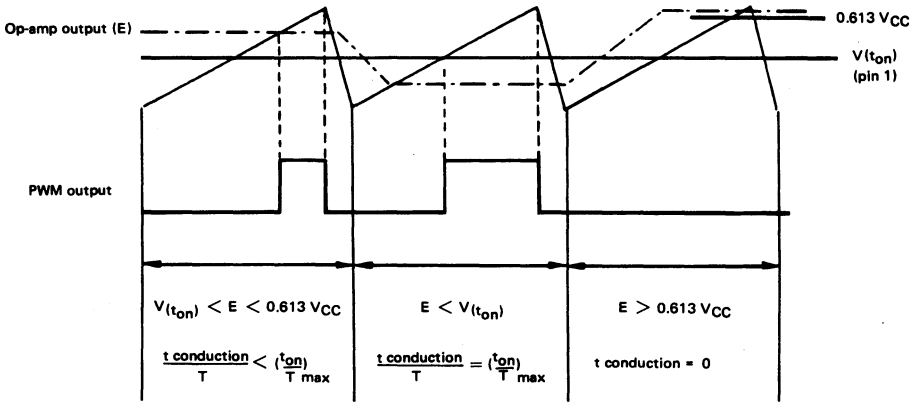
An internal voltage divider between V_{CC} and ground presets the maximum ON time to 50 % of the period. This limit can be externally altered by paralleling two external resistors across the internal divider ones. These resistors should be lower than the 30 kΩ internal resistors.

Minimum conduction time

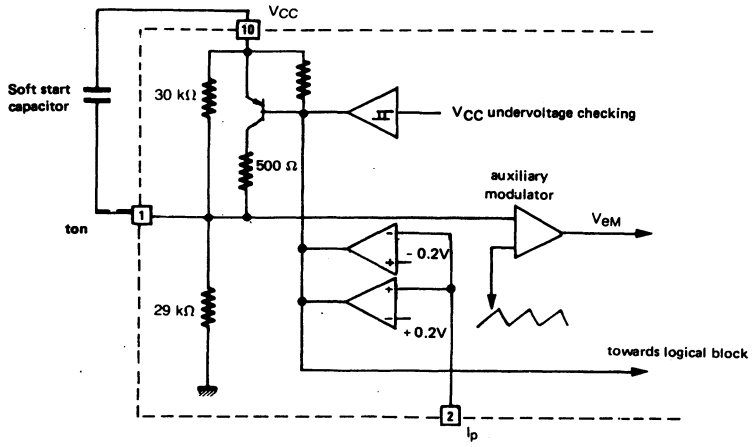
In order to allow the discharge of the snubber network, a minimum on-time is set at about 5 % of the period. Any attempt to set a lower value results in a no-conduction state.



MAXIMUM DUTY CYCLE AS A FUNCTION OF VOLTAGE ON PIN 1 NORMALIZED TO V_{CC}



OPERATION OF THE PWM DUTY CYCLE LIMITATIONS



INTERNAL CIRCUIT CONFIGURATION RELATED TO PIN 1

PROTECTION ELEMENTS

V_{CC} supply check

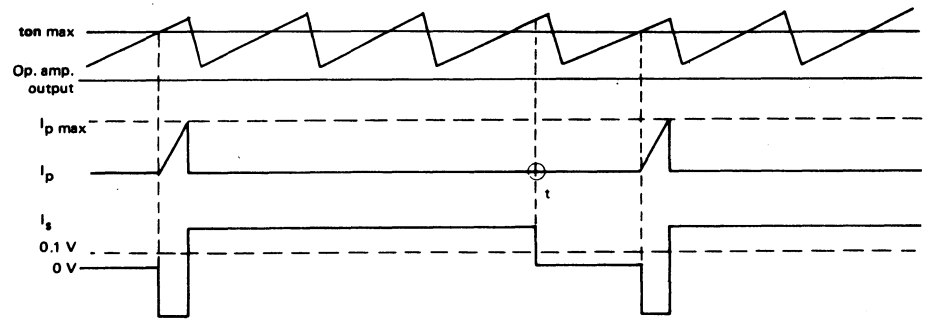
A comparator pulls pin 1 up to V_{CC} as long as V_{CC} has not reached 6.5 V, or if V_{CC} exceeds 14 V. A soft start can be achieved by connecting a capacitor between pin 1 and ground or V_{CC} (see figure above).

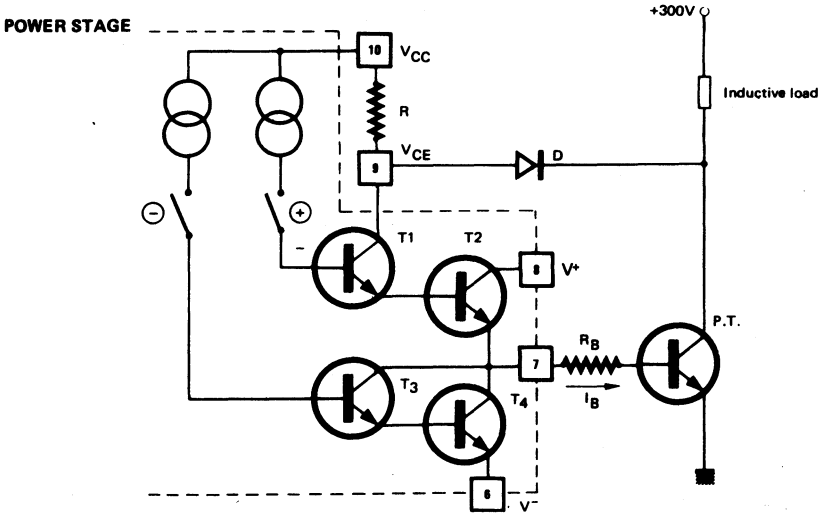
Primary current limitation

The primary current is measured across a shunt, and compared to reference voltage of + 0.2 V and −0.2 V respectively. When the detector senses an over-current, the output is turned off. The information coming from the comparators is also transmitted to pin 1 , so that, during a permanent overload, the external capacitor integrates the oversteps, thus reducing the duty cycle.

Secondary current

An internal comparator which threshold is 0.1 volt checks after each oscillator period that the secondary current has been completely drained to zero before storing energy again in the primary inductance, thus avoiding excess of core magnetization. When a secondary winding is continuously short-circuited, the total flow of current I_s spreads over several periods, during which the output is inhibited.





SIMPLIFIED CIRCUIT OF THE OUTPUT STAGES

Positive stage

A feed-back loop provides an output current matched to the instantaneous requirement of the switching transistor. The higher the level of saturation of this transistor, the greater proportion of the current flowing through resistor R is shunted by diode D. Thus the base current of T_2, and consequently the output current of the IC, decreases.

Transistor T_1 remains saturated. The voltage V_{CE} of the power transistor (P.T.) is given approximately by :

$$(V_{CE})\ P.T. = (V_{BE})\ P.T. + R_B.I_B$$

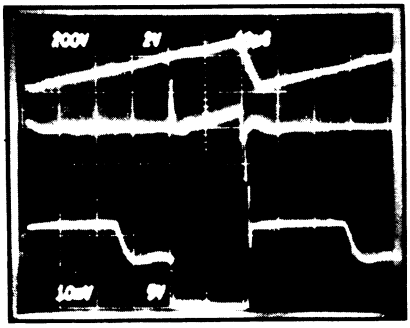
Resistor R_B stabilizes the feed-back loop. Its value must be as low as possible, generally around 1 Ω.

Negative stage

As the voltage V_{CE} of the switching transistor rises above 5 V, the negative stage of the UAA4001 is set into conduction. Transistors T_3 and T_4, in a darlington configuration, apply a high reverse base current to the switching transistor, which results in a very fast turn-off.

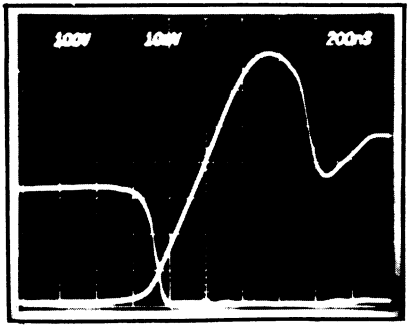
For further information concerning the UAA4001 internal structure, please refer to application note NA-011 A edited by THOMSON SEMICONDUCTORS

TYPICAL WAVEFORMS



Oscillator V_8
2 V/div
Base current
1 A/div
Collector
voltage
200 V/div

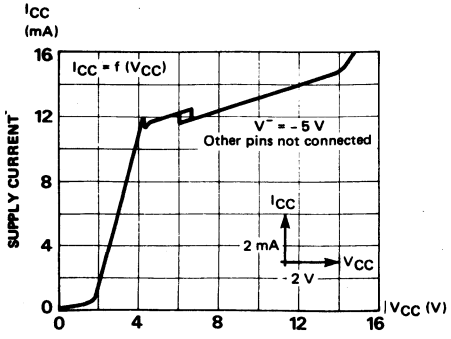
SWITCHING TRANSISTOR BASE CURRENT AND COLLECTOR VOLTAGE DURING ONE OSCILLATOR PERIOD



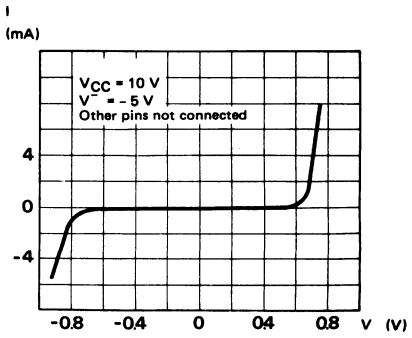
VCE : Collector voltage 100 V/div

I_C : Collector current 1 A/div

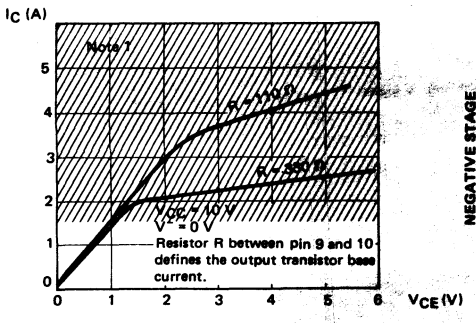
SWITCHING TRANSISTOR COLLECTOR VOLTAGE AND CURRENT



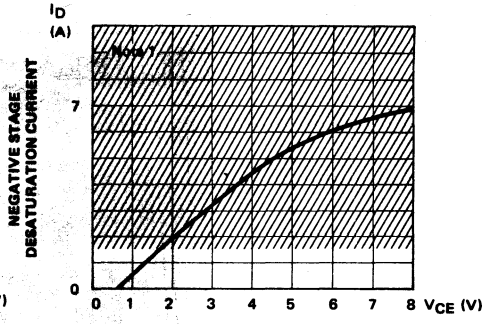
SUPPLY CURRENT I_{CC} AS A FUNCTION OF SUPPLY VOLTAGE



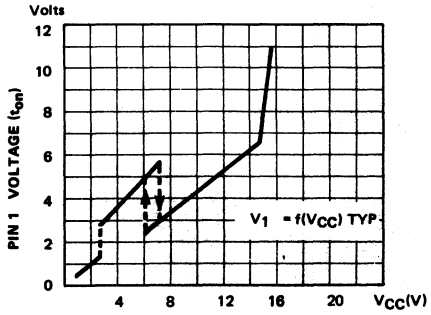
PIN 2 AND 3 CURRENT - VOLTAGE CHARACTERISTICS



POSITIVE STAGE OUTPUT
TRANSISTOR COLLECTOR CHARACTERISTICS



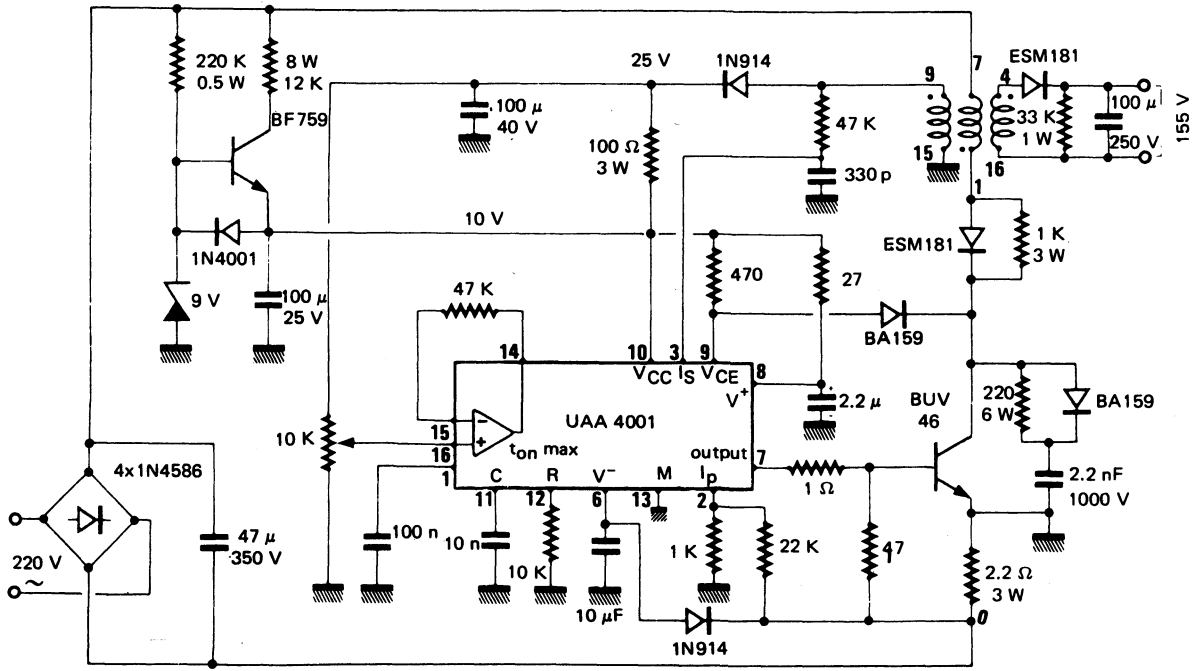
NEGATIVE STAGE OUTPUT
TRANSISTOR COLLECTOR CHARACTERISTICS



SUPPLY VOLTAGE

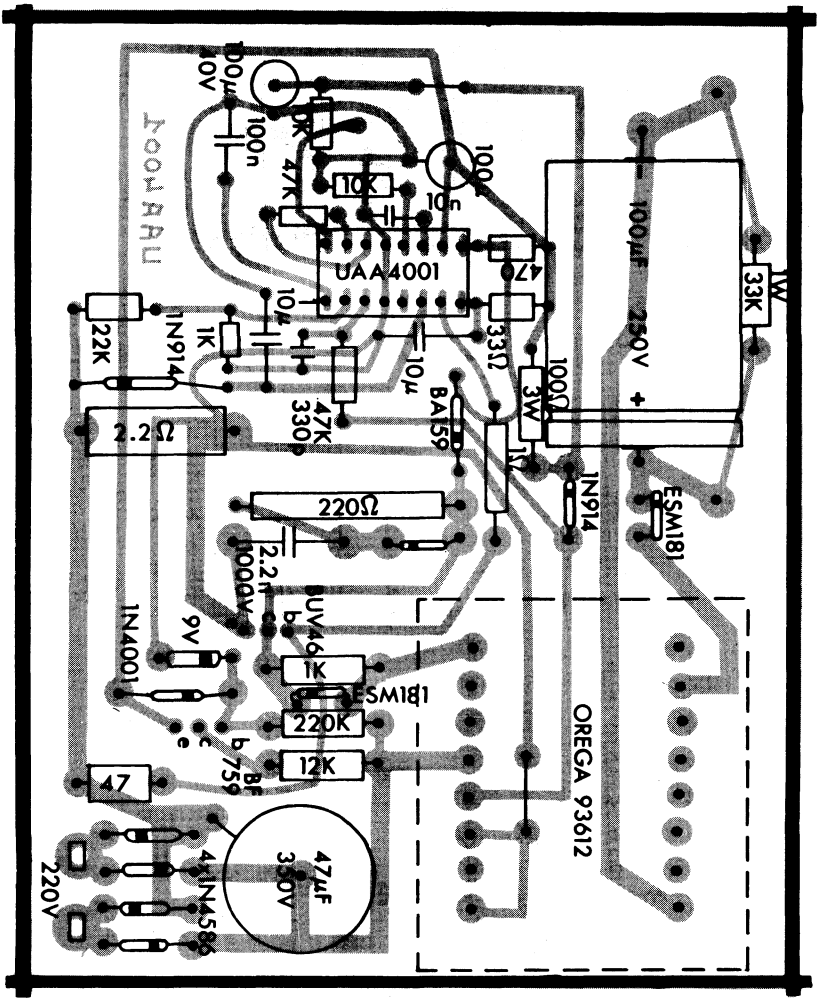
Note 1 : Operation in the shadowed area is strictly forbidden in order to avoid permanent damage to the device. Power supply currents have to be limited to 1.5 A.

TYPICAL APPLICATION : 100W FLY-BACK CONVERTER

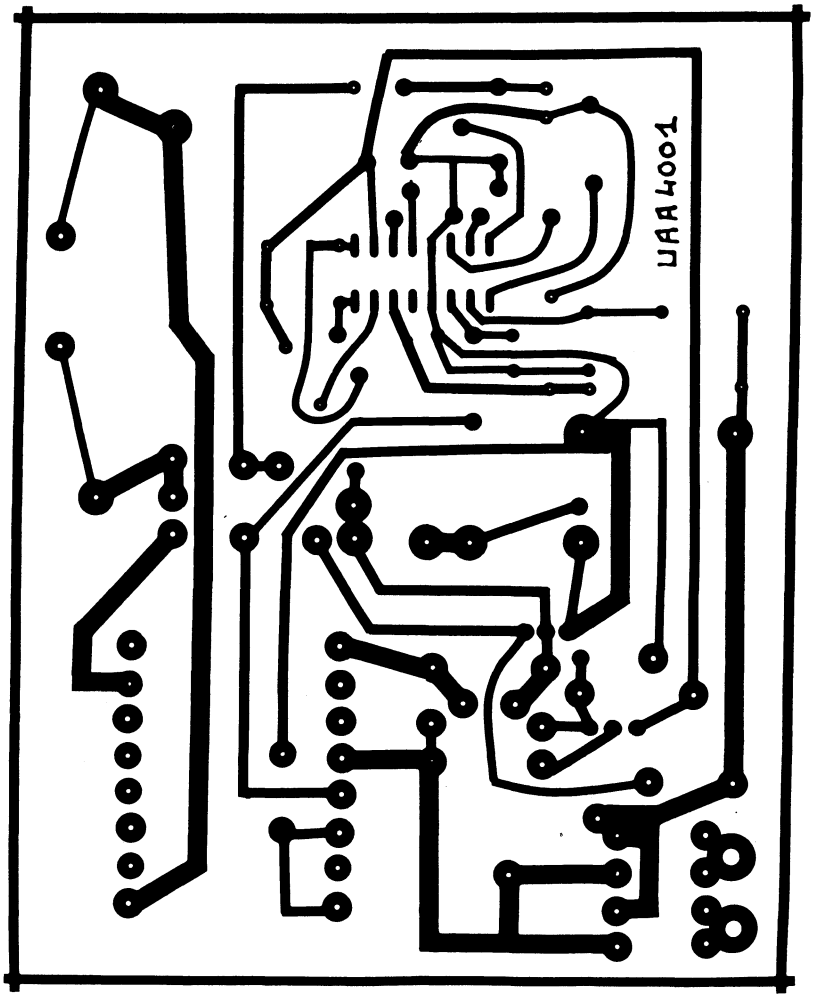


TRANSFORMER TYPE IS OREGA 93612

COMPONENT LAYOUT

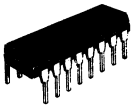


COPPER SIDE

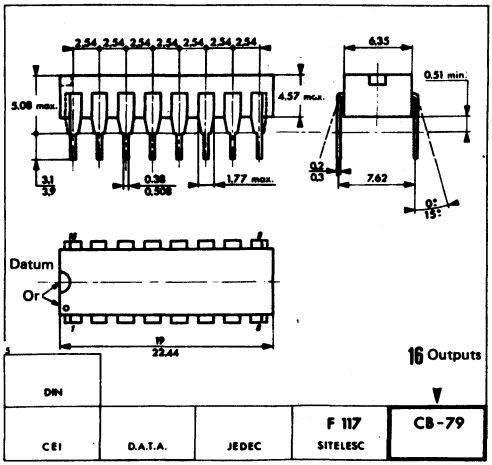


FOR MORE DETAILS ON THIS APPLICATION AND ON THE UAA4001,
REPORT TO APPLICATION NOTES NA-011 AND NA-019

CASE CB-79



DP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTORS

UAA4006

ADVANCE INFORMATION

REGULATOR FOR SWITCH MODE POWER SUPPLY

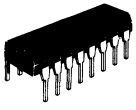
The UAA4006 is a regulation and control device for fly back switch mode power supplies using one transistor.

- Includes oscillator, PWM and error amplifier
- Soft start
- Direct drive of the switching transistor
- Self-regulated positive base current (peak 1.5 A)
- Negative base current providing fast turn-off, and allowing the best use of the safe operating area (peak 1.5 A)
- Switching transistor protected against saturation failure
- Immediate limitation of the collector current
- Positive power supply check
- On chip thermal protection
- Adjustable minimum conducting time or no-conduction for use of a snubber circuit
- Steady internal reference voltage
- Start-up with very low supply current.

REGULATOR FOR SWITCH MODE POWER SUPPLY

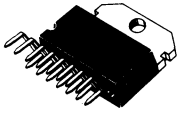
CASES

CB-79



DP SUFFIX
PLASTIC PACKAGE

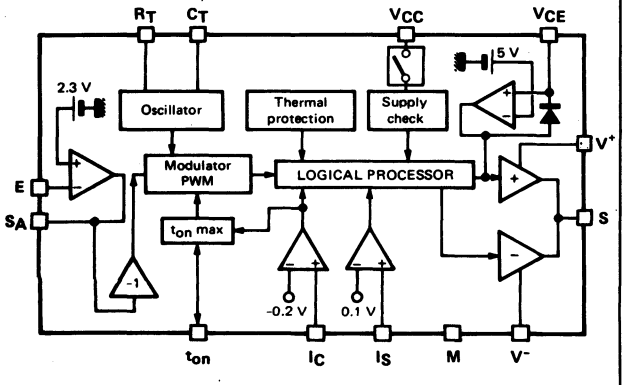
CB-501



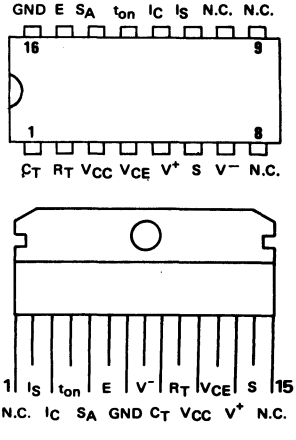
SP SUFFIX
PLASTIC PACKAGE

5

BLOCK DIAGRAM



PIN ASSIGNMENT



SP8211R1-A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 15	V
Supply voltage V^+ V^-	 V^+ V^-	 + 15 - 6	 V V
Voltage between pin 11 and 13	$V^+ - V^-$	+ 18	V
Output current	I_S	± 1.6	A
Current into input I_C (internal protaction diodes)		± 5	mA
Current into input I_S		± 5	mA
Minimum value of resistance R_T	R_T	10	KΩ
Junction temperature	T_j	- 40+ 150	°C
Storage temperature	T_{stg}	- 40+ 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal resistance Junction-ambient Junction-case	 $R_{th(j-a)}$ $R_{th(j-c)}$	 50 7	 °C/W °C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25° C ; V_{CC} = 10 V ; V^- = –5 V (unless otherwise noted).

Characteristic	Min	Typ	Max	Unit
Supply voltage V_{CC} (rise/fall)	7.2/6.2	–	15	
Current I_{CC} (V_{CC} < 7 V) or (V_{CC} < 6 V)	–	0.4	1	mA
Current I_{CC} (V_{CC} = 10 V)	–	10	–	mA
Supply voltage V^+	4	–	15	V
Supply voltage V^-	0	–	- 6	V
Threshold of input I_C	–	–0.15	–	V
I_C input current ($V(I_C)$ = 0 V)	–	5	20	µA
Threshold of input I_S	–	0.1	–	V
I_S input current ($V(I_S)$ = 0 V)	–	5	20	µA
OP ampli open loop gain	60	–	–	dB
OP ampli offset voltage	–	5	–	mV
Internal reference voltage	–	2.3	–	V
Oscillator frequency	–	$2/R_TC_T$	50	KHz
Value of resistance R_T	30	50	150	KΩ
Dead time (R_{ton} < 0.2 R_T)	–	0.1 T	–	
Output current ($V^+ - V_S$ = 3 V ; $V_S - V^-$ = 3 V)	± 1.5	–	–	A
V_{CE} comparator threshold voltage	–	5	–	V
t_{on} min adjustable range	1	–	10	µs
Max duty cycle $(\frac{t_{on}}{T})_M$	–	$1 - \frac{R_{ton}}{2R_T}$		

CIRCUIT DESCRIPTION

OSCILLATOR

It is a sawtooth generator whose fall time is much inferior to rise time. The period is $T = 0.5\ R_T C_T$.
The voltage swing is about $V_{CC}/2$ and the low level is 1.5 V.
The maximum working frequency is 50 KHz.
Resistor R_T also adjusts the t_{on} min duration (see logical processor).

PULSE WIDTH MODULATOR (PWM)

A signal with a variable duty cycle is generated by a comparison between pin C_T voltage (oscillator) and a voltage equal to $(V_{CC} - 3\ V - V_A)$ where V_A is the output voltage of the error amplifier.
A second comparator limits the maximum conduction ratio by a comparison between the sawtooth and pin t_{on} voltage. If $V(t_{on}) = 0$, there is an internal fixed dead time ($\simeq 0.1T$).
The maximum duty cycle is :

$$\left(\frac{t_{on}}{T}\right)_M = 1 - \frac{R_{ton}}{2R_T}$$

CURRENT LIMITATION

A level lower than – 0.15 V on pin I_C involves two actions :

- A direct action through a logic processor which stops the drive until the end of the period.
- An indirect action through the t_{on} function. The change of state at the output of comparator I_C is applied to pin t_{on} as long as the current overload stands. By inserting capacitor C_B between pin t_{on} and V_{CC} (about 0.1 μF), the voltage at this point rises up from a quantity ΔV proportional to the duration and the frequency of the oversteps. This will consequently lower the maximum conduction ratio, thus decreasing the frequency of the oversteps.
At the end of an overload state, capacitor C_B slowly charges up through a 20 K internal impedance, in order to come back progressively to normal operation.
This capacitor also achieves a slow start during power-up.

NOTE : If capacitor C_B is omitted direct action will only be implemented.

SUPERVISION OF THE SECONDARY CURRENT

A new cycle of conduction can only begin after the secondary current has completely decreased down to zero, in order to avoid the magnetization of the transformer core, in case of short circuit or heavy overload on the secondary winding.
The zero crossing of the secondary current is detected by comparator I_S whose threshold is 0.1 V.

ERROR AMPLIFIER

It is an operational amplifier whose open loop gain is greater than 1000.
The input currents are lower than 1 μA, and the input offset voltage is lower than 5 mV. The input common mode voltage can range from 0 V to $(V_{CC} - 3\ V)$.

PROTECTION AGAINST DESATURATION

If, because of a too low base current or a too heavy load, voltage V_{CE} on the switching transistor goes beyond 4.5 V approximately, the output of comparator V_{CE} swings, and the drive is interrupted.

START SWITCH

An internal switch is inserted between pin V_{CC} and the internal V_{CC} supply line. At power-up, this switch closes down when V_{CC} reaches 7.2 V. The leakage current $(I_{CC})_L$ is about 0.4 mA before the switch gets closed. This original feature enables the start of the converter by means of a high value resistance directly connected between V_{CC} and the high voltage supply.
The smoothing capacitor on V_{CC} supply provides the energy required for the start.
At last, V_{CC} must go below 6.2 V to turn the internal switch off.

THERMAL PROTECTION

It is active when the temperature of the junction reaches 160°C.

LOGICAL PROCESSOR

A logical unit processes the informations coming from the fault detectors, and ensures that the output signal fulfils two conditions :

- No double pulse inside a period : the occurrence of a defect is memorized until the end of the period.
- To allow the discharge of a snubber network, the minimum width of the output pulse is settled at a given value t_{on} min through an internal monostable.

If this monostable is not triggered, there is no conduction.
The duration t_{on} min is programmable with resistor R_T through the relationship :

$$t_{on}\ \text{min} = 0.09\ R_T - 2$$
$$(\mu s) \qquad (k\Omega)$$

OUTPUT STAGE

ON-state

The positive stage achieves a very efficient drive of the switching transistor.
Its features are essentially :

- Direct drive (neither inductance, nor transformer).
- The transistor stays in a quasi-saturation mode, and thus has a reduced storage time.
- The drive energy is strictly limited to what is necessary.
- Easy implementation.

K_1 is closed to turn the positive stage on. The maximum value of the positive base current is settled by the limitation resistor R.
Diode D keeps Q in a quasi-saturation mode : the more Q gets saturated, the more diode D will derive an important part of the drive current i_{B1}, through diode D_1.
Resistor R_B has a low value (about 1 Ω), and is used to stabilize the regulation loop.
For a good efficiency of the negative drive, it should be kept as low as possible.
Integrated Darlington T_1 is able to supply a peak current of 1.5 A with a 2 V saturation voltage.
The voltage V_{CE} on transistor Q is :
$V_{CE} \simeq V_D + R_B I_{B1}$

OFF-state

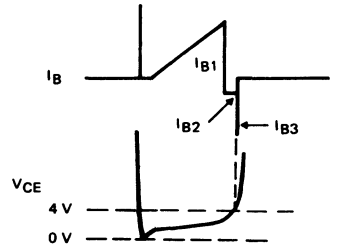
The turn off is done in two steps :

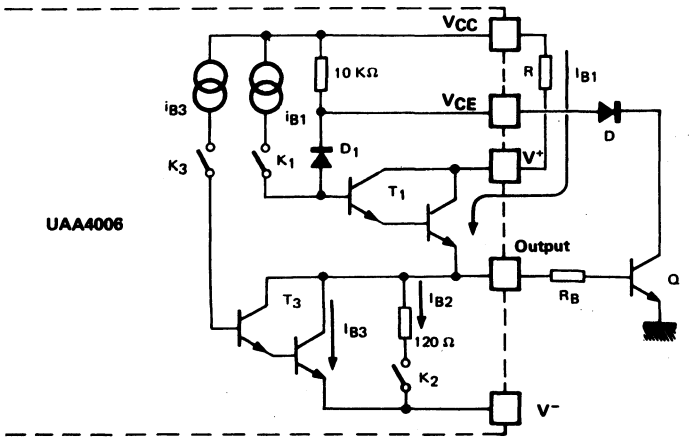
- An immediate action thanks to K_2 which connects the base of the switching transistor to the negative supply through a 120 Ω integrated resistor (current I_{B2}).
- A delayed action through K_3 which is closed only after the desaturation of the external transistor.

This moment is detected by comparator V_{CE}, when V_{CE} reaches 4 V.
Darlington T_2 can supply 1.5 A with a 2 V saturation voltage (current I_{B3}).

NOTE : The negative drive I_{B3} for the removal of the stored charges is delayed in order to limit the slope dI_B/dt at the on-off transition. A high dI_B/dt might indeed lead to a destructive overheating of the base-collector junction (see "The power transistor in its environment" Thomson-CSF Division Semiconducteurs Discrets).

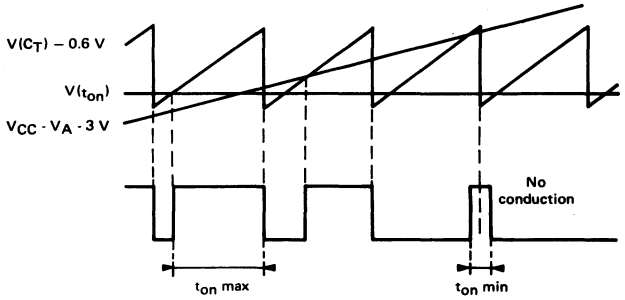
SELF REGULATED BASE CURRENT $I_B = f(V_{CE})$



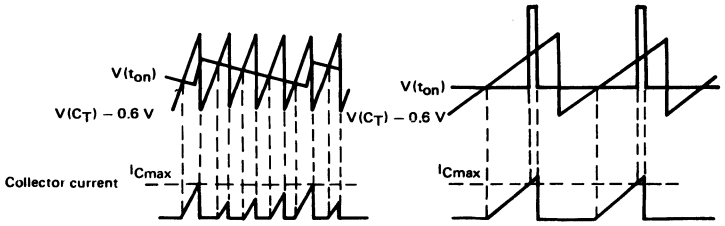


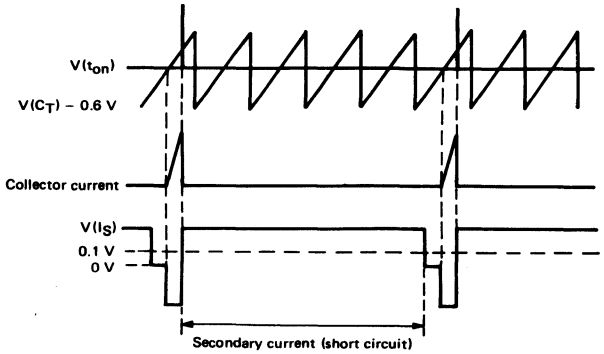
TYPICAL WAVEFORMS

LIMITS OF THE DUTY CYCLE

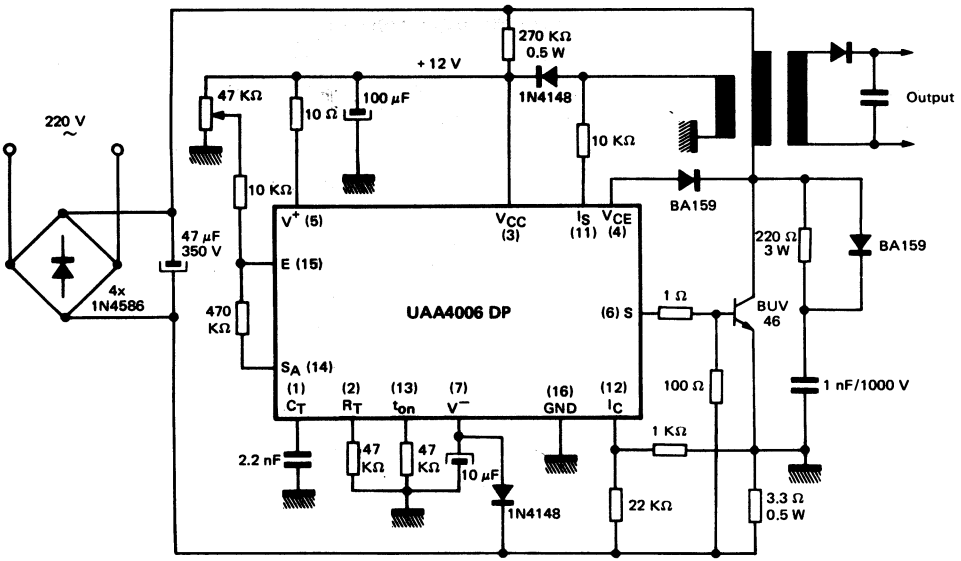


CURRENT LIMITATION



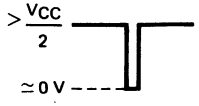


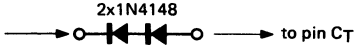
50 W FLY-BACK CONVERTER



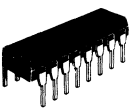
EXTERNAL SYNCHRONIZATION

The oscillator can be slaved to an external synchro pulse provided Fext ⩽ 0.85 F. In that case Rt_{on} should be lowered from about 20% to correct the maximum conduction ratio. The end of the period coincides with the occurrence of the pulse.

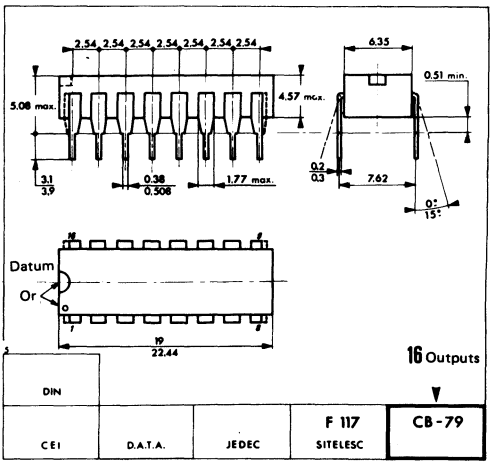




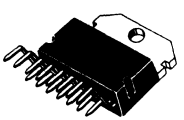
CASE CB-79



DP SUFFIX
PLASTIC PACKAGE



CASE CB-501



SP SUFFIX
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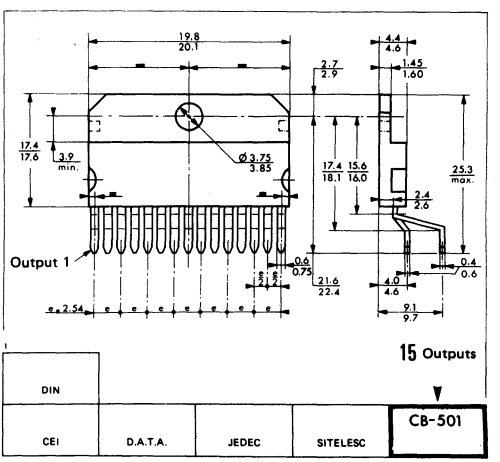


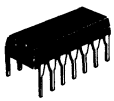
This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

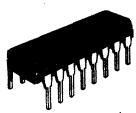
NOTES

MOTOR CONTROL

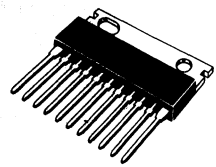
6

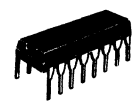
MOTOR CONTROL


DIL14 (CB-504)


DIL16 (CB-79)


DIL8 (CB-98)


SIL11 (CB-173)


DIL16 (CB-502)

CONTROL MOTOR

Function	Features	Part number	Package	Page
DC MOTOR REGULATION AND CONTROL	SWITCH MODE REGULATOR • Direct drive of the switching transistor or darlington. • Includes oscillator, PWM, and error amplifier. • Self regulated base current (peak 1.5 A). • Full protection of switching transistor and output stage. • Locked rotor protection.	UAA4003	DIL 16 (CB-79)	633
	SPEED REGULATOR For permanent magnet DC motors for use in record players, tape recorders, toys... low cost applications.	TDA1154	DIL 8 (CB-98)	615
	FLEXIBLE SPEED REGULATOR For permanent magnet DC motors for use in record players,tape recorders,... • Flexibility to adapt to motors with widely varying characteristics. • Electronic speed change. • High starting current.	TDA1041	DIL 14 (CB-504)	611
UNIVERSAL OR DC MOTOR REGULATION AND PROG.	MOTOR SPEED DIGITAL REGULATOR • Compatible with transistor or triac drive. • Complete digital control. • Mask-programmable regulation and control functions. • Two operating modes : autonomous microprocessor peripheral. • Several safety functions.	EF4443	DIL 16 (CB-79)	609
STEPPER MOTOR DRIVING	STEPPER MOTOR DRIVE CIRCUIT • Circuitry for bipolar chopper drive of one phase winding. • Half step and full step mode. • Wide range of current control (5 to 1000 mA). • Selectable current levels.	TEA3717	DIL 16 (CB-502)	621
	QUAD HIGH CURRENT, HIGH VOLTAGE DARLINGTON • V_{CEX} : 105 V - I_C max : 1.8 A • Typical application : Four phase unipolar. Stepper motor drive.	TEB1013	SIL 11 (CB-173)	629

THOMSON SEMICONDUCTORS

EF4443

PRODUCT PREVIEW

ELECTRIC MOTOR SPEED REGULATOR

The EF4443 circuit combines the necessary circuitry for the programmation and the regulation of the speed of a D.C. or a universal electric motor while ensuring several safety functions.

Two operation modes are available :

- an autonomous (AU) mode in which the speed references are stored in an internal read-only memory. The reference changes are controlled by external switches.
- a microprocessor peripheral (MP) mode in which the speed references are sent in real time by a microprocessor.

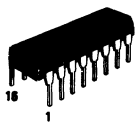
The EF4443 circuit is a+ 9 V supply, N-channel MOS device.

MOS

(N-CHANNEL, SILICON GATE DEPLETION LOAD)

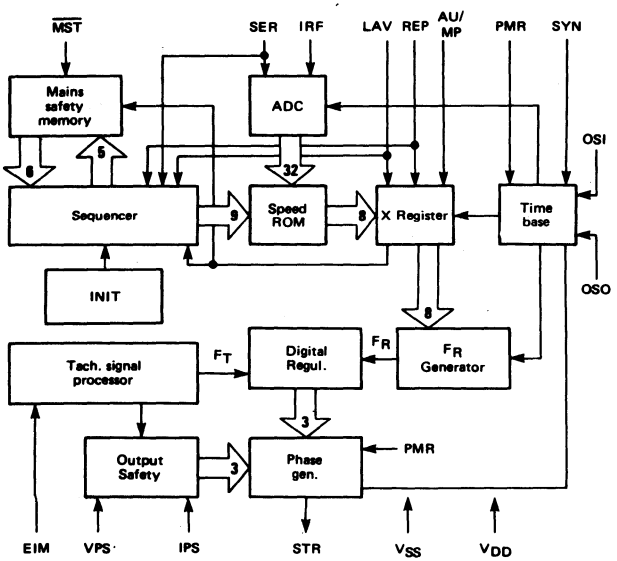
ELECTRIC MOTOR SPEED REGULATOR

CASE CB-79

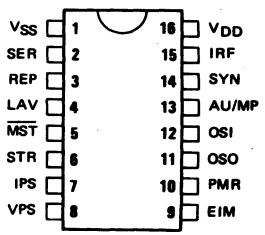


P SUFFIX
PLASTIC PACKAGE

FIGURE 1 – BLOCK DIAGRAM



PIN ASSIGNMENT



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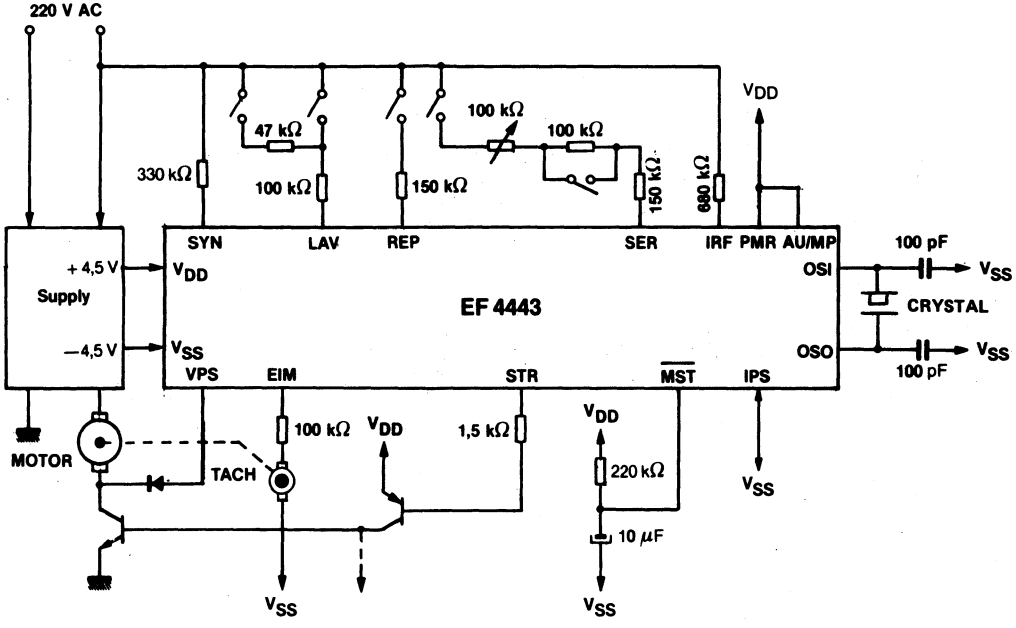
PP8317-A

TYPICAL APPLICATION



THOMSON SEMICONDUCTORS

TDA1041

ADVANCE INFORMATION

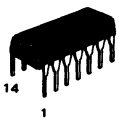
SPEED REGULATOR FOR DC MOTORS

The TDA1041 monolithic integrated circuit is a speed regulator for permanent magnet DC motors for use in record players, tape recorders and in-car cassette players.
The motor speed is regulated to compensate for variations in battery voltage, temperature and load. The part's performance is significantly higher than that of conventional circuits using discrete components.

- The flexibility to adapt to motors with widely varying characteristics.
- Electronic speed change.
- High-stability internal reference voltage.
- Low saturation voltage.
- High starting current.

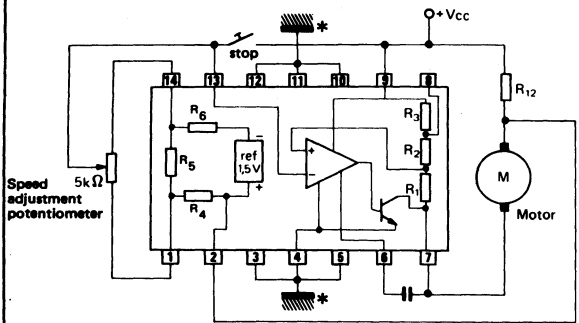
SPEED REGULATOR FOR DC MOTORS

CASE CB-504



DP14 SUFFIX
PLASTIC PACKAGE

APPLICATION CIRCUIT



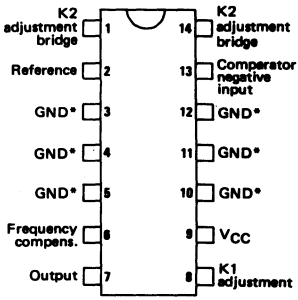
R_1 = 6,8 kΩ
R_2 = 1,2 kΩ
R_3 = 1,4 kΩ
R_4 = 1 kΩ
R_5 = 2,7 kΩ
R_6 = 2,3 kΩ

*Pins 3-4-5-10-11-12 have to be connected to wide copper area on printed board for good dissipation.

$1\,V < c.e.m.f. < 3\,V$ $\quad R_{12} = \frac{R_{MOT}}{2,7}$

$1,8\,V < c.e.m.f. < 6\,V$ $\quad R_{12} = \frac{R_{MOT}}{6}$, R_3 short-circuited

PIN ASSIGNMENT



*Grounds have to be connected together to wide copper area on printed board for good dissipation.

SP8242-A

6

MAXIMUM RATINGS

$T_{amb} = 25°C$

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	$3.8 \leq V_{CC} \leq 18$	V
Maximum output current	I_O	1	A
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	- 40,+ 150	°C

THERMAL CHARACTERISTICS

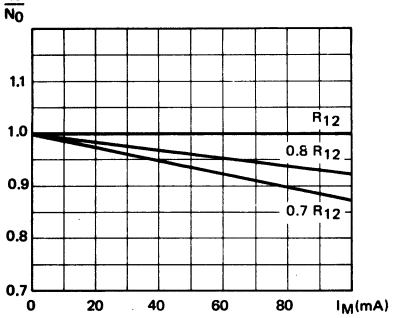
Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	60	°C/W
Junction-case thermal resistance	$R_{th(j-c)}$	15	°C/W

ELECTRICAL CHARACTERISTICS

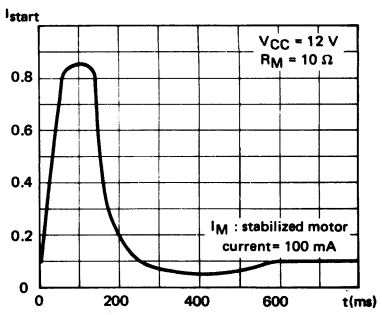
$T_{amb} = 25°C$; $V_{CC} = 9$ V (unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Reference voltage between pin 2 and 14	$V_{(ref)}$	0.7	0.95	1.15	V
Regulator supply current	I_{CC}	–	$6+\frac{I_O}{80}$	–	mA
Reference voltage temperature coefficient (without load) T_{amb} = 0 to 70 °C	$\frac{\Delta V_{(ref)}}{\Delta t_{(vj)}}$	–	–0.1	–	mV/°C
Reference voltage versus supply voltage (without load)	ΔV_{ref}				mV
V_{CC} = 6 to 15 V		- 3	0	+ 3	
V_{CC} = 4 to 18 V		- 15	0	+ 15	
Amplifier input current	I_{IB}	–	4	15	μA
Output transistor saturation voltage	V_{CEsat}				V
I_O = 0.2 A		–	0.15	–	
I_O = 0.8 A		–	1	1.8	
Starting current	I_O				A
V_{CC} = 3.8 V ; R_{MOT} = 10 Ω		0.3	–	–	
V_{CC} = 12 V ; R_{MOT} = 10 Ω		0.7	0.85	–	
Speed regulation versus load (I_O = 50 to 100 mA)	$\frac{\Delta\omega}{\omega}$	–	0.6	–	%
Speed regulation coefficient versus supply voltage $\frac{\Delta V_{CC}}{V_{CC}} = \pm 33$ % ; I_O = 70 mA	$\frac{\Delta\omega}{\omega}$	–	± 0.3	–	%

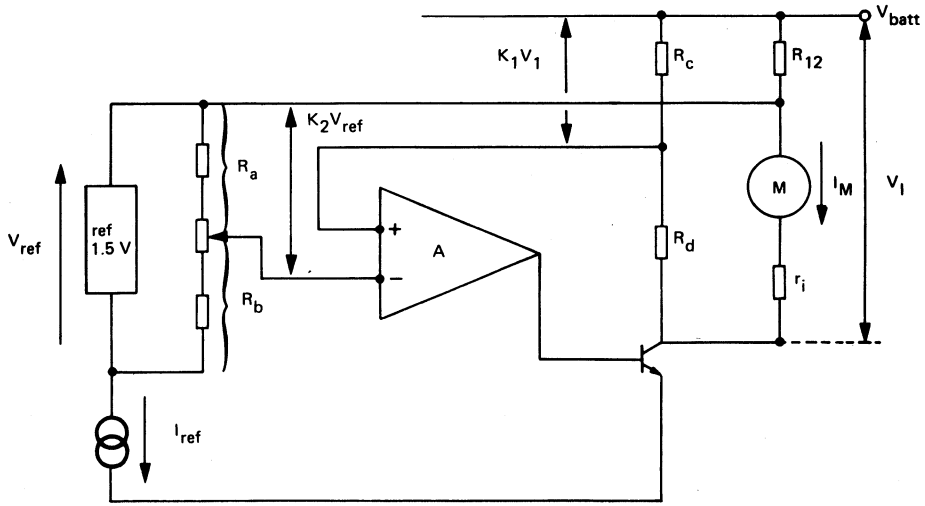
SPEED REGULATION VERSUS LOAD



STARTING CURRENT VERSUS TIME



OPERATING PRINCIPLE



Amplifier gain
$A = \infty$

$$K_1 = \frac{R_c}{R_c + R_d} \qquad K_2 = \frac{R_a}{R_a + R_b}$$

The motor back e.m.f. (E) is proportional to the speed (N in rpm).

(1)
$E = K\phi N$
ϕ = flux
K = motor constant
N = number of revolutions

The motor current (I_M) is proportional to the torque (C_M)

(2)
$$I_M = \frac{C_M}{K\phi}$$

The motor voltage is :

(3)
$$V_M = E + r_i \cdot I_M$$

where
r_i = motor internal resistance

The circuit operates by compensating for any variation in r_i in order to maintain E constant as follows :

The motor current I_M causes a voltage drop in r_i. If the torque varies with a constant motor voltage, the back e.m.f. E varies, as does the speed N.

Assuming that the amplifier gain A is very high :

(4)
$$V_1 = V_M + R_{12} I_M + R_{12} I_{ref}$$

(5)
$$K_1 V_1 = K_2 V_{ref} + R_{12} (I_M + I_{ref})$$

Combining equations (4) and (5) :

(6)
$$K_1 E + K_1 I_M (r_i + R_{12}) + K_1 R_{12} I_{ref} = K_2 V_{ref} + R_{12} (I_M + I_{ref})$$

(7)
$$E = \frac{K_2}{K_1} V_{ref} + I_{ref} R_{12} (\frac{1}{K_1} - 1) + I_M [R_{12} (\frac{1}{K_1} - 1) - r_i]$$
$$= K\phi N$$

The term $[R_{12} (\frac{1}{K_1} - 1) - r_i]$ may be eliminated by selecting an appropriate value for R_{12}.

Equation (7) is then written :

(8)
$$E = \frac{K_2}{K_1} V_{ref} + R_{12} (\frac{1}{K_1} - 1) I_{ref} = K\phi N$$

As the terms of equation (8) are constant, neither E nor N varies. V_{ref} is the reference voltage stabilized against variations in supply voltage and temperature. The required value for R_{12} is :

(9)
$$R_{12} = \frac{r_i}{\frac{1}{K_1} - 1}$$

The closed loop system formed by the integrated circuit, the motor and R_{12} features both voltage and current feedback.

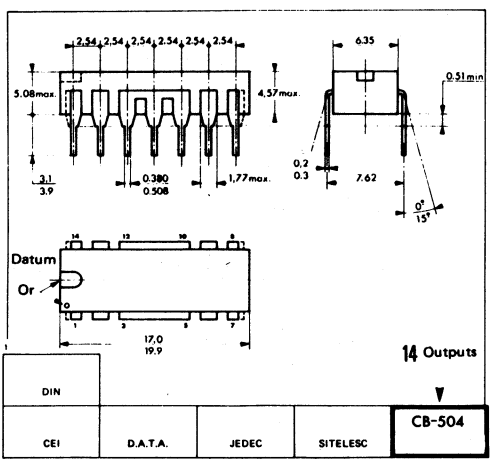
The system is conditionally stable if :

$$R_{12} \leqslant \frac{r_i}{\frac{1}{K_1} - 1}$$

In practice, the value of R_{12} is calculated to compensate for spread in terms of the value of R_{12} and the motor parameters.

CASE CB-504

DP14 SUFFIX
PLASTIC PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

TDA1154

SPEED REGULATOR FOR DC MOTORS

The TDA 1154 is a monolithic integrated circuit intended for permanent magnet DC motors speed regulation in record players, tape recorders, cassette recorders, toys.
It offers speed regulation with power supply voltage, temperature and load changes much higher than conventional circuits built with discrete components do.
Main features are:

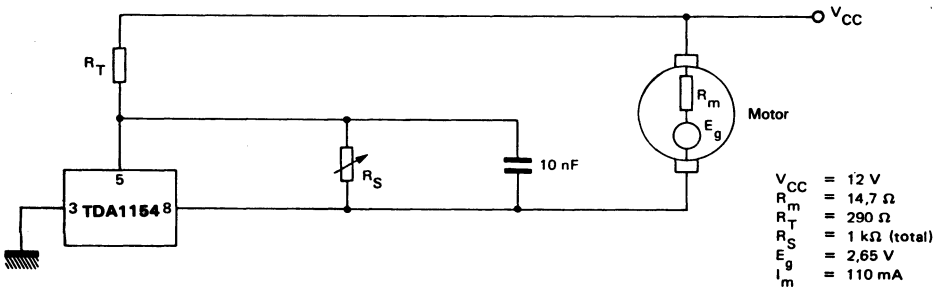
- Matching flexibility to motors with various characteristics
- Current limitation
- Reference voltage 1,2 V
- Starting current 0,5 A to 2,5 V
- Reflection coefficient K = 20
- Supply voltage $\leqslant$ 20 V

SPEED REGULATOR FOR DC MOTORS

CASE CB-98

DP SUFFIX
PLASTIC PACKAGE

APPLICATION CIRCUIT



V_{CC}	=	12 V
R_m	=	14,7 Ω
R_T	=	290 Ω
R_S	=	1 kΩ (total)
E_g	=	2,65 V
I_m	=	110 mA

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NT8036R1-A

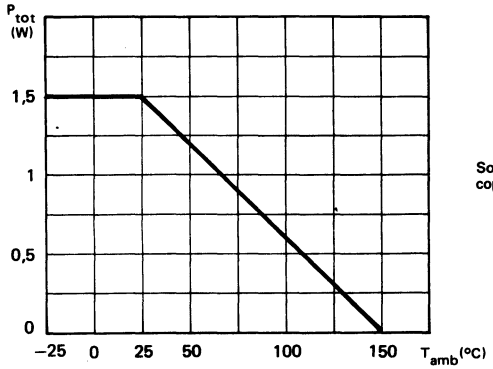
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	20	V
Maximum output current	I_O	1,2	A
Power dissipation	P_{tot}	(see curve)	W
Junction temperature	Tj	150	°C
Storage temperature	T_{stg}	− 55 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	85	°C/W
Junction-case thermal resistance	$R_{th(j-c)}$	19	°C/W

MAXIMUM POWER DISSIPATION



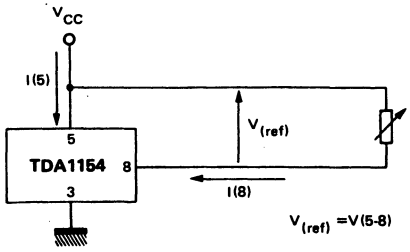
Soldering on a P.C. board, copper area: 5 cm²

PIN CONFIGURATION

CASE CB-98

Pins 6 and 7: No connected

TEST CIRCUIT



$V_{(ref)} = V(5\text{-}8)$

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Reference voltage (V_{CC} = 6 V; I(8) = 0.1 A)	$V_{(ref)}$	1.15	1.25	1.35	V
Reference voltage temperature coefficient V_{CC} = 6 V; I(8) = 0.1 A; T_{amb} = − 20 °C + 70 °C	$\frac{\Delta V_{(ref)}}{V_{(ref)}} / \Delta T$	–	0.02	–	% / °C
Line regulator V_{CC} = 4 − 18 V; I(8) = 0.1 A	$\frac{\Delta V_{(ref)}}{V_{(ref)}} / \Delta V_{CC}$	–	0.02	–	% / °C
Load regulator V_{CC} = 6V; I(8) = 25 = 400 mA	$\frac{\Delta V_{(ref)}}{V_{(ref)}} / \Delta I(8)$	–	0.009	–	% / mA
Minimum supply voltage I(8) = 0.1 A; $\frac{\Delta V_{(ref)}}{V_{(ref)}}$ = − 5 %	V (5 − 3)	–	2.1	2.5	V
Starting current (*) V_{CC} = 5 V; $\frac{\Delta V_{(ref)}}{V_{(ref)}}$ = − 50 %	I(8)	1.2	–	–	A
Starting current V_{CC} = 2.5 V; $\frac{\Delta V_{(ref)}}{V_{(ref)}}$ = − 50 %	I(8)	0.5	0.8	–	A
Quiescent current on pin 5 V_{CC} = 6 V; I(8) = 100 μA	I_O (5)	–	1.7	–	mA
$K = \frac{\Delta I(8)}{\Delta I(5)}$ reflection coefficient V_{CC} = 6 V; I(8) = 0.1 A	K	18	20	22	
K spread versus V_{CC} V_{CC} = 6 − 18 V; I(8) = 0.1 A	$\frac{\Delta K}{K} / \Delta V_{CC}$	–	0.45	–	% / V
K spread versus I(8) V_{CC} = 6 V; I(8) = 25 − 400 mA	$\frac{\Delta K}{K} / \Delta I(8)$	–	0.005	–	% / mA
K spread versus temperature V_{CC} = 6 V; I(8) = 0.1 A; T_{amb} = 20 °C, + 70 °C	$\frac{\Delta K}{K} / \Delta T$	–	0.02	–	% / °C

(*) An internal protection reduce this current if the temperature of the junction increase : I(8) = 0.75 A to t_j = 140°C.

OPERATING MODE

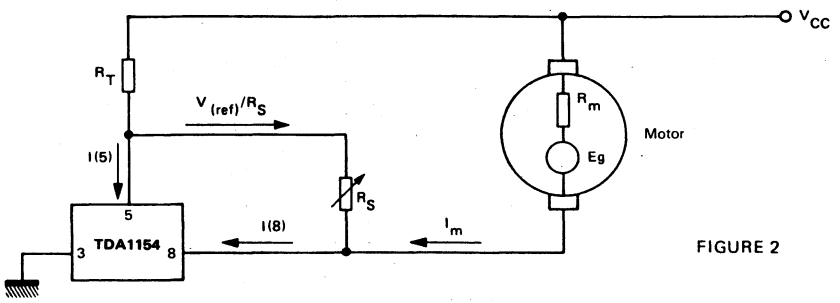


FIGURE 2

Voltage between pins 5 and 8 its held constant by the circuit.

$V(5-8) = V_{(ref)} = 1,2\ V$

Current I(5) consumed on pin 5 by the circuit is equal to $I_O(5)$ = 1,7 mA (constant) plus $I_O(8) = I(8) / K$ I(8) is the current flowing through pin 8).

$I(5) = I_O(5) + I(8)\ K \quad (I_O(5) = 1,7\ mA;\ K = 20)$

Now $I(8) = I_m + \frac{V_{(ref)}}{R_S}$, therefore: $Eg = \underbrace{I_m\left[\frac{R_T}{K} - R_m\right]}_{(1)} + \underbrace{V_{(ref)}\left[\frac{R_T}{R_S}\left(1 + \frac{1}{K}\right) + 1\right]}_{(2)} + R_T I_O(5)$

Motor speed witll be independent of resisting torque if Eg does not depend to I_m, in other words if term (1) equals zero or:

$$\boxed{R_T = K R_m\ (K = 20)}$$

Eg being motor back electromotive force and R_m its internal resistance.

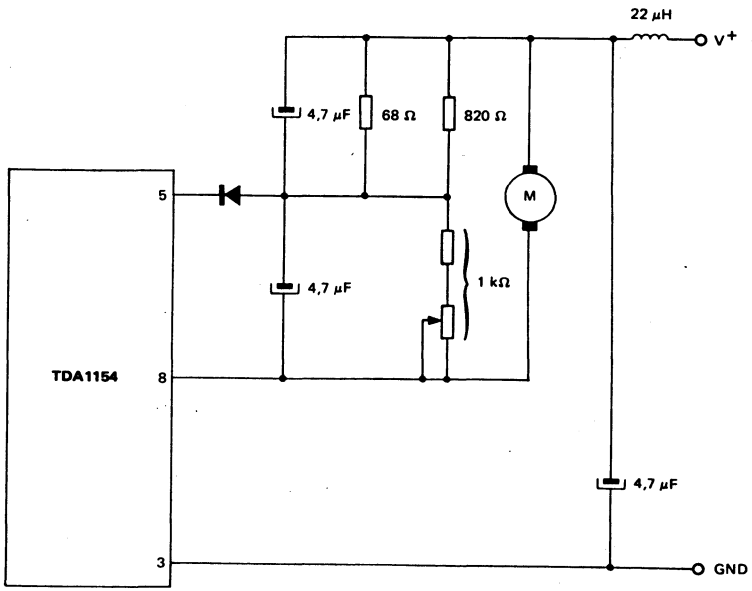
$$Eg + R_m I_m = R_T\left[I(5) + \frac{V_{(ref)}}{R_S}\right] + V_{(ref)}$$

If $R_T > KRm$ an instability may occur owing to an over compensation.

Back electromotive force Eg, corresponding to the wanted speed, gives R_S value by term (2):

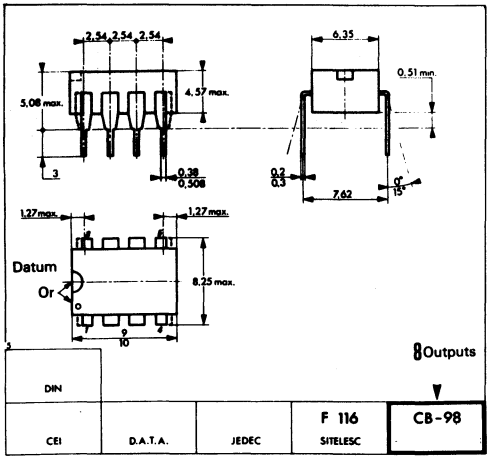
$$R_S = R_T \frac{V_{(ref)}\ (1 + 1/K)}{Eg - V_{(ref)} - R_T I_O(5)} \# R_T \frac{V_{(ref)}}{Eg - V_{(ref)} - R_T I_O(5)} \quad \begin{cases} V_{(ref)} = 1,2\ V \\ I_O(5) = 1,7\ mA \end{cases}$$

APPLICATION CIRCUIT



CASE CB-98

DP SUFFIX
PLASTIC PACKAGE



These specifications are subject to change without notice.
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THOMSON SEMICONDUCTORS

TEA3717

ADVANCE INFORMATION

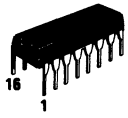
STEPPER MOTOR DRIVE CIRCUIT

The TEA3717 is a bipolar monolithic integrated circuit intended to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL-compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two TEA3717 and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

- Half-step and full-step mode.
- Bipolar drive of stepper motor for maximum motor performance.
- Built-in protection diodes.
- Wide range of current control 5 to 1000 mA.
- Wide voltage range 10 to 45 V.
- Designed for unstabilized motor supply voltage.
- Current levels can be selected in steps or varied continuously.

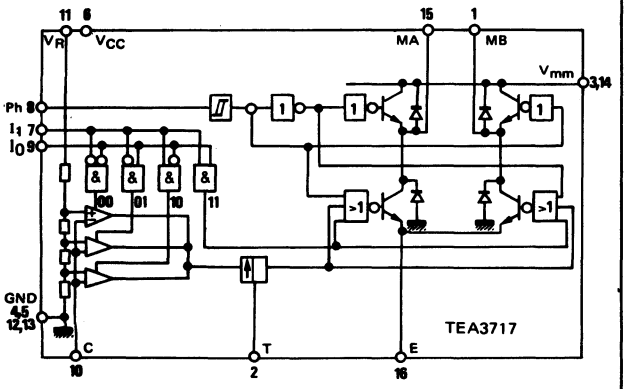
STEPPER MOTOR DRIVE CIRCUIT

CASE CB-502

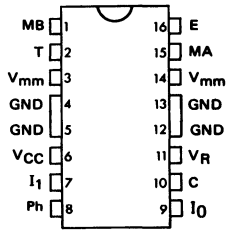


DP SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



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NT8231-A

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC} V_{mm}	7 45	V V
Input voltage Logic inputs Analog input Reference input	V_I	 6 V_{CC} 15	V
Input current Logic inputs Analog inputs	I_I	 -10 -10	mA
Output current	I_O	±1	A
Junction temperature	T_j	+150	°C
Operating ambient temperature range	T_{oper}	0,+70	°C
Storage temperature range	T_{stg}	-55,+150	°C

THERMAL CHARACTERISTICS

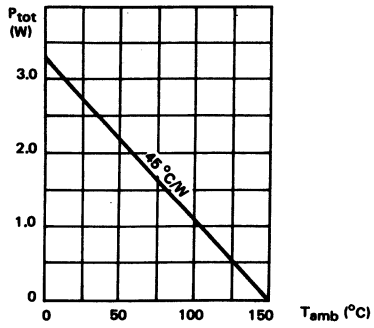
Characteristic	Symbol	Value	Unit
Thermal resistance Junction case Junction ambient	 $R_{th(j-c)}$ $R_{th(j-a)}$*	 11 45	 °C/W °C/W

* Soldered on a 35 μm thick 40 cm^2 PC board copper area.

RECOMMENDED OPERATING CONDITIONS

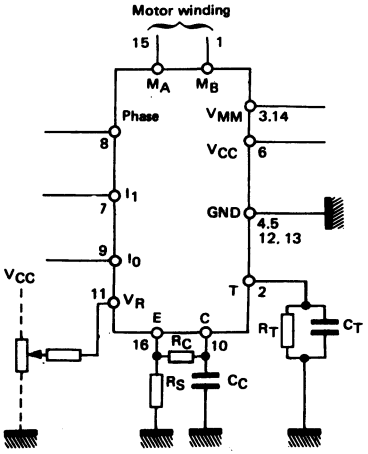
Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Supply voltage	V_{mm}	10	–	40	V
Output current	I_m	0.020	–	1	A
Ambient temperature	T_{amb}	0	–	70	°C
Rise time, logic inputs	t_r	–	–	2	μs
Fall time, logic inputs	t_f	–	–	2	μs

MAXIMUM POWER DISSIPATION



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply current	I_{CC}	–	–	25	mA
High level input voltage - Logic inputs	V_{IH}	2.0	–	–	V
Low level input voltage - Logic inputs	V_{IL}	–	–	0.8	V
High level input current - Logic inputs (V_I = 2.4 V)	I_{IH}	–	–	20	µA
Low level input current - Logic inputs (V_I = 0.4 V)	I_{IL}	-0.4	–	–	mA
Comparator threshold voltage* (V_R = 5.0 V)					
I_0 = 0 ; I_1 = 0	V_{CH}*	390	420	440	mV
I_0 = 1 ; I_1 = 0	V_{CM}*	230	250	270	mV
I_0 = 0 ; I_1 = 1	V_{CL}*	65	80	90	mV
Comparator input current	I_{CO}	-20	–	20	µA
Output leakage current (I_O = 1 ; I_1 = 1 ; T_{amb} = +25°C)	I_{off}	–	–	100	µA
Total saturation voltage drop (I_m = 500 mA)	V_{sat}	–	–	4.0	V
Total power dissipation	P_{tot}				W
I_m = 500 mA ; f_s = 30 KHz		–	1.8	2.3	
I_m = 800 mA ; f_s = 30 KHz		–	3.7	–	
Cut off time (See figure 1 and 2, V_{mm} = 10 V ; $t_{on} \geq 5$ µs)	t_{off}	25	30	35	µs
Turn off delay (See figure 1 and 2, T_{amb} = 25°C ; $dU_k/dt \geq 50$ mV/µs)	t_d	–	1.6	2.0	µs



R_S = 1 Ω, inductance free
R_C = 1 kΩ
C_C = 820 pF, ceramic
R_T = 56 kΩ
C_T = 820 pF, ceramic

FIGURE 1

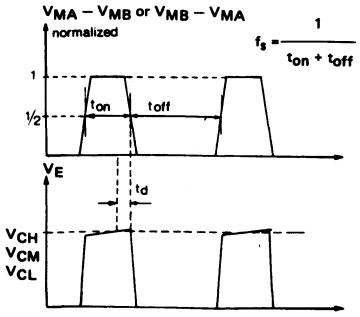


FIGURE 2

FUNCTIONAL DESCRIPTION

The circuit is intended to drive a bipolar constant current through one motor winding. The constant current is generated through switch mode regulation.
There is a choice of three different current levels with the two logic inputs I_0 and I_1. The current can also be switched off completely.

INPUT LOGIC

If any of the logic inputs is left open, the circuit will treat it as a high level input.

I_0	I_1	Current level
H	H	No current
L	H	Low current
H	L	Medium current
L	L	Maximum current

PHASE — This input determines the direction of current flow in the winding, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short circuit occurs in the output stage during phase-shift. High level on the PHASE-input causes the motor current flow from M_A through the winding to M_B.

I_0 and I_1 — The current level in the motor winding is selected with these inputs. The values of the different current levels are determined by the reference voltage V_R together with the value of the sensing resistor R_S.

CURRENT SENSOR

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_0 and I_1. The motor current flows through the sensing resistor R_S. When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator output goes high, which triggers the pulse generator and its output goes high during a fixed pulse time (t_{off}), thus switching off the power feed to the motor winding, and causing the motor current to decrease during t_{off}.

SINGLE-PULSE GENERATOR

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, t_{off}, which is determined by the timing components R_T anc C_T.

$t_{off} = 0.69 \cdot R_T C_T$

Functional blocks

A. TTL compatible input logic
B. Current sensor
C. Single-pulse generator (monostable)
D. Output stage with protection diodes.

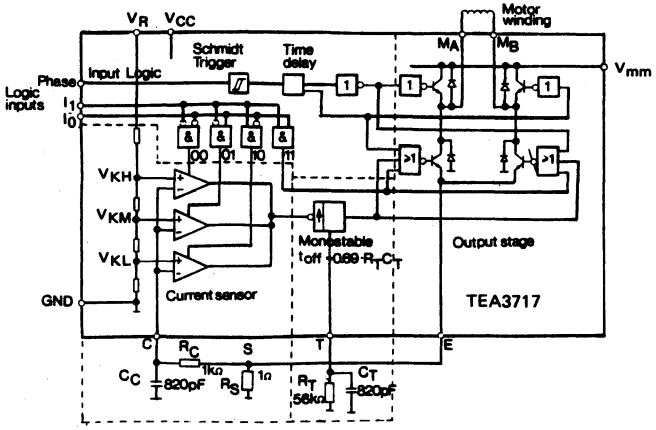


FIGURE 3

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}.
If a new trigger signal should occur during t_{off}, it is ignored.

OUTPUT STAGE

The output stage contains four Darlington transistors and four diodes, connected in an H-bridge. The two sinking transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.
It should be noted however, that it is not permitted to short circuit the outputs.

V_{CC}, V_{mm}

The circuit will stand any order of turn-on or turn-off of the supply voltages V_{CC} and V_{mm}. Normal du/dt values are then assumed.

ANALOG CONTROL

The current levels can be varied continuously if V_R is varied as e.g. in Figure 1.

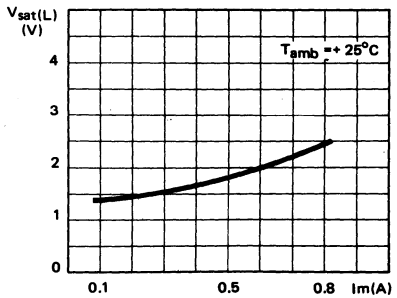


FIGURE 4 – TYPICAL SOURCE SATURATION VOLTAGE V_S OUTPUT CURRENT

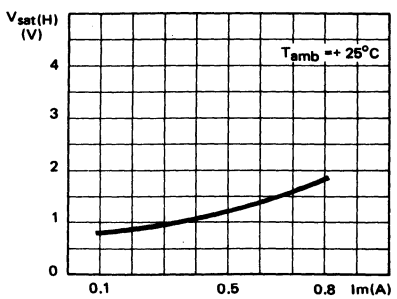


FIGURE 5 – TYPICAL SINK SATURATION VOLTAGE V_S OUTPUT CURRENT

TYPICAL APPLICATION

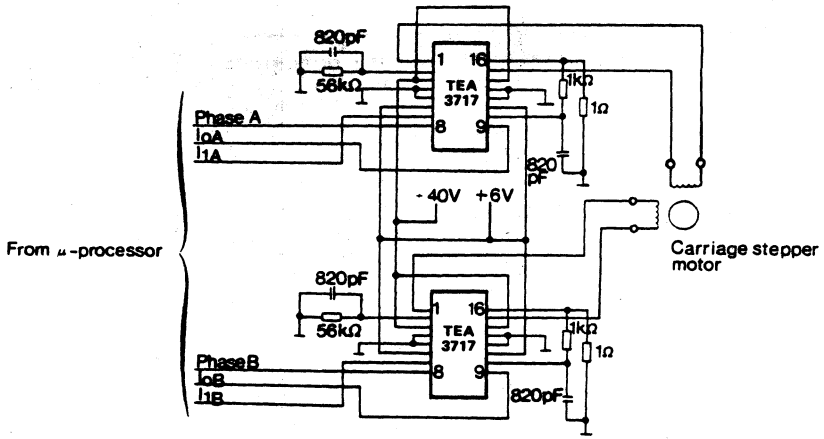


FIGURE 6 – SERIAL PRINTER CARRIAGE DRIVE

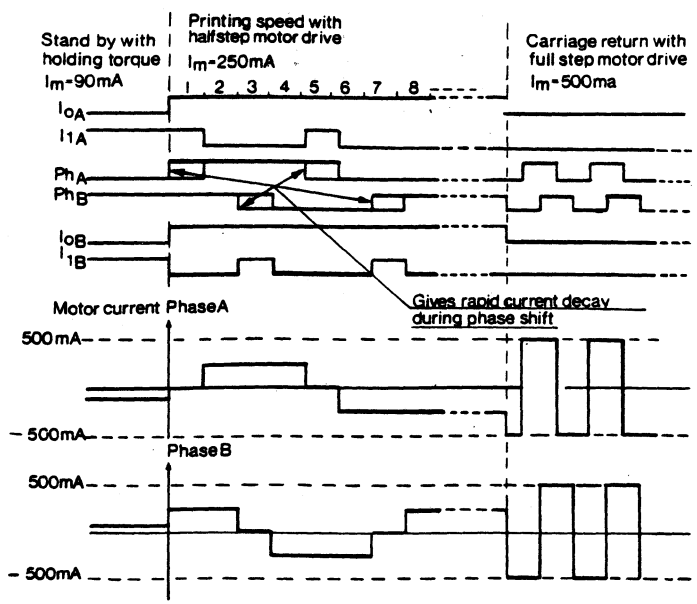
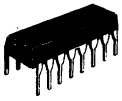
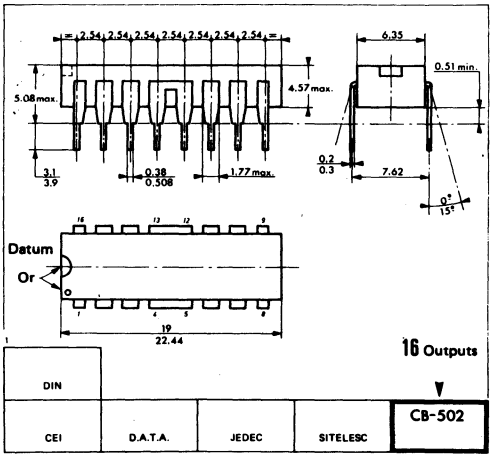


FIGURE 7 – PRINCIPAL OPERATING SEQUENCE

CASE CB-502



DP SUFFIX
PLASTIC PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTORS

TEB1013

QUADRUPLE DARLINGTON
QUAD DARLINGTON SWITCHES

Le TEB 1013 est un circuit intégré monolithique destiné à la commutation de hautes tensions et de forts courants.

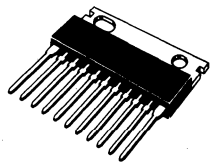
Il comprend quatre transistors Darlington avec un émetteur commun, collecteurs ouverts et diodes de protection.

The TEB 1013 is a monolithic integrated circuit for high current and high voltages switching applications.

It comprises four Darlington transistors with common emitter, open collectors and a clamping diode associated with it.

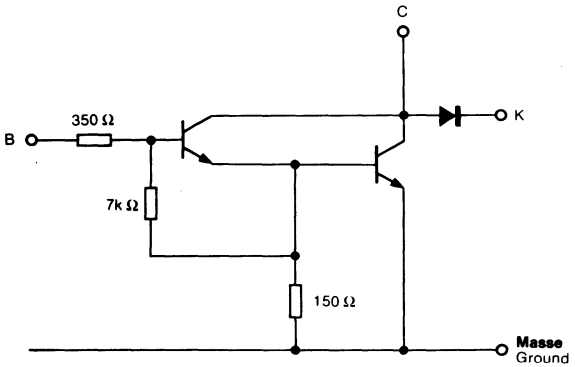
QUADRUPLE DARLINGTON
QUAD DARLINGTON
SWITCHES

BOITIER CB-173
CASE



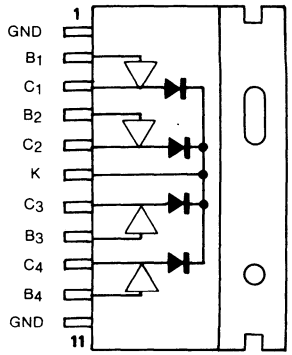
SUFFIXE SP
BOITIER PLASTIQUE
SP SUFFIX
PLASTIC PACKAGE

SCHEMA ELECTRIQUE
SCHEMATIC



1/4 TEB 1013

BROCHAGE
PIN CONFIGURATION



NT8119R1

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VALEURS LIMITES ABSOLUES
ABSOLUTE MAXIMUM RATINGS

T_{amb} = +25 °C (sauf indication contraire)
(unless otherwise stated)

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITIONS	VALEURS VALUES
Tension de claquage Breakdown voltage	BV_{CEO}	I_C = 10 mA	80 V
Tension collecteur émetteur Collector emitter voltage	BV_{CEX}	I_C = 5 mA, V_{BE} = −0,2 V	105 V.
Courant collecteur continu Collector current d.c.	I_C		2 A
Courant collecteur (répétitif) Collector current (repetitif)	I_C		3 A
Puissance dissipée Power dissipation	P_{tot}	T_{amb} < 70 °C (sans radiateur - without heatsink)	2,2 W
Température de jonction Junction temperature	T_j		150 °C
Température de stockage Storage temperature	T_{stg}		−55 °C à T_{to} +150 °C

CARACTERISTIQUES ELECTRIQUES
ELECTRICAL CHARACTERISTICS

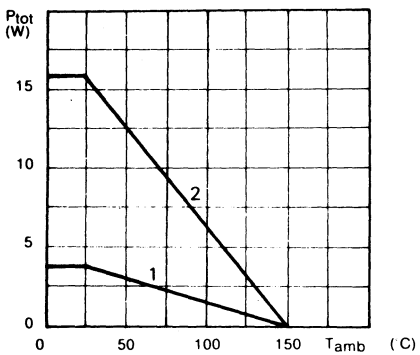
T_{amb} = +25 °C (sauf indication contraire)
(unless otherwise stated)

PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	CONDITIONS DE MESURE TEST CONDITIONS	VALEURS VALUES			UNITES UNITS
			Min.	Typ.	Max.	
Courant de fuite collecteur-émetteur Leakage current collector-emitter	I_{CEO}	V_{CE} = 90 V			50	µA
Tension de saturation collecteur-émetteur Collector-emitter saturation voltage	$V_{CE\ sat}$	I_C = 125 mA, I_B = 2 mA		0,9		V
		I_C = 500 mA, I_B = 10 mA			1,25	
		I_C = 1,7 A, I_B = 10 mA			2	
Gain statique en courant D.C. forward current gain	h_{FE}	I_C = 1 A, V_{CE} = 5 V I_C = 1,7 A, V_{CE} = 11 V	1 700 900	4 000		
Courant d'entrée Input current	I_{in}	V_I = 3,75 V V_I = 2,4 V **Collecteur ouvert** Open collector			11,5 7	mA
Tension d'entrée Input voltage	V_{in}	**OFF condition** **ON condition**	 2,4		0,4	V
Tension de la diode en direct Forward diode voltage	V_O	I = 500 mA I = 1,7 A			1,5 2,5	V
Courant de la diode en inverse Reverse diode current		V_R = 60 V			100	µA
Temps d'établissement Turn on time	t_{on}	I_C = 1,5 A (fig. 4)		200		ns
Temps de coupure Turn off time	t_{off}	I_C = 1,5 A (fig. 4)		700		ns

CARACTÉRISTIQUES THERMIQUES
THERMAL *CHARACTERISTICS*

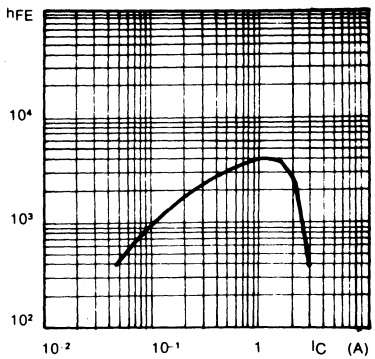
PARAMETRES PARAMETERS	SYMBOLES SYMBOLS	UNITES UNITS
Résistance thermique jonction-ambiante Junction-ambient thermal resistance	$R_{th\ (j\_a)}$	**35 °C max.**
Résistance thermique jonction-boitier Junction to case thermal resistance	$R_{th\ (j\_a)}$	**3 °C max.**

Figure 1
DISSIPATION DE PUISSANCE MAXIMALE
MAXIMUM POWER DISSIPATION



(1) sans radiateur
without heatsink
(2) avec radiateur 5 °C/W
with heatsink 5 °C/W

Figure 2
GAIN EN COURANT EN FONCTION DU COURANT COLLECTEUR
DC CURRENT GAIN VERSUS COLLECTOR CURRENT



(*) Largeur d'impulsion 300µs, rapport cyclique 1,5 %
Pulse width 300µs, duty cycle 1,5 %

Figure 3 - AIRE DE SECURITE
SAFE OPERATING AREA

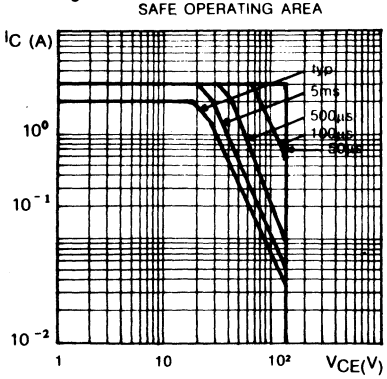
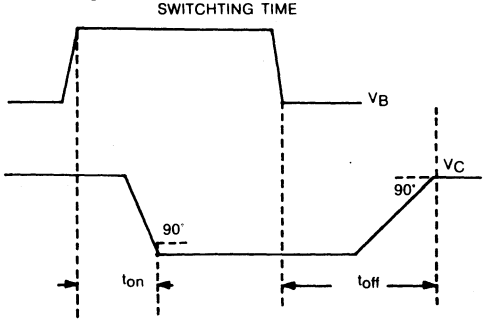


Figure 4 - TEMPS DE COMMUTATION
SWITCHTING TIME



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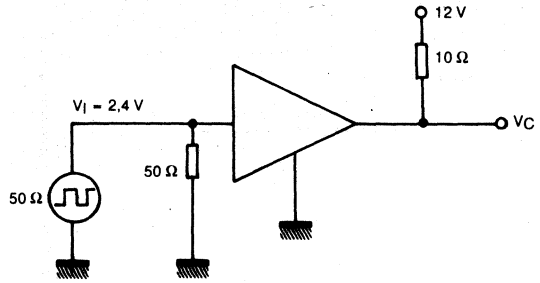
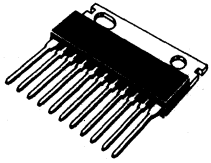
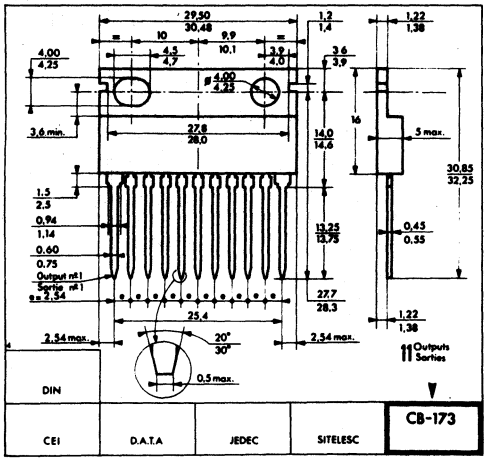


Figure 5
CIRCUIT DE TEST
TEST CIRCUIT

BOITIER CB-173
CASE



SUFFIXE SP
BOITIER PLASTIQUE
SP SUFFIX
PLASTIC PACKAGE



Ces spécifications peuvent changer sans préavis.
Consultez notre réseau de vente pour connaître la disponibilité des différentes versions de ce circuit.

THOMSON SEMICONDUCTORS

UAA4003

ADVANCE INFORMATION

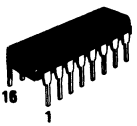
SWITCH MODE REGULATOR FOR DC MOTORS

The UAA4003 is a regulation and control device for the drive of a DC motor with a pulse-width modulator.

- Includes oscillator, PWM and error amplifier
- Soft start
- Direct drive of the switching transistor (or Darlington)
- Self-regulated positive base current (peak 1.5 A)
- Negative base current providing fast turn-off, and allowing the best use of the safe operating area (peak 1.5 A)
- Switching transistor protected against saturation failure
- Immediate limitation of the collector current
- Power supply check
- On-chip thermal protection
- Includes 2 μs minimum conducting time (or no conduction) for use of a snubber circuit.

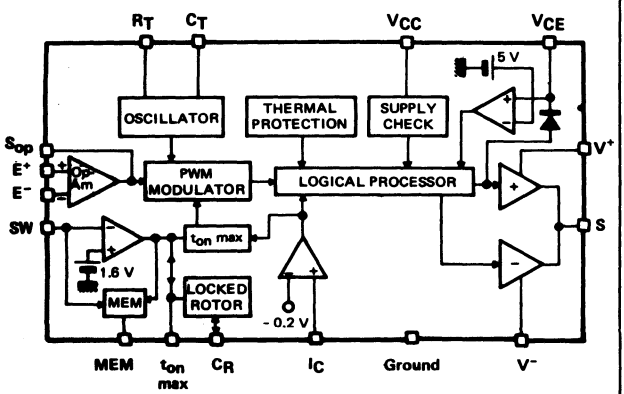
SWITCH MODE REGULATOR FOR DC MOTORS

CASE CB-79

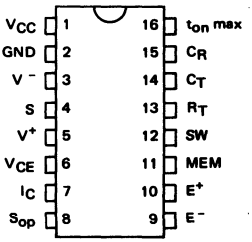


DP SUFFIX
PLASTIC CASE

BLOCK DIAGRAM



PIN ASSIGNMENT



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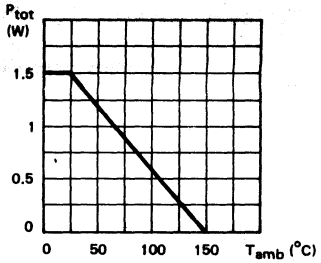
SP8204R1-A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	+ 15	V
Supply voltage V^+ V^-	 V^+ V^-	 + 15 - 9	 V V
Voltage between pin 5 and 3	$V^+ - V^-$	+ 18	V
Output current	I_O	± 2	A
MEM output current	–	10	mA
Current into input I_C (internal protection diodes)	–	± 5	mA
Minimum value of resistance R_T	R_T	10	KΩ
Junction temperature	T_j	- 40+ 150	°C
Storage temperature	T_{stg}	- 40+ 150	°C

MAXIMUM POWER DISSIPATION



THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	$R_{th(j-a)}$	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} =+25°C ; V_{CC} = 10 V ; V^-= - 5 V (unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	6.2	–	14	V
Quiescent current (V_{CC} = 10 V)	I_{CC}	–	10	–	mA
Supply voltage	V^+	4	–	14	V
Supply voltage	V^-	0	–	- 8	V
Threshold of input I_C	V_I	–	- 0.2	–	V
I_C input current (V(7) = 0 V)	–	–	5	20	µA
Op ampli open loop gain	A_V	60	–	–	dB
Op ampli input current	–	–	–	1	µA
Op ampli offset voltage	–	–	5	–	mV
Op ampli common mode voltage	–	0	–	V_{CC} - 3	V
Oscillator frequency	F_{osc}	–	$\frac{2}{R_T C_T}$	50	KHz
Value of resistance R_T	R_T	10	50	500	KΩ
Dead time	–	–	5	–	µs
Output current (V (5) – V (4) = 3 V)	I_O	± 1.5	–	–	A
Input current into pin 12 (SW) (V(12) = 0 V)	–	–	25	50	µA
MEM output current (open collector) (V(11) = 0.3 V)	–	1.2	–	–	mA
"Locked rotor" time constant (V_{CC} = 10 V)	–	–	0.3	–	s/µF
V_{CE} comparator threshold voltage	–	–	5	–	V
Time constant t_{on} min	t_{on} min	–	2	–	µs

CIRCUIT DESCRIPTION

OSCILLATOR

It is a sawtooth generator whose fall time is much inferior to rise time. The period is $T = 0.5\ R_T C_T$, R_T and C_T being tied between pins 13 and 14 respectively, and ground.
The voltage swing is about $V_{CC}/2$ and the low level is 1.5 V.
The maximum working frequency is 50 KHz.

PULSE WIDTH MODULATOR (PWM)

A signal with a variable duty cycle is generated by a comparison between pin 14 voltage (oscillator) and pin 8 voltage (output of the error amplifier).
A second comparator limits the maximum conduction ratio by a comparison between the sawtooth and pin 16 voltage (t_{on} max). If $V_{16} = 0$, there is an internal fixed dead time ($\simeq 5\ \mu s$).

CURRENT LIMITATION

A level lower than - 0.2 V on pin 7 (I_C) involves two actions :

- A direct action through a logic processor which stops the drive until the end of the period.
- An indirect action through the t_{on} max function. The change of state at the output of comparator I_C is applied to pin 16 as long as the current overload stands. By inserting capacitor C_B between pin 16 and V_{CC} (about 0.1 μF), the voltage at this point rises up from a quantity ΔV proportional to the duration and the frequency of the oversteps. This will consequently lower the maximum conduction ratio, thus decreasing the frequency of the oversteps.
At the end of an overload state, capacitor C_B slowly charges through a 20 KΩ internal impedance, in order to come back progressively to normal operation.
This capacitor also achieves a soft start during power up operation.

NOTE : It is possible to use direct action only provided pin 16 is tied to ground.
In that case, the functions "locked rotor" and "memory" cannot be used.

LOCKED ROTOR

A voltage greater than 1.5 V at pin 16 starts up the linear charge of a capacitor C_R connected between pin 15 and ground (3 μF/s).
If V_{16} becomes lower than 1.5 V again before V_{15} reaches V_{CC}, capacitor C_R is quickly discharged.
If the defect keeps staying, V_{15} reaches V_{CC}, and the output is definitively cut. They are two possible ways to come back to normal drive :

- Tie temporarily pin 12 (SW) to ground.
- Tie temporarily pin 15 to ground to discharge C_R.

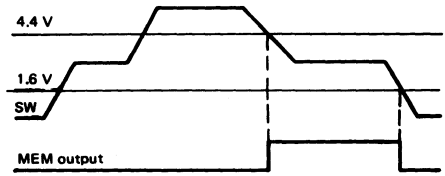
If this function is not to be used, simply tie pin 15 to ground.

ERROR AMPLIFIER

It is an operational amplifier whose open loop gain is greater than 1000.
The input currents are lower than 1 μA, and the input offset voltage is typically 5 mV. The input common mode voltage can range from 0 V to ($V_{CC} - 3$ V).

MEMORY AND INHIBITION

Input SW (pin 12) senses a logical three state signal. The response of the output MEM is represented hereunder :



When the input signal is lower than 1.6 V, there is an inhibition of the output drive through the t_{on} max function. In this case the voltage on pin 16 remains near V_{CC}.
If the input SW becomes greater than 1.6 V, the voltage V_{16} goes down slowly by means of capacitor C_B. The restart is done in a soft way.

PROTECTION AGAINST DESATURATION

If, because of a too low base current or a too heavy load, voltage V_{CE} on the switching transistor goes beyond 4.5 V approximately, the output of comparator V_{CE} swings, and the drive is interrupted.

POWER SUPPLY CHECK

The drive is disabled if V_{CC} is inferior to 6.2 V. Pin 3 should be connected to a voltage equal or inferior to 0.5 V.
In particular, it should not be left unconnected.

THERMAL PROTECTION

It is active when the temperature of the junction reaches 150°C.

LOGICAL PROCESSOR

A logical unit processes the informations coming from the fault detectors, and ensures that the output signal fulfils two conditions :

- No double pulse inside a period : the occurrence of a defect is memorized until the end of the period.
- To allow the discharge of a snubber network, the minimum width of the output pulse is settled at 2 μs through an internal monostable. If this monostable is not triggered, there is no conduction.

OUTPUT STAGE

ON-state

The positive drive achieves a very efficient drive of the switching transistor.
Its features are essentially :

- Direct drive (neither inductance, nor transformer).
- The transistor stays in a quasi-saturation mode, and thus has a reduced storage time.
- The drive energy is strictly limited to what is necessary.
- Easy implementation.

K_1 is closed to turn the positive stage on. The maximum value of the positive base current is settled by the limitation resistance R.
Diode D keeps Q in a quasi-saturation mode : the more Q gets saturated, the more diode D will derive an important part of the drive current i_{B1}, through diode D_1.
Resistance R_B has a low value (about 1 Ω), and is used to stabilize the regulation loop.
For a good efficiency of the negative drive, it should be kept as low as possible.
Integrated Darlington T_1 is able to supply a peak current of 1.5 A with a 2 V saturation voltage.
The voltage V_{CE} on transistor Q is :
$V_{CE} \simeq V_D + R_B I_{B1}$

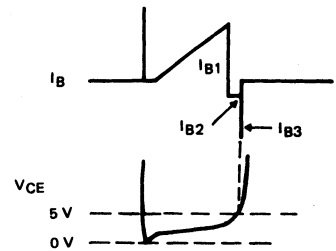
OFF-state

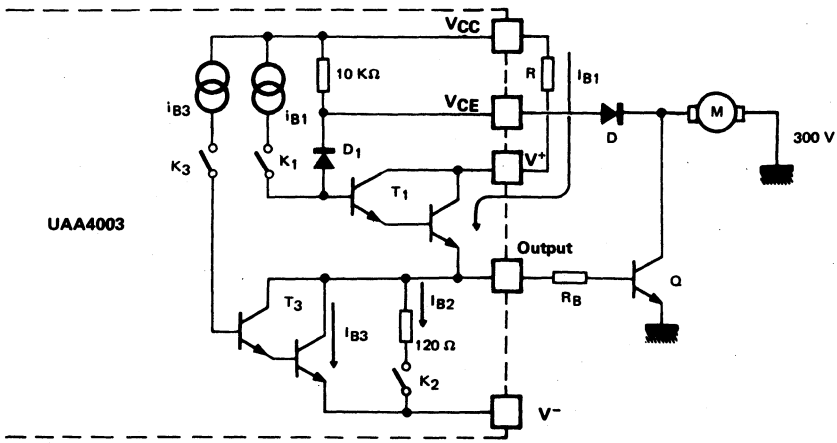
The turn off is done in two steps :

- An immediate action thanks to K_2 which connects the base of the switching transistor to the negative supply through a 120 Ω integrated resistance (current I_{B2}).
- A delayed action through K_3 which is closed only after the desaturation of the external transistor.
This moment is detected by comparator V_{CE}, when V_{CE} reaches 4.5 V.
Darlington T_2 can supply 1.5 A with a 2 V saturation voltage (current I_{B3}).

NOTE : The negative drive I_{B3} for the removal of the stored charges is delayed in order to limit the slope dI_B/dt at the on-off transition. A high dI_B/dt might indeed lead to a destructive overheating of the base-collector junction (see "The power transistor in its environment" Thomson-CSF Division Semiconducteurs Discrets).

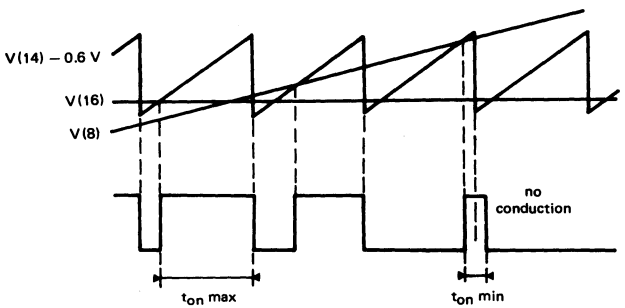
SELF REGULATED BASE CURRENT $I_B = f(V_{CE})$



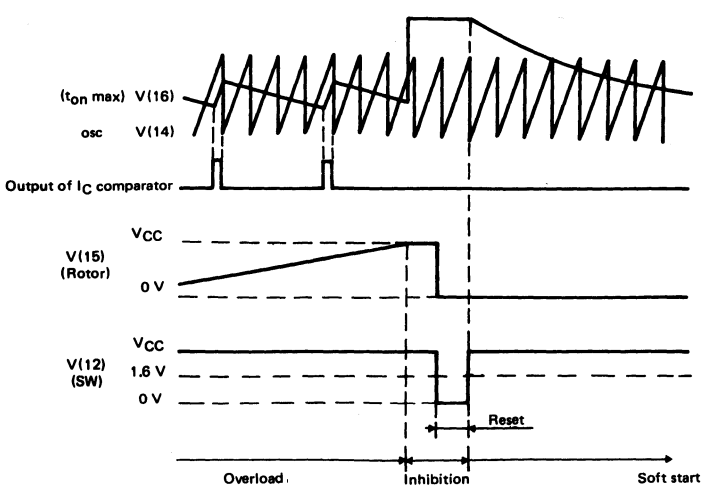


TYPICAL WAVEFORMS

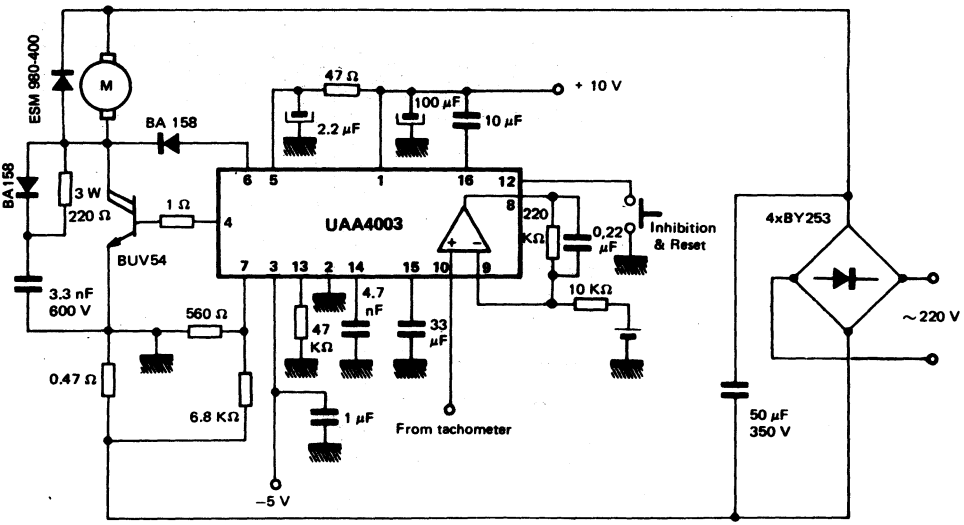
LIMITS OF THE DUTY CYCLE



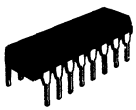
"CURRENT LIMITATION" AND "LOCKED ROTOR" OPERATION



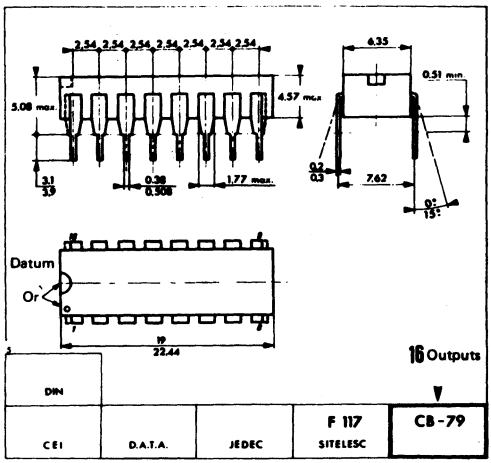
SPEED REGULATOR 1.5 KW



CB-79



DP SUFFIX
PLASTIC PACKAGE



This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

GENERAL INFORMATION

7

QUALITY INFORMATION

The microelectronics revolution has brought innovation on a massive scale. This company's privileged position within the THOMSON group allows us to benefit from and to bring you the benefits of the technological achievements of an international research and development network.

We are therefore in a position to offer our partners products embodying original and varied technical solutions. Excellent performance in terms of reliability is achieved through the use of state of the art production techniques and the application of a rigorous Quality Assurance program. The purpose of this chapter is to familiarize our partners with the methods adopted to achieve these results : constant improvements in terms of production and production monitoring, and increased collaboration with the users of our products.

THOMSON SEMICONDUCTORS AND QUALITY

The first factor in the quality of our components is the care lavished on their development by our design departments, using concepts founded in our own experience and sophisticated electronic data processing aids.

Production monitoring

Quality is achieved in the manufacture of a product. THOMSON SEMICONDUCTORS uses state of the art manufacturing techniques including :

* Ion implantation and various passivating methods.
* Combination of digital and analog circuitry on the same chip using integrated injection logic.
* High-frequency and high-voltage processes.
* A variety of assembly technologies, including VLSI chip bonding, and experience in the assembly of dissipative packages.
* Fully automated manufacture.

Each operation is the subject of a rigorous quality check, to verify that it conforms to manufacturing standards.

Finished circuits are individually measured on sophisticated test machines. Complex and optimized test sequences enable us to offer highly sophisticated functions.

Conformity control

To guarantee the quality of products as shipped to customers, the Quality Assurance program tests samples from each manufacturing batch. These test methods enable us not only to monitor the efficiency of tests applied previously, but also to obtain a complete image of product quality at the various manufacturing levels.

The average quality level actually obtained for a number of batches is significantly better than the Acceptable Quality Levels (AQL), which are meaningful only as limiting values. Our average quality level improved from 800 ppm in 1981 to 600 ppm in 1982 (major mechanical and electrical defects). Our targets are 500 ppm in 1983 and 300 ppm in 1985.

Achieving figures of this kind calls for constant improvement and monitoring of manufacturing operations. They are feasible only in the context of products mass-produced on an industrial scale.

Reliability testing

(See also General Reliability Report)

Under the THOMSON SEMICONDUCTORS Quality Assurance program, samples are regularly subjected to mechanical and electrical endurance testing under extreme conditions.

In particular, components are subjected to long-term operation tests (at least 2000 hours) at junction temperatures of at least 125°C, and where applicable under dynamic signal conditions.

Failure analysis

Parts found to be out of limits in sampling tests prior to shipping or during endurance testing are analyzed using state of the art test facilities.

Causes of defects are immediately communicated to the relevant manufacturing departments so that corrective action may be taken.

COLLABORATION WITH THOMSON SEMICONDUCTORS PRODUCT USERS

The practical utilization of our products in customers' applications is an area where the results achieved can in all cases be improved through close collaboration between THOMSON SEMICONDUCTORS and the customer. With quality as common goal, such collaboration has two aspects :

1 - Achieving a zero defect rate in products delivered and in use. This calls for joint optimization of the methods adopted by THOMSON SEMICONDUCTORS and by the customer, so as to have the best possible knowledge of the electrical parameters of the application.Communications between the respective technical departments must be direct, frequent and fast.

2 - Improving reliability so that the systems in which these products are used achieve low failure rates, enhancing the corporate image of the equipment manufacturer concerned. Where parts fail to give satisfaction, it is our wish that they should be returned to us as soon as possible, with maximum information as to the nature of the problem, a schematic of the equipment, and so on. All such parts will be carefully examined by our analysis laboratory.

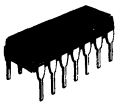
Responsibility for the defect may rest with THOMSON SEMICONDUCTORS (manufacturing defects and errors on testing).On the other hand, parts returned to us for examination may also be found to conform to our test programs.In such cases, analysis may show up a problem in the application of the product (overloading, damage or destruction through inproper use, inappropriate parameters, incomplete specification).

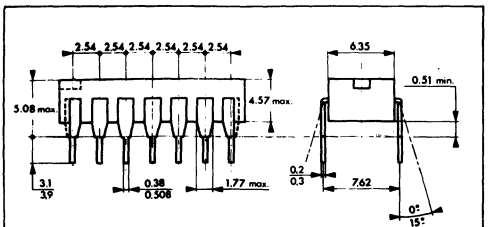
The conclusions of this analysis will be communicated to the product user. According to the nature of the problems encountered, there may be a range of possible solutions, again calling for close collaboration.

Furthermore, the experience acquired through such operations enables us to enhance the effectiveness of corrective measures applied at the production and product improvement levels.

CONCLUSION

Close collaboration with users and the use of state of the art techniques leading to a high level of quality at the production stage in conjunction with long-term test programs enable us to continually improve our products, and provide a jumping off point for further innovation with constantly increasing levels of quality to achieve constantly increasing customer satisfaction.





14 Outputs

DIN				
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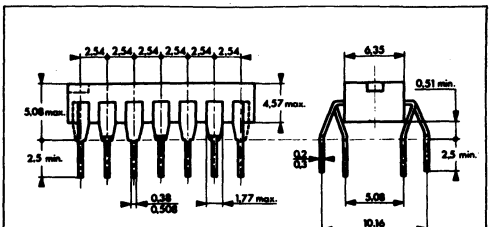
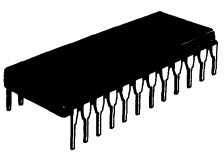
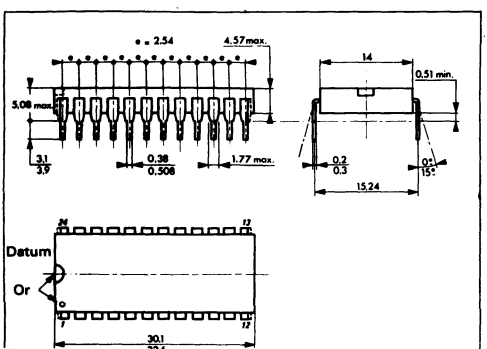
	D.A.T.A.	JEDEC	SITELESC	



14 Outputs

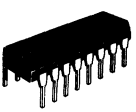
DIN	SOT-57			
CEI	MP 181	JEDEC	SITELESC	CB-21
	D.A.T.A.			

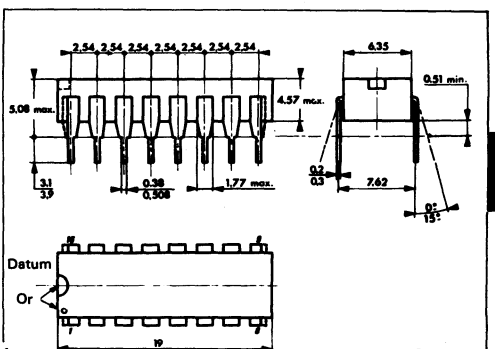




24 Outputs

DIN				
CEI	D.A.T.A.	JEDEC	F 118 SITELESC	CB-68



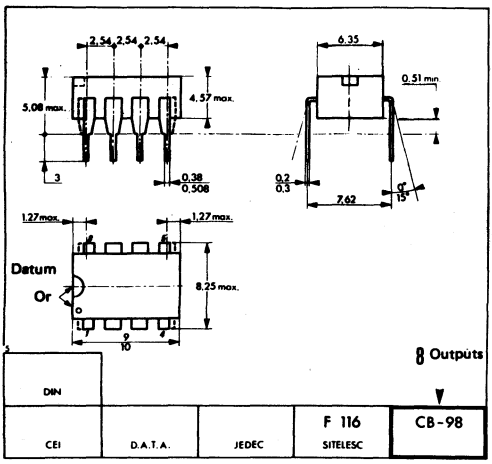


16 Outputs

DIN				
CEI	D.A.T.A.	JEDEC	F 117 SITELESC	CB-79

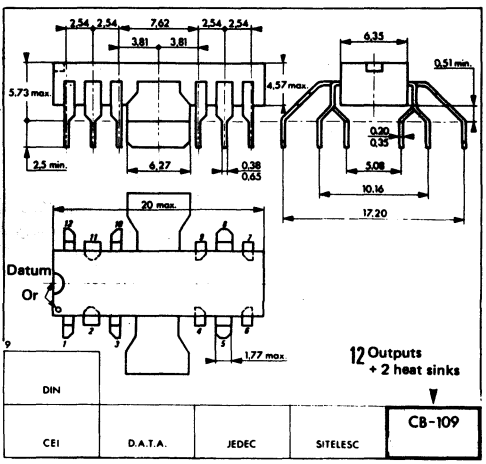
7

PACKAGES



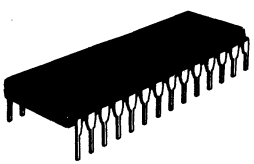
8 Outputs

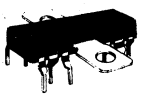
DIN				
CEI	D.A.T.A.	JEDEC	F 116 SITELESC	CB-98

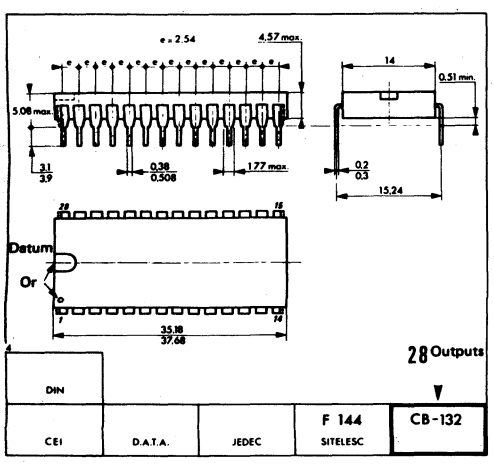


12 Outputs
+ 2 heat sinks

DIN				
CEI	D.A.T.A.	JEDEC	SITELESC	CB-109

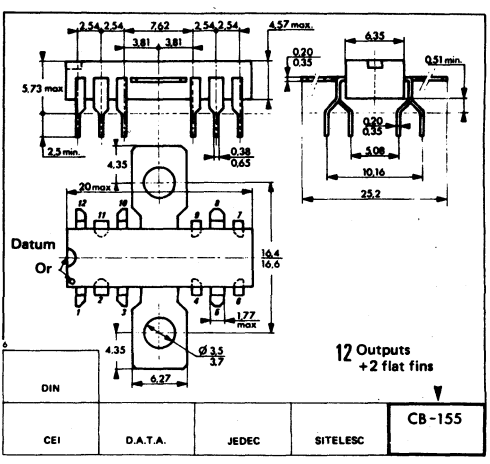






28 Outputs

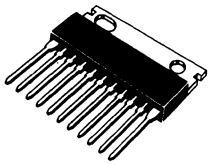
DIN				
CEI	D.A.T.A.	JEDEC	F 144 SITELESC	CB-132

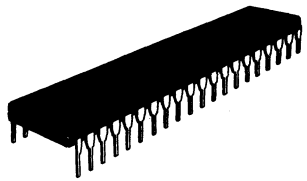


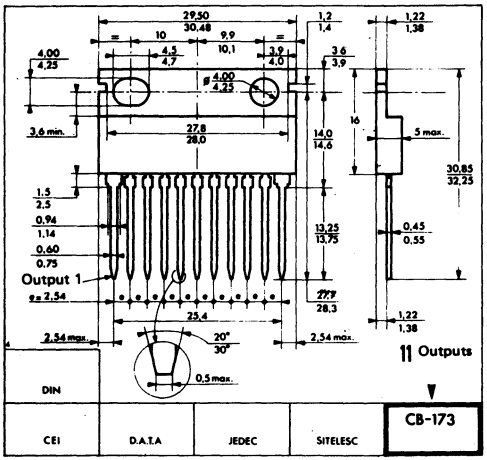
12 Outputs
+2 flat fins

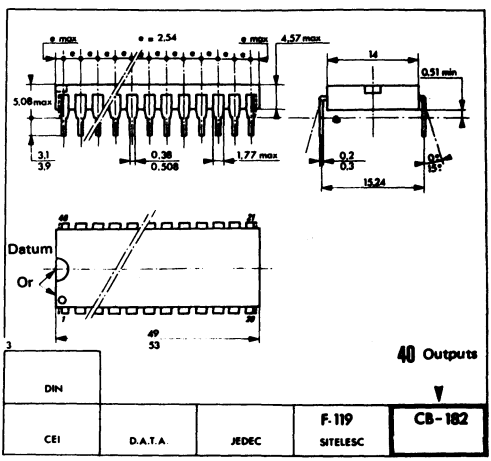
DIN				
CEI	D.A.T.A.	JEDEC	SITELESC	CB-155

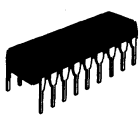
PACKAGES

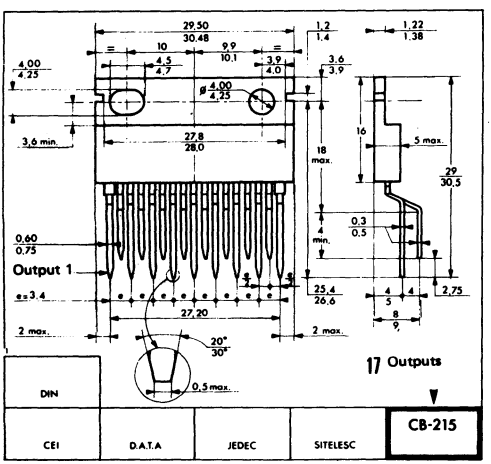


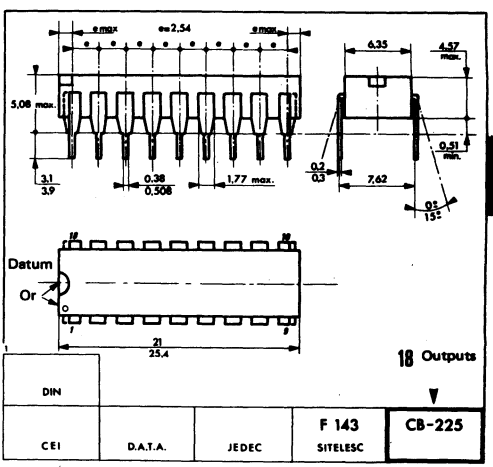



29,50
30,48
10
9,9
10,1
1,2
1,4
1,22
1,38
4,00
4,25
4,5
4,7
3,9
4,0
3,6
3,9
ø 4,00
4,25
3,6 min.
27,8
28,0
14,0
14,6
16
5 max.
30,85
32,25
1,5
2,5
0,94
1,14
0,60
0,75
Output 1
13,25
13,75
0,45
0,55
e = 2,54
27,9
28,3
1,22
1,38
25,4
2,54 max.
20°
30°
2,54 max.
0,5 max.
11 Outputs
DIN
CEI
D.A.T.A
JEDEC
SITELESC
CB-173


e max
e = 2,54
e max
4,57 max.
14
0,51 min
5,08 max
3,1
3,9
0,38
0,508
1,77 max.
0,2
0,3
0,5
15°
15,24
Datum
Or
49
53
40 Outputs
DIN
CEI
D.A.T.A.
JEDEC
F-119
SITELESC
CB-182

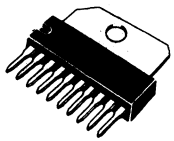


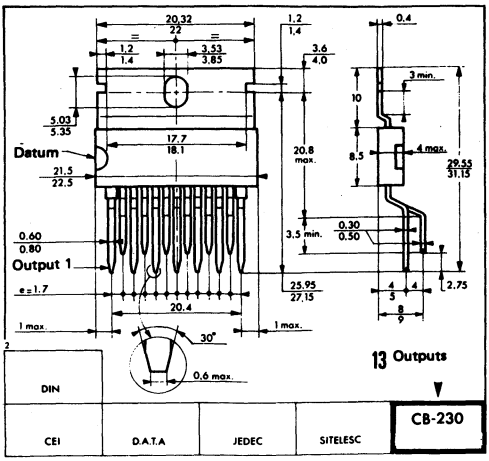

29,50
30,48
10
9,9
10,1
1,2
1,4
1,22
1,38
4,00
4,25
4,5
4,7
3,9
4,0
3,6
3,9
ø 4,00
4,25
3,6 min.
27,8
28,0
18
max.
16
5 max.
29
30,5
0,60
0,75
Output 1
0,3
0,5
4
min.
e = 3,4
25,4
26,6
4
5
4
8
9
2,75
27,20
2 max.
2 max.
20°
30°
0,5 max.
17 Outputs
DIN
CEI
D.A.T.A
JEDEC
SITELESC
CB-215


e max
e = 2,54
e max
6,35
4,57
max.
5,08 max.
3,1
3,9
0,38
0,508
1,77 max.
0,2
0,3
7,62
0,51
min.
0,5
15°
Datum
Or
21
25,4
18 Outputs
DIN
CEI
D.A.T.A.
JEDEC
F 143
SITELESC
CB-225

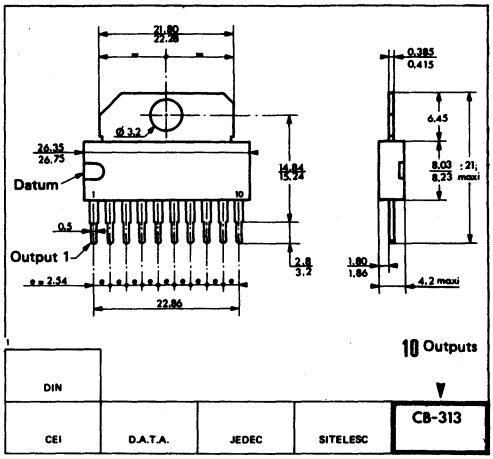
7

PACKAGES

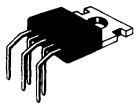


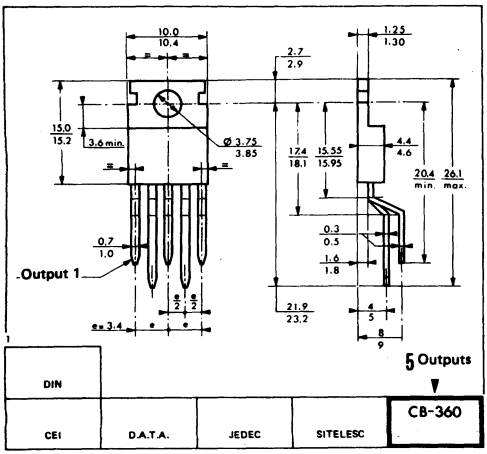


DIN				
CEI	D.A.T.A	JEDEC	SITELESC	CB-230

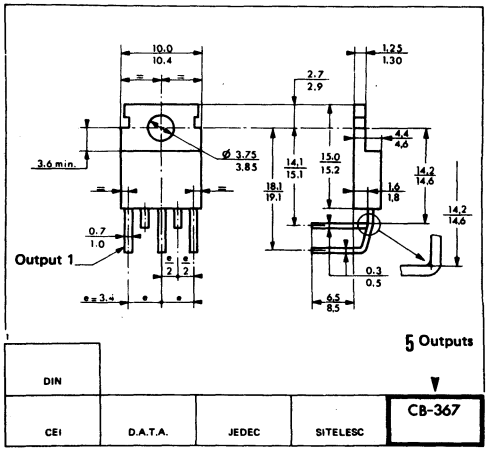


DIN				
CEI	D.A.T.A.	JEDEC	SITELESC	CB-313



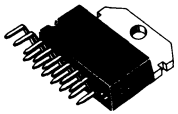


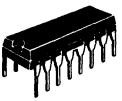
DIN				
CEI	D.A.T.A.	JEDEC	SITELESC	CB-360

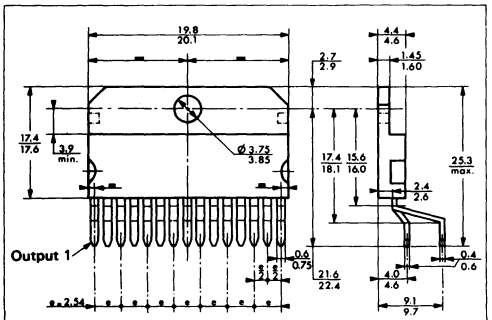


DIN				
CEI	D.A.T.A.	JEDEC	SITELESC	CB-367

PACKAGES

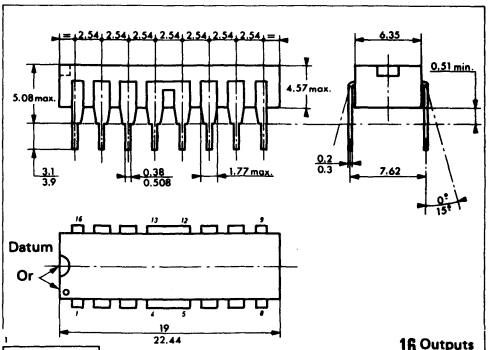






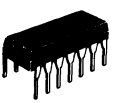
15 Outputs

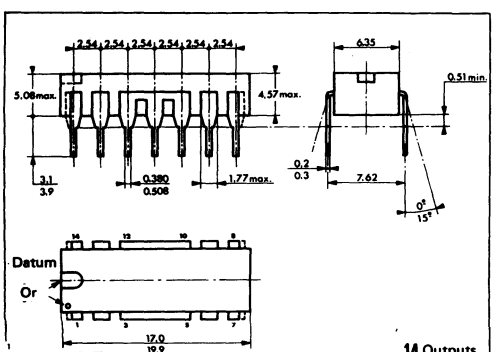
DIN				
CEI	D.A.T.A.	JEDEC	SITELESC	CB-501



16 Outputs

DIN				
CEI	D.A.T.A.	JEDEC	SITELESC	CB-502





14 Outputs

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7

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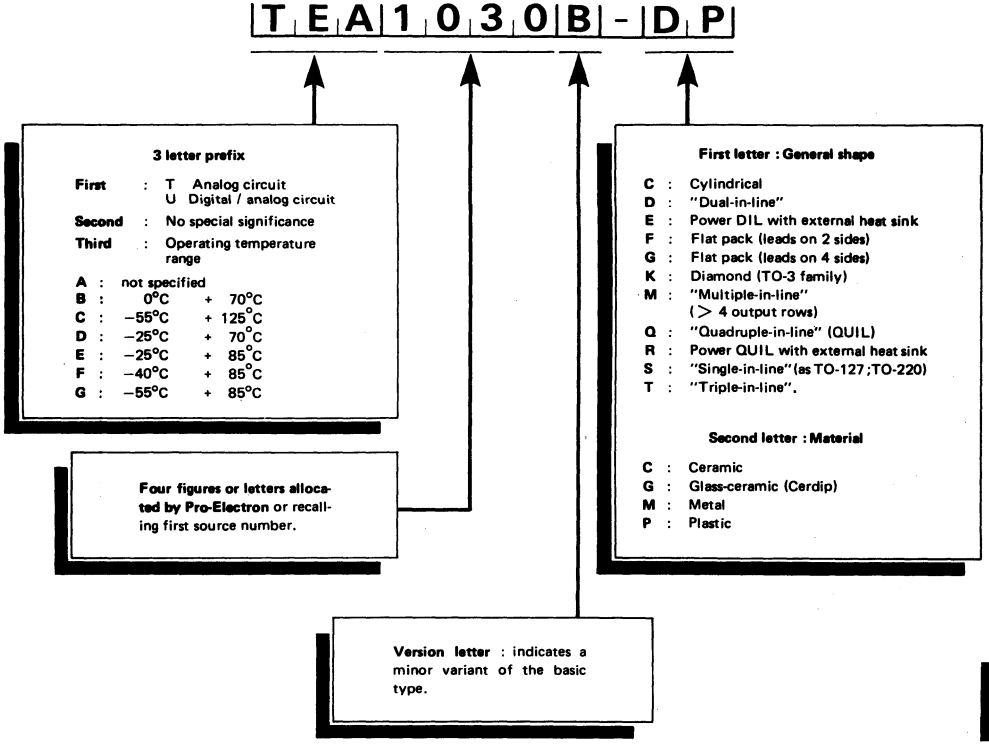

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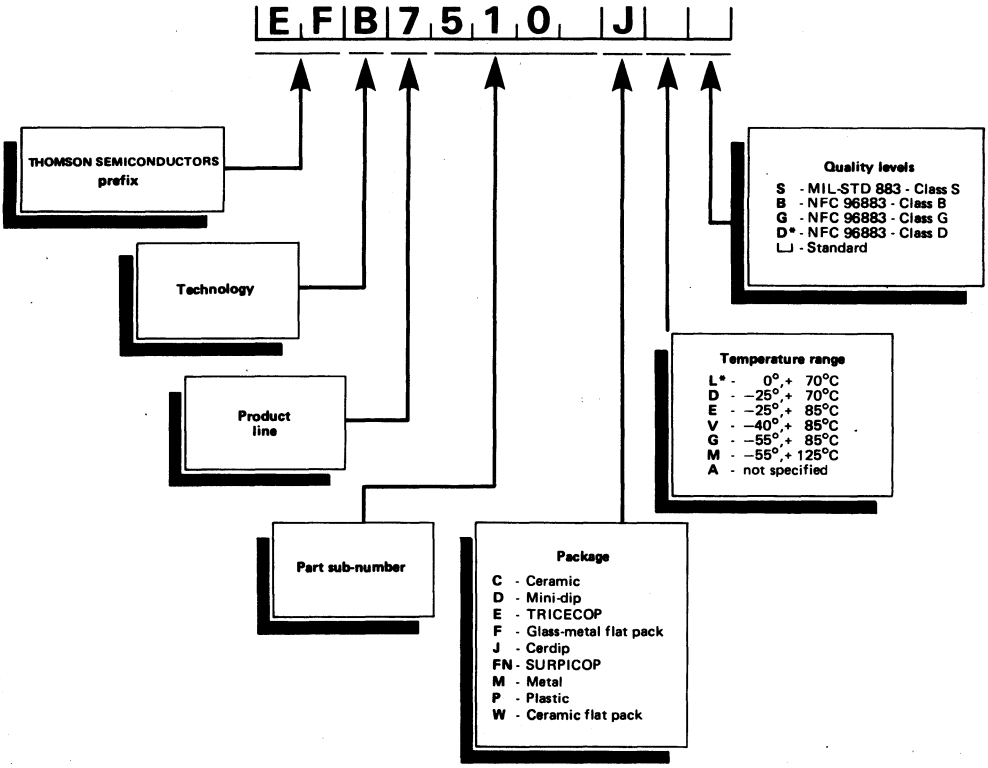
MOS CIRCUITS



* May be omitted.

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