BIPOLAR DIGITAL ICs

DATA BOOK 1985/86

THOMSON SEMICONDUCTEURS

BIPOLAR DIGITAL ICs

Over the last four years, THOMSON SEMICONDUCTEURS has developed a new high performance line of standard Digital Bipolar ICs including advanced PROMs, microprocessors (2900 second source) and gate arrays.

In order to provide first range VLSI functions for high speed applications, THOMSON SEMICONDUCTEURS uses the necessary technologies such as H-BIP1 (advanced TTL process), H-BIP2 (lateral oxide isolation process) and Triple Diffused (2 μ - size and wafer stepper).

Concerning the future, THOMSON SEMICONDUCTEURS will carry on its PROM plan (from 8 K up to 128 K) using state-of-the-art H-BIP3 process (full oxide isolation process).

For more information about new products, please contact your local THOMSON SEMICONDUCTEURS sales representatives and ask for specific technical literature.

The specification of the devices referred to in this data book may have changed. For up dated information regarding static and dynamic characteristics, please consult the current issue of the relevant data sheet.

Industrial power: a solid support

Thousands of people trained to our exacting professional standards, the latest state-of-the-art production and control equipment, product design aided by powerful data processing resources - all these made it possible to produce millions of integrated circuits and discrete components in these THOMSON SEMICONDUCTEURS plants last year :

In France

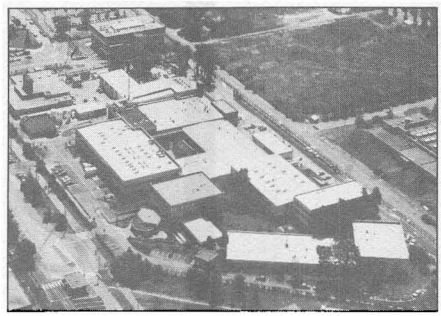
- St-Egreve: - bipolar integrated circuits, ECL-TTL gate arrays, bipolar custom products.
  - military and Hi-Rel integrated circuits covering the whole product spectrum according to international standards. (MIL-STD-883 C and European standards).
- Grenoble: MOS circuits & microsystems, CMOS, MOS custom products.
- Rousset: MOS circuits.
- Aix-en-Provence: switching power transistors, rectifiers, zeners.
- Tours: thyristors and triacs, switching power MOS transistors, zeners.
- Alençon: power modules, molding and assembly of semiconductors to perform complex functions, thyristors, triacs, rectifier diodes and zeners.

In United States

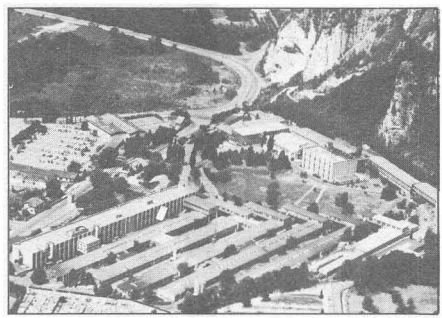
- Montgomeryville, PA: RF and microwave power transistors for mobile communications. TV transmission, radar, IFF, DME, and TACAN applications.

In Morocco, Brazil, the Philippines and Singapore

- Assembly and test centers.



MOS circuit plant in Grenoble (France)



Bipolar and military & space circuits plants in St-Egreve (France)

Commercial network: a worlwide service

THOMSON SEMICONDUCTEURS has one of the most comprehensive service and technical networks in the world at its disposal, with commercial services operating in Germany, Austria, Belgium, Brazil, Canada, Spain, France, Hong Kong, Ireland, Italy, Japan, Morocco, the Netherlands, Singapore, the United Kingdom, and the United States, in addition to its worldwide distribution network.

THOMSON SEMICONDUCTEURS is always at the customer's service, with technical assistance, applications laboratories, software, and development of microcontrollers, gate array networks and custom circuits available to meet their needs.

THOMSON SEMICONDUCTEURS
created by the THOMSON Group to meet today's most demanding technological changes.

With its four divisions-MOS, Bipolar, Discrete, Military & Space-THOMSON SEMICONDUCTEURS represents a major commitment to the advancement of electronics. It has enabled the THOMSON Group to implement a whole new set of strategies, technologies, production capabilities, technical and commercial services, and to focus on delivering effective answers to the multiple challenges facing today's electronics industry.

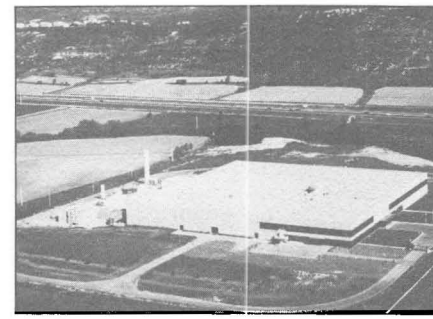
Technological competence: a guarantee

THOMSON SEMICONDUCTEURS maintains Research and Development Laboratories in Grenoble, St-Egreve, Tours, Rousset, Aix-en-Provence and Montgomeryville, PA (USA). Together with their Central Laboratories. THOMSON SEMICONDUCTEURS conducts highly independent research, and offers its customers the latest advances in technology:

Research activities dedicated to the development of new and improved products are carried out simultaneously in all these laboratories.

Among the more significant developments:
- Improved MOS and bipolar technologies for linear and digital LSI circuits and power circuits.
- New packaging processes to increase miniaturization and improve reliability; e.g. SO, SOT, plastic and ceramic chip-carriers.
- New power circuit packages: TOP 3, ISOTOP, etc.
- Technologies of the future, notably in solid state physics leading to the development of new components in professional, industrial and consumer electronics, as well as the telecommunications and computer aided design fields.

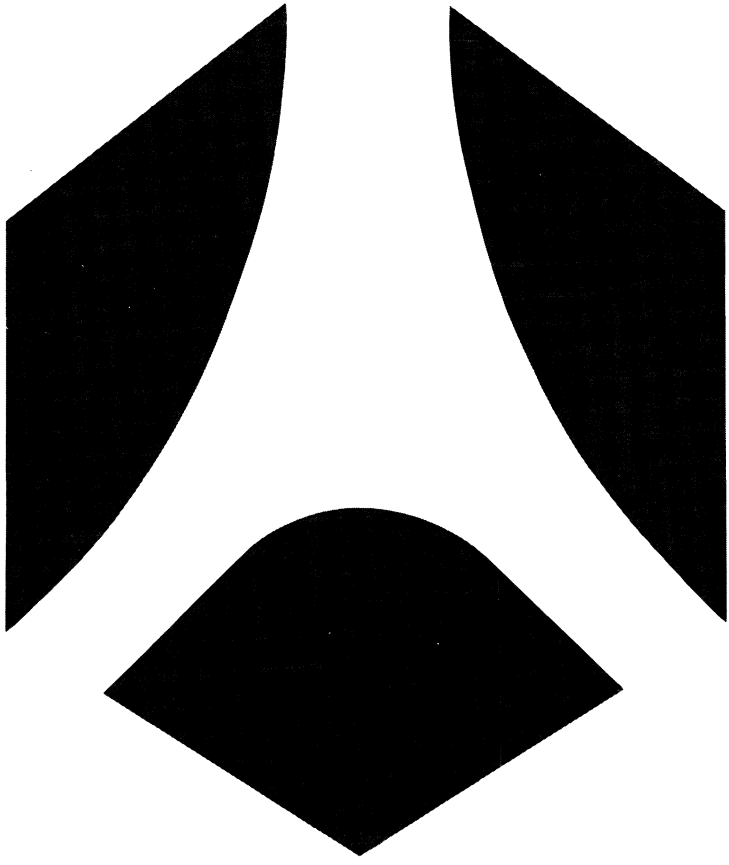
A full 20% of THOMSON SEMICONDUCTEURS sales revenues are reinsvested in Research and Development.



MOS circuit plant in Rousset (France)

CONTENTS

● Hi-Rel versions available - See chapter 4



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Bipolar memories

BIPOLAR MEMORY CROSS REFERENCE

PROM Kbytes	AMD	FAIRCHILD	FUJITSU	HARRIS	MMI	NS	SIGNETICS	TEXAS	THOMSON SC
8 K	27S181	93Z451	7132	7681	6381	–	82S181A	–	**TS71181A**
	27S181A	–	–	–	–	–	82S181B	–	**TS71181B**
	–	–	–	–	–	–	–	–	**TS71181C**
	27S281A	–	–	–	–	–	–	–	**TS71281C**
16 K	–	–	–	–	–	–	82S191	–	**TS71191**
	27S191	93Z511	7138	76161	–	87S191	82S191A	28S166	**TS71191A**
	–	–	–	–	–	–	–	–	**TS71191B**
	27S191A	–	–	–	631681	–	–	–	**TS71191C**
	27S291A	–	–	–	–	–	–	–	**TS71291C**
32 K	–	–	7142	76321	63S3281	–	82S321	–	**TS71321C**
64 K	27S49	–	7143	76641	–	–	–	–	**TS71641**

THOMSON SEMICONDUCTEURS

TS71180
TS71181
TS71280
TS71281

PRODUCT PREVIEW

8 K FAST PROMs

The TS71180, 71181, 71280, 71281 are programmable read-only memories (PROM) organized in 1024 words by 8-bit configuration and are field programmable. They are shipped in an unprogrammed form and have "0" in all locations.

These PROM's are available with open collector (TS71180/71280) or three state outputs (TS71181/71281).

- Fast access times :
  Address access time : 25 ns max (TS71180C-71181C-71280C-71281C)
  35 ns max (TS71180B-71181B-71280B-71281B)
  45 ns max (TS71180A-71181A-71280A-71281A)

- Low voltage programming
- Highly reliable fuses Ti/W for ultra-fast programming
- Low power Schottky technology (oxide isolation process)
- TTL compatible
- Industry standard pin configuration.

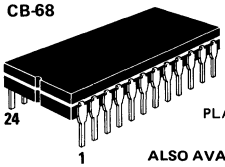
APPLICATIONS
- Microprogramming
- Hardwired algorithms
- Random logic
- Code conversion
- Sequential controllers

8 K FAST PROMs

1

CASES

CB-68



TS71180
TS71181

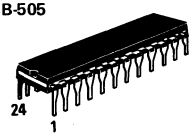
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

C SUFFIX
CERAMIC PACKAGE

CB-505



TS71280
TS71281

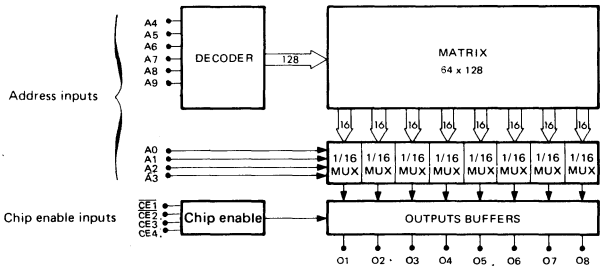
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

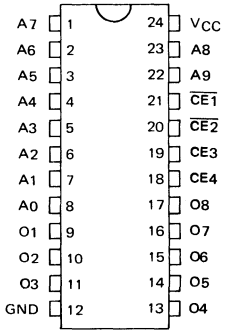
J SUFFIX
CERDIP PACKAGE

C SUFFIX
CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



V_{CC} : Power supply voltage (DC + 5 V)
O1 to O8 : Outputs.

Ref. 04565

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THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	C suffix	M suffix	Unit
Power supply	V_{CC}	5 ± 5 %	5 ± 10 %	V
Operating temperature	T_{oper}	- 0, + 70	- 55, + 125	°C
Storage temperature	T_{stg}	- 65, + 150	- 65, + 150	°C

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum input current at V_{OL} max (V_{CC} = V_{CC} max, V_I = 0.45 V)	I_{IL}	–	–	- 0.25	–	–	- 0.25	mA
Maximum input current at V_{IH} min (V_{CC} = V_{CC} max, V_I = 2.7)	I_{IH}	–	–	40	–	–	40	µA
Maximum input current (V_{CC} = V_{CC} max, V_I = 5.5 V)	I_{IR}	–	–	40	–	–	50	µA
Low level input voltage	V_{IL}	–	–	0.8	–	–	0.8	V
High level input voltage	V_{IH}	2	–	–	2	–	–	V
Short-circuit output current (V_{CC} = V_{CC} max, V_O = 0) (Note 1)	I_{SC}	- 20	–	- 70	- 15	–	- 85	mA
Low level output voltage (V_{CC} = V_{CC} min, I_{OL} = 16 mA, V_I = V_{IH} or V_{IL})	V_{OL}	–	–	0.45	–	–	0.5	V
High level output voltage (V_{CC} = V_{CC} min, I_{OH} = 2 mA, V_I = V_{IH} or V_{IL})	V_{OH}	2.4	–	–	2.4	–	–	V
Power supply current (All inputs are grounded V_{CC} = V_{CC} max)	I_{CC}	–	–	175	–	–	185	mA
Clamping input voltage (V_{CC} = V_{CC} min, V_I = −18 mA)	V_I	–	–	- 1.2	–	–	- 1.2	V
Output leakage current (V_{CC} = V_{CC} max, $\overline{CE1}$ = 2.4 V, CE2 = CE3 = 0.4 V)								
V_O = 5.5 V 71180/71280	I_{OFF}	–	–	+ 40	–	–	+ 60	µA
V_O = 5.5 V 71181/71281	I_{OZH}	–	–	+ 40	–	–	+ 60	µA
V_O = 0.5 V 71181/71281	I_{OZL}	–	–	- 40	–	–	- 60	µA
Input capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_I	–	5	–	–	5	–	pF
Output capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_O	–	8	–	–	8	–	pF

Note 1 : Only one output should be shorted at a time, otherwise permanent damage to the device may result.

Note 2 : These parameters are not 100 % tested, but are periodically sampled.

SWITCHING CHARACTERISTICS (These times are measured from threshold to threshold)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Address access time (A0-A9) → (O1....O8)	t_{AA}							ns
TS71180A, TS71181A, TS71280A, TS71281A		–	–	45	–	–	70	
TS71180B, TS71181B, TS71280B, TS71281B		–	–	35	–	–	50	
TS71180C, TS71181C, TS71280C, TS71281C		–	–	25	–	–	30	
Chip enable access time ($\overline{CE1}$, $\overline{CE2}$, CE3, CE4) → (O1....O8)	t_{CE}							ns
TS71180A, TS71181A, TS71280A, TS71281A		–	–	30	–	–	40	
TS71180B, TS71181B, TS71280B, TS71281B		–	–	25	–	–	30	
TS71180C, TS71181C, TS71280C, TS71281C		–	–	20	–	–	25	
Chip disable time ($\overline{CE1}$, $\overline{CE2}$, CE3, CE4) → (O1....O8)	t_{CD}							ns
TS71180A, TS71181A, TS71280A, TS71281A		–	–	30	–	–	40	
TS71180B, TS71181B, TS71280B, TS71281B		–	–	25	–	–	30	
TS71180C, TS71181C, TS71280C, TS71281C		–	–	20	–	–	25	

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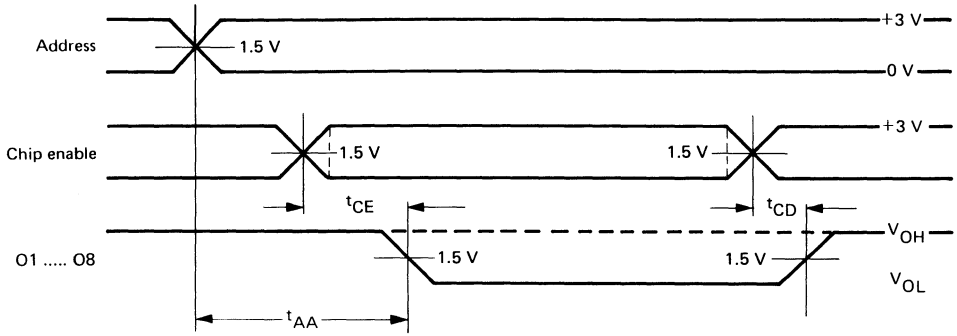
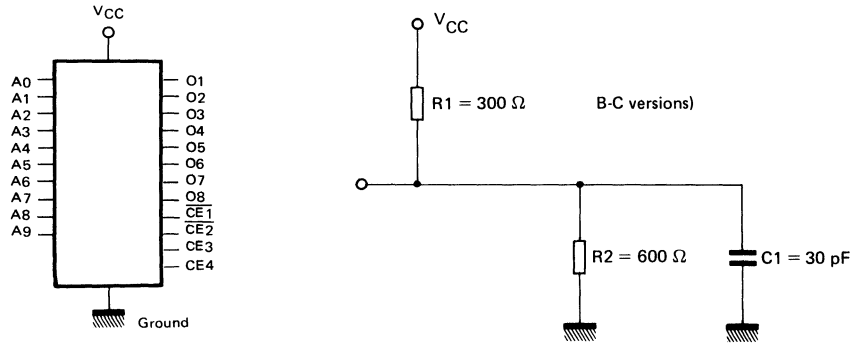
READING SEQUENCE



DYNAMIC TEST

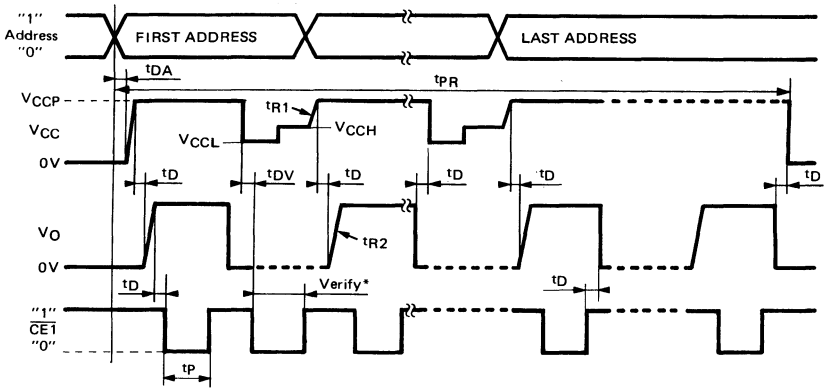


PROGRAMMING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} programming pulse	V_{CCP}	12.5	–	13	V
V_{CC} during verify	V_{CCL} V_{CCH}	4.5 –	– –	– 5.5	V V
Programming supply current (V_{CCP} = 12.75 ± 0.25 V)	I_{CCP}	–	420	550	mA
Input voltage	V_{IL} V_{IH}	0 2.4	– –	0.5 5.5	V V
Output programming voltage	V_O	11.5	12	12.5	V
Output programming current (V_O = 12 ± 0.5)	I_O	–	1.5	–	mA
V_{CC} pulse rise time	t_{R1}	5	–	10	µs
Output pulse rise time	t_{R2}	10	–	20	µs
$\overline{CE1}$ programming pulse width	t_P	40	50	60	µs
Address set-up time / V_{CCP}	t_{DA}	100	–	–	ns
Pulse sequence delay	t_D	10	–	–	µs
Delay time before verify	t_{DV}	3	–	–	µs
Programming time (V_{CC} = V_{CCP})	t_{PR}	–	–	10	s
Allowed fusing attempts		–	–	1	

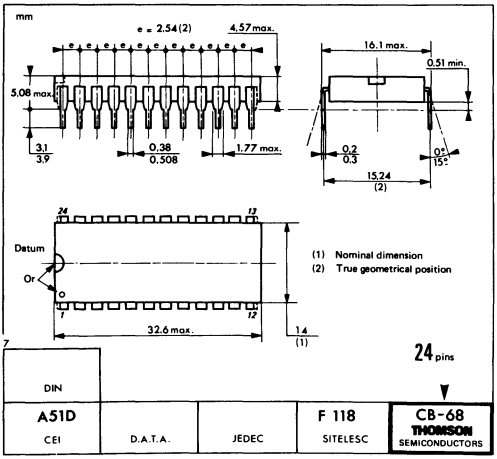
1. Select the address to be programmed. Apply $\overline{CE1}$ = H ; CE2 = H ; CE3 = H.
2. After a delay $t_{DA} \geqslant 100$ ns, raise V_{CC} to V_{CCP} = 12.75 V ± 0.25 V.
3. After a delay $t_D \geqslant 10$ µs, apply V_O = 12 ± 0.5 V to the output to be programmed. Program one output at the time. Other outputs are open.
4. After a delay $t_D \geqslant 10$ µs, apply a logic low level to the $\overline{CE1}$ input. This level will be held during t_P = 50 ± 10 µs.
5. After a delay $t_D \geqslant 10$ µs, remove output voltage V_O from the output to be programmed.
6. After a delay $t_D \geqslant 10$ µs, lower the voltage V_{CCP} to V_{CC} = 5 ± 0.5 V.
7. After a delay $t_{DV} \geqslant 3$ µs, apply a logic low level to the $\overline{CE1}$ input and verify that the programmed output remains in the high state for V_{CCH} = 5.5 V and V_{CCL} = 4.5 V (*). Then, apply a logic high level to the $\overline{CE1}$ chip select input.
8. Repeat steps 1 through 7 to program other locations of the PROM.

TYPICAL PROGRAMMING SEQUENCE



* Programming verification at both max and min V_{CC} is optional (V_{CCH}, V_{CCL}).

CASES



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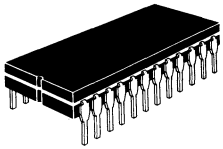
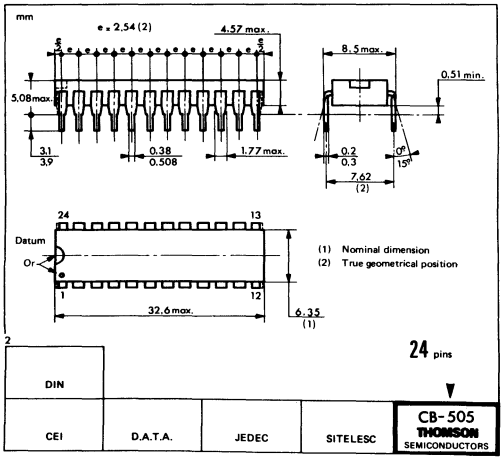


TS71180
TS71181

C SUFFIX
CERAMIC PACKAGE

ALSO AVAILABLE
J SUFFIX
CERDIP PACKAGE



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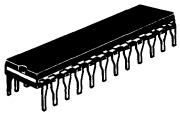


TS71280
TS71281

C SUFFIX
CERAMIC PACKAGE

ALSO AVAILABLE
J SUFFIX CERDIP PACKAGE
P SUFFIX PLASTIC PACKAGE

ORDERING INFORMATION

TS71181C | C | P | -D

- TS71181C: Part number
- C: Oper. temp.
- P: Package
- -D: Screening class

The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

	PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
		C	M	P	J	C	E	Std	-D	G/B	B/B
45 ns	TS71180A, TS71181A	●		●	●			●	●		
	TS71280A, TS71281A	●		●	●			●	●		
35 ns	TS71180B, TS71181B	●		●	●			●	●		
	TS71280B, TS71281B,	●		●	●			●	●		
25 ns	TS71180C, TS71181C	●		●	●			●	●		
	TS71280C, TS71281C	●		●	●			●	●		

Examples : TS71181CP, TS71181CP-D, TS71181CJ, TS71181CJ-D

Oper. temp. : C : 0°C to +70°C, **M :** −55°C to +125°C.
Package : P : Plastic DIL, **J :** Cerdip DIL, **C :** Ceramic DIL, **E :** Ceramic LCC.
Screening classes : Std (no end-suffix), **−D :** NFC 96883 level D.
G/B : NFC 96883 level G, **B/B :** MIL-STD-883 level B and NFC 96883 level B.

This is advance information on a new product. Specifications and information herein are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTEURS

TS71190
TS71191
TS71290
TS71291

ADVANCE INFORMATION

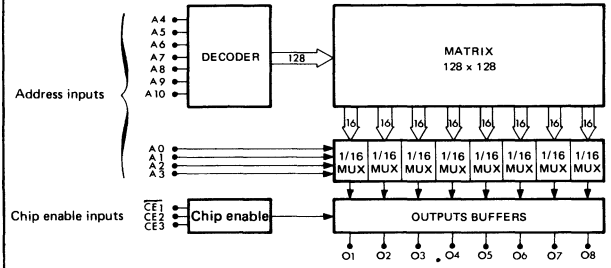
16 K FAST PROMs

The TS71190, 71191, 71290, 71291 are programmable read-only memories (PROM) organized in a 2048 words by 8-bit configuration and are field programmable. They are shipped in an unprogrammed form and have "0" in all locations.
These PROM's are available with open collector (TS71190/71290) or three state outputs (TS71191/71291).

- Fast access times :
  Address access time : 80 ns max. (TS71190, TS71191)
  60 ns max. (TS71190A, TS71191A)
  45 ns max. (TS7190B, TS71191B)
  35 ns max. (TS71190C, TS71191C)
  (TS71290C, TS71291C)
- Temperature compensating circuits to achieve a wide range of operation
- Low voltage programming
- Highly reliable fuses Ti/W for ultra-fast programming
- Low power Schottky technology
- TTL compatible
- Industry standard pin configuration.

APPLICATIONS
- Microprogramming
- Hardwired algorithms
- Random logic
- Code conversion
- Sequential controllers

BLOCK DIAGRAM



16 K FAST PROMs

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CASES

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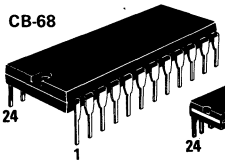

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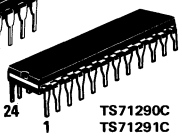


TS71290C
TS71291C

P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE
C SUFFIX CERAMIC PACKAGE
J SUFFIX CERDIP PACKAGE

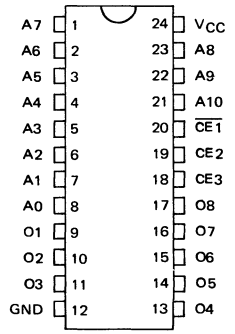
CB-707

TS71191A,B

E SUFFIX
TRICECOP (LCC)
CHIP CARRIER PACKAGE

Hi-Rel versions available - See chapter 4

PIN ASSIGNMENT



A0 to A10 : Address inputs
$\overline{CE1}$, CE2, CE3 : Chip enable inputs
V_{CC} : Power supply voltage (DC + 5 V)
O1 to O8 : Outputs.

Ref.01310

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THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	C suffix	M suffix	Unit
Power supply	V_{CC}	5 ± 5 %	5 ± 10 %	V
Operating temperature	T_{oper}	- 0, + 70	- 55, + 125	°C
Storage temperature	T_{stg}	- 65, + 150	- 65, + 150	°C

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum input current at V_{OL} max (V_{CC} = V_{CC} max, V_I = 0.45 V)	I_{IL}	–	–	- 0.25	–	–	- 0.25	mA
Maximum input current at V_{IH} min (V_{CC} = V_{CC} max, V_I = 2.7)	I_{IH}	–	–	40	–	–	40	µA
Maximum input current (V_{CC} = V_{CC} max, V_I = 5.5 V)	I_{IR}	–	–	40	–	–	50	µA
Low level input voltage	V_{IL}	–	–	0.8	–	–	0.8	V
High level input voltage	V_{IH}	2	–	–	2	–	–	V
Short-circuit output current (Note 1) V_{CC} = V_{CC} max, V_O = 0 — 71191,A,B,C 71291	I_{SC}	- 20	–	- 70	- 15	–	- 85	mA
Low level output voltage (V_{CC} = V_{CC} min, V_I = V_{IH} or V_{IL}) I_{OL} = 9.6 mA — 71190,A	V_{OL}	–	0.35	0.45	–	0.35	0.5	V
I_{OL} = 16 mA — 71190B,C 71191B,C 71290C 71291C		–	0.35	0.45	–	0.35	0.5	V
High level output voltage (V_{CC} = V_{CC} min, I_{OH} = 2 mA, V_I = V_{IH} or V_{IL})	V_{OH}	2.4	–	–	2.4	–	–	V
Power supply current (All inputs are grounded V_{CC} = V_{CC} max)	I_{CC}	–	135	175	–	135	185	mA
Clamping input voltage (V_{CC} = V_{CC} min, V_I = −18 mA)	V_I	–	–	- 1.2	–	–	- 1.2	V
Output leakage current (V_{CC} = V_{CC} max, $\overline{CE1}$ = 2.4 V, CE2 = CE3 = 0.4 V), V_O = 5.5 V — 71190,A,B,C/71290C	I_{OFF}	–	–	+ 40	–	–	+ 60	µA
V_O = 5.5 V — 71191,A,B,C/71291C	I_{OZH}	–	–	+ 40	–	–	+ 60	µA
V_O = 0.5 V — 71191,A,B,C/71291C	I_{OZL}	–	–	- 40	–	–	- 60	µA
Input capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_I	–	5	–	–	5	–	pF
Output capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_O	–	8	–	–	8	–	pF

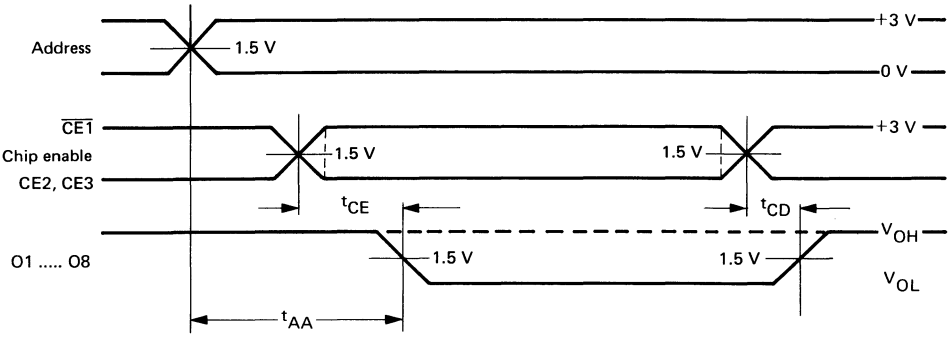
Note 1 : Only one output should be shorted at a time, otherwise permanent damage to the device may result.

Note 2 : These parameters are not 100 % tested, but are periodically sampled.

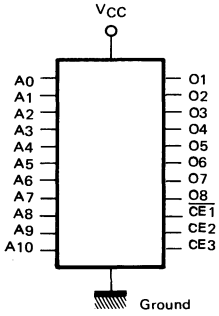
SWITCHING CHARACTERISTICS (These times are measured from threshold to threshold)

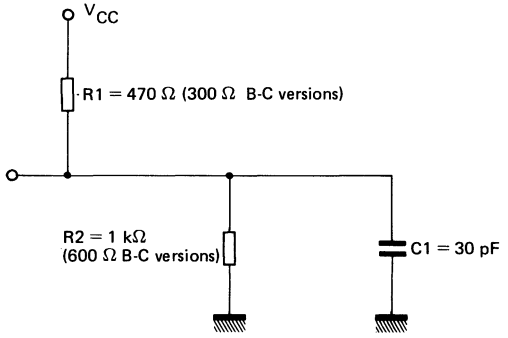
Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Address access time (A0 - A10) ⟶ (O1 ..... O8)	t_{AA}							ns
TS71190 - TS71191		–	40	80	–	50	100	
TS71190A - TS71191A		–	40	60	–	50	80	
TS71190B, TS71191B		–	–	45	–	–	65	
TS71190C, TS71191C TS71290C, TS71291C		–	–	35	–	–	55	
Chip enable access time ($\overline{CE1}$, CE2, CE3) ⟶ (O1 ..... O8)	t_{CE}							ns
TS71190,A/TS71191,A		–	20	35	–	20	45	
TS71190B, TS71191B		–	–	30	–	–	35	
TS71190C, TS71191C TS711290C, TS71291C		–	–	25	–	–	30	
Chip disable time ($\overline{CE1}$, CE2, CE3) ⟶ (O1 ..... O8)	t_{CD}							ns
TS71190,A/TS71191,A		–	20	35	–	20	45	
TS71190B, TS71191B		–	–	30	–	–	35	
TS71190C, TS71191C TS71290C, TS71291C		–	–	25	–	–	30	

READING SEQUENCE



DYNAMIC TEST



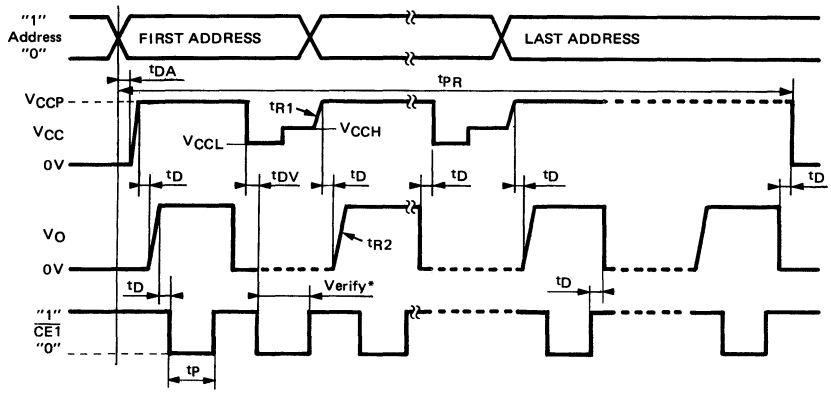


PROGRAMMING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} programming pulse	V_{CCP}	12.5	–	13	V
V_{CC} during verify	V_{CCL} V_{CCH}	4.5 –	– –	– 5.5	V V
Programming supply current (V_{CCP}= 12.75 ±0.25 V)	I_{CCP}	–	420	550	mA
Input voltage	V_{IL} V_{IH}	0 2.4	– –	0.5 5.5	V V
Output programming voltage	V_O	11.5	12	12.5	V
Output programming current (V_O= 12 ±0.5)	I_O	–	1.5	–	mA
V_{CC} pulse rise time	t_{R1}	5	–	10	µs
Output pulse rise time	t_{R2}	10	–	20	µs
$\overline{CE_1}$ programming pulse width	t_P	40	50	60	µs
Address set-up time / V_{CCP}	t_{DA}	100	–	–	ns
Pulse sequence delay	t_D	10	–	–	µs
Delay time before verify	t_{DV}	3	–	–	µs
Programming time (V_{CC}= V_{CCP})	t_{PR}	–	–	10	s
Allowed fusing attempts		–	–	1	

1. Select the address to be programmed. Apply $\overline{CE1}$ = H ; CE2 = H ; CE3 = H.
2. After a delay $t_{DA} \geqslant 100$ ns, raise V_{CC} to V_{CCP} = 12.75 V ± 0.25 V.
3. After a delay $t_D \geqslant 10$ µs, apply V_O = 12 ± 0.5 V to the output to be programmed. Program one output at the time. Other outputs are open.
4. After a delay $t_D \geqslant 10$ µs, apply a logic low level to the $\overline{CE1}$ input. This level will be held during t_P = 50 ± 10 µs.
5. After a delay $t_D \geqslant 10$ µs, remove output voltage V_O from the output to be programmed.
6. After a delay $t_D \geqslant 10$ µs, lower the voltage V_{CCP} to V_{CC} = 5 ± 0.5 V.
7. After a delay $t_{DV} \geqslant 3$ µs, apply a logic low level to the $\overline{CE1}$ input and verify that the programmed output remains in the high state for V_{CCH} = 5.5 V and V_{CCL} = 4.5 V (*). Then, apply a logic high level to the $\overline{CE1}$ chip select input.
8. Repeat steps 1 through 7 to program other locations of the PROM.

TYPICAL PROGRAMMING SEQUENCE



* Programming verification at both max and min V_{CC} is optional (V_{CCH}, V_{CCL}).

ORDERING INFORMATION

TS71191 | M | J | B/B

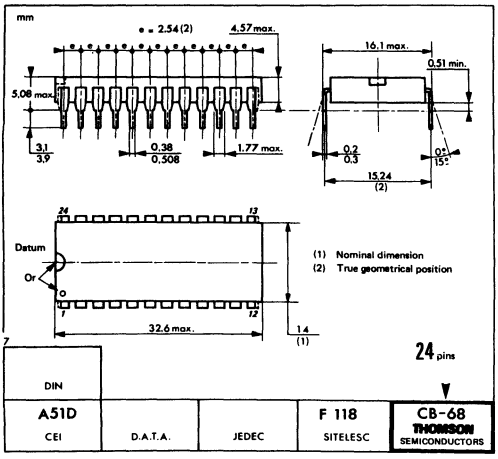
- TS71191: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

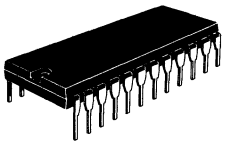
	PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
		C	M	P	J	C	E	Std	–D	G/B	B/B
80 ns	TS71190	●		●	●			●	●		
	TS71191	●		●	●			●	●		
			●		●			●		●	
			●			●	●	●		●	●
60 ns	TS71190A	●		●	●			●	●		
	TS71191A	●		●	●			●	●		
			●		●			●		●	
			●			●	●	●		●	●
45 ns	TS71190B	●		●	●			●	●		
	TS71191B	●		●	●			●	●		
			●		●			●		●	
			●			●	●	●		●	●
35 ns	TS71190C	●		●	●			●	●		
	TS71191C	●		●	●			●	●		
			●		●			●		●	
			●			●	●	●		●	●
	TS71290C	●		●	●			●	●		
	TS71291C	●		●	●			●	●		
			●		●			●		●	
			●			●		●		●	●

Examples : TS71190CP, TS71190CP-D, TS71190CJ, TS71190CJ-D

Oper. temp. : C : 0°C to + 70°C, **M :** – 55°C to + 125°C.
Package : P : Plastic DIL, **J :** Cerdip DIL, **C :** Ceramic DIL, **E :** Ceramic LCC.
Screening classes : Std (no end-suffix), **–D :** NFC 96883 level D.
G/B : NFC 96883 level G, **B/B :** MIL-STD-883 level B and NFC 96883 level B.



CASE CB-68



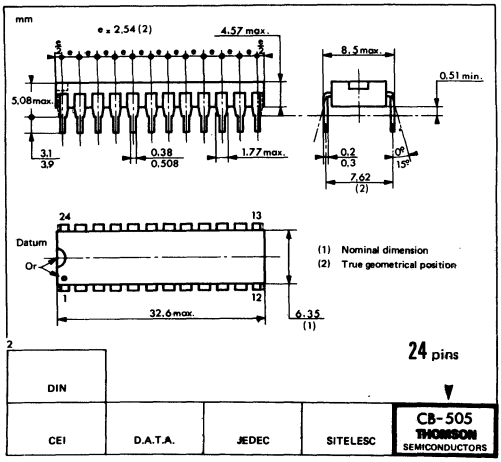
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

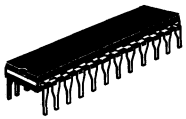
C SUFFIX
CERAMIC PACKAGE

J SUFFIX
CERDIP PACKAGE

CASES



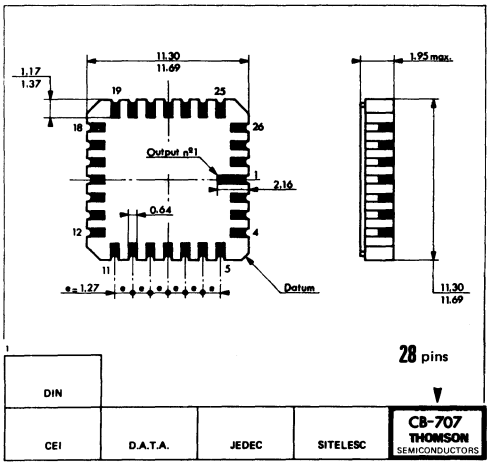
CB 505



TS71290C
TS71291C

P SUFFIX
PLASTIC PACKAGE

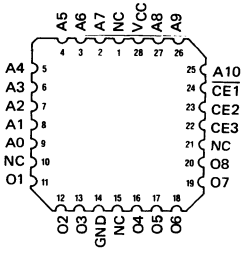
ALSO AVAILABLE
C SUFFIX CERAMIC PACKAGE
J SUFFIX CERDIP PACKAGE



CB-707

TS71190A,B
TS71191A,B

E SUFFIX
TRICECOP (LCC)
CHIP CARRIER PACKAGE



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Please inquire with our sales offices about the availability of the different packages.

Printed in France

THOMSON SEMICONDUCTEURS

TS71321

PRODUCT PREVIEW

32 K FAST PROMs

The TS71321 is programmable read-only memory (PROM) organized in a 4096 words by 8-bit configuration and is field programmable. It is shipped in an unprogrammed form and has "0" in all allocations. This PROM's is available with three state outputs (TS71321).

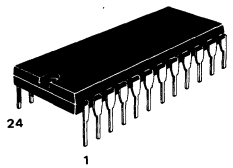
- Fast access times :
  Address access time : 45 ns max TS71321C
  55 ns max TS71321B
- Low voltage programming
- Highly reliable fuses Ti/W for ultra-fast programming
- Low power Schottky technology (oxide isolation process)
- TTL compatible
- Industry standard pin configuration.

APPLICATIONS
- Microprogramming
- Hardwired algorithms
- Random logic
- Code conversion
- Sequential controllers

32 K FAST PROMs

1

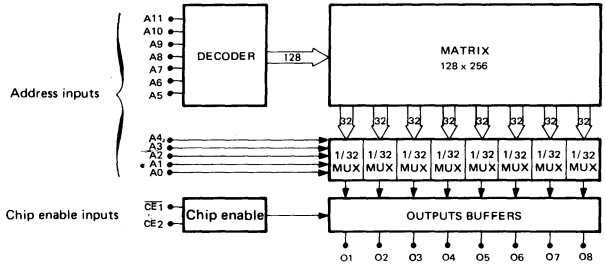
CASE CB-68



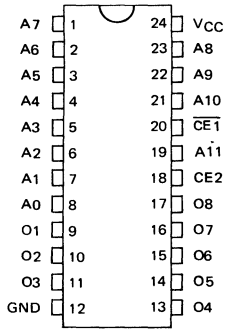
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE
J SUFFIX CERDIP PACKAGE
C SUFFIX CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



V_{CC} : Power supply voltage (DC + 5 V)
O1 to O8 : Outputs.

Ref. 04586

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45, av. de l'Europe - 78140 VELIZY - FRANCE
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THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	C suffix	M suffix	Unit
Power supply	V_{CC}	5 ± 5 %	5 ± 10 %	V
Operating temperature	T_{oper}	- 0, + 70	- 55, + 125	°C
Storage temperature	T_{stg}	- 65, + 150	- 65, + 150	°C

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum input current at V_{OL} max (V_{CC} = V_{CC} max, V_I = 0.45 V)	I_{IL}	–	–	- 0.25	–	–	- 0.25	mA
Maximum input current at V_{IH} min (V_{CC} = V_{CC} max, V_I = 2.7)	I_{IH}	–	–	40	–	–	40	µA
Maximum input current (V_{CC} = V_{CC} max, V_I = 5.5 V)	I_{IR}	–	–	40	–	–	50	µA
Low level input voltage	V_{IL}	–	–	0.8	–	–	0.8	V
High level input voltage	V_{IH}	2	–	–	2	–	–	V
Short-circuit output current (V_{CC} = V_{CC} max, V_O = 0) (Note 1)	I_{SC}	- 20	–	- 70	- 15	–	- 85	mA
Low level output voltage (V_{CC} = V_{CC} min, I_{OL} = 16 mA, V_I = V_{IH} or V_{IL})	V_{OL}	–	–	0.45	–	–	0.5	V
High level output voltage (V_{CC} = V_{CC} min, I_{OH} = 2 mA, V_I = V_{IH} or V_{IL})	V_{OH}	2.4	–	–	2.4	–	–	V
Power supply current (All inputs are grounded V_{CC} = V_{CC} max)	I_{CC}	–	–	175	–	–	185	mA
Clamping input voltage (V_{CC} = V_{CC} min, V_I = −18 mA)	V_I	–	–	- 1.2	–	–	- 1.2	V
Output leakage current (V_{CC} = V_{CC} max, $\overline{CE1}$ = 2.4 V, CE2 = CE3 = 0.4 V)								
V_O = 5.5 V	I_{OZH}	–	–	+ 40	–	–	+ 60	µA
V_O = 0.5 V	I_{OZL}	–	–	- 40	–	–	- 60	µA
Input capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_I	–	5	–	–	5	–	pF
Output capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_O	–	8	–	–	8	–	pF

Note 1 : Only one output should be shorted at a time, otherwise permanent damage to the device may result.

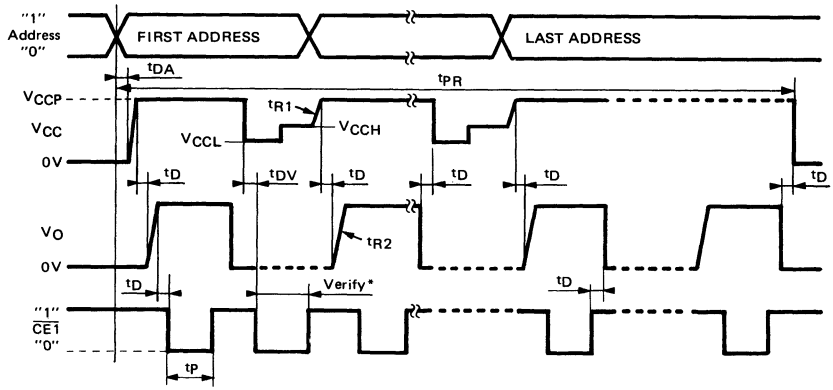
Note 2 : These parameters are not 100 % tested, but are periodically sampled.

PROGRAMMING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} programming pulse	V_{CCP}	12.5	–	13	V
V_{CC} during verify	V_{CCL} V_{CCH}	4.5 –	– –	– 5.5	V V
Programming supply current (V_{CCP} = 12.75 ± 0.25 V)	I_{CCP}	–	420	550	mA
Input voltage	V_{IL} V_{IH}	0 2.4	– –	0.5 5.5	V V
Output programming voltage	V_O	11.5	12	12.5	V
Output programming current (V_O = 12 ± 0.5)	I_O	–	1.5	–	mA
V_{CC} pulse rise time	t_{R1}	5	–	10	µs
Output pulse rise time	t_{R2}	10	–	20	µs
$\overline{CE_1}$ programming pulse width	t_P	40	50	60	µs
Address set-up time / V_{CCP}	t_{DA}	100	–	–	ns
Pulse sequence delay	t_D	10	–	–	µs
Delay time before verify	t_{DV}	3	–	–	µs
Programming time (V_{CC} = V_{CCP})	t_{PR}	–	–	10	s
Allowed fusing attempts		–	–	1	

1. Select the address to be programmed. Apply $\overline{CE1}$ = H ; CE2 = H ; CE3 = H.
2. After a delay $t_{DA} \geqslant 100$ ns, raise V_{CC} to V_{CCP} = 12.75 V ± 0.25 V.
3. After a delay $t_D \geqslant 10$ µs, apply V_O = 12 ± 0.5 V to the output to be programmed. Program one output at the time. Other outputs are open.
4. After a delay $t_D \geqslant 10$ µs, apply a logic low level to the $\overline{CE1}$ input. This level will be held during t_P = 50 ± 10 µs.
5. After a delay $t_D \geqslant 10$ µs, remove output voltage V_O from the output to be programmed.
6. After a delay $t_D \geqslant 10$ µs, lower the voltage V_{CCP} to V_{CC} = 5 ± 0.5 V.
7. After a delay $t_{DV} \geqslant 3$ µs, apply a logic low level to the $\overline{CE1}$ input and verify that the programmed output remains in the high state for V_{CCH} = 5.5 V and V_{CCL} = 4.5 V (*). Then, apply a logic high level to the $\overline{CE1}$ chip select input.
8. Repeat steps 1 through 7 to program other locations of the PROM.

TYPICAL PROGRAMMING SEQUENCE

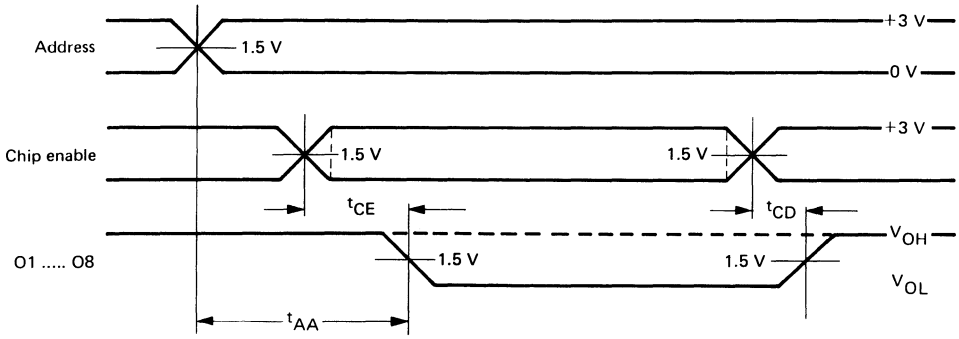


* Programming verification at both max and min V_{CC} is optional (V_{CCH}, V_{CCL}).

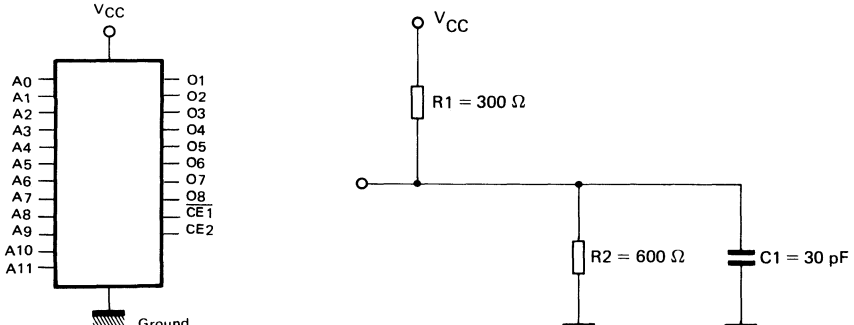
SWITCHING CHARACTERISTICS (These times are measured from threshold to threshold)

Characteristic		Symbol	C suffix			M suffix			Unit
			Min	Typ	Max	Min	Typ	Max	
Address access time	(A0-A11) → (O1....O8)	t_{AA}							ns
TS71321B			–	–	55	–	–	65	
TS71321C			–	–	45	–	–	60	
Chip enable access time	($\overline{CE1}$, CE2) → (O1....O8)	t_{CE}							ns
TS71321B			–	–	35	–	–	40	
TS71321C			–	–	20	–	–	30	
Chip disable time	(CE1, CE2) → (O1....O8)	t_{CD}							ns
TS71321B			–	–	35	–	–	40	
TS71321C			–	–	20	–	–	30	

READING SEQUENCE



DYNAMIC TEST



ORDERING INFORMATION

TS71321C | C | P | −D

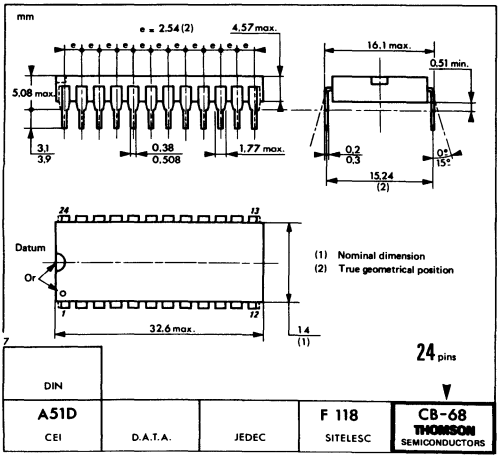
- TS71321C: Part number
- C: Oper. temp.
- P: Package
- −D: Screening class

The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

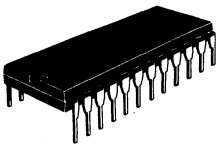
PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	−D	G/B	B/B
TS71321C 45 ns	●		●	●			●	●		
TS71321B 55 ns	●		●	●			●	●		

Examples : TS71321CP, TS71321CP-D, TS71321CJ, TS71321CJ-D

Oper. temp. : C : 0°C to + 70°C, **M :** −55°C to +125°C.
Package : P : Plastic DIL, **J :** Cerdip DIL, **C :** Ceramic DIL, **E :** Ceramic LCC.
Screening classes : Std (no end-suffix), **−D :** NFC 96883 level D.
G/B : NFC 96883 level G, **B/B :** MIL-STD-883 level B and NFC 96883 level B.



CASE CB-68



P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX	C SUFFIX
CERDIP PACKAGE	CERAMIC PACKAGE

This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTEURS

TS71640
TS71641

PRODUCT PREVIEW

64 K FAST PROMs

The TS71640, 71641 are programmable read-only memories (PROM) organized in a 8192 words by 8-bit configuration and are field programmable. They are shipped in an unprogrammed form and have "0" in all allocations. These PROM's are available with open collector (TS71640) or three state outputs (TS71641).

- Fast access times :
  Address access time : 55 ns max.
  Enable access time : 30 ns max.

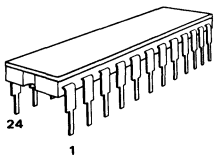
- Highly reliable shorting junction concept
- Low power Schottky technology (oxide isolation process)
- TTL compatible
- Industry standard pin configuration.

APPLICATIONS
- Microprogramming
- Hardwired algorithms
- Random logic
- Code conversion
- Sequential controllers

64 K FAST PROMs

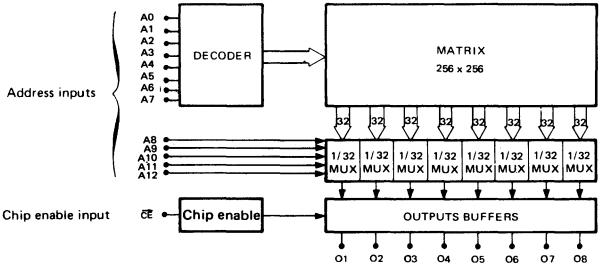
1

CASE CB-68

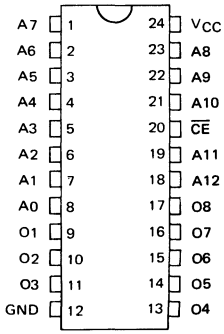


C SUFFIX
CERAMIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



V_{CC} : Power supply voltage (DC + 5 V)
O1 to O8 : Outputs.

Ref.04575

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THOMSON COMPONENTS

MAXIMUM RATINGS

Rating	Symbol	C suffix	M suffix	Unit
Power supply	V_{CC}	5 ± 5 %	5 ± 10 %	V
Operating temperature	T_{oper}	- 0, + 70	- 55, + 125	°C
Storage temperature	T_{stg}	- 65, + 150	- 65, + 150	°C

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C (unless otherwise noted)

Characteristic	Symbol	C suffix			M suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum input current at V_{OL} max (V_{CC} = V_{CC} max, V_I = 0.45 V)	I_{IL}	–	–	- 0.25	–	–	- 0.25	mA
Maximum input current at V_{IH} min (V_{CC} = V_{CC} max, V_I = 2.7)	I_{IH}	–	–	40	–	–	40	µA
Maximum input current (V_{CC} = V_{CC} max, V_I = 5.5 V)	I_{IR}	–	–	40	–	–	50	µA
Low level input voltage	V_{IL}	–	–	0.8	–	–	0.8	V
High level input voltage	V_{IH}	2	–	–	2	–	–	V
Short-circuit output current (V_{CC} = V_{CC} max, V_O = 0) (Note 1)	I_{SC}	- 20	–	- 70	- 15	–	- 85	mA
Low level output voltage (V_{CC} = V_{CC} min, I_{OL} = 16 mA, V_I = V_{IH} or V_{IL})	V_{OL}	–	–	0.45	–	–	0.5	V
High level output voltage (V_{CC} = V_{CC} min, I_{OH} = 2 mA, V_I = V_{IH} or V_{IL})	V_{OH}	2.4	–	–	2.4	–	–	V
Power supply current (All inputs are grounded V_{CC} = V_{CC} max)	I_{CC}	–	–	175	–	–	185	mA
Clamping input voltage (V_{CC} = V_{CC} min, V_I = −18 mA)	V_I	–	–	- 1.2	–	–	- 1.2	V
Output leakage current (V_{CC} = V_{CC} max, $\overline{CE1}$ = 2.4 V, CE_2 = CE_3 = 0.4 V)								
V_O = 5.5 V 71640	I_{OFF}	–	–	+ 40	–	–	+ 60	µA
V_O = 5.5 V 71641	I_{OZH}	–	–	+ 40	–	–	+ 60	µA
V_O = 0.5 V 71641	I_{OZL}	–	–	- 40	–	–	- 60	µA
Input capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_I	–	5	–	–	5	–	pF
Output capacitance (V_I = 2 V @ f = 1 MHz) (Note 2)	C_O	–	8	–	–	8	–	pF

Note 1 : Only one output should be shorted at a time, otherwise permanent damage to the device may result.

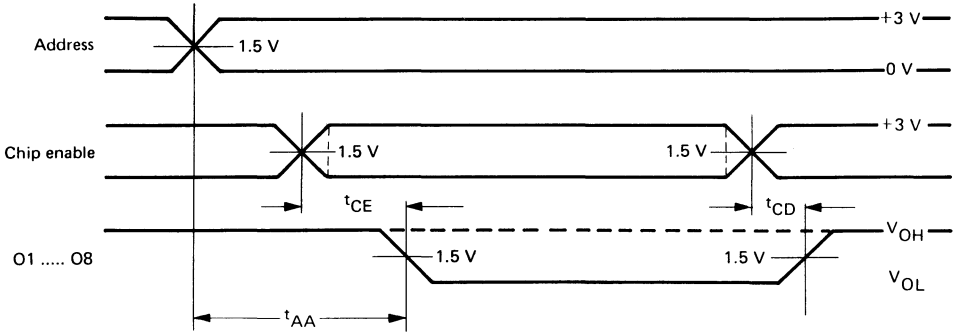
Note 2 : These parameters are not 100 % tested, but are periodically sampled.

SWITCHING CHARACTERISTICS (These times are measured from threshold to threshold)

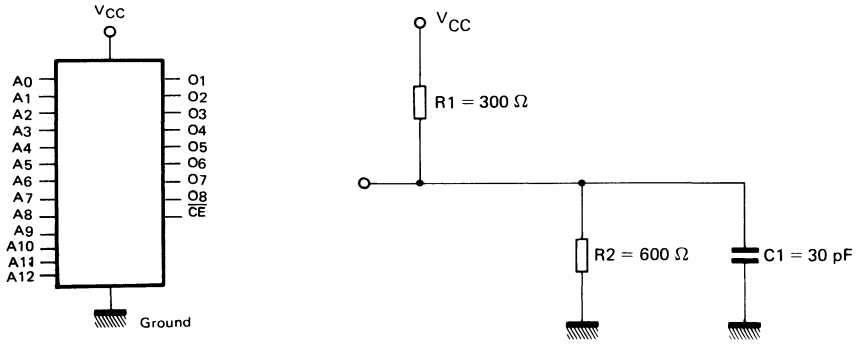
Characteristic		Symbol	C suffix			M suffix			Unit
			Min	Typ	Max	Min	Typ	Max	
Address access time	(A0 - A12) ⟶ (O1 ..... O8)	t_{AA}	–	–	55	–	–	65	ns
Chip enable access time	($\overline{CE}$) ⟶ (O1 ..... O8)	t_{CE}	–	–	30	–	–	35	ns
Chip disable time	($\overline{CE}$) ⟶ (O1 ..... O8)	t_{CD}	–	–	30	–	–	35	ns

1

READING SEQUENCE



DYNAMIC TEST



ORDERING INFORMATION

TS71640 | P | -D

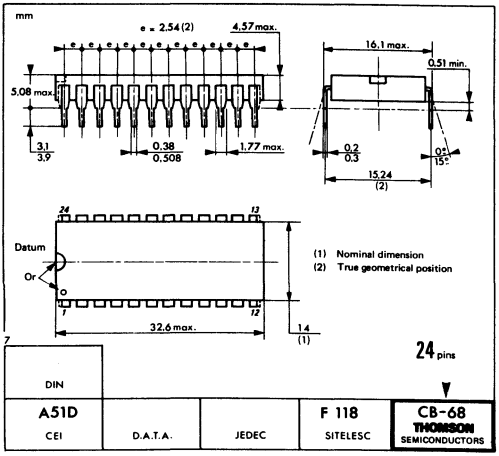
- TS71640: Part number
- P: Package
- -D: Screening class
- Oper. temp.

The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

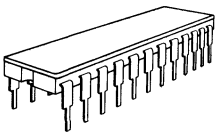
PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	-D	G/B	B/B
TS71640	●		●	●			●	●		
TS71641	●		●	●			●	●		

Examples : TS71640CP, TS71640CP-D, TS71640CJ, TS71640CJ-D

Oper. temp. : C : 0°C to + 70°C, **M :** −55°C to +125°C.
Package : P : Plastic DIL, **J :** Cerdip DIL, **C :** Ceramic DIL, **E :** Ceramic LCC.
Screening classes : Std (no end-suffix), **−D :** NFC 96883 level D.
G/B : NFC 96883 level G, **B/B :** MIL-STD-883 level B and NFC 96883 level B.

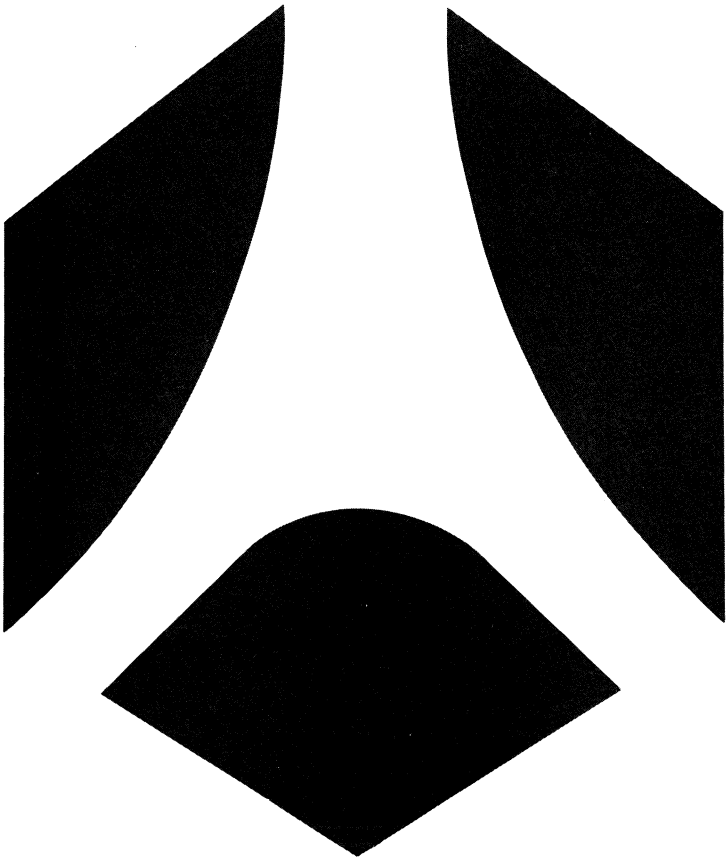


CASE CB-68



C SUFFIX
CERAMIC PACKAGE

This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.



2

Bipolar microprocessor series

THOMSON SEMICONDUCTEURS

TS2901 B

4-BIT BIPOLAR MICROPROCESSOR SLICE

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the TS2901B will allow efficient emulation of almost any digital computing machine.
The device, as shown in the block diagram (next page), consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

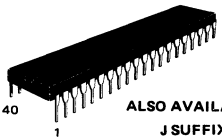
- Two-address architecture
  Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection
  ALU data is selected from five source parts for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU
  Add and shift operations take only one cycle.
- Four status flags
  Carry, overflow, zero, and negative.
- Expandable.
  Connect any number of 2901's together for longer word lengths.
- Microprogrammable
  Three groups of three bits each for source operand, ALU function, and destination control.

For applications information see the last part of this data sheet and chapters III and IV of **Bit Slice Microprocessor Design**, Mick & Brick.

4-BIT BIPOLAR
MICROPROCESSOR SLICE

CASE CB-182

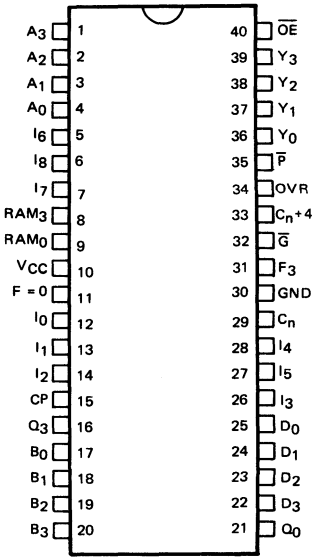
P SUFFIX
PLASTIC PACKAGE



ALSO AVAILABLE
J SUFFIX
CERDIP PACKAGE

Hi-Rel versions available - See chapter 4

PIN ASSIGNMENT



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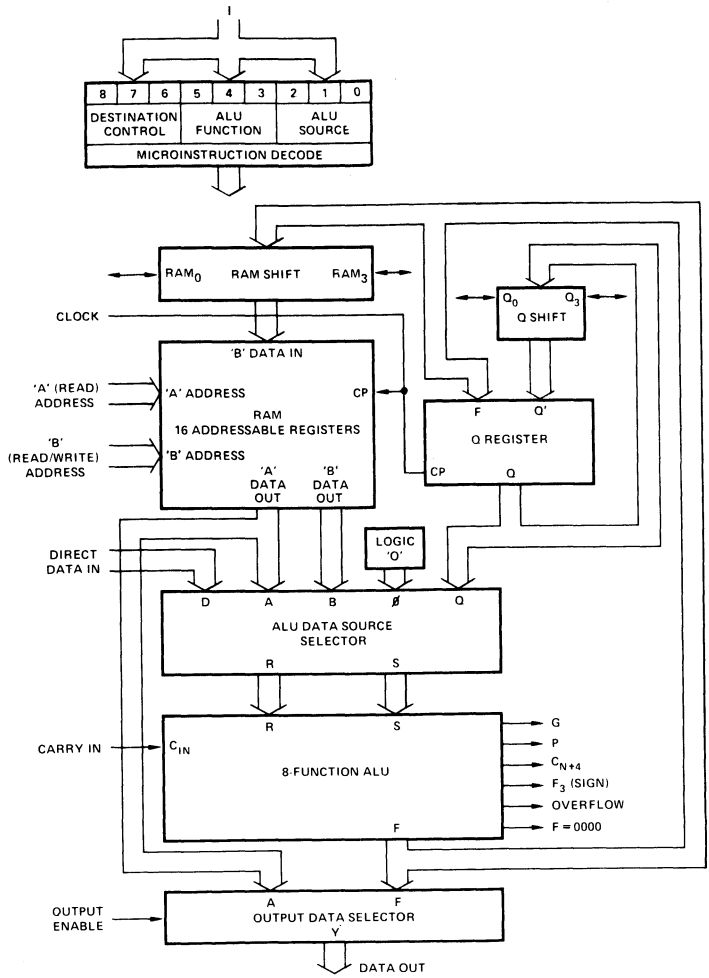
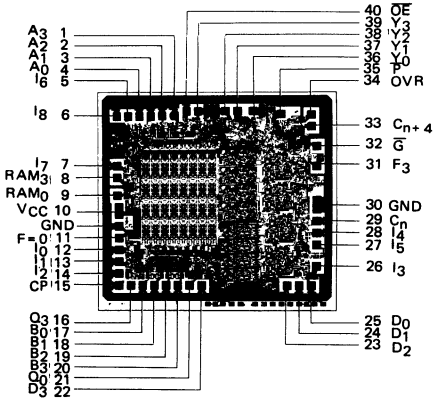
THOMSON COMPONENTS

BLOCK DIAGRAM

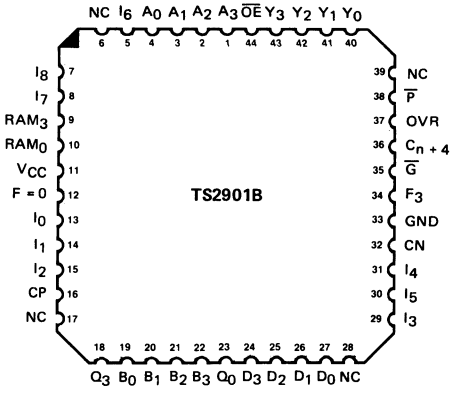


METALLIZATION AND PAD LAYOUT



TS2901B
Die size : 3.310 x 3.015 mm

CHIP CARRIER



2

PIN DEFINITION

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.

Y_{0-3} The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{G}$, $\overline{P}$ The carry generate and propagate outputs of the internal ALU. These signals are used with the 2902A for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_3 The most significant ALU output bit.

C_n The carry-in to the internal ALU.

C_{n+4} The carry-out of the internal ALU.

CP The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The 2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the 2902A. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 4.

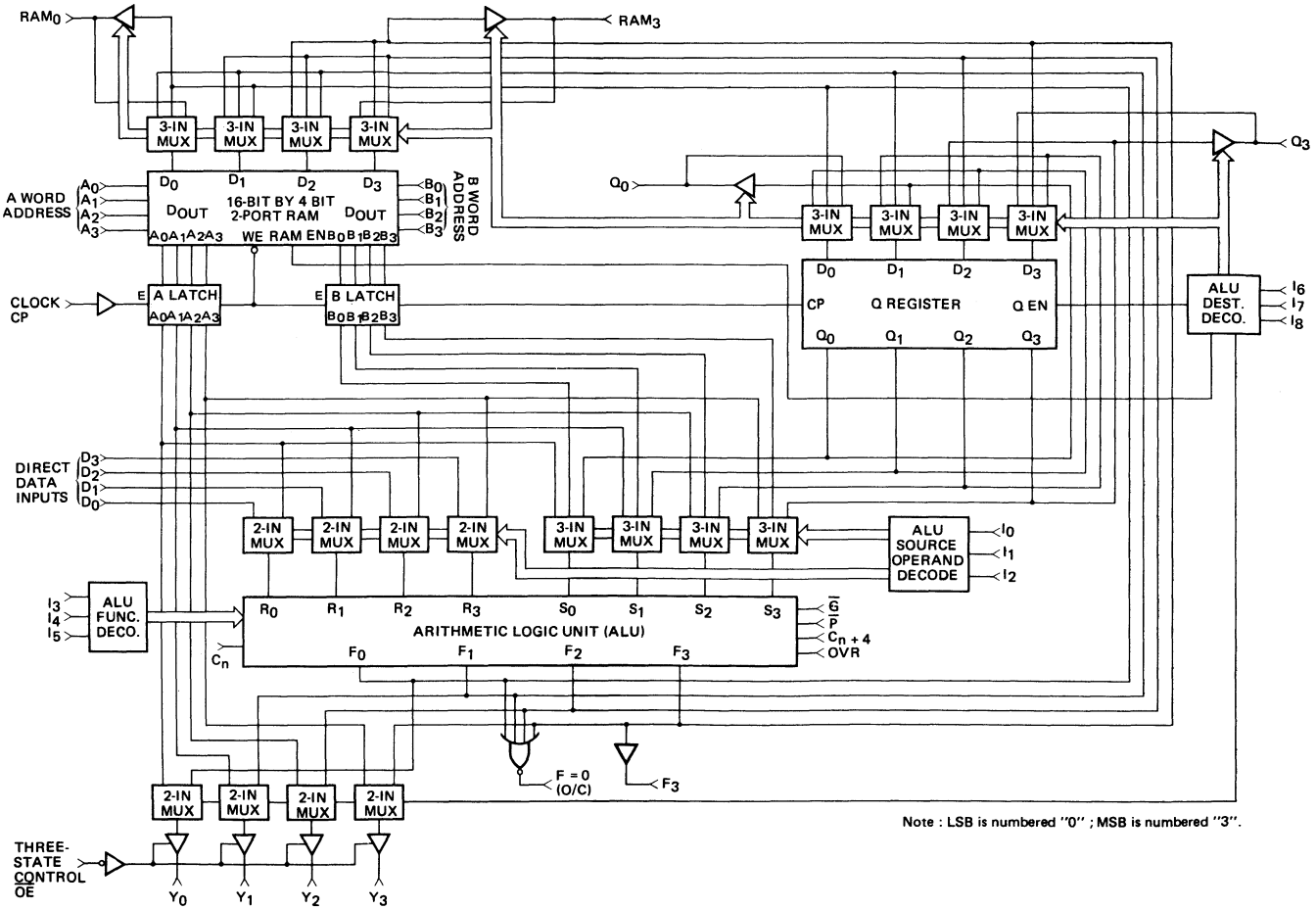
The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately *shifted up or* down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input to the 2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.



Note : LSB is numbered "0" ; MSB is numbered "3".

Figure 1. Detailed TS2901B Microprocessor Block Diagram.

Mnemonic	MICRO CODE I_2	I_1	I_0	Octal Code	ALU SOURCE OPERANDS R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE I_5	I_4	I_3	Octal Code	ALU Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	R ∀ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE I_8	I_7	I_6	Octal Code	RAM FUNCTION Shift	Load	Q-REG. FUNCTION Shift	Load	Y OUTPUT	RAM SHIFTER RAM_0	RAM_3	Q SHIFTER Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

OCTAL I_{210} / I_{543} ALU Source / ALU Function	0	1	2	3	4	5	6	7
	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0 $C_n = L$ R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
0 $C_n = H$ R Plus S	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1 $C_n = L$ S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
1 $C_n = H$ S Minus R	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2 $C_n = L$ R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
2 $C_n = H$ R Minus S	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3 R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4 R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5 $\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6 R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7 R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus ; − = Minus ; V = OR ; ∧ = AND ; ∀ = EX.OR

Figure 5. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight *source operand pairs available* to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the 2901 can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	A∨Q
3 1		A∨B
3 5		D∨A
3 6		D∨Q
6 0	EX-OR	A∀Q
6 1		A∀B
6 5		D∀A
6 6		D∀Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 6. ALU Logic Mode Functions.

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q–1	PASS	Q
1 3		B–1		B
1 4		A–1		A
2 7		D–1		D
2 2	1's Comp.	–Q–1	2's Comp. (Negate)	–Q
2 3		–B–1		–B
2 4		–A–1		–A
1 7		–D–1		–D
1 0	Subtract (1's Comp)	Q–A–1	Subtract (2's Comp)	Q–A
1 1		B–A–1		B–A
1 5		A–D–1		A–D
1 6		Q–D–1		Q–D
2 0		A–Q–1		A–Q
2 1		A–B–1		A–B
2 5		D–A–1		D–A
2 6		D–Q–1		D–Q

Figure 7. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the 2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $R \forall S$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0\,(G_0 + \overline{C_n})}$	See note

Note: $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 8.

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600μA, F_3	2.4			
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	μA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.		Y_0, Y_1, Y_2, Y_3 V_O = 2.4V			50	μA
				Y_0, Y_1, Y_2, Y_3 V_O = 0.5V			−50	
				$RAM_{0,3}$, $Q_{0,3}$ V_O = 2.4V (Note 4)			100	
				$RAM_{0,3}$, $Q_{0,3}$ V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR, $\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}$, $Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	COM'L and MIL	T_A = 25°C		160	250	mA
			COM'L Only	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			MIL Only	T_C = −55°C to +125°C			280	
				T_C = +125°C			198	

Notes
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three state output is OFF.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

Part number	V_{CC}	Temperature
CP, CJ	4.75 V to 5.25 V	T_A = 0°C to + 70°C
MJ, ME	4.50 V to 5.50 V	T_C = - 55°C to + 125°C

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. THOMSON-EFCIS recommends using $V_{IL} \leqslant 0.4$ V and $V_{IH} \geqslant 2.4$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function and AC tests as three distinct groups of tests.

I. 2901B Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the 2901 B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers:

TS2901B CP
TS2901B CJ

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	69ns
Maximum Clock Frequency to shift Q (50 % duty cycle, I = 432 or 632)	16MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	69ns

B. Combinational Propagation Delays.

C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
Cn	30	29	20	–	37	29	38	–
I012	50	47	45	45	56	53	57	–
I345	51	52	52	45	60	49	53	–
I678	28	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ↓	49	48	47	37	58	55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	69 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	51	0
Cn	–	–	39	0
I012	–	–	56	0
I345	–	–	55	0
I678	11	Do Not Change		0
RAM0, 3, Q0, 3	–	–	16	0

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	35	25

Notes :

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

II. 2901B Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the 2901 B over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers:

TS2901B MJ
TS2901B-ME

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.	88ns
Maximum Clock Frequency to shift Q (50 % duty cycle, I = 432 or 632)	15MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	88ns

B. Combinational Propagation Delays.

C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	82	84	80	70	90	86	94	–
D	44	38	40	34	50	45	48	–
Cn	34	32	24	–	38	31	39	–
I012	53	50	47	46	65	55	58	–
I345	58	58	58	48	64	56	55	–
I678	29	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	50	–	–	–	–	–	–	–
Clock ↓	53	50	49	41	63	58	61	31

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	30	0 (Note 3)	88 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	55	0
Cn	–	–	42	0
I012	–	–	58	0
I345	–	–	62	0
I678	14	Do Not Change		0
RAM0, 3, Q0, 3	–	–	18	3

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

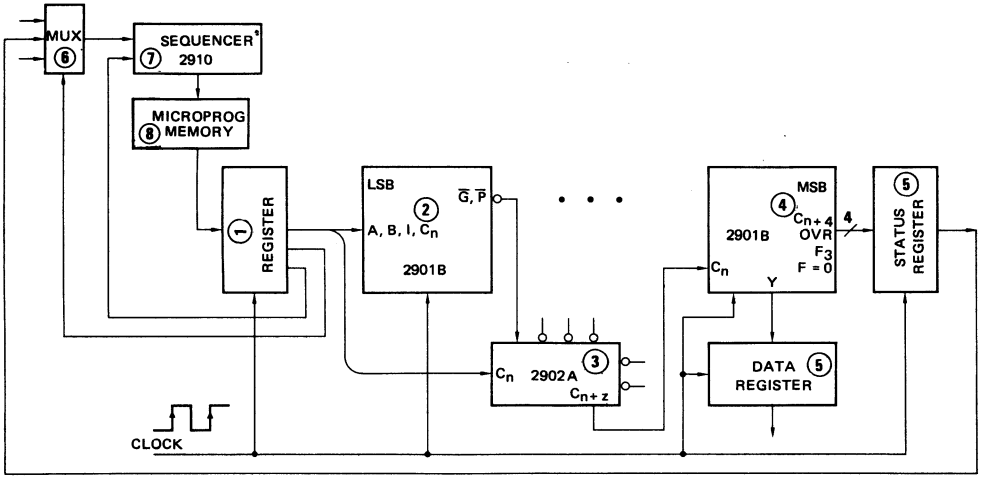
Input	Output	Enable	Disable
$\overline{OE}$	Y	40	25

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It *includes* ***all*** *the time from* stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than 2901B are representative for available MSI parts.



Pipelined System. Add without Simultaneous Shift.

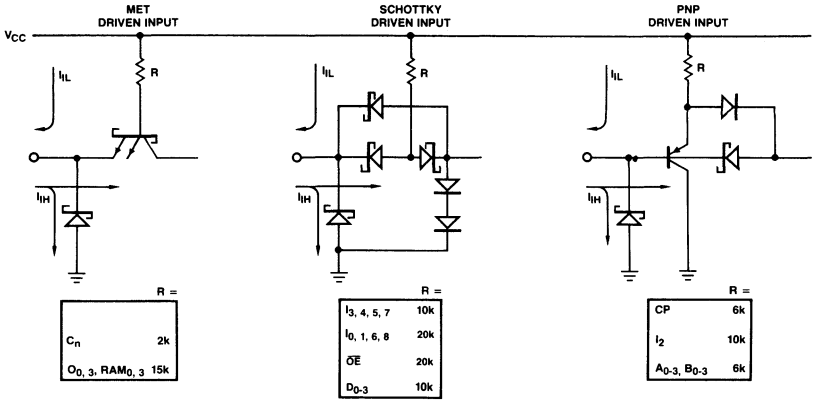
	DATA LOOP		
1	Register	Clock to Output	15
+ 2	2901B	A, B to G, P	50
+ 3	2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	10
+ 4	2901B	C_n to C_{n+4}, OVR, F_3, F = 0, Y	37
+ 5	Register	Set-up Time	5
			117ns

	CONTROL LOOP		
1	Register	Clock to Output	15
+ 6	MUX	Select to Output	20
+ 7	2910	CC to Output	45
+ 8	PROM	Access Time	55
+ 1	Register	Set-up Time	5
			140ns

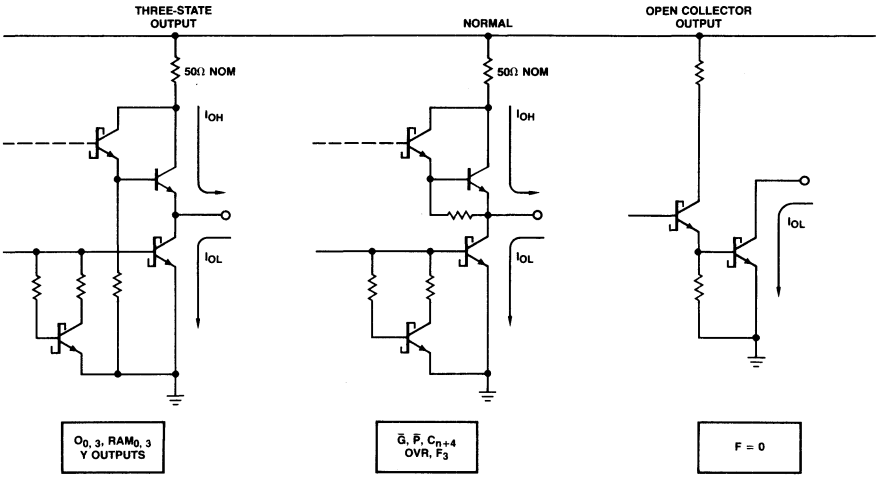
Minimum clock period = 140ns

Figure 9.

TTL INPUT/OUTPUT CURRENT INTERFACES



$C_I \approx 5.0$ pF. all inputs

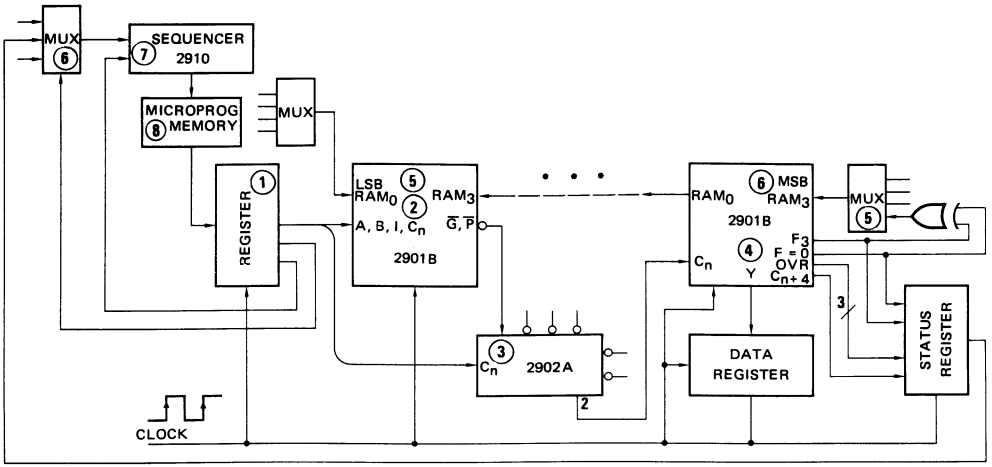


$C_O \approx 5.0$ pF all outputs

Figure 10.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS (Cont.)

Speeds used in calculations for parts other than 2901B are representative for available MSI parts.



Pipelined System. Simultaneous Add and Shift Down.

DATA LOOP		
① Register	Clock to Output	15
+ ② 2901B	A, B to $\overline{G}$, $\overline{P}$	50
+ ③ 2902A	$\overline{G}_0\overline{P}_0$ to C_{n+z}	10
+ ④ 2901B	C_n to F_3, OVR	29
+ ⑤ XOR and MUX		21
+ ⑥ 2901B	RAM_3 Set-up	16
		141ns

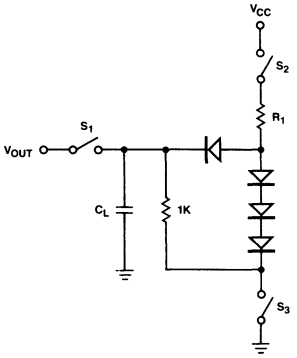
CONTROL LOOP		
① Register	Clock to Output	15
+ ⑥ MUX	Select to Output	20
+ ⑦ 2910	CC to Output	45
+ ⑧ PROM	Access Time	55
+ ① Register	Set-up Time	5
		140ns

Minimum clock period = 141ns

Figure 9 (Cont).

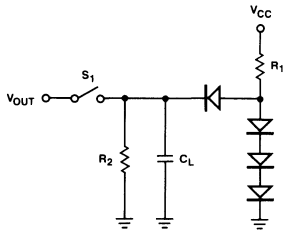
TEST OUTPUT LOAD CONFIGURATIONS FOR 2901B

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

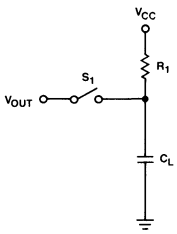
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR 2901B

Pin #	Pin Label	Test Circuit	R_1	R_2
3	RAM_3	A	560	1K
5	RAM_0	A	560	1K
7	F = 0	C	270	–
13	Q_3	A	560	1K
18	Q_0	A	560	1K
28	F_3	B	620	3.9K
29	G	B	220	1.5K
30	C_{n+4}	B	360	2.4K
31	OVR	B	470	3K
32	P	B	470	3K
33-36	Y_{0-3}	A	220	1K

USING THE TS2901B

BASIC SYSTEM ARCHITECTURE

The 2901 is designed to be used in microprogrammed systems. The nine instruction lines, the A and B addresses, and the D data inputs normally will all come from registers clocked at the same time as the 2901 . The register inputs come from a ROM or PROM – the "microprogram store." This memory contains sequences of microinstructions, typically 28 to 40 bits wide, which apply the proper control signals to the 2901s, and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the 2910 microprogram sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The 2910 is controlled by some of the bits coming from the microprogram store. Essentially these bits are the "next instruction" control.

Note that with the microprogram register in-between the microprogram memory store and the 2901s , an instruction accessed on one cycle is executed on the next cycle. As one instruction is executed, the next instruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the 2901s occurs in parallel with the access time of the microprogram store. Without the "pipeline register," these two functions must occur serially.

EXPANSION OF THE 2901

The 2901 is a four-bit CPU slice. Any number of 2901s can be interconnected to form CPUs of 12, 16, 24, 36 or more bits, in four-bit increments. Figure 12 illustrates the interconnection of three 2901s to form a 12-bit CPU, using ripple carry. Figure 13 illustrates a 16-bit CPU using carry lookahead, and Figure 14 is the general carry lookahead scheme for long words.

With the exception of the carry interconnection, all expansion schemes are the same. Refer to Figure 12. The Q_3 and RAM_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the Q_0 and RAM_0 pins of the adjacent more significant device. These connections allow the Q-registers of all 2901 s to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to three-state multiplexers which can be controlled by the microcode to select the appropriate input signals to the shift inputs. (See Figure 15).

The open collector F = 0 outputs of all the 2901 s are connected together and to a pull-up resistor. This line will go HIGH if and only if the ouput of the ALU contains all zeroes. Most systems will use this line as the Z (zero) bit of the processor status word.

The overflow and F_3 pins are generally used only at the most significant end of the array, and are meaningful only when two's complement signed arithmetic is used. The overflow pin is the

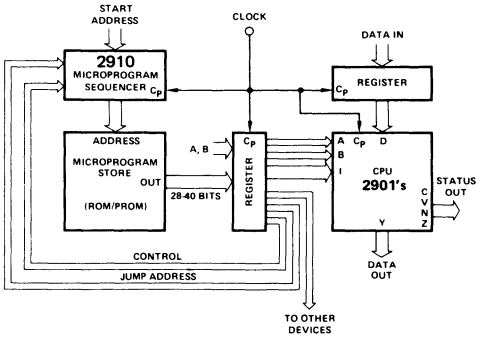


Figure 11. Microprogrammed Architecture Around 2901s.

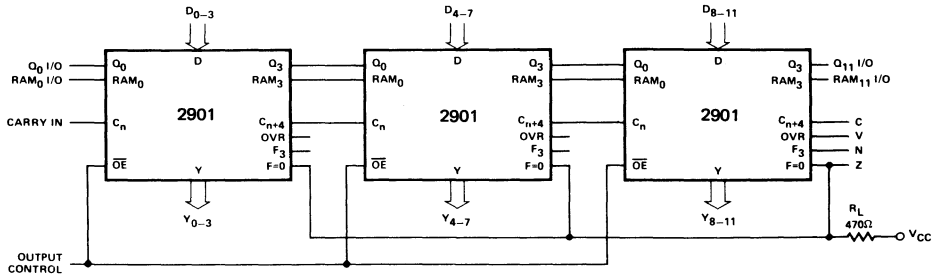


Figure 12. Three 2901s Used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B, and I Pins on all Devices are Connected together.

Exclusive-OR of the carry-in and carry-out of the sign bit (MSB). It will go HIGH when the result of an arithmetic operation is a number requiring more bits than are available, causing the sign bit to be erroneous. This is the overflow (V) bit of the processor status word. The F_3 pin is the MSB of the ALU output. It is the sign of the result in two's complement notation, and should be used as the Negative (N) bit of the processor status word.
The carry-out from the most significant 2901 (C_{n+4} pin) is the carry-out from the array, and is used as the carry (C) bit of the processor status word.

Carry interconnections between devices may use either ripple carry or carry lookahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next more significant device. Carry lookahead uses the 2902A lookahead carry generator.

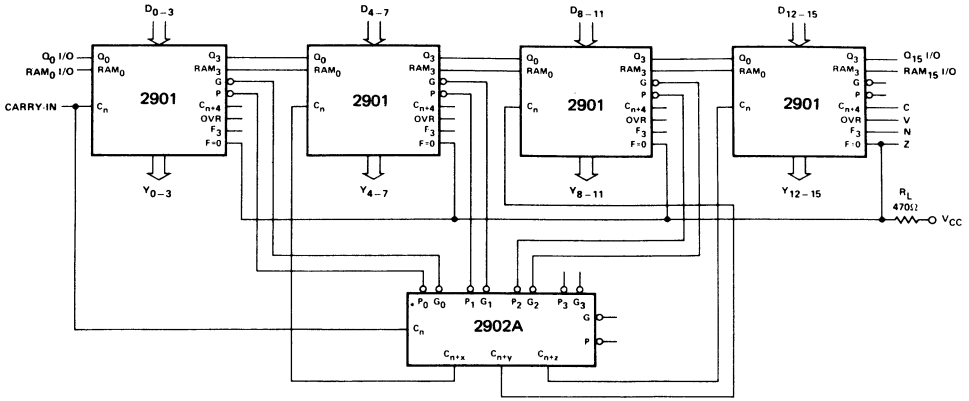


Figure 13. Four 2901s in a 16-Bit CPU Using the 2902A for Carry Lookahead.

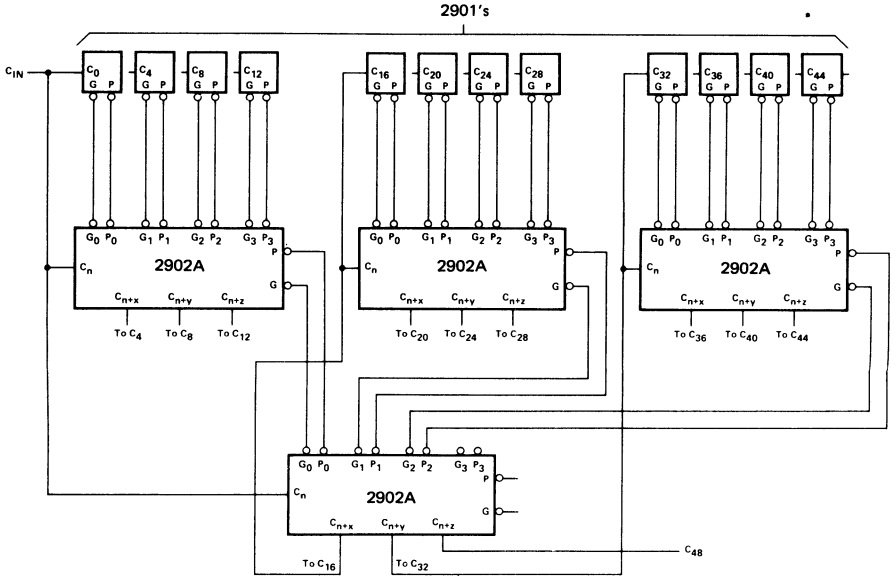


Figure 14. Carry Lookahead Scheme for 48-Bit CPU Using 12x2901s. The Carry-Out Flag (C_{48}) should be taken from the Lower 2902A Rather than the Right-Most 2901 for Higher Speed.

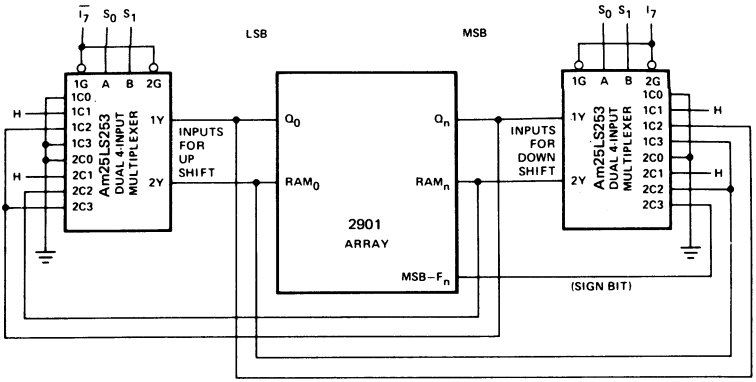


Figure 15. Three-State Multiplexers Used on Shift I/O Lines.

2

SHIFT I/O LINES AT THE END OF THE ARRAY

The Q-register and RAM left/right shift data transfers occur between devices over bidirectional lines. At the ends of the array, three-state multiplexers are used to select what the new inputs to the registers should be during shifting. The 2904 includes these multiplexers in a single LSI chip. Figure 19 shows two Am25LS253 dual four-input multiplexers connected to provide four shift modes. Instruction bit I_7 (from the 2901) is used to select whether the left-shift multiplexer or the right-shift multiplexer is active. The four shift modes in this example are:

Zero A LOW is shifted into the MSB of the RAM on a down shift. If the Q-register is also shifted, then a LOW is deposited in the Q-register MSB. If the RAM or both registers are shifted up, LOWs are placed in the LSBs.

One Same as zero, but a HIGH level is deposited in the LSB or MSB.

Rotate A single precision rotate. The RAM MSB shifts into the LSB on a right shift and the LSB shifts into the MSB on a left shift. The Q-register, if shifted, will rotate in the same manner.

Arithmetic A double-length Arithmetic Shift if Q is also shifted. On an up shift a zero is loaded into the Q-register LSB and the Q-register MSB is loaded into the RAM LSB. On a down shift, the RAM LSB is loaded into the Q-register MSB and the ALU output MSB (F_n, the sign bit) is loaded into the RAM MSB. (This same bit will also be in the next less significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}		One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1		One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

Figure 16 illustrates the interconnections for a hardware multiplication using the 2901. The system shown uses two devices for 8 x 8 multiplication, but the expansion to more bits is simple – the significant connections are at the LSB and MSB only.

The basic technique used is the "add and shift" algorithm. One clock cycle is required for each bit of the multiplier. On each cycle, the LSB of the multiplier is examined; if it is a "1", then the multiplicand is added to the partial product to generate a new partial product. The partial product is then shifted one place toward the LSB, and the multiplier is also shifted one place toward the LSB. The old LSB of the multiplier is discarded. The cycle is then repeated on the new LSB of the multiplier available at Q_0.

The multiplier is in the 2901 Q-register. The multiplicand is in one of the registers in the register stack, R_a. The product will be developed in another of the registers in the stack, R_b.

The A address inputs are used to address the multiplicand in R_a, and the B address inputs are used to address the partial product in R_b. On each cycle, R_a is conditionally added to R_b, depending on the LSB of Q as read from the Q_0 output, and both Q and the ALU output are shifted down one place. The instruction lines to the 2901 on every cycle will be:

I_{876} = 4 (shift register stack input and Q register left)
I_{543} = 0 (Add)
I_{210} = 1 or 3 (select A, B or 0, B as ALU sources)

Figure 16 shows the connections for multiplication. The circled numbers refer to the paragraphs below.

1. The adjacent pins of the Q-register and RAM shifters are connected together so that the Q-registers of both (or all) 2901s shift left or right as a unit. Similarly, the entire eight-bit (or more) ALU output can be shifted as a unit prior to storage in the register stack.

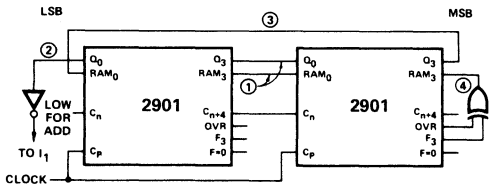


Figure 16. Interconnection for Dedicated Multiplication (8 by 8 bit) (Corresponding A, B, and I Connected together).

2. The shift output at the LSB of the Q-register determines whether the ALU source operands will be A and B (add multiplicand to partial product) or 0 and B (add nothing to partial product. Instruction bit I_1 can select between A, B or 0, B as the source operands; it can be driven directly from the complement of the LSB of the multiplier.

3. As the new partial product appears at the input to the register stack, it is shifted left by the RAM shifter. The new LSB of the partial product, which is complete and will not be affected by future operations, is available on the RAM_0 pin. This signal is returned to the MSB of the Q-register. On each cycle then, the just-completed LSB of the product is deposited in the MSB of the Q-register; the Q-register fills with the least significant half of the product.

4. As the ALU output is shifted down on each cycle, the sign bit of the new partial product should be inserted in the RAM MSB shift input. The F_3 flag will be the correct sign of the partial product unless overflow has occurred. If overflow occurs during an addition or subtraction, the OVR flag will go HIGH and F_3 is not the sign of the result. The sign of the result must then be the complement of F_3. The correct sign bit to shift into the MSB of the partial product is therefore $F3 \oplus OVR$; that is, F_3 if overflow has not occurred and $\overline{F_3}$ if overflow has occurred. On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction rather than addition should be performed, because the sign bit of the multiplier carries negative rather than positive arithmetic weight.

$$Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0$$

This scheme will produce a correct two's complement product for all multiplicands and multipliers in two's complement notation.

Figure 17is a table showing the input states of the 2901 for each step of a signed, two's complement multiplication. The 2904 LSI chip conveniently implements the required shift linkages and the EX-OR function for this algorithm.

Initial Register States

R	
0	Multiplier
1	Multiplicand
2	X
3	X

2901 Microcode

Program 2's Comp. Multiply

Final Register States

R	
0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
O ∨ A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
O ∧ B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = \overline{Q_0}$ LO	0	–	RAM_0	–	$F_3 \forall OVR$		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = \overline{Q_0}$ LO	1	–	RAM_0	–	$F_3 \forall OVR$		
O ∨ Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 17.

HARDWARE DIVISION

Division, unlike multiplication, is much more difficult to realize. One of these *difficulties can be easily understood* by visualizing a 2n-bit Dividend (X) and an n-bit Divisor (Y). The Quotient (Q) can range from 1 bit (when X < Y) to 2 n bits (when Y = 1), discarding the attempt to divide by 0. In most of the divide functions, the Remainder (R) is as important to find as is the Quotient – there is no equivalent to it in multiplication. Division becomes even more complicated when negative numbers are represented in the 2's complement notation. In the "everyday" decimal system, using Sign-and-Magnitude notation, dealing with negative numbers is relatively easy: The sign of the quotient is determined first and then a normal division is performed. Note that in this "normal" division we first "guess" the first digit of the quotient by comparing the most significant part of the dividend to the divisor. Then verify our guess by a multiplication (no "direct" division method is known), and continue to do so for all of the other digits, shifting the divisor to the right one place at a time.

The most straightforward division scheme (for unsigned numbers) is Subsequent Subtraction. The algorithm is as follows: Subtract divisor from dividend and increment a counter (initially reset to zero). Continue to do so as long as the Remainder is positive. When the Remainder becomes negative cancel the last step; i.e., add back divisor and decrement counter. The counter will contain the Quotient and the Remainder will be correct. The main drawback of this scheme is, of course, the great number of arithmetic operations needed. Again, when dealing with signed numbers, the subtraction should be substituted by addition and vice versa.

A more rapid division can be realized by calculating the Quotient digits instead of counting them. In this algorithm, the divisor is first subtracted from the most significant part of the dividend. If the remainder is positive, the quotient digit is "1," otherwise the subtraction is cancelled (by adding the divisor to the remainder) and the quotient digit will be "0." Now shift the remainder one place to the right (much like you do in a "paper and pencil" division) and repeat until all the quotient digits have been calculated. This algorithm is called "Restoring Division." When signed numbers are involved, inversion of the operations and the quotient digits will be necessary and correction should be performed in some cases. Some time is wasted in the Restoring Division because for every "0" digit in the quotient, two arithmetic operations are needed. This can be saved in the "Non-Restoring Division."

The basis of Non-Restoring Division is the same as in Restoring Division. Consider first unsigned (positive) numbers only. At the beginning, the divisor is subtracted from the most significant part of the dividend. If the result (first remainder) is positive (or zero), the first quotient digit is "1." Otherwise, the quotient digit is "0," but do not restore. Shift divisor one place to the right (or remainder to the left) and add if last quotient digit was "0;" otherwise subtract. Determine quotient digit as before and continue until all quotient digits have been computed. The remainder will be correct if it is non-negative, otherwise correction is needed by a restoring operation (on the remainder only). Extreme care should be taken of the number of bits and the value of the divisor. Assuming the divisor has n bits and the dividend as 2n bits, the above process develops n + 1 bits of the quotient. This will not be sufficient if the divisor is a small number and more digits are needed in the quotient. This condition can be easily detected as the most significant half of the dividend will be greater than the divisor in this case and division can then be terminated after setting the overflow flag. The flow chart for unsigned nonrestoring division is shown in Figure 21.

The unsigned division scheme can be applied to signed *positive* numbers without any change. When negative numbers are encountered, however, changes in the algorithm are necessary. The straightforward method of signed division seems to be "division in the first quadrant." In that scheme, negative numbers are 2's complemented to obtain positive numbers, remembering the changes done. If overflow occurs when the dividend is complemented (i.e., dividend is -2^{2n-1}, the least negative number), the overflow flag can be set and an exit from the routine taken. This is due to the fact that (-2^{2n-1}) divided by any number of n-bits cannot be represented in n bits. On the other hand, if overflow occurs when the divisor is complemented, a more complex action is needed. In this case, the dividend and the divisor should be shifted right by one place and the shifted out bit should be stored in a flag, say "Z." At the same time, a flag, "W" should also be set to indicate that division by -2^n is being attempted. These actions need to be taken since the quotient might be representable in n bits. (Here instead of dividend = divisor quotient or remainder, we have [dividend /2] = [divisor /2] * quotient + [rem /2]. The remainder obtained should be shifted left and the bit Z be added to give the correct remainder.) The division is performed on possible numbers, and finally 2's complementing is done whenever necessary. Figure 18 is the flowchart for this algorithm.

Figure 19 is the Interconnection Diagram for Division Algorithm. It is assumed that the most significant half Dividend is in Register R_X (it will be lost during the division and replaced by the Remainder), the least significant half in the Q Register and that the Divisor is in Register R_Y. The Quotient will be generated in the Q register.

After checking the signs of the Dividend and Divisor, setting the flags and negating (using 23 or 24 octal as I_5 through I_0 ALU control bits) when necessary the overflow condition should be checked. If R_X is greater than , then R_Y, overflow occurs, hence the division can be terminated by setting the overflow flag.

The first step in the Division routine is a subtract, then shift the R_X and Q registers up. I_{876} will be 6 in octal while $I_{210} = 1$ in octal and $I_5 = I_4$ = LOW. Pulling the CL bit in the microcode to HIGH, both I_3 and C_n will be high and the ALU is performing a 2's complement subtract. The sign of the Remainder will be latched in the Status Register and the complement of it will be stored in the LSB of the Q register during the shift up operation, which also discards the sign bit of the Remainder.

Now repeating the same operation for all of the other bits of the Remainder with the CL bit in the microcode LOW will leave the control of I_3 to the (complemented) previous sign bit. If it was "0" (R < 0), I_3 and C_n will be HIGH and the ALU will subtract; if it was 1 (R > 0), I_3 and C_n will be LOW and the ALU will ADD, as required. In each up shift, the complement of the present sign bit will be placed at the right of the Quotient, again, as required.

At the end of the division, the sign bit of the Remainder should be examined and if it is HIGH, the Divisor should be added to it. This can be easily implemented (not depicted on **Figure 19**) by performing an unconditional ADD (with C_n LOW), letting I_2 LOW, I_0 HIGH and controlling I_1 by the complement of the sign of the Remainder, thus adding to the RX either RY (if $R_S = 1$) or zero (if $R_S = 0$). If the dividend and divisor were shifted right because the divisor was equal to -2^n, the true remainder is obtained by shifting the remainder left and adding the flag "Z." The above method generates n + 1 bits of the quotient ($q_n \ldots q_0$) of which $q_n = 0$, since most significant half of dividend is less than the divisor. The overflow flag should be set if $q_{n-1} = 1$ since $q_{n-1} \ldots q_0$ is an unsigned positive number.

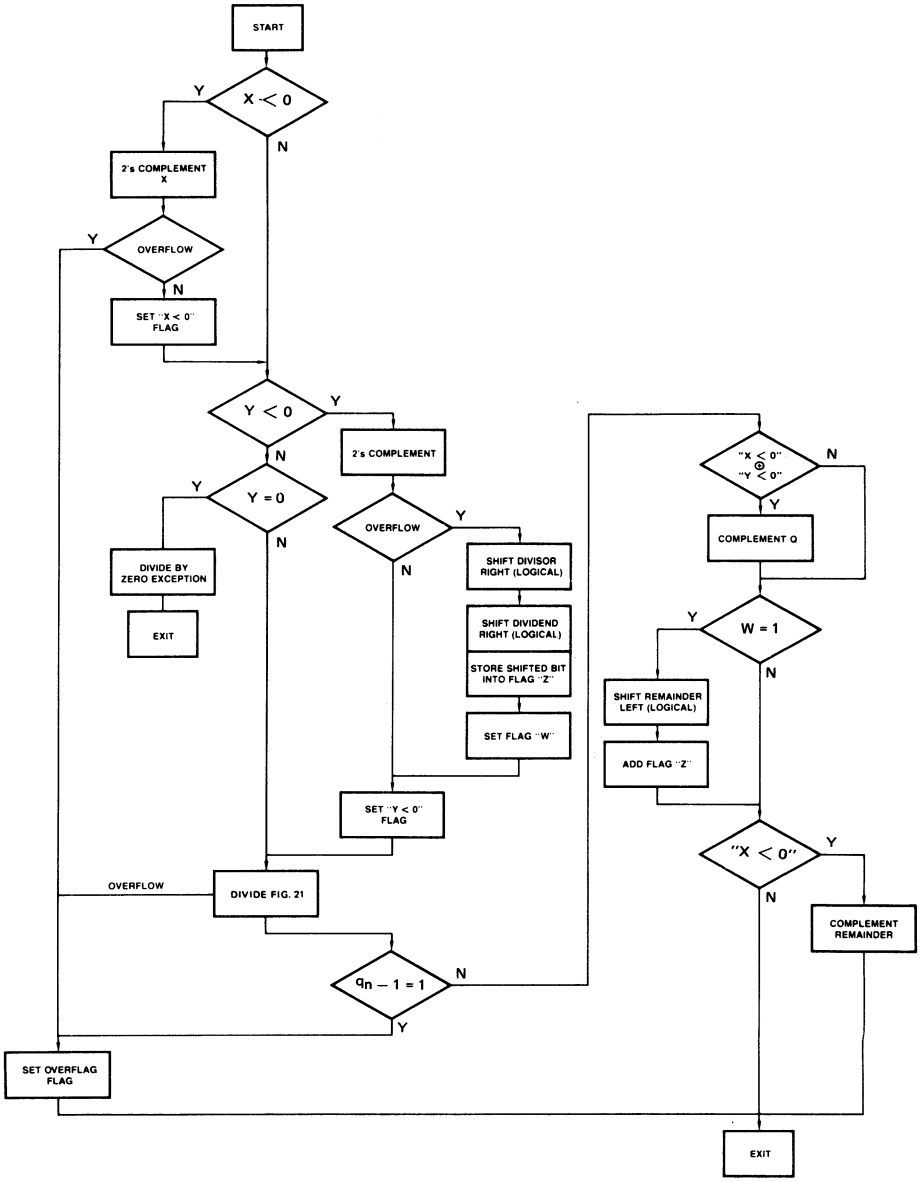


Figure 18. Flowchart for Division with Signed Numbers (Quotient = q_n, $q_{n-1} \ldots q_0$ where $q_n = 0$)

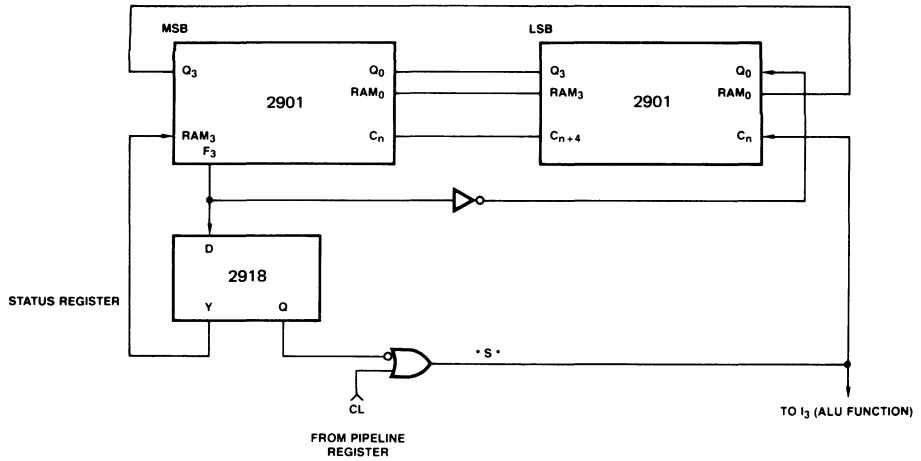


Figure 19. Interconnections for Dedicated Division

Initial Register Status

R

0	MSH Dividend
1	Divisor
Q	LSH Dividend

2901 Microcode

Program: 2's Complement Division

Final Register Status

R

0	Remainder
1	Divisor
Q	Quotient

S, F	D	Description	CL	Repeat	Pin Status (Octal)										Jump	
					A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	to	If
(B−A) *2	B	First Subtract & Shift	1	–	1	0	6	1	1	1	F_3	X	0	X		
(B±A) *2	B	Loop Subtract/Add & Shift	0	N	1	0	6	1/0	1	1/0	F_3	X	0	X		
B+0	B	Correct Remainder	X	–	1	0	3	0	1/3	0	X	X	X	X		

k = Number of leading zeros of the Divisor

N = Number of bits in the Divisor

Figure 20. 2901 Microcode for Dedicated Division

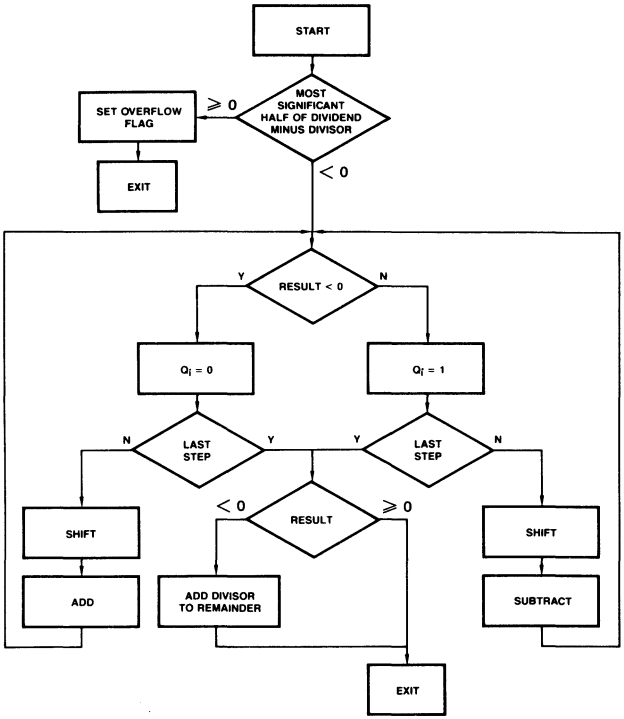


Figure 21. Flowchart for Nonrestoring Division (Unsigned Numbers)

Finally, the Quotient and/or Remainder should be 2's complemented again according to the flags. Complementation of the remainder cannot generate an overflow – because the maximum remainder after divide (Figure 21) is 0011 . . . 1 and the remainder correction when W = 1 can make the remainder at most 0111 . . . 1.

EXAMPLES OF SOME OTHER OPERATIONS

1. Byte Swapping

Occasionally the two halves of a 16-bit word must be swapped. D_{0-7} is interchanged with D_{8-15}. The quickest way to perform this operation is to rotate the word in RAM, shifting two bits at a time. Only four shift cycles are required. The same register is selected on both the A and B ports; the two are added together with carry-in connected to carry-out, producing a right shift of one place; then the ALU is shifted right one more place prior to storage.

Byte Swap of R_0

A = B = 0 I = 701 $RAM_0 = RAM_{15}$ $C_{IN} = C_{OUT}$

Repeat 4 times.

2. Instruction Fetch Cycle

Execution of a macroinstruction generally begins with an instruction fetch cycle. The current contents of the PC (in one of the registers) is the address of the macroinstruction to be fetched, and must be read out to the memory address register. Then the PC is incremented to point to the next macroinstruction. The macroinstruction obtained from memory is then loaded into the microprogram sequencer to cause a jump to the microcode for executing the instruction.

The PC can be read out and incremented in one cycle by using the 2901 destination code 2, and addressing the PC with both the A and B addresses. The current value of PC will appear on the Y outputs, and PC+1 will be returned to the register. If the PC is in register 15, then:

A = B = 15, I = 203, Carry-in = 1

The PC will be on the Y outputs via the RAM A-port. On the clock LOW-to-HIGH transition, the program counter is incremented and the value on the Y outputs is loaded into the memory address register. During the following cycle, the memory is read and, on the next clock LOW-to-HIGH transition the instruction from the memory is dropped into the instruction register. The fetch operation requires only two microcycles.

ORDERING INFORMATION

TS2901B | M | J | B/B

- TS2901B: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	– D	G/B	B/B
TS2901B	●		●	●			●	●		
		●		●	●	●	●		●	●

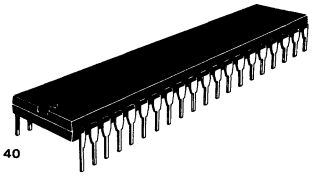
Examples : TS2901BCP, TS2901BCP-D, TS2901BCJ, TS2901BCJ-D
TS2901BMJ, TS2901BMJG/B, TS2901BMJB/B,...

Oper. temp. : **C** : 0°C to + 70°C, **M** : – 55°C to + 125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic LCC, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **– D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

2

CASE CB-182

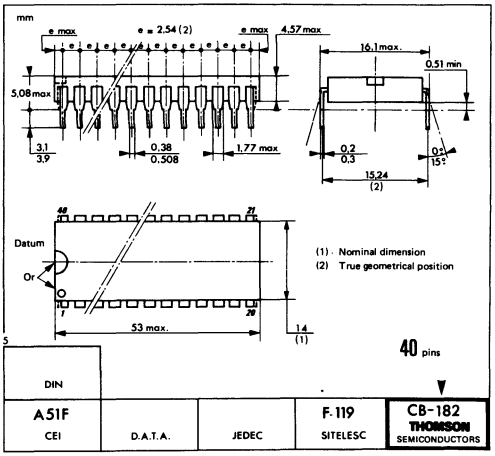
P SUFFIX
PLASTIC PACKAGE



ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTEURS

TS2901C

4-BIT BIPOLAR MICROPROCESSOR

The TS2901 industry standard four-bit microprocessor slice is a high-speed cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The microinstruction flexibility of the TS2901 permits efficient emulation of almost any digital computing machine.

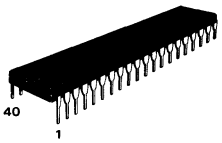
The device, as shown in the block diagram (next page), consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. The TS2901C is a plug-in replacement for TS2901B, but is 33% faster than the TS2901B.

- Two-address architecture : independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU : performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection : ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU : add and shift operations take only one cycle.
- Four status flags : carry, overflow, zero, and negative.
- Expandable : connect any number of TS2901s together for longer word lengths.
- Microprogrammable : three groups of three bits each for source operand ALU function and destination control.
- Fast : TS2901C is up to 33 % faster than TS2901B. The TS2901C meets or exceeds all of the specifications for the TS2901B.
- H-BIP2 : TS2901C is processed with THOMSON SEMICONDUCTORS proprietary H-BIP2 process.

For applications information see the last part of this data sheet and chapters III and IV of **Bit Slice Microprocessor Design**, by Mick and Brick, Mc Graw Hill Publishers.

4-BIT BIPOLAR MICROPROCESSOR

CASE CB-182



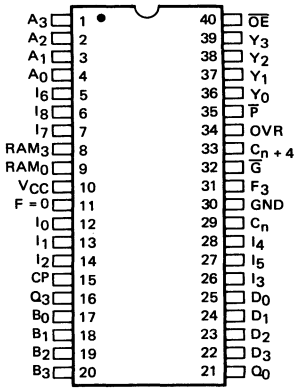
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX	E SUFFIX
CERDIP PACKAGE	CHIP CARRIER

Hi-Rel versions available - See chapter 4

PIN ASSIGNMENT



Ref. 01245-R1

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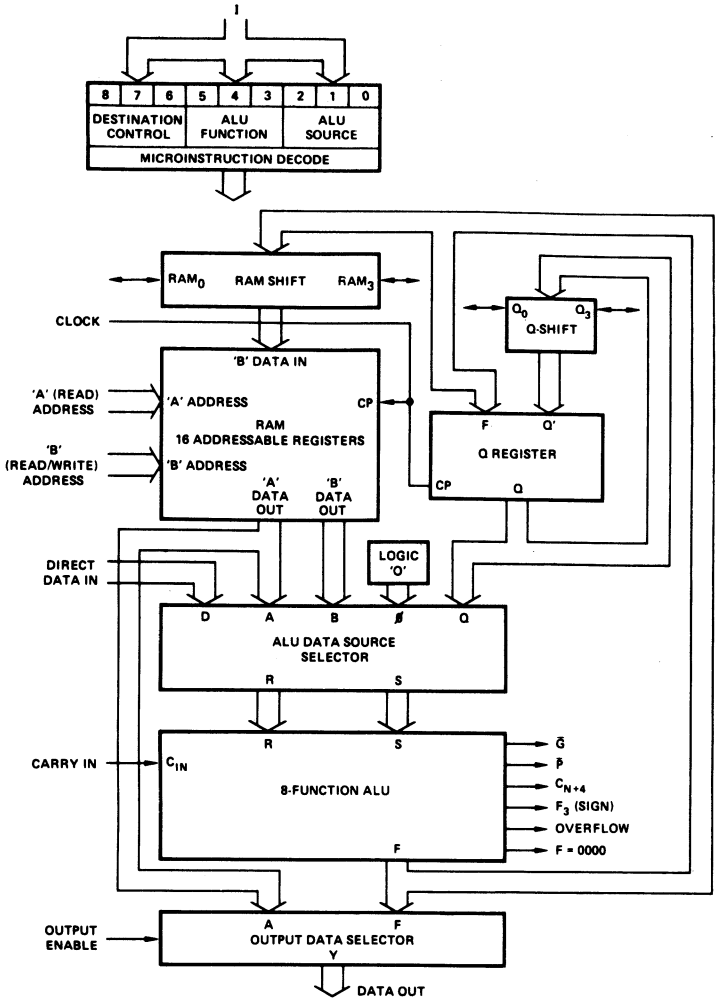
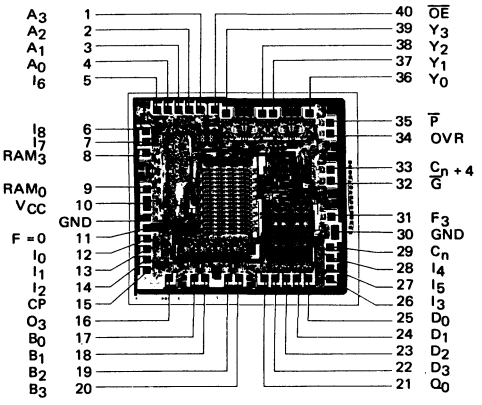
THOMSON COMPONENTS

MICROPROCESSOR SLICE BLOCK DIAGRAM



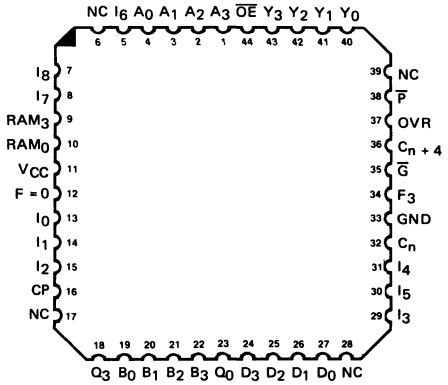
METALLIZATION AND PAD LAYOUT



TS2901C

Die size : 3.300 x 3.120 mm

LEADLESS CHIP CARRIER



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PIN DEFINITION

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM$_3$ A shift line at the MSB of the Q register (Q_3) and the register stack (RAM$_3$). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM$_3$ pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM$_0$ Shift lines like Q_3 and RAM$_3$, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM$_3$ pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.

Y_{0-3} The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{G}$, $\overline{P}$ The carry generate and propagate outputs of the internal ALU. These signals are used with the 2902A for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_3 The most significant ALU output bit.

C_n The carry-in to the internal ALU.

C_{n+4} The carry-out of the internal ALU.

CP The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The 2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the 2902A. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 4.

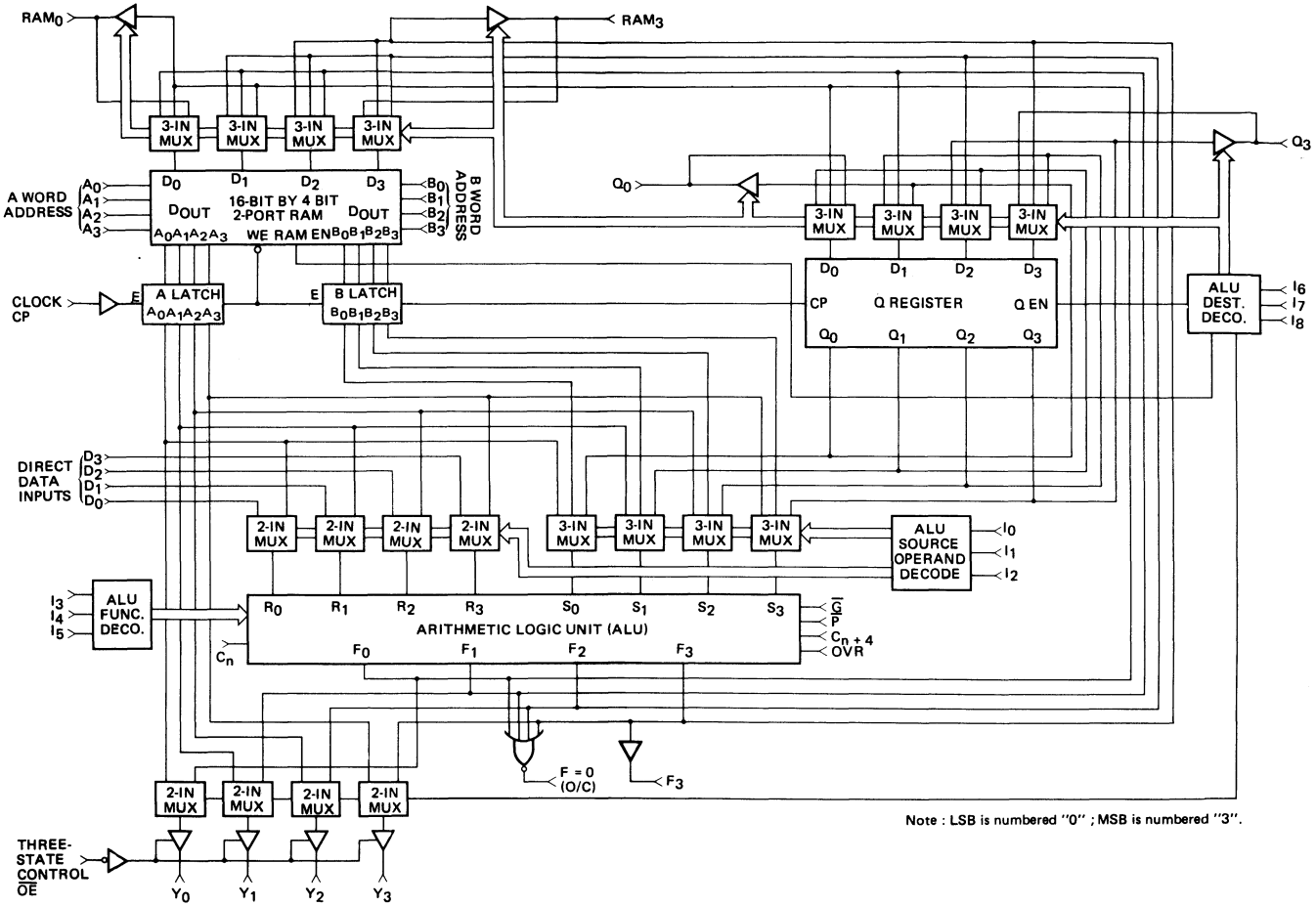
The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input to the 2901 controls the RAM, the Q register and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.



Note : LSB is numbered "0" ; MSB is numbered "3".

Figure 1. Detailed TS2901C Microprocessor Block Diagram.

FUNCTIONAL TABLES

Mnemonic	MICRO CODE I_2	I_1	I_0	Octal Code	ALU SOURCE OPERANDS R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE I_5	I_4	I_3	Octal Code	ALU Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	R ∀ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE I_8	I_7	I_6	Octal Code	RAM FUNCTION Shift	Load	Q-REG. FUNCTION Shift	Load	Y OUTPUT	RAM SHIFTER RAM_0	RAM_3	Q SHIFTER Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

OCTAL I_{210}	ALU Source / I_{543} / ALU Function	0	1	2	3	4	5	6	7
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus ; − = Minus ; V = OR ; Λ = AND ; ∀ = EX.OR

Figure 5. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the 2901 can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	A∨Q
3 1		A∨B
3 5		D∨A
3 6		D∨Q
6 0	EX-OR	A∀Q
6 1		A∀B
6 5		D∀A
6 6		D∀Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 6. ALU Logic Mode Functions.

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q−1	PASS	Q
1 3		B−1		B
1 4		A−1		A
2 7		D−1		D
2 2	1's Comp.	−Q−1	2's Comp. (Negate)	−Q
2 3		−B−1		−B
2 4		−A−1		−A
1 7		−D−1		−D
1 0	Subtract (1's Comp)	Q−A−1	Subtract (2's Comp)	Q−A
1 1		B−A−1		B−A
1 5		A−D−1		A−D
1 6		Q−D−1		Q−D
2 0		A−Q−1		A−Q
2 1		A−B−1		A−B
2 5		D−A−1		D−A
2 6		D−Q−1		D−Q

Figure 7. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the 2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0\,(G_0 + \overline{C_n})}$	See note

Note: $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 8.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

Part Number Suffix	V_{CC}	Temperature
C SUFFIX	4.75V to 5.25V	T_A = 0°C to +70°C
M SUFFIX	4.50V to 5.50V	T_C = −55°C to +125°C

Figure 9

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Figure 10.

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600μA, F_3	2.4			
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	μA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.		Y_0, Y_1, Y_2, Y_3 V_O = 2.4V			50	μA
				Y_0, Y_1, Y_2, Y_3 V_O = 0.5V			−50	
				$RAM_{0,3}$, $Q_{0,3}$ V_O = 2.4V (Note 4)			100	
				$RAM_{0,3}$, $Q_{0,3}$ V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR, $\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}$, $Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	COM'L and MIL	T_A = 25°C		160	250	mA
			COM'L Only	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			MIL Only	T_C = −55°C to +125°C			280	
				T_C = +125°C			198	

Notes:
1. V_{CC} conditions shown as MIN or MAX, refer to the military (±10%) or commercial (±5%) V_{CC} limits.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be stored at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. Worst case I_{CC} is measured at the lowest temperature in the specified operating range.
6. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

I. 2901C Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the 2901C over the commercial operating range of 0°C to + 70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers:

TS2901C CP
TS2901C CJ

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	31ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32MHz
Minimum Clock LOW Time	15ns
Minimum Clock HIGH Time	15ns
Minimum Clock Period	31ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	40	40	40	37	40	40	40	–
D	30	30	30	30	38	30	30	–
Cn	22	22	20	–	25	22	25	–
I012	35	35	35	37	37	35	35	–
I345	35	35	35	35	38	35	35	–
I678	25	–	–	–	–	–	26	26
A Bypass ALU (I = 2XX)	35	–	–	–	–	–	–	–
Clock ⌐	35	35	35	35	35	35	35	28

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	1 (Note 3)	30, 15 + T_{PWL} (Note 4)	1
B Destination Address	15	Do Not Change		1
D	–	–	25	0
Cn	–	–	20	0
I012	–	–	30	0
I345	–	–	30	0
I678	10	Do Not Change		0
RAM0, 3, Q0, 3	–	–	12 10	0

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	23	23

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

II. 2901C Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the 2901C over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers:

TS2901C MJ
TS2901C ME

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	32ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31MHz
Minimum Clock LOW Time	15ns
Minimum Clock HIGH Time	15ns
Minimum Clock Period	32ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	48	48	48	44	48	48	48	
D	37	37	37	34	40	37	37	
Cn	25	25	21		28	25	28	
I012	40	40	40	44	44	40	40	
I345	40	40	40	40	40	40	40	
I678	29						29	29
A Bypass ALU (I = 2XX)	40							
Clock ↓	40	40	40	40	40	40	40	33

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	2 (Note 3)	30, 15 + T_{PWL} (Note 4)	2
B Destination Address	15	Do Not Change		2
D			25	0
Cn			20	0
I012			30	0
I345			30	0
I678	10	Do Not Change		0
RAM0, 3, Q0, 3			12/10	0

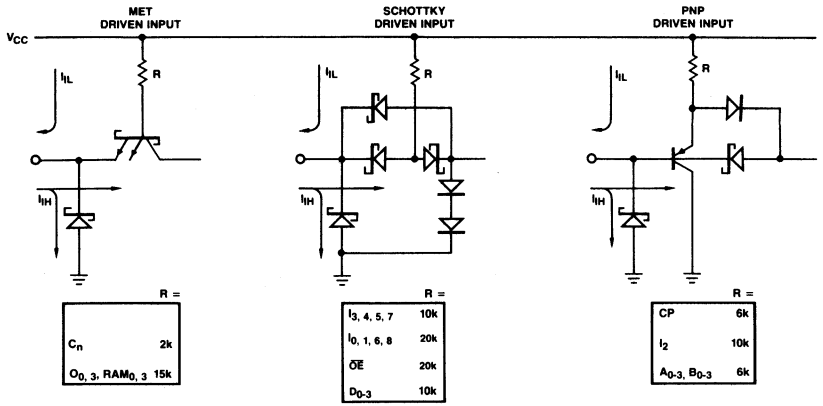
D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	25	25

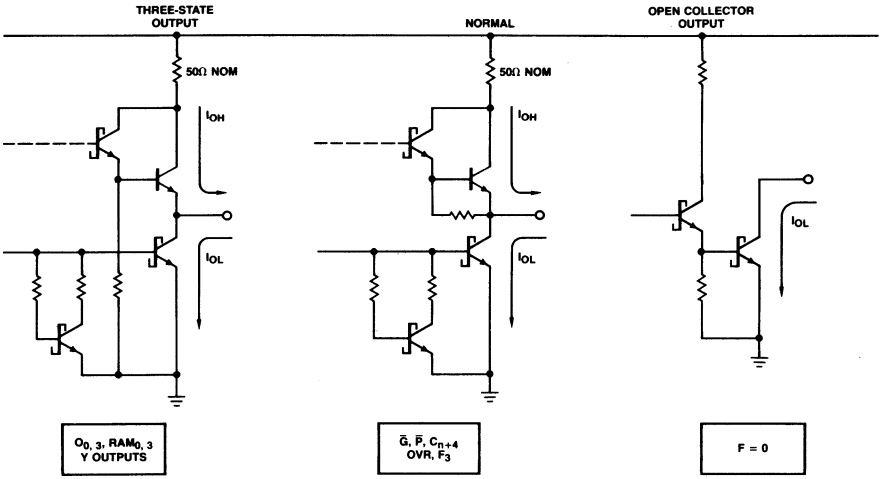
Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

TTL INPUT/OUTPUT CURRENT INTERFACES



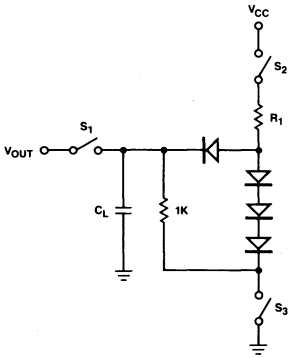
$C_I \approx 5.0pF$, all inputs



$C_O \approx 5.0pF$, all outputs

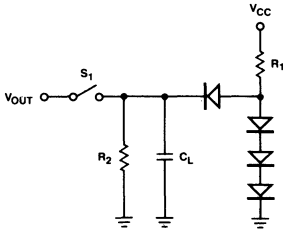
TEST OUTPUT LOAD CONFIGURATIONS FOR 2901C

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

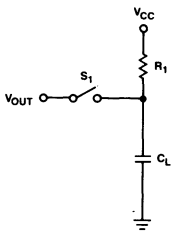
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

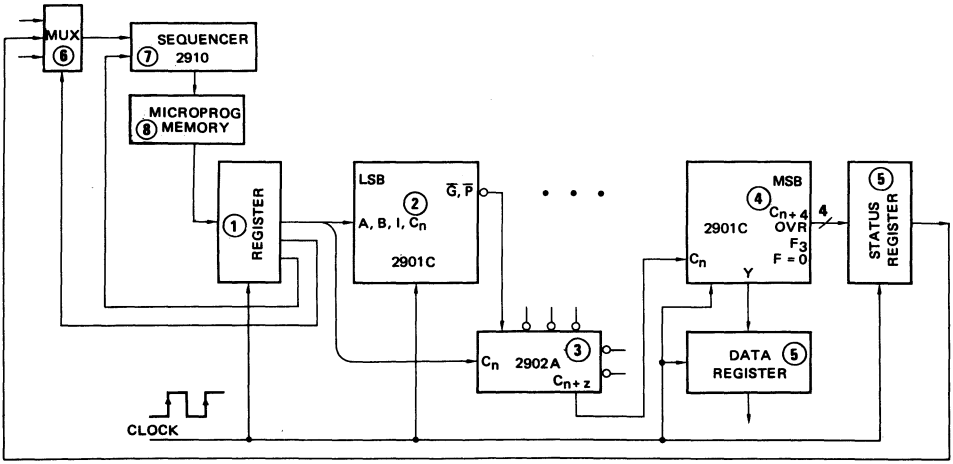
Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR 2901C

Pin #	Pin Label	Test Circuit	R_1	R_2
3	RAM_3	A	560	1K
5	RAM_0	A	560	1K
7	F = 0	C	270	–
13	Q_3	A	560	1K
18	Q_0	A	560	1K
28	F_3	B	620	3.9K
29	G	B	220	1.5K
30	C_{n+4}	B	360	2.4K
31	OVR	B	470	3K
32	P	B	470	3K
33-36	Y_{0-3}	A	220	1K

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than 2901C are representative for available MSI parts.



Pipelined System. Add without Simultaneous Shift.

DATA LOOP

	(1) Register	Clock to Output	9
+	(2) 2901C	A, B to $\overline{G}$, $\overline{P}$	37
+	(3) 2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	10
+	(4) 2901C	C_n to C_{n+4}, OVR, F_3, F = 0, Y	25
+	(5) Register	Set-up Time	2
			83ns

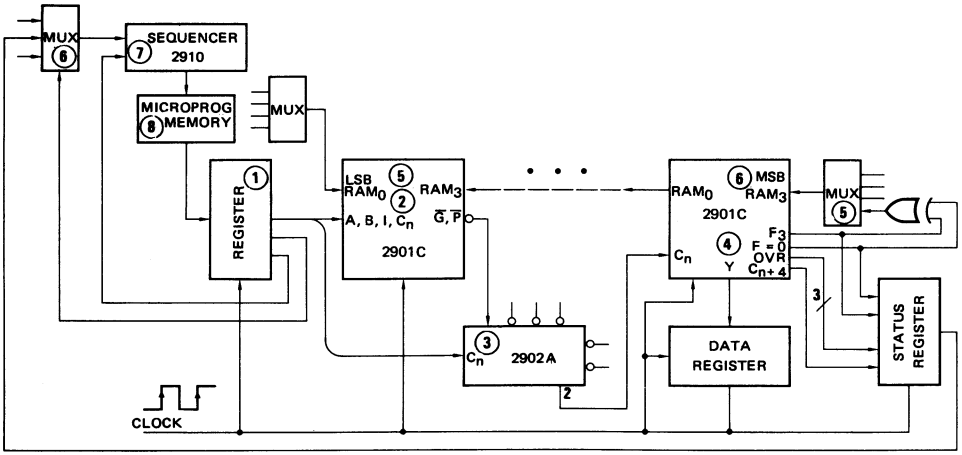
CONTROL LOOP

	(1) Register	Clock to Output	9
+	(6) MUX	Select to Output	13
+	(7) 2910	CC to Output	45
+	(8) PROM	Access Time	40
+	(1) Register	Set-up Time	2
			109ns

Minimum clock period = 109ns

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS (Cont.)

Speeds used in calculations for parts other than 2901C are representative for available MSI parts.



Pipelined System. Simultaneous Add and Shift Down.

DATA LOOP			
①	Register	Clock to Output	9
+ ②	2901C	A, B to G, P	37
+ ③	2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	10
+ ④	2901	C_n to F_3, OVR	25
+ ⑤	XOR and MUX		21
+ ⑥	2901	RAM_3 Set-up	12
			114ns

CONTROL LOOP			
①	Register	Clock to Output	9
+ ⑥	MUX	Select to Output	13
+ ⑦	2910	CC to Output	45
+ ⑧	PROM	Access Time	40
+ ①	Register	Set-up Time	2
			109ns

Minimum clock period = 114ns

USING THE TS2901C

BASIC SYSTEM ARCHITECTURE

The 2901 is designed to be used in microprogrammed systems. The nine instruction lines, the A and B addresses, and the D data inputs normally will all come from registers clocked at the same time as the 2901 . The register inputs come from a ROM or PROM – the "microprogram store." This memory contains sequences of microinstructions, typically 28 to 40 bits wide, which apply the proper control signals to the 2901s, and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the 2910 microprogram sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The 2910 is controlled by some of the bits coming from the microprogram store. Essentially these bits are the "next instruction" control.

Note that with the microprogram register in-between the microprogram memory store and the 2901s , an instruction accessed on one cycle is executed on the next cycle. As one instruction is executed, the next instruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the 2901s occurs in parallel with the access time of the microprogram store. Without the "pipeline register," these two functions must occur serially.

EXPANSION OF THE 2901

The 2901 is a four-bit CPU slice. Any number of 2901s can be interconnected to form CPUs of 12, 16, 24, 36 or more bits, in four-bit increments. Figure 12 illustrates the interconnection of three 2901s to form a 12-bit CPU, using ripple carry. Figure 13 illustrates a 16-bit CPU using carry lookahead, and Figure 14 is the general carry lookahead scheme for long words.

With the exception of the carry interconnection, all expansion schemes are the same. Refer to Figure 12. The Q_3 and RAM_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the Q_0 and RAM_0 pins of the adjacent more significant device. These connections allow the Q-registers of all 2901 s to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to three-state multiplexers which can be controlled by the microcode to select the appropriate input signals to the shift inputs. (See Figure 15).

The open collector F = 0 outputs of all the 2901 s are connected together and to a pull-up resistor. This line will go HIGH if and only if the ouput of the ALU contains all zeroes. Most systems will use this line as the Z (zero) bit of the processor status word.

The overflow and F_3 pins are generally used only at the most significant end of the array, and are meaningful only when two's complement signed arithmetic is used. The overflow pin is the

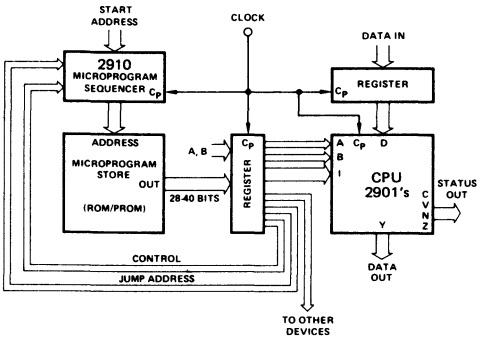


Figure 11. Microprogrammed Architecture Around 2901s.

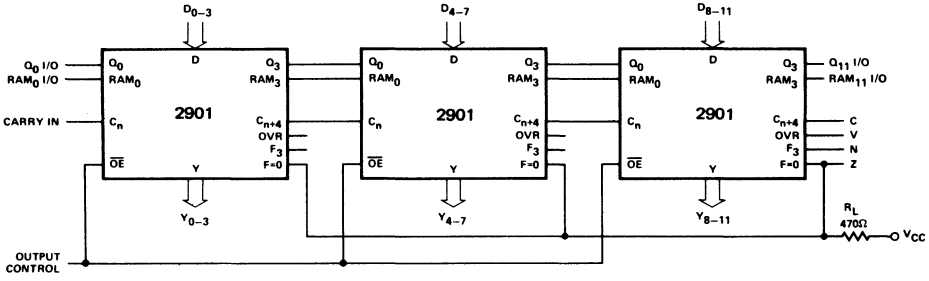


Figure 12. Three 2901s Used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B, and I Pins on all Devices are Connected together.

Exclusive-OR of the carry-in and carry-out of the sign bit (MSB). It will go HIGH when the result of an arithmetic operation is a number requiring more bits than are available, causing the sign bit to be erroneous. This is the overflow (V) bit of the processor status word. The F_3 pin is the MSB of the ALU output. It is the sign of the result in two's complement notation, and should be used as the Negative (N) bit of the processor status word.
The carry-out from the most significant 2901 (C_{n+4} pin) is the carry-out from the array, and is used as the carry (C) bit of the processor status word.

Carry interconnections between devices may use either ripple carry or carry lookahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next more significant device. Carry lookahead uses the 2902A lookahead carry generator.

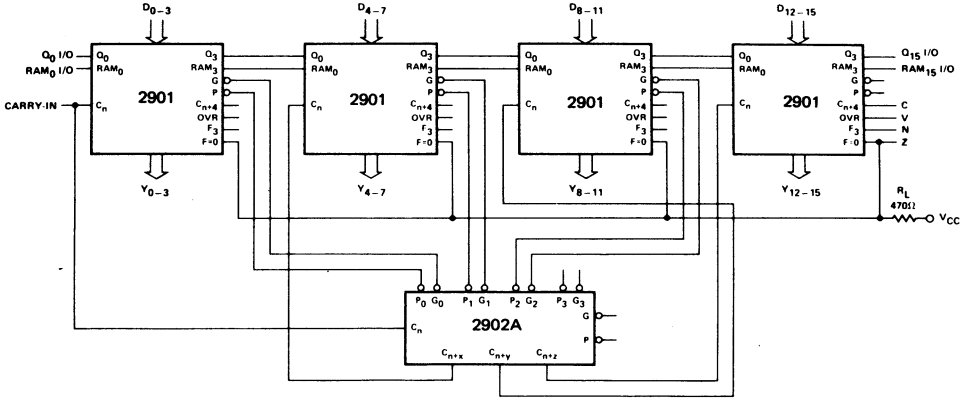


Figure 13. Four 2901s in a 16-Bit CPU Using the 2902A for Carry Lookahead.

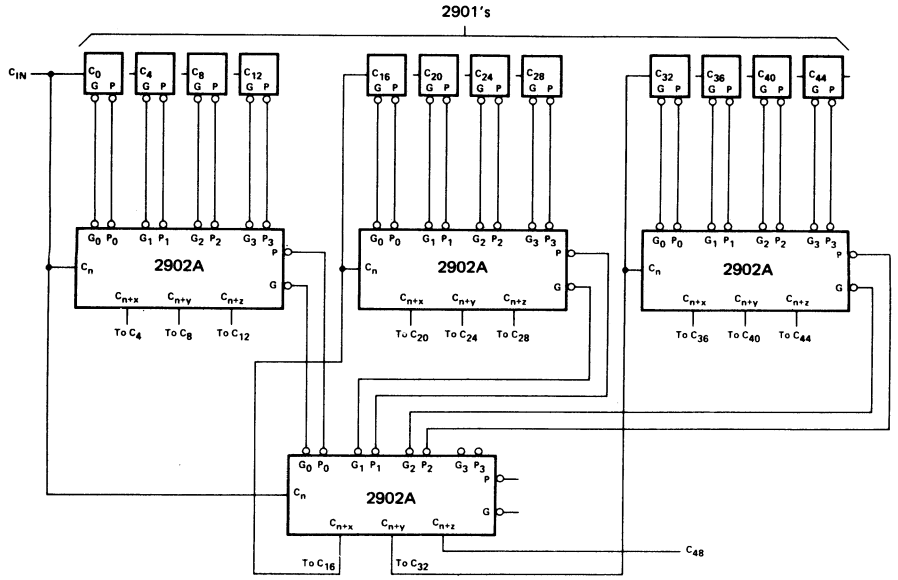


Figure 14. Carry Lookahead Scheme for 48-Bit CPU Using 12x2901s. The Carry-Out Flat (C_{48}) should be taken from the Lower 2902A Rather than the Right-Most 2901 for Higher Speed.

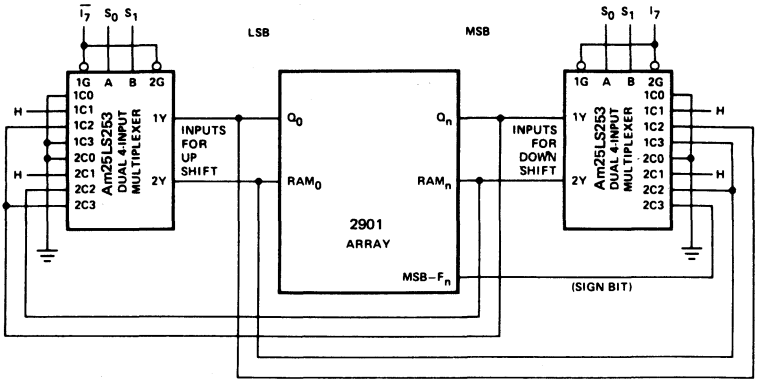


Figure 15. Three-State Multiplexers Used on Shift I/O Lines.

SHIFT I/O LINES AT THE END OF THE ARRAY

The Q-register and RAM left/right shift data transfers occur between devices over bidirectional lines. At the ends of the array, three-state multiplexers are used to select what the new inputs to the registers should be during shifting. The 2904 includes these multiplexers in a single LSI chip. Figure 19 shows two Am25LS253 dual four-input multiplexers connected to provide four shift modes. Instruction bit I_7 (from the 2901) is used to select whether the left-shift multiplexer or the right-shift multiplexer is active. The four shift modes in this example are:

Zero A LOW is shifted into the MSB of the RAM on a down shift. If the Q-register is also shifted, then a LOW is deposited in the Q-register MSB. If the RAM or both registers are shifted up, LOWs are placed in the LSBs.

One Same as zero, but a HIGH level is deposited in the LSB or MSB.

Rotate A single precision rotate. The RAM MSB shifts into the LSB on a right shift and the LSB shifts into the MSB on a left shift. The Q-register, if shifted, will rotate in the same manner.

Arithmetic A double-length Arithmetic Shift if Q is also shifted. On an up shift a zero is loaded into the Q-register LSB and the Q-register MSB is loaded into the RAM LSB. On a down shift, the RAM LSB is loaded into the Q-register MSB and the ALU output MSB (F_n, the sign bit) is loaded into the RAM MSB. (This same bit will also be in the next less significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}		One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1		One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

Figure 16 illustrates the interconnections for a hardware multiplication using the 2901. The system shown uses two devices for 8 x 8 multiplication, but the expansion to more bits is simple – the significant connections are at the LSB and MSB only.

The basic technique used is the "add and shift" algorithm. One clock cycle is required for each bit of the multiplier. On each cycle, the LSB of the multiplier is examined; if it is a "1", then the multiplicand is added to the partial product to generate a new partial product. The partial product is then shifted one place toward the LSB, and the multiplier is also shifted one place toward the LSB. The old LSB of the multiplier is discarded. The cycle is then repeated on the new LSB of the multiplier available at Q_0.

The multiplier is in the 2901 Q-register. The multiplicand is in one of the registers in the register stack, R_a. The product will be developed in another of the registers in the stack, R_b.

The A address inputs are used to address the multiplicand in R_a, and the B address inputs are used to address the partial product in R_b. On each cycle, R_a is conditionally added to R_b, depending on the *LSB of Q as read from the* Q_0 output, and both Q and the ALU output are shifted down one place. The instruction lines to the 2901 on every cycle will be:

I_{876} = 4 (shift register stack input and Q register left)
I_{543} = 0 (Add)
I_{210} = 1 or 3 (select A, B or 0, B as ALU sources)

Figure 16 shows the connections for multiplication. The circled numbers refer to the paragraphs below.

1. The adjacent pins of the Q-register and RAM shifters are connected together so that the Q-registers of both (or all) 2901s shift left or right as a unit. Similarly, the entire eight-bit (or more) ALU output can be shifted as a unit prior to storage in the register stack.

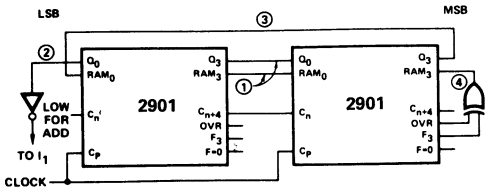


Figure 16. Interconnection for Dedicated Multiplication (8 by 8 bit) (Corresponding A, B, and I Connected together).

2. The shift output at the LSB of the Q-register determines whether the ALU source operands will be A and B (add multiplicand to partial product) or 0 and B (add nothing to partial product. Instruction bit I_1 can select between A, B or 0, B as the source operands; it can be driven directly from the complement of the LSB of the multiplier.

3. As the new partial product appears at the input to the register stack, it is shifted left by the RAM shifter. The new LSB of the partial product, which is complete and will not be affected by future operations, is available on the RAM_0 pin. This signal is returned to the MSB of the Q-register. On each cycle then, the just-completed LSB of the product is deposited in the MSB of the Q-register; the Q-register fills with the least significant half of the product.

4. As the ALU output is shifted down on each cycle, the sign bit of the new partial product should be inserted in the RAM MSB shift input. The F_3 flag will be the correct sign of the partial product unless overflow has occurred. If overflow occurs during an addition or subtraction, the OVR flag will go HIGH and F_3 is not the sign of the result. The sign of the result must then be the complement of F_3. The correct sign bit to shift into the MSB of the partial product is therefore $F3 \oplus OVR$; that is, F_3 if overflow has not occurred and $\overline{F_3}$ if overflow has occurred. On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction rather than addition should be performed, because the sign bit of the multiplier carries negative rather than positive arithmetic weight.

$$Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0$$

This scheme will produce a correct two's complement product for all multiplicands and multipliers in two's complement notation.

Figure 17is a table showing the input states of the 2901 for each step of a signed, two's complement multiplication. The 2904 LSI chip conveniently implements the required shift linkages and the EX-OR function for this algorithm.

Initial Register States

R

0	Multiplier
1	Multiplicand
2	X
3	X

2901 Microcode

Program 2's Comp. Multiply

Final Register States

R

0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
O∨A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
O∧B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = Q_0 LO$	0	–	RAM_0	–	$F_3 \forall OVR$		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = Q_0 LO$	1	–	RAM_0	–	$F_3 \forall OVR$		
O∨Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 17.

HARDWARE DIVISION

Division, unlike multiplication, is much more difficult to realize. One of these difficulties can be easily understood by visualizing a 2n-bit Dividend (X) and an n-bit Divisor (Y). The Quotient (Q) can range from 1 bit (when X < Y) to 2 n bits (when Y = 1), discarding the attempt to divide by 0. In most of the divide functions, the Remainder (R) is as important to find as is the Quotient – there is no equivalent to it in multiplication. Division becomes even more complicated when negative numbers are represented in the 2's complement notation. In the "everyday" decimal system, using Sign-and-Magnitude notation, dealing with negative numbers is relatively easy: The sign of the quotient is determined first and then a normal division is performed. Note that in this "normal" division we first "guess" the first digit of the quotient by comparing the most significant part of the dividend to the divisor. Then verify our guess by a multiplication (no "direct" division method is known), and continue to do so for all of the other digits, shifting the divisor to the right one place at a time.

The most straightforward division scheme (for unsigned numbers) is Subsequent Subtraction. The algorithm is as follows: Subtract divisor from dividend and increment a counter (initially reset to zero). Continue to do so as long as the Remainder is positive. When the Remainder becomes negative cancel the last step; i.e., add back divisor and decrement counter. The counter will contain the Quotient and the Remainder will be correct. The main drawback of this scheme is, of course, the great number of arithmetic operations needed. Again, when dealing with signed numbers, the subtraction should be substituted by addition and vice versa.

A more rapid division can be realized by calculating the Quotient digits instead of counting them. In this algorithm, the divisor is first subtracted from the most significant part of the dividend. If the remainder is positive, the quotient digit is "1," otherwise the subtraction is cancelled (by adding the divisor to the remainder) and the quotient digit will be "0." Now shift the remainder one place to the right (much like you do in a "paper and pencil" division) and repeat until all the quotient digits have been calculated. This algorithm is called "Restoring Division." When signed numbers are involved, inversion of the operations and the quotient digits will be necessary and correction should be performed in some cases. Some time is wasted in the Restoring Division because for every "0" digit in the quotient, two arithmetic operations are needed. This can be saved in the "Non-Restoring Division."

The basis of Non-Restoring Division is the same as in Restoring Division. Consider first unsigned (positive) numbers only. At the beginning, the divisor is subtracted from the most significant part of the dividend. If the result (first remainder) is positive (or zero), the first quotient digit is "1." Otherwise, the quotient digit is "0," but do not restore. Shift divisor one place to the right (or remainder to the left) and add if last quotient digit was "0;" otherwise subtract. Determine quotient digit as before and continue until all quotient digits have been computed. The remainder will be correct if it is non-negative, otherwise correction is needed by a restoring operation (on the remainder only). Extreme care should be taken of the number of bits and the value of the divisor. Assuming the divisor has n bits and the dividend as 2n bits, the above process develops n + 1 bits of the quotient. This will not be sufficient if the divisor is a small number and more digits are needed in the quotient. This condition can be easily detected as the most significant half of the dividend will be greater than the divisor in this case and division can then be terminated after setting the overflow flag. The flow chart for unsigned nonrestoring division is shown in Figure 21.

The unsigned division scheme can be applied to signed *positive* numbers without any change. When negative numbers are encountered, however, changes in the algorithm are necessary. The straightforward method of signed division seems to be "division in the first quadrant." In that scheme, negative numbers are 2's complemented to obtain positive numbers, remembering the changes done. If overflow occurs when the dividend is complemented (i.e., dividend is $-2^{2n}-1$, the least negative number), the overflow flag can be set and an exit from the routine taken. This is due to the fact that $(-2^{2n}-1)$ divided by any number of n-bits cannot be represented in n bits. On the other hand, if overflow occurs when the divisor is complemented, a more complex action is needed. In this case, the dividend and the divisor should be shifted right by one place and the shifted out bit should be stored in a flag, say "Z." At the same time, a flag, "W" should also be set to indicate that division by -2^n is being attempted. These actions need to be taken since the quotient might be representable in n bits. (Here instead of dividend = divisor quotient or remainder, we have [dividend /2] = [divisor /2] * quotient + [rem /2]. The remainder obtained should be shifted left and the bit Z be added to give the correct remainder.) The division is performed on possible numbers, and finally 2's complementing is done whenever necessary. Figure 18 is the flowchart for this algorithm.

Figure 19 is the Interconnection Diagram for Division Algorithm. It is assumed that the most significant half Dividend is in Register R_X (it will be lost during the division and replaced by the Remainder), the least significant half in the Q Register and that the Divisor is in Register R_Y. The Quotient will be generated in the Q register.

After checking the signs of the Dividend and Divisor, setting the flags and negating (using 23 or 24 octal as I_5 through I_0 ALU control bits) when necessary the overflow condition should be checked. If R_X is greater than , then R_Y, overflow occurs, hence the division can be terminated by setting the overflow flag.

The first step in the Division routine is a subtract, then shift the R_X and Q registers up. I_{876} will be 6 in octal while I_{210} = 1 in octal and $I_5 = I_4$ = LOW. Pulling the CL bit in the microcode to HIGH, both I_3 and C_n will be high and the ALU is performing a 2's complement subtract. The sign of the Remainder will be latched in the Status Register and the complement of it will be stored in the LSB of the Q register during the shift up operation, which also discards the sign bit of the Remainder.

Now repeating the same operation for all of the other bits of the Remainder with the CL bit in the microcode LOW will leave the control of I_3 to the (complemented) previous sign bit. If it was "0" (R < 0), I_3 and C_n will be HIGH and the ALU will subtract; if it was 1 (R > 0), I_3 and C_n will be LOW and the ALU will ADD, as required. In each up shift, the complement of the present sign bit will be placed at the right of the Quotient, again, as required.

At the end of the division, the sign bit of the Remainder should be examined and if it is HIGH, the Divisor should be added to it. This can be easily implemented (not depicted on Figure 19) by performing an unconditional ADD (with C_n LOW), letting I_2 LOW, I_0 HIGH and controlling I_1 by the complement of the sign of the Remainder, thus adding to the RX either RY (if R_S = 1) or zero (if R_S = 0). If the dividend and divisor were shifted right because the divisor was equal to -2^n, the true remainder is obtained by shifting the remainder left and adding the flag "Z." The above method generates n + 1 bits of the quotient ($q_n \ldots q_0$) of which q_n = 0, since most significant half of dividend is less than the divisor. The overflow flag should be set if $q_{n-1} = 1$ since $q_{n-1} \ldots q_0$ is an unsigned positive number.

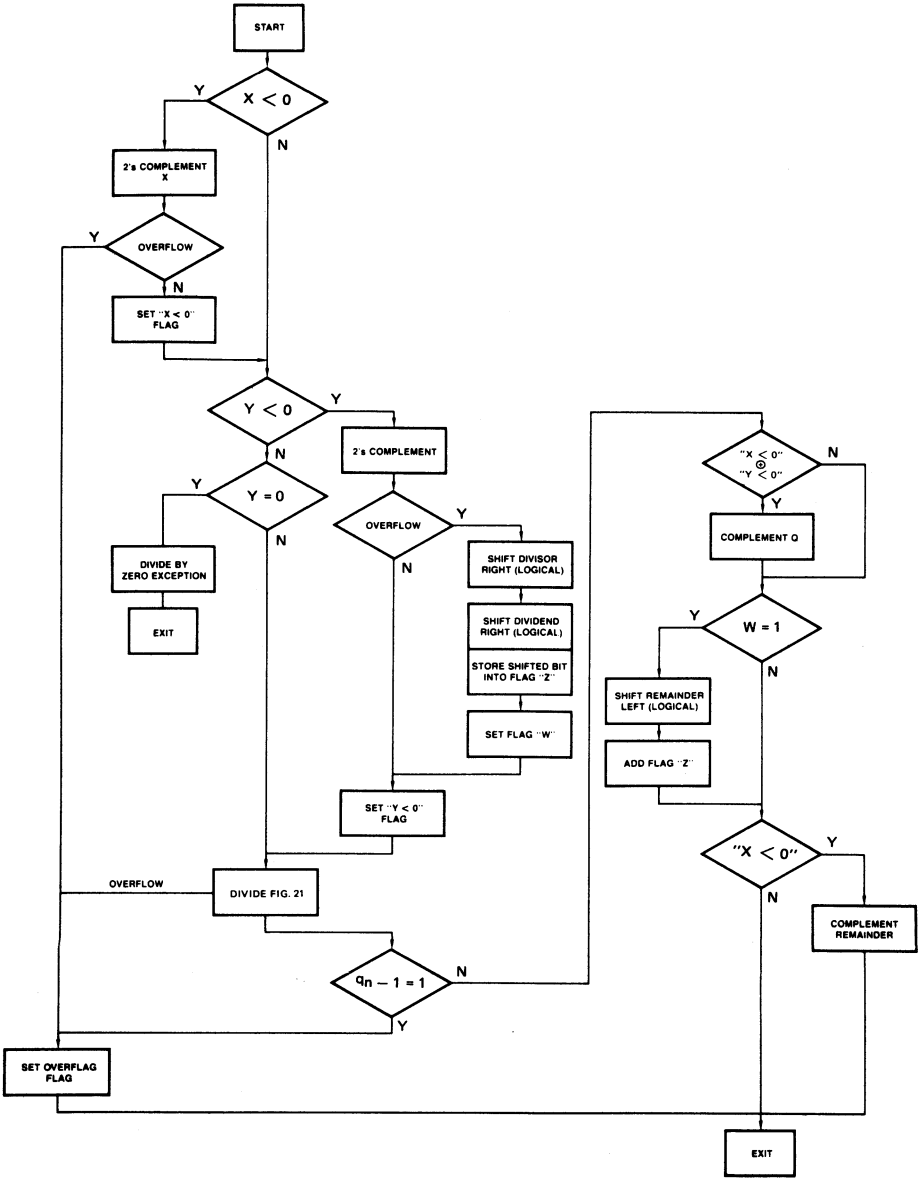


Figure 18. Flowchart for Division with Signed Numbers (Quotient = $q_n, q_{n-1} \ldots q_0$ where q_n=0)

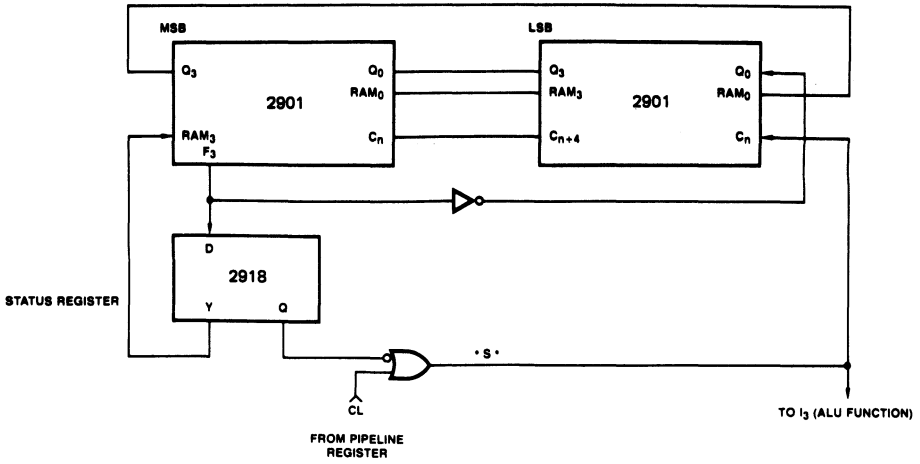


Figure 19. Interconnections for Dedicated Division

Initial Register Status

R

0	MSH Dividend
1	Divisor
Q	LSH Dividend

2901 Microcode

Program: 2's Complement Division

Final Register Status

R

0	Remainder
1	Divisor
Q	Quotient

S, F	D	Description	CL	Repeat	Pin Status (Octal)										Jump
					A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	to If
(B−A) *2	B	First Subtract & Shift	1	–	1	0	6	1	1	1	F_3	X	0	X	
(B±A) *2	B	Loop Subtract/Add & Shift	0	N	1	0	6	1/0	1	1/0	F_3	X	0	X	
B+0	B	Correct Remainder	X	–	1	0	3	0	1/3	0	X	X	X	X	

k = Number of leading zeros of the Divisor

N = Number of bits in the Divisor

Figure 20. 2901 Microcode for Dedicated Division

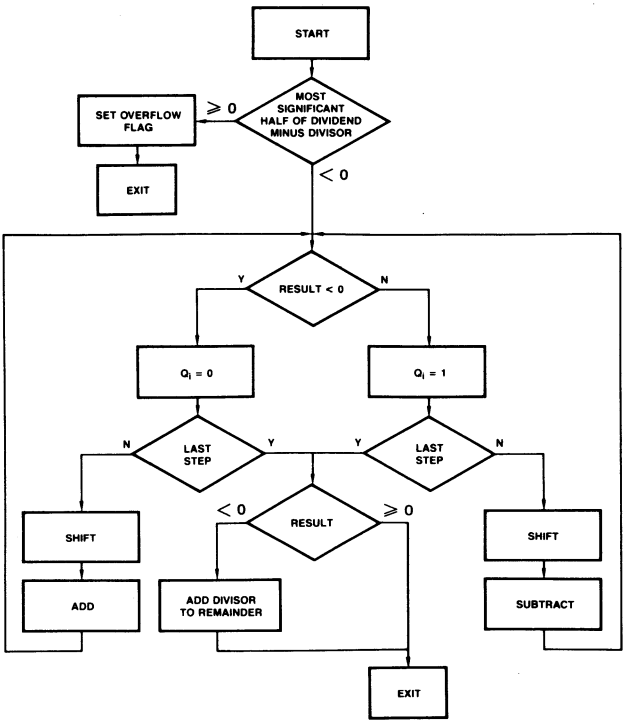


Figure 21. Flowchart for Nonrestoring Division (Unsigned Numbers)

Finally, the Quotient and/or Remainder should be 2's complemented again according to the flags. Complementation of the remainder cannot generate an overflow – because the maximum remainder after divide (Figure 21) is 0011 . . . 1 and the remainder correction when W = 1 can make the remainder at most 0111 . . . 1.

EXAMPLES OF SOME OTHER OPERATIONS

1. Byte Swapping

Occasionally the two halves of a 16-bit word must be swapped. D_{0-7} is interchanged with D_{8-15}. The quickest way to perform this operation is to rotate the word in RAM, shifting two bits at a time. Only four shift cycles are required. The same register is selected on both the A and B ports; the two are added together with carry-in connected to carry-out, producing a right shift of one place; then the ALU is shifted right one more place prior to storage.

Byte Swap of R_0

A = B = 0 I = 701 $RAM_0 = RAM_{15}$ $C_{IN} = C_{OUT}$

Repeat 4 times.

2. Instruction Fetch Cycle

Execution of a macroinstruction generally begins with an instruction fetch cycle. The current contents of the PC (in one of the registers) is the address of the macroinstruction to be fetched, and must be read out to the memory address register. Then the PC is incremented to point to the next macroinstruction. The macroinstruction obtained from memory is then loaded into the microprogram sequencer to cause a jump to the microcode for executing the instruction.

The PC can be read out and incremented in one cycle by using the 2901 destination code 2, and addressing the PC with both the A and B addresses. The current value of PC will appear on the Y outputs, and PC+1 will be returned to the register. If the PC is in register 15, then:

A = B = 15, I = 203, Carry-in = 1

The PC will be on the Y outputs via the RAM A-port. On the clock LOW-to-HIGH transition, the program counter is incremented and the value on the Y outputs is loaded into the memory address register. During the following cycle, the memory is read and, on the next clock LOW-to-HIGH transition the instruction from the memory is dropped into the instruction register. The fetch operation requires only two microcycles.

ORDERING INFORMATION

TS2901C | M | J | B/B

- TS2901C: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

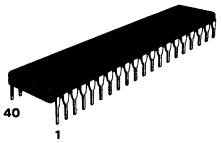
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2901C	●		●	●			●	●		
		●		●	●	●	●		●	●

Examples : TS2901CCP, TS2901CCP-D, TS2901CCJ, TS2901CCJ-D
TS2901CMJ, TS2901CMJG/B, TS2901CMJB/B,...

Oper. temp. : **C** : 0°C to + 70°C, **M** : – 55°C to + 125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

CASE CB-182

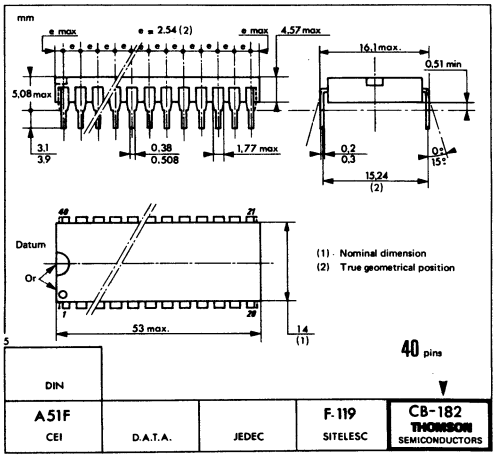


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTEURS

TS2902 A

HIGH-SPEED LOOK-AHEAD CARRY GENERATOR

The TS2902A is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The TS2902A is generally used with the 2910 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

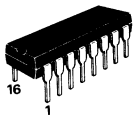
The logic equations provided at the outputs are :

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

- Provides look-ahead carries accross a group of four 2901 or 2903 microprocessor ALU's.
- Capability of multi-level look-ahead for high-speed arithmetic opeation over large word lengths.
- Typical carry propagation delay of 4.5 ns.

HIGH-SPEED LOOK-AHEAD CARRY GENERATOR

CASE CB-79



P SUFFIX
PLASTIC PACKAGE

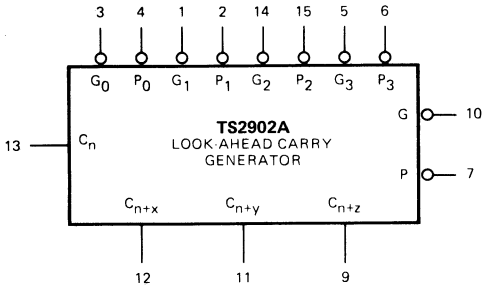
ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER

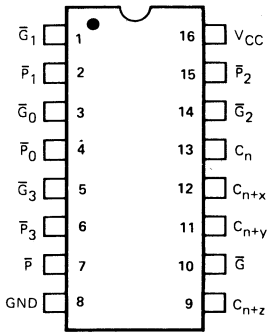
Hi-Rel versions available - See chapter 4

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



Ref. 01250 - R1

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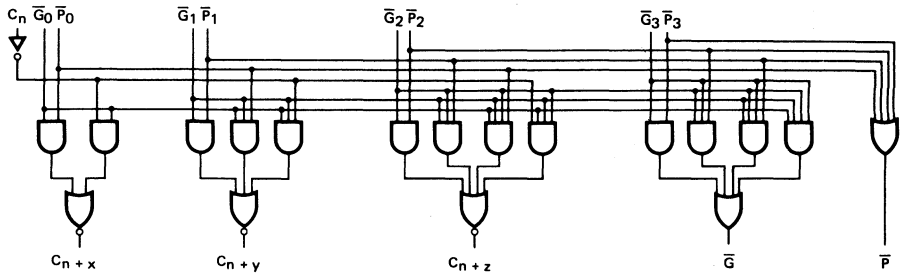
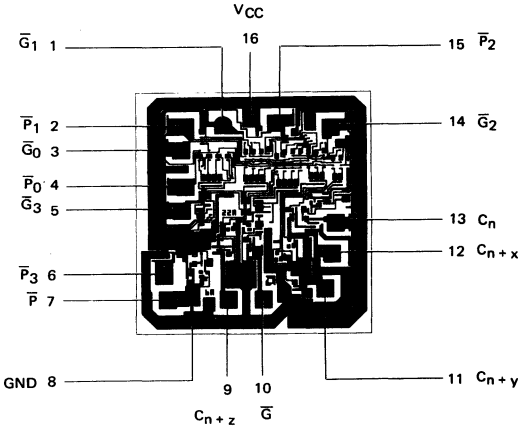
THOMSON COMPONENTS

LOGIC DIAGRAM

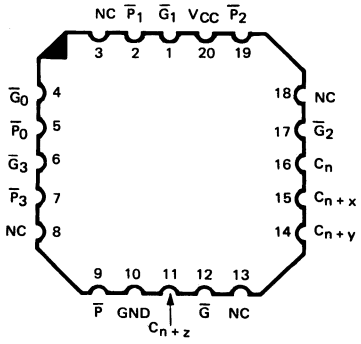


Metallization and Pad Layout



Die size : 1.778 x 1.575 mm

CHIP CARRIER



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

C SUFFIX	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
M SUFFIX	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	C_n			−2	mA
			$\overline{P}_3$			−4	
			$\overline{P}_2$			−6	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			−8	
			$\overline{G}_0, \overline{G}_2$			−14	
			$\overline{G}_1$			−16	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n			50	µA
			$\overline{P}_3$			100	
			$\overline{P}_2$			150	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			200	
			$\overline{G}_0, \overline{G}_2$			350	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 3)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Outputs LOW	MIL		69	99	mA
			COM'L		69	109	
		V_{CC} = MAX., All Ouputs HIGH	MIL		35		mA
			COM'L		35		

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}		6.5	10	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}		4.5	7	ns	
t_{PHL}			4.5	7		
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$		5	7.5	ns	
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i$ to $\overline{P}$		4.5	6.5	ns	
t_{PHL}			6.5	10		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Max.	T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}		13		15	ns	C_L = 50pF, R_L = 280Ω
t_{PHL}			14		16.5	ns	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}		8		9.5	ns	
t_{PHL}			9		11.5	ns	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$		12		16.5	ns	
t_{PHL}			12		13.5	ns	
t_{PLH}	$\overline{P}_i$ to $\overline{P}$		9.5		11.5	ns	
t_{PHL}			11		12	ns	

DEFINITION OF FUNCTIONAL TERMS

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth 2901 microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2 and n+3 microprocessor ALU slices.

G_i, P_i Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

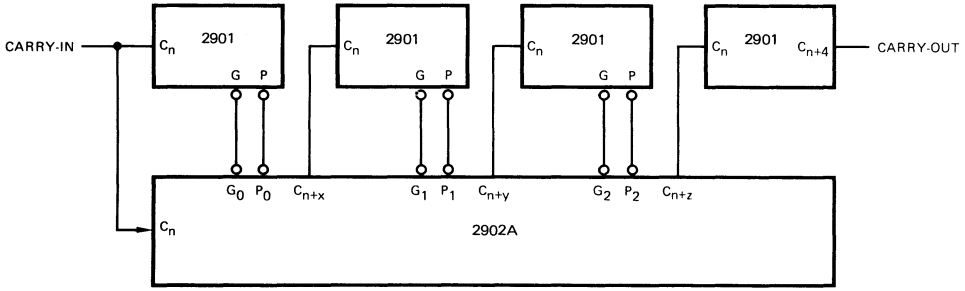
G, P Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

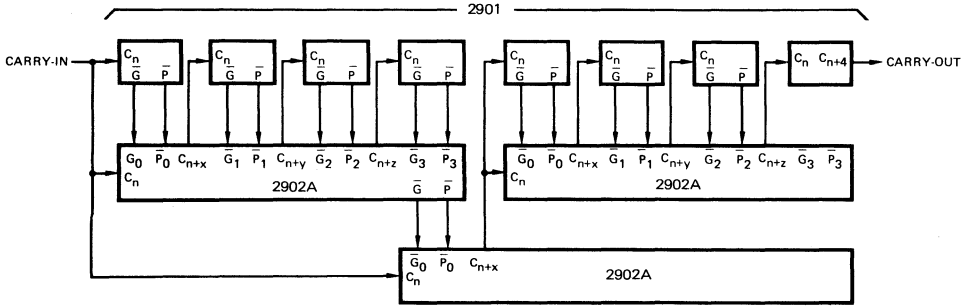
Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

APPLICATIONS



16-BIT CARRY LOOK-AHEAD CONNECTION.



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

ORDERING INFORMATION

TS2902A | M | J | B/B

- TS2902A: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

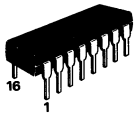
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2902A	●		●	●			●	●		
		●		●	●	●	●		●	●

Examples :TS2902ACP, TS2902ACP-D, TS2902ACJ, TS2902ACJ-D
TS2902AMJ, TS2902AMJG/B, TS2902AMJB/B,...

Oper. temp. : **C** : 0°C to + 70°C, **M** : – 55°C to + 125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

CASE CB-79

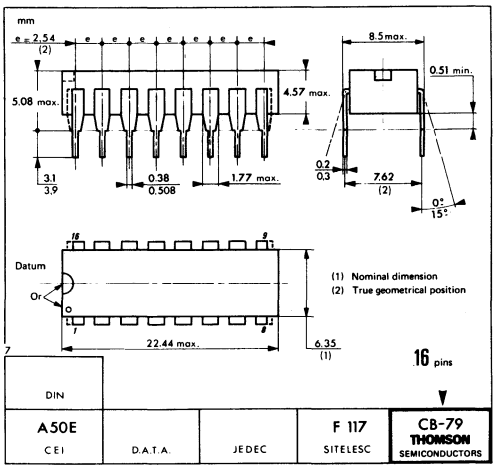


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTEURS

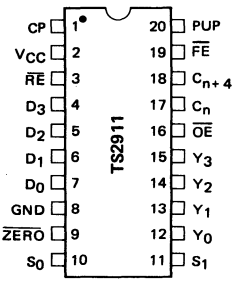
TS2909, A
TS 2911, A

MICROPROGRAM SEQUENCERS

The TS2909A is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two TS2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).
The TS2909 can select an address from any of four sources. They are : 1) a set of external direct inputs (D) ; 2) external data from the R inputs, stored in an internal register ; 3) a four-word deep push/pop stack ; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.
The TS2911 is an identical circuit to the TS2909, except the four OR inputs are removed and the D and R inputs are tied together. The TS2911 is in a 20-pin package. The TS2909A and 2911A are direct plug-in replacements for the TS2909 and 2911, but are about 25 % faster.

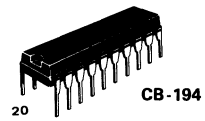
- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (TS2909 only)
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- TS2909 in 28-pin package
- TS2911 in 20-pin package
- New high-speed versions (TS2909A and 2911A) are plug-in replacements for original TS2909 and 2911.
- Critical path speeds will be improved by about 25 %.

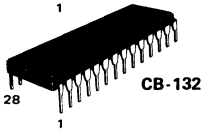
For applications information, see Chapter II of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.



MICROPROGRAM SEQUENCERS

CASES





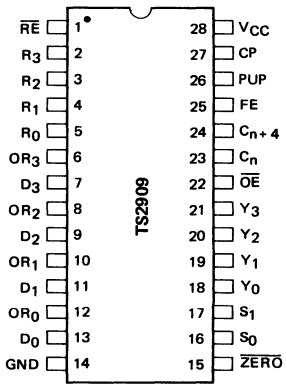
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

Hi-Rel versions available - See chapter 4

PIN ASSIGNMENT



Ref. 01255-R1

THOMSON SEMICONDUCTEURS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (1) 39.46.97.19 / Telex : 204780F

THOMSON COMPONENTS

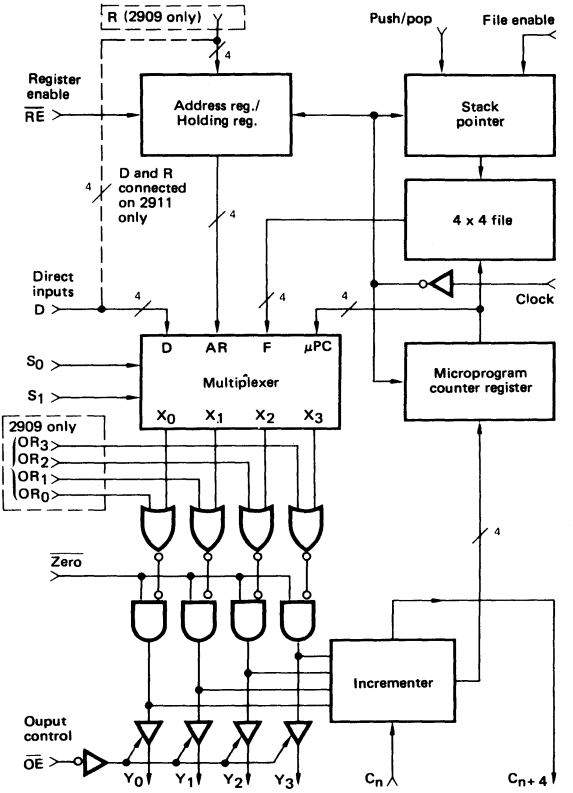
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

Operating Range	Part Number Suffix	Power Supply	Temperature Range
Commercial	C SUFFIX	5.0V ±5%	T_A = 0°C to +70°C
Military	M SUFFIX	5.0V ±10%	T_C = −55°C to +125°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Notes)
(For TS2909, TS2911, TS2909A, TS2911A)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA, 2909/11				0.4	Volts
			I_{OL} = 8.0mA, 2909/11				0.45	
			I_{OL} = 12mA, 2909/11 (Note 5)				0.5	
			I_{OL} = 16mA, 2909A/11A				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL, 2909/11				0.7	Volts
			All others				0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n				40	μA
			Push/Pop				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 6V, V_{OUT} = .5V	$Y_0 - Y_3$		−30		−100	mA
			C_{n+4}		−30		−85	
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)	COM'L and MIL	T_A = +25°C			130	mA
			COM'L Only	T_A = 0 to +70°C			130	
			MIL Only	T_C = −55 to +125°C			140	
				T_C = +125°C			110	
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.7 V	Y_{0-3}	V_{OUT} = 0.4 V			−20	μA
I_{OZH}				V_{OUT} = 2.7 V			20	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs high. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 12mA guarantee applies only to Y_0, Y_1, Y_2 and Y_3.
6. **For the 2911 and 2911A, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).**

TS2909 and TS2911 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II, and III below define the timing characteristics of the TS2909 and 2911 over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e. clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading. The data on this page applies to the following part numbers:

Operating Range	Part Numbers	Power Supply	Temperature Range
Com'l	2909CH, CJ 2911CH, CJ	5.0V ±5%	T_A = 0°C to +70°C
Mil	2909MJ 2911MJ	5.0V ±10%	T_C = −55°C to +125°C

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	35
Minimum Clock HIGH Time	30	35

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

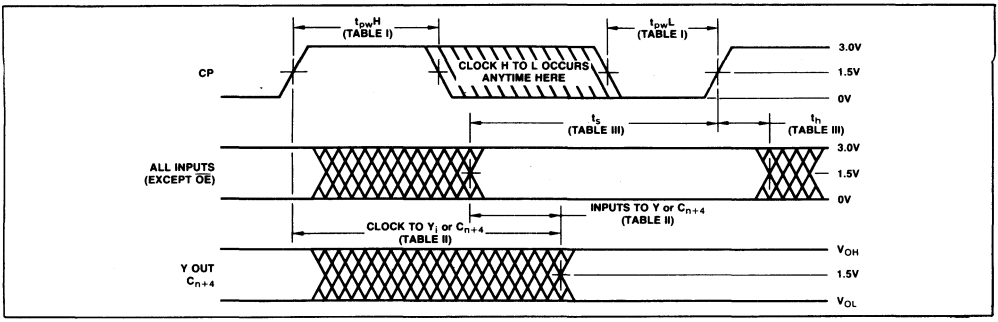
From Input	COMMERCIAL Y	COMMERCIAL C_{n+4}	MILITARY Y	MILITARY C_{n+4}
D_i	17	30	20	32
S_0, S_1	30	48	40	50
OR_i	17	30	20	32
C_n	–	14	–	16
$\overline{ZERO}$	30	48	40	50
$\overline{OE}$ LOW (enable)	25	–	25	–
$\overline{OE}$ HIGH (disable)*	25	–	25	–
Clock ↑ S_1S_0 = LH	43	55	50	62
Clock ↑ S_1S_0 = LL	43	55	50	62
Clock ↑ S_1S_0 = HL	80	95	90	102

*C_L = 5.0pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL Set-Up Time	COMMERCIAL Hold Time	MILITARY Set-Up Time	MILITARY Hold Time
$\overline{RE}$		22	5	22	5
R_i	2	10	5	12	5
PUSH/POP		26	6	30	7
$\overline{FE}$		26	5	30	5
C_n		28	5	30	5
D_i		30	0	35	3
OR_i		30	0	35	3
S_0, S_1		45	0	50	0
$\overline{ZERO}$		45	0	50	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On 2911, R_i and D_i are internally connected together and labeled D_i. Use R_i set-upsand hold times when D inputs are used to load register.



TS2909A and TS2911A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II and III below define the timing characteristics of the 2909A / 2911A over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading. The data on this page applies to the following part numbers:

Operating Range	Part Numbers	Power Supply	Temperature Range
Com'l	2909A CH, CJ 2909A CH, CJ	5.0V ±5%	T_A = 0°C to +70°C
Mil	2909A MJ, ME 2911A MJ, ME	5.0V ±10%	T_C = −55°C to +125°C

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

Time	COMMERCIAL	MILITARY
Minimum Clock LOW Time	20	20
Minimum Clock HIGH Time	20	20

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

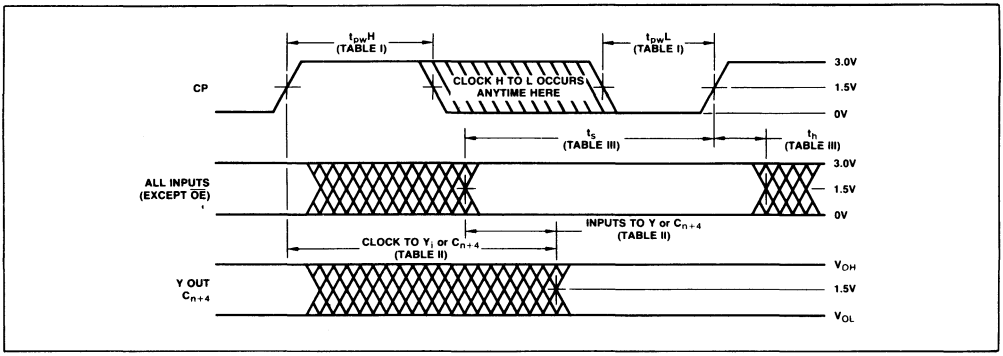
	COMMERCIAL		MILITARY	
From Input	Y	C_{n+4}	Y	C_{n+4}
D_i	17	22	20	25
S_0, S_1	29	34	29	34
OR_i	17	22	20	25
C_n	–	14	–	16
$\overline{ZERO}$	29	34	30	35
OE LOW (enable)	25	–	25	–
OE HIGH (disable)*	25	–	25	–
Clock ↑ S_1S_0 = LH	39	44	45	50
Clock ↑ S_1S_0 = LL	39	44	45	50
Clock ↑ S_1S_0 = HL	44	49	53	58

*C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

		COMMERCIAL		MILITARY	
From Input	Notes	Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		19	4	19	5
R_i	2	10	4	12	5
PUSH/POP		25	4	27	5
FE		25	4	27	5
C_n		18	4	18	5
D_i		25	0	25	0
OR_i		25	0	25	0
S_0, S_1		25	0	29	0
$\overline{ZERO}$		25	0	29	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On 2911A, R_i and D_i are internally connected and labeled D_i. Use R_i set-up and hold times when Dinputs are used to load register.



OPERATION OF THE 2909/2911

Figure 1 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 1 also shows the truth table for the output control and for the control of the push/pop stack. Figure 2 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the 2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Address/Holding Register	AR
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 1.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 –	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J –	Push μPC	Set-up Loop
N N+1	0 0 1 X –	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K –	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra –	Jump to Address in STK0; Push μPC	
N N+1	1 0 1 X –	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D –	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D –	Jump to Address on D	JMP D

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STKO is the location addressed by the stack pointer.

Figure 2. Output and Internal Next-Cycle Register States for TS2909/2911

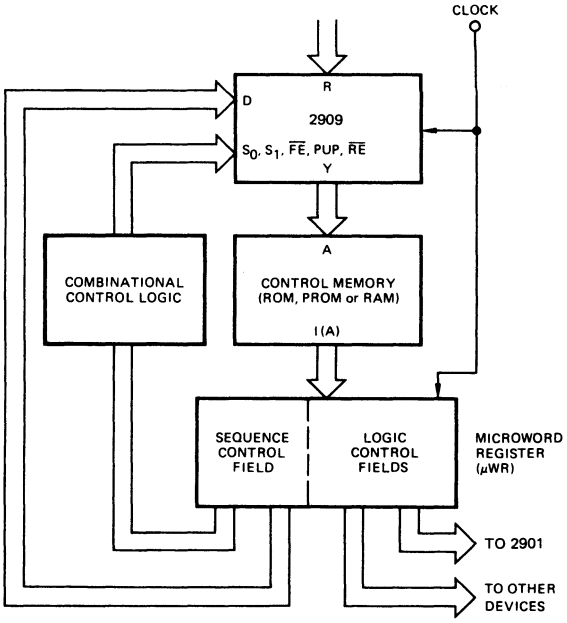


Figure 3. Microprogram Sequencer Control.

DEFINITION OF TERMS

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the 2909. They are :

Inputs to TS2909/2911

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs from the TS2909/2911

Y_i	Address outputs from 2909. (Address inputs to control memory)
C_{n+4}	Carry out from the incrementer

Internal Signals

μPC	Contents of the microprogram counter
AR	Contents of the address/holding register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External to the TS2909/2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

Figure 4 illustrates the execution of a subroutine using the 2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the 2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the comand "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the 2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 5 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J – 1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_6	J+3	–
T_7	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I(A)
T_4	A+1	–
T_5	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)		

Figure 4. Subroutine Execution. C_n = HIGH

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J – 1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_9	J+3	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A+1	–
T_5	A+2	JSR B
T_7	A+3	–
T_8	A+4	RTS
	–	–
	–	–
	–	–
	–	–
T_6	B	RTS
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)

Figure 5. Two Nested Subroutines. Routine B is Only One Instruction. C_n = HIGH

USING THE TS2909 AND TS2911

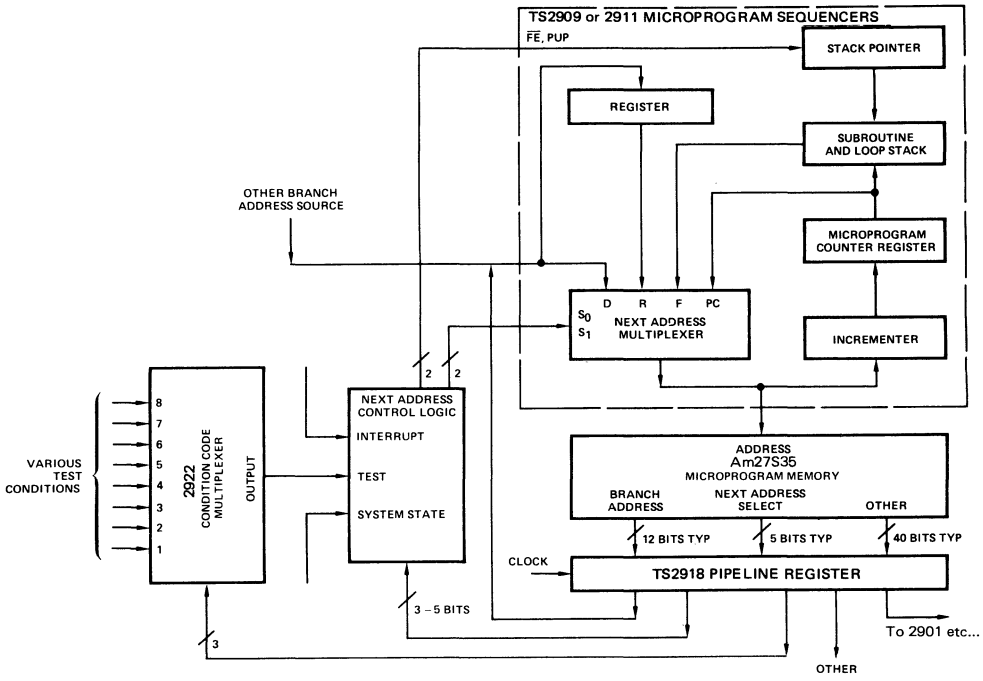
The TS2909 and 2911 are four-bit slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the TS2909 and 2911 apart from the 2910, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The 2909 or 2911 should be selected instead of the 2910 under the following conditions :

- Address less than 8 bits and not likely to be expanded
- Address longer than 12 bits
- More complex instruction set needed than is available on 2910

Architecture of the Control Unit

The recommended architecture using the 2909 or 2911 is shown in Figure 6. Note that the path from the pipeline register output through the next address logic, multiplexer, and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return-from-subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the 2909 or 2911. The block labeled "next address logic" may consist of simple gates, a PROM or a PLA, but it should be all combinational.

Figure 6. Recommanded Computer Control Unit Architecture Using the TS2911 or 2909



Expansion of the TS2909 or 2911

Figure 7 shows the interconnection of three 2911's to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the 2911 Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a micro-address register is placed at the 2911 output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a set-up time prior to the clock.

Selecting Between the TS2909 and 2911

The difference between the 2909 and the 2911 involves two signals: the data inputs to the holding register and the "OR" inputs. In the 2909, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the 2911, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 8. Using the 2909, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the 2911, it is more common to connect the 2911's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 8 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

Figure 7. Twelve Bit Sequencer.

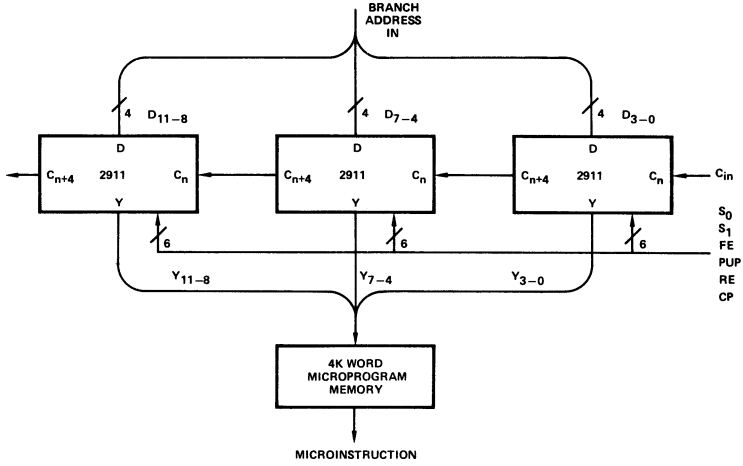
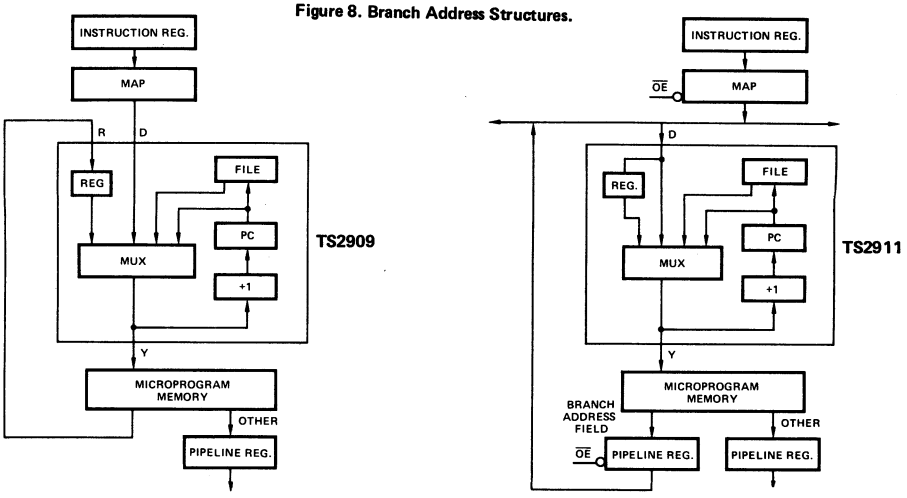


Figure 8. Branch Address Structures.



The second difference between the 2909 and 2911 is that the 2909 has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply tying several test conditions into the OR lines. See Figure 9. Typically, a branch is taken to an address with zeroes in the least significant bits. These bits are replaced with 1's or 0's by test conditions applied to the OR lines. In Figure 9, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110, or 1111.

How to Perform Some Common Functions with the TS2909 or 2911

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	1	0	0	1	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	1	1	1	1	X

Feed data on D inputs straight through to memory address lines. Increment address and place in PC.

3. JUMP-TO-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	1	1	1	0	1

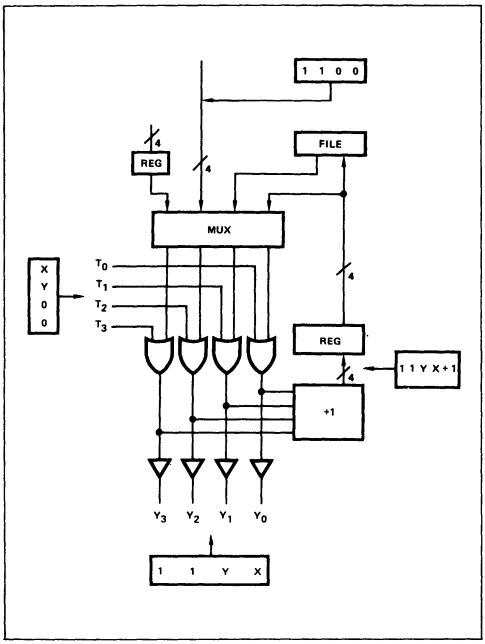
Sub-routine address fed from D inputs to memory address. Current PC is pushed onto stack, where it is saved for the return.

4. RETURN-FROM-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	1	1	0	0	0

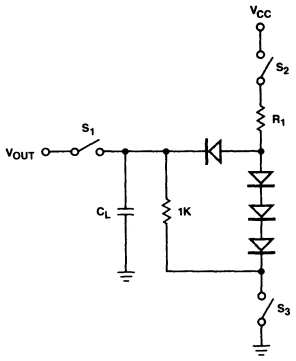
The address at the top of the stack is applied to the microprogram memory, and is incremented for PC on the next cycle. The stack is popped to remove the return address.

Figure 9. Use of OR Inputs to Obtain 4 - Way Branch.



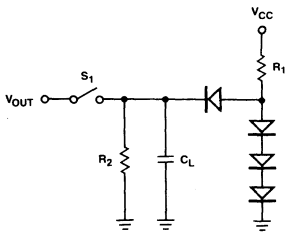
TEST OUTPUT LOAD CONFIGURATIONS FOR TS2909/2911 AND TS2909A/2911A

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC test except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS

Pin # (DIP)	Pin Label	Test Circuit	2909		2909A	
			R_1	R_2	R_1	R_2
18-21	Y_{0-3}	A	300	1K	220	1K
24	C_{n+4}	B	470	2.4K	220	2.4K

TEST OUTPUT LOADS

Pin # (DIP)	Pin Label	Test Circuit	2911		2911A	
			R_1	R_2	R_1	R_2
12-15	Y_{0-3}	A	300	1K	220	1K
18	C_{n+4}	B	470	2.4K	220	2.4K

ARCHITECTURE OF THE TS2909/2911

The TS2909/2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 10.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the 2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The TS2909/2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y+1→μPC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y→μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage – the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The TS2909/2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

ORDERING INFORMATION

TS2909A | M | J | B/B

- TS2909A: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

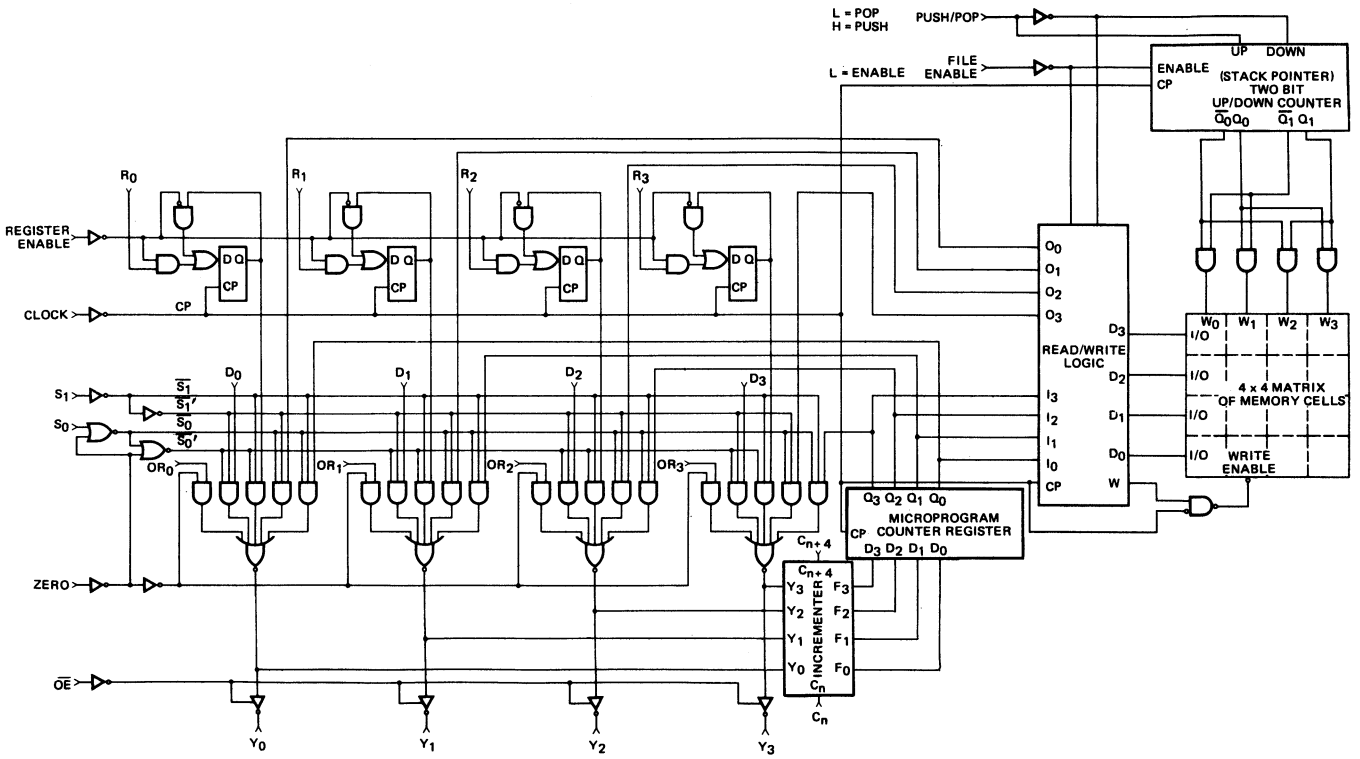
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2909A	●		●	●			●	●		
		●		●	●	●	●		●	●
TS2911A	●		●	●			●	●		
		●		●	●	●	●		●	●

Examples : TS2909ACP, TS2909ACP-D, TS2909ACJ, TS2909ACJ-D
TS2909AMJ, TS2909AMJG/B, TS2909AMJB/B,...

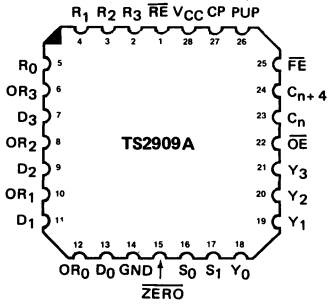
Oper. temp. : C : 0°C to 70°C, **M :** –55°C to +125°C.
Package : P : Plastic DIL, **J :** Cerdip DIL, **C :** Ceramic DIL, **E :** Ceramic LCC.
Screening classes : Std (no end-suffix), **–D :** NFC 96883 level D.
G/B : NFC 96883 level G, **B/B :** MIL-STD-883 level B and NFC 96883 level B.

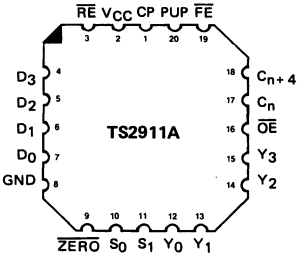
Figure 10. Microprogram Sequencer Block Diagram.



Note : R_i and D_i connected together on TS2911 and OR_i removed.

LEADLESS CHIP CARRIERS

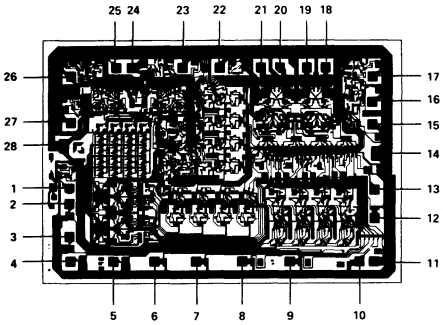




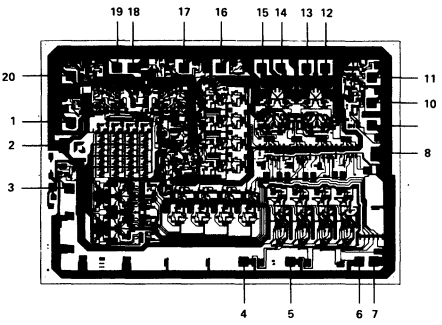
Metallization and Pad Layouts

TS2909

Die size : 4.200 x 2.900 mm



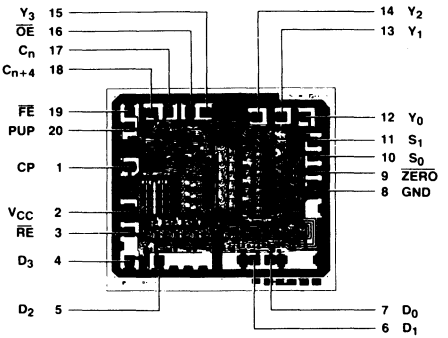
TS2911



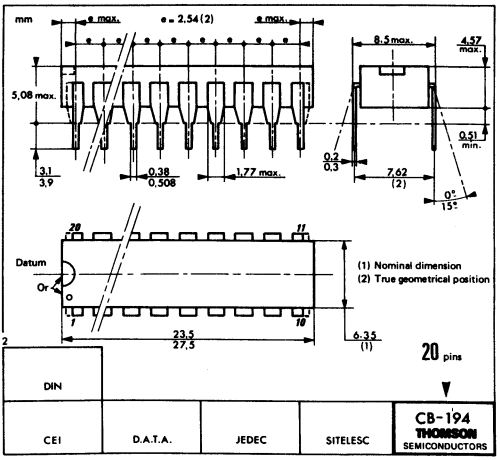
Pin numbers correspond to DIP pin-out.

TS2911A

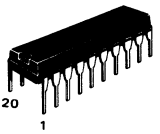
Die size : 2.490 x 2.210 mm



CASES



CB-194

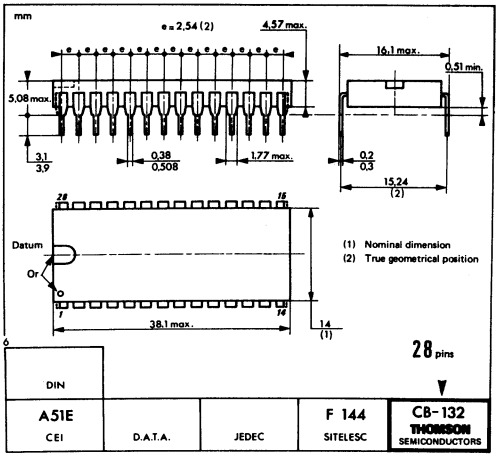


P SUFFIX
PLASTIC PACKAGE

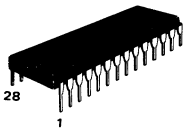
ALSO AVAILABLE

E SUFFIX
CHIP CARRIER

J SUFFIX
CERDIP PACKAGE



CB-132



P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

E SUFFIX
CHIP CARRIER

J SUFFIX
CERDIP PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTEURS

TS2910

MICROPROGRAM CONTROLLER

The TS2910 Microprogram controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability ; there are five levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

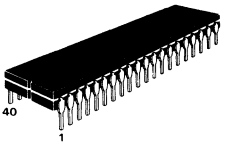
During each microinstruction, the Microprogram controller provides a 12-bit address from one of four sources : 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address ; 2) an external (direct) input (D) ; 3) a register/counter (R) retaining data loaded during a previous microinstruction ; or 4) a five-deep last-in, first-out stack (F).

- Twelve Bit Wide : address up to 4096 words of microcode with one chip. All internal elements are a full 12 bit wide.
- Internal Loop Counter : pre-settable 12-bit down-counter for repeating instructions and counting loop iterations.
- Four Address Sources : microprogram address may be selected from microprogram counter, branch address bus, 5-level push/pop stack, or internal holding register.
- Sixteen Powerful Microinstructions
  Executes 16 sequence control instructions, most of which are conditional on external condition input, state of internal loop counter, or both.
- Output Enable Controls for Three Branch Address Sources Built-in decoder function to enable external devices onto branch address bus. Eliminates external decoder.
- All Registers Positive Edge-triggered : simplifies timing problems. Eliminates long set-up times.
- Fast Control from Condition Input : delay from condition code input to address output only 21 ns typical.

For applications information, see Chapter II of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

MICROPROGRAM CONTROLLER

CASE CB-182



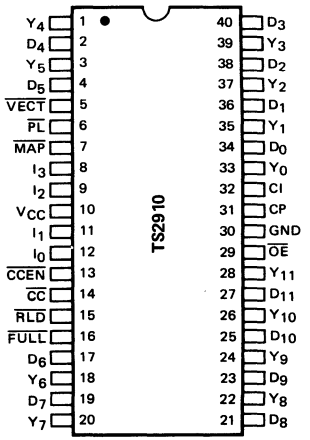
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX	**E SUFFIX**
CERDIP PACKAGE	CHIP CARRIER

Hi-Rel versions available - See chapter 4

PIN ASSIGNMENT



Ref. 01260-R1

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THOMSON COMPONENTS

BLOCK DIAGRAM

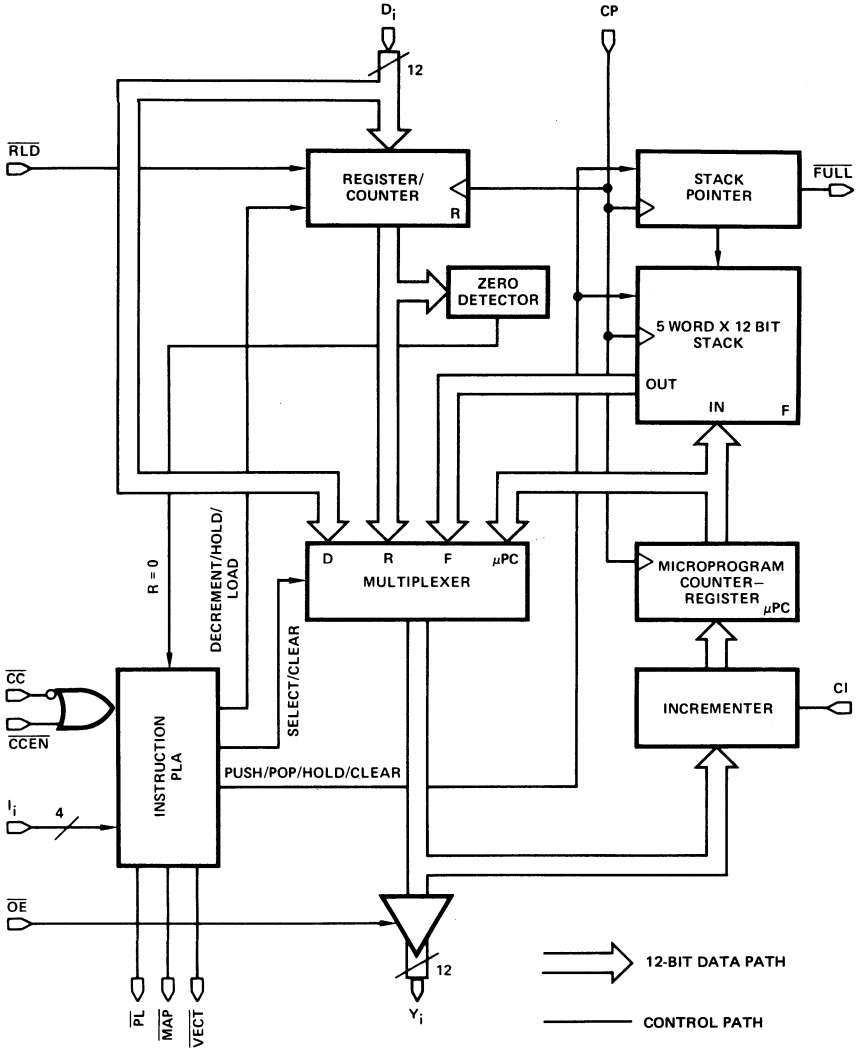


Figure 1

ARCHITECTURE OF THE TS2910

The TS2910 is a bipolar microprogram controller intended for use in high-speed microprocessor applications. It allows addressing of up to 4K words of microprogram. A block diagram is shown in Figure 1.

The controller contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. When its load control, $\overline{RLD}$, is LOW, new data is loaded on a positive clock transition. A few instructions include load; in most systems, these instructions will be sufficient, simplifying the microcode. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

The TS2910 contains a microprogram counter (μPC) that is composed of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). Sequential microinstructions are thus executed. When the carry-in is LOW, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). The same microinstruction is thus executed any number of times.

The third source for the multiplexer is the direct (D) input. This source is used for branching.

The fourth source available at the multiplexer input is a 5-word by 12-bit stack (file). The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a pop.

The stack pointer operates as an up/down counter. During microinstructions 1, 4, and 5, the PUSH operation may occur. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (Instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one. The depth can grow to five. After a depth of five is reached, $\overline{FULL}$ goes LOW. Any further PUSHes onto a full stack overwrite information at the top of the stack, but leave the stack pointer unchanged. This operation will usually destroy useful information and is normally avoided. A POP from an empty stack may place non-meaningful data on the Y outputs, but is otherwise safe. The stack pointer remains at zero whenever a POP is attempted from a stack already empty.

The register/counter is operated during three microinstructions (8, 9, 15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions. The register/counter is arranged such that if it is preloaded with a number N and then used as a loop termination counter, the sequence will be executed exactly N+1 times. During instruction 15, a three-way branch under combined control of the loop counter and the condition code is available.

The device provides three-state Y outputs. These can be particularly useful in designs requiring automatic checkout of the processor. The microprogram controller outputs can be forced into the high-impedance state, and pre-programmed sequences of microinstructions can be executed via external access to the address lines.

OPERATION

Table I shows the result of each instruction in controlling the multiplexer which determines the Y outputs, and in controlling the three enable signals $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. The effect on the register/counter and the stack after the next positive-going clock edge is also shown. The multiplexer determines which internal source drives the Y outputs. The value loaded into μPC is either identical to the Y output, or else one greater, as determined by CI. For each instruction, one and only one of the three outputs $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$ is LOW. If these outputs control three-state enables for the primary source of microprogram jumps (usually part of a pipeline register), a PROM which maps the instruction to a microinstruction starting location, and an optional third source (often a vector from a DMA or interrupt source), respectively, the three-state sources can drive the D inputs without further logic.

Several inputs, as shown in Table II, can modify instruction execution. The combination $\overline{CC}$ HIGH and $\overline{CCEN}$ LOW is used as a test in 9 of the 16 instructions. $\overline{RLD}$, when LOW, causes the D input to be loaded into the register/counter, overriding any HOLD or DEC operation specified in the instruction. $\overline{OE}$, normally LOW, may be forced HIGH to remove TS2910 Y outputs from a three-state bus.

The stack, a five-word last-in, first-out 12-bit memory, has a pointer which addresses the value presently on the top of the stack. Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever else the stack is empty, the contents of the top of stack is undefined until a PUSH occurs. Any POPs performed while the stack is empty put undefined data on the F outputs and leave the stack pointer at zero.

Any time the stack is full (five more PUSHes than POPs have occurred since the stack was last empty), the $\overline{FULL}$ warning output occurs. This signal first appears on the microcycle after a fifth PUSH. No additional PUSH should be attempted onto a full stack; if tried, information within the stack will be overwritten and lost.

TABLE I. INSTRUCTIONS

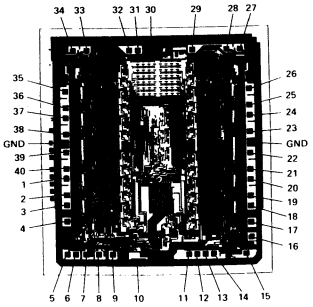
I_3-I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠ 0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

Note 1 : If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold ; else load. X = Don't Care

TABLE II. PIN FUNCTIONS

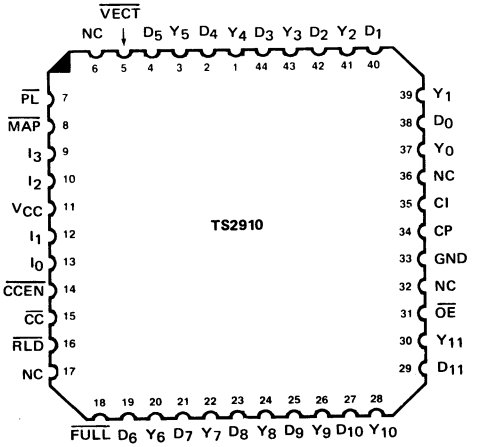
Abbreviation	Name	Function
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D_0 is LSB
I_i	Instruction Bit i	Selects one-of-sixteen instructions for the TS2910
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	Carry-In	Low order carry input to incrementer for microprogram counter
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge
V_{CC}	+5 Volts	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB
$\overline{FULL}$	Full	Indicates that five items are on the stack
$\overline{PL}$	Pipeline Address Enable	Can select #1 source (usually Pipeline Register) as direct input source
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually Mapping PROM or PLA) as direct input source
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source

Metallization and Pad Layout



TS2910
Die size : 4.320 x 4.930 mm
(Note: Numbers refer to DIP connections)

CHIP CARRIER



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V
MIL T_C = −55°C to +125°C V_{CC} = 5.0V ±10% MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.6mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	Y_{0-11}, I_{OL} = 12mA			0.5	Volts
			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$, $\overline{FULL}$, I_{OL} = 8mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-11}			−0.87	mA
			CI, $\overline{CCEN}$			−0.54	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$			−0.72	
			$\overline{CC}$			−1.31	
			CP			−2.14	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-11}			80	µA
			CI, $\overline{CCEN}$			30	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$			40	
			$\overline{CC}$			50	
			CP			100	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V			−50	µA
I_{OZH}			V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current	V_{CC} = MAX.	T_A = 25°C		195	320	mA
			C SUFFIX: T_A = 0°C to +70°C			344	
			C SUFFIX: T_A = +70°C			280	
			M SUFFIX: T_C = −55°C to +125°C			340	
			M SUFFIX: T_C = +125°C			227	

Notes: 1. For conditions shown as MIN., or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment, (not functionally tested).

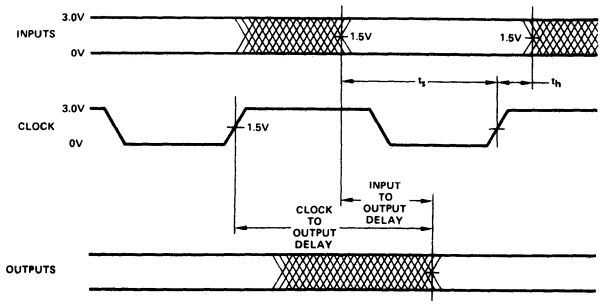


Figure 2. Switching Waveforms.

See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs. See Figure 5 for timing of a typical CCU cycle.

TS2910 SWITCHING CHARACTERISTICS

The tables below define the 2910 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

C SUFFIX (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	24	6
$D_i \rightarrow PC$	58	4
I_0-I_3	104	0
$\overline{CC}$	80	0
$\overline{CCEN}$	80	0
CI	46	5
$\overline{RLD}$	36	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	20	–	–
I_0-I_3	70	51	–
$\overline{CC}$	43	–	–
$\overline{CCEN}$	45	–	–
CP (Note 2) I = 8, 9, 15	100	–	60
	125	–	60
CP All other I	55	–	60
$\overline{OE}$ (Note 3)	35/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	50	ns
Minimum Clock HIGH Time	35	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	138	ns
	163	
Minimum Clock Period, I=14	93	ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

M SUFFIX (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	28	6
$D_i \rightarrow PC$	62	4
I_0-I_3	110	0
$\overline{CC}$	86	0
$\overline{CCEN}$	86	0
CI	58	5
$\overline{RLD}$	42	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	25	–	–
I_0-I_3	75	58	–
$\overline{CC}$	48	–	–
$\overline{CCEN}$	50	–	–
CP (Note 2) I = 8, 9, 15	106	–	67
	130	–	67
CP All other I	61	–	67
$\overline{OE}$ (Note 3)	40/30	–	–

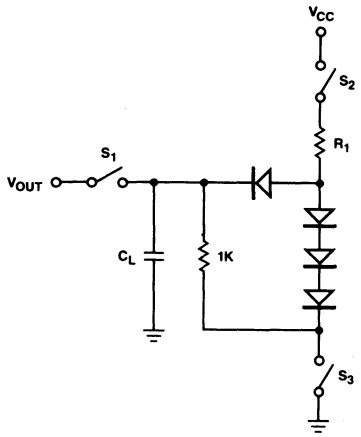
C. Clock Requirements (Note 1)

Minimum Clock LOW Time	58	ns
Minimum Clock HIGH Time	42	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	143	ns
	167	
Minimum Clock Period, I=14	100	ns

NOTES:
1. Clock periods for instructions not specified are determined by external conditions.
2. These instructions are conditional on the counter. Use the shorter specified delay times if the previous instruction could produce no change in the counter or could only decrement the counter. Use the longer delays from CP to outputs if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.
3. Enable/Disable. Disable times measured to 0.5V change on output voltage level with C_l = 5.0pF.

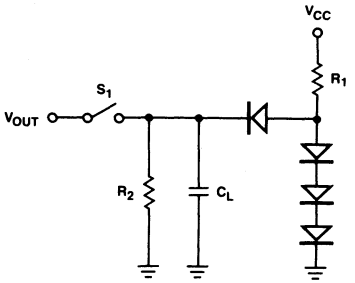
TEST OUTPUT LOAD CONFIGURATIONS FOR TS2910

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR TS2910

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	$Y_{0\text{-}11}$	A	300	1K
5	$\overline{VECT}$	B	470	1.5K
6	$\overline{PL}$	B	470	1.5K
7	$\overline{MAP}$	B	470	1.5K
16	$\overline{FULL}$	B	470	1.5K

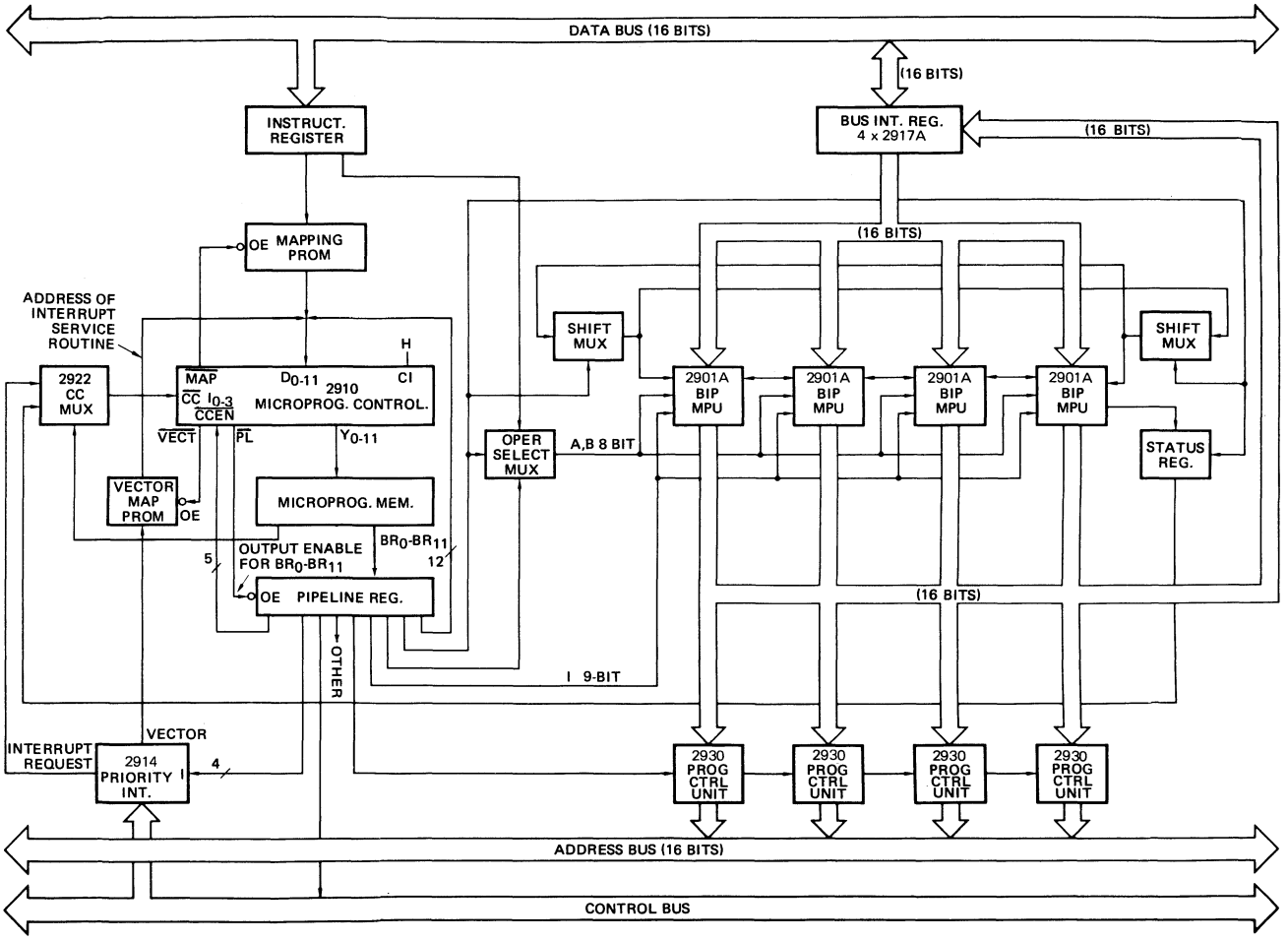
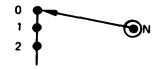
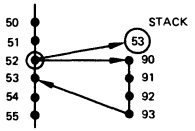


Figure 3. Typical Bipolar Microcomputer Using TS2910

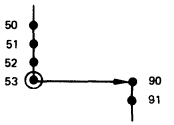
0 JUMP ZERO (JZ)



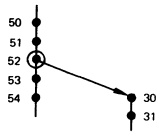
1 COND JSB PL (CJS)



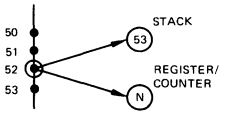
2 JUMP MAP (JMAP)



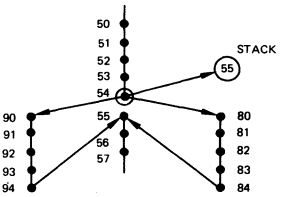
3 COND JUMP PL (CJP)



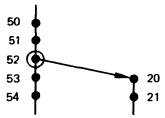
4 PUSH/COND LD CNTR (PUSH)



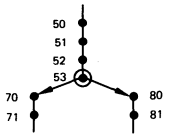
5 COND JSB R/PL (JSRP)



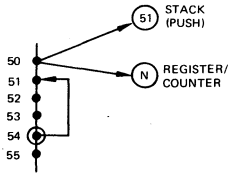
6 COND JUMP VECTOR (CJV)



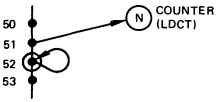
7 COND JUMP R/PL (JRP)



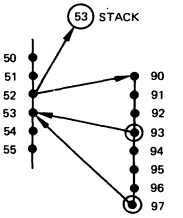
8 REPEAT LOOP, CNTR ≠ 0 (RFCT)



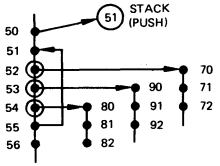
9 REPEAT PL, CNTR ≠ 0 (RPCT)



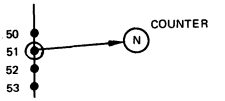
10 COND RETURN (CRTN)



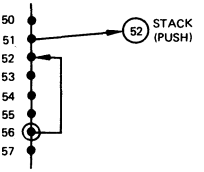
11 COND JUMP PL & POP (CJPP)



12 LD CNTR & CONTINUE (LDCT)



13 TEST END LOOP (LOOP)



14 CONTINUE (CONT)

15 THREE-WAY BRANCH (TWB)

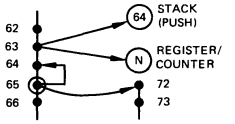


Figure 4. TS2910 Execution Examples.

THE TS2910 INSTRUCTION SET

The 2910 provides 16 instructions which select the address of the next *microinstruction to be executed*. Four of the instructions are unconditional – their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by an external, data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter. The instruction set is shown in Table I. In this discussion it is assumed that C_i is tied HIGH.

In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered to have been passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is, it forces a pass. Other ways of using $\overline{CCEN}$ include (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally ; OR (3) tying it to the source of 2910 instruction bit I_0, which leaves instructions 4, 6, and 10 as data-dependent but makes others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depends on the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected. These instructions are useful for executing a microinstruction loop a known number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

Perhaps the best technique for understanding the 2910 is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, Figure 4 is included and depicts examples of all 16 instructions.

The examples given in Figure 4 should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed. For example, the CONTINUE instruction, instruction number 14, as shown in Figure 4, simply means that the contents of microprogram memory word 50 is executed, then the contents of word 51 is executed. This is followed by the contents of microprogram memory word 52 and the contents of microprogram memory word 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the text to follow will explain what the conditional choices are in each example.

Instruction 0, JZ (JUMP and ZERO, or RESET) unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

Instruction 1 is a CONDITIONAL JUMP-TO-SUBROUTINE via the address provided in the pipeline register. As shown in Figure 4, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register, the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead. Thus, the CONDITIONAL JUMP-TO-SUBROUTINE instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the TEST input is such that location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

Instruction 2 is the JUMP MAP instruction. This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine. In the example of Figure 4, microinstructions at locations 50, 51, 52, and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.

Instruction 3, CONDITIONAL JUMP PIPELINE, derives its branch address from the pipeline register branch address value ($BR_0 - BR_{11}$ in Figure 2). This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some function. This usually has the effect of resetting the input being tested until some point in the future. Figure 4 shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or location 30 in this example. If the test is passed, the value currently in the pipeline register (30) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is 53.

Instruction 4 is the PUSH/CONDITIONAL LOAD COUNTER instruction and is used primarily for setting up loops in microprogram firmware. In Figure 4, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field. Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will

THE TS2910 INSTRUCTION SET (Cont.)

describe how to use the pushed value and the register/counter for looping.

Instruction 5 is a CONDITIONAL JUMP-TO-SUBROUTINE via the register/counter or the contents of the PIPELINE register. As shown in Figure 4, a PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A return-from-subroutine (instruction number 10) returns the microprogram flow to address 55. In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Let's assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the 2910 register / counter when the contents of address 54 are in the pipeline register. This requires that the instruction at address 53 load the register/counter. Now, during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

Instruction 6 is a CONDITIONAL JUMP VECTOR instruction which provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the 2910 output, $\overline{VECT}$ is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter. In the example of Figure 4, if the CONDITIONAL JUMP VECTOR instruction is contained at location 52, execution will continue at vector address 20 if the $\overline{CC}$ input is LOW and the microinstruction at address 53 will be executed if the $\overline{CC}$ input is HIGH.

Instruction 7 is a CONDITIONAL JUMP via the contents of the 2910 REGISTER/COUNTER or the contents of the PIPELINE register. This instruction is very similar to instruction 5; the conditional jump-to-subroutine via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is performed with 7. Figure 4 depicts this instruction as a branch to one of two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 is being executed. As the contents of address 53 is clocked into the pipeline register, the value 70 is loaded into the register/counter in the 2910. The value 80 is available when the contents of address 53 is in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

Instruction 8 is the REPEAT LOOP, COUNTER ≠ ZERO instruction. This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack. If the register counter contains zero, the loop exit condition is occuring; control falls through to the next sequential microinstruction by selecting μPC; the stack is POP'd by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

An example of the REPEAT LOOP, COUNTER ≠ ZERO instruction is shown in Figure 4. In this example, location 50 most likely would contain a PUSH/CONDITIONAL LOAD COUNTER instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop. This method allows a loop to be executed 1 to 4096 times. If it is desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

Instruction 9 is the REPEAT PIPELINE REGISTER, COUNTER ≠ ZERO instruction. This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested five deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In the example of Figure 4, the REPEAT PIPELINE, COUNTER ≠ ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.

Instruction 10 is the conditional RETURN-FROM-SUBROUTINE instruction. As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed. If the test is failed, the next sequential microinstruction is performed. The example in Figure 4 depicts *the use of the* conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes. This example first shows a jump-to-subroutine at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed. The program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force

THE TS2910 INSTRUCTION SET (Cont.)

$\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

Instruction 11 is the CONDITIONAL JUMP PIPELINE register address and POP stack instruction. This instruction provides another technique for loop termination and stack maintenance. The example in Figure 4 shows a loop being performed from address 55 back to address 51. The instructions at locations 52, 53, and 54 are all conditional JUMP and POP instructions. At address 52, if the $\overline{CC}$ input is LOW, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55. An instruction sequence as described here, using the CONDITIONAL JUMP PIPELINE and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.

Instruction 12 is the LOAD COUNTER AND CONTINUE instruction, which simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed. There are altogether three ways of loading the counter – the explicit load by this instruction 12; the conditional load included as part of instruction 4; and the use of the $\overline{RLD}$ input along with any instruction. The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width. This instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.

Instruction 13 is the TEST END-OF-LOOP instruction, which provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop, via the file, if the test is failed else to continue to the next sequential instruction. The example in Figure 4 shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed, which also causes the stack to be POP'd; thus, accomplishing the required stack maintenance.

Instruction 14 is the CONTINUE instruction, which simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.

Instruction 15, THREE-WAY BRANCH, is the most complex. It provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack. Instruction 15 performs a decrement-and-branch-until-zero function similar to instruction 8. The next address is taken from the top of the stack until the count reaches zero; then the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken; the microprogram counter register furnishes the next address. When the loop is ended, either by the count becoming zero, or by passing the conditional test, the stack is POP'd by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

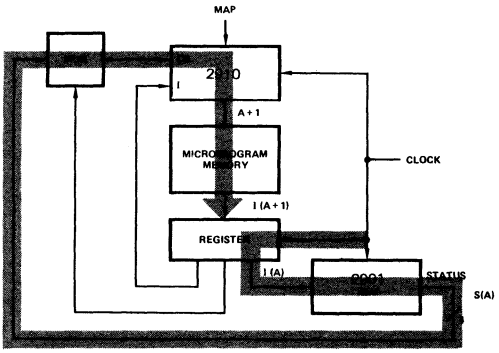
As one example, consider the case of a memory search instruction. As shown in Figure 4, the instruction at microprogram address 63 can be Instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before giving up. Location 64 contains a microinstruction which fetches the next operand from the memory area to be searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and also is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address. When the count becomes zero, the microprogram branches to location 72, which does whatever is necessary if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles this case. Whether the instruction ends by finding a match or not, the stack will have been POP'd once, removing the value 64 from the top of the stack.

OTHER ARCHITECTURES USING THE TS2910

(Shading shows path(s) which usually limit speed)

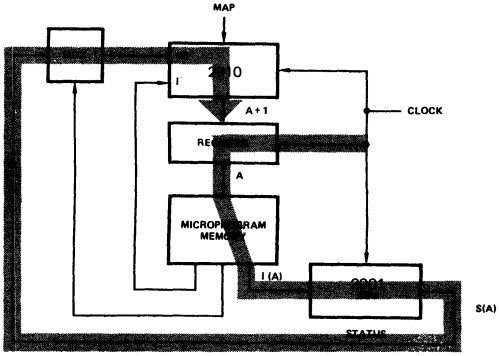
Figure 6.

A. Instruction Based



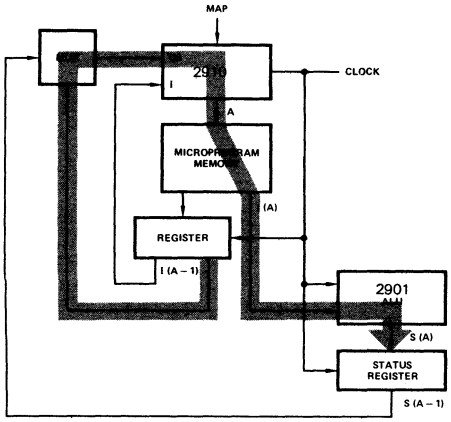
A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and 2901 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

B. Addressed Based



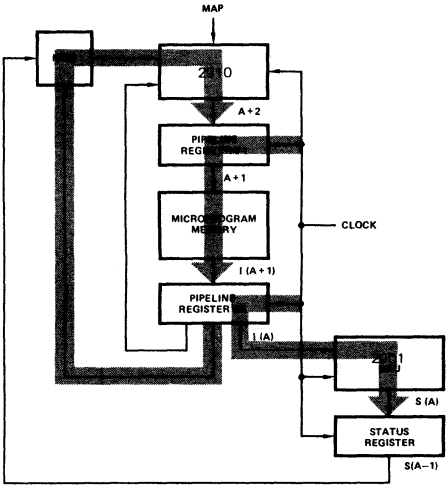
The Register at the 2910 output contains the address of the microinstruction being executed. The Microprogram Memory and 2901 are in series in the critical path. This architecture provides about the same speed as the Instruction based architecture, but requires fewer register bits, since only the address (typically 10-12 bits) is stored instead of the instruction (typically 40-60 bits).

C. Data Based



The Status Register provides conditional Branch control based on results of previous ALU cycle. The Microprogram Memory and 2901 are in series in the critical paths.

D. Two Level Pipeline Based



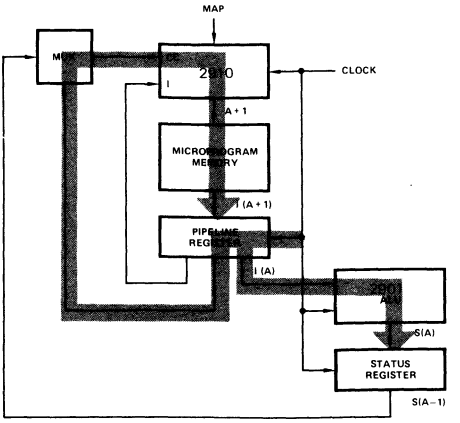
Two level pipeline provides highest possible speed. It is more difficult to program because the selection of a microinstruction occurs two instructions ahead of its execution.

ARCHITECTURE USING THE TS2910

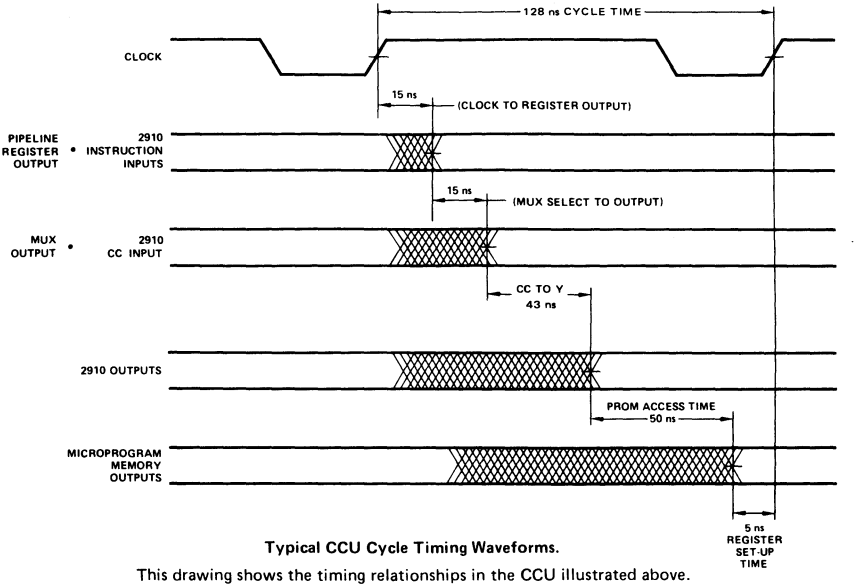
(Shading shows path(s) which usually limit speed)

Figure 5.

One Level Pipeline Based
(Recommended)



One level pipeline provides better speed than most other architectures. The μProgram Memory and the 2901 array are in parallel speed paths instead of in series. This is the recommended architecture for 2900 designs.



Typical CCU Cycle Timing Waveforms.

This drawing shows the timing relationships in the CCU illustrated above.

ORDERING INFORMATION

TS2910 | M | J | B/B

- TS2910: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

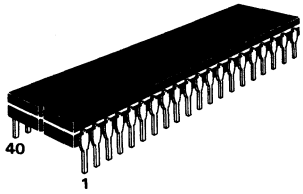
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2910	●		●	●			●	●		
		●		●	●	●	●		●	●

Examples : TS2910CP, TS2910CP-D, TS2910CJ, TS2910CJ-D
TS2910MJ, TS2910MJG/B, TS2910MJB/B,...

Oper. temp. : **C** : 0°C to + 70°C, **M** : – 55°C to + 125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

CASE CB-182

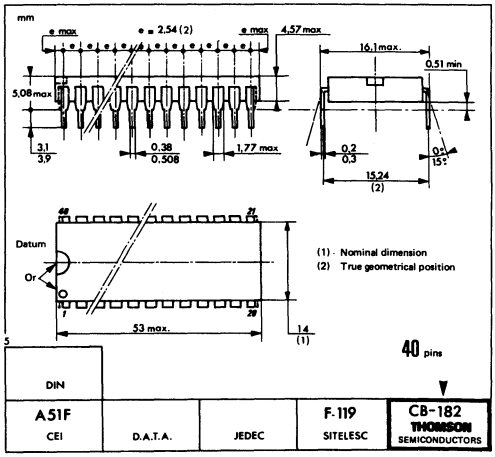


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTEURS

TS2914

VECTORED PRIORITY INTERRUPT CONTROLLER

The TS2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the TS2914 makes it ideal for use in 2900 family microcomputer designs.

The TS2914 receives interrupt requests on 8 interrupt input lines (P0-P7), A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three bit encoded vector representing the highest numbered input which is not masked.

An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the TS2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins). Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

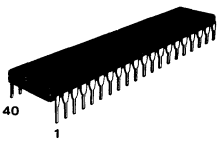
The TS2914 is controlled by a 4-bit instruction field 10-13. The command on the instruction lines is executed if IE is LOW and is ignored if IE is HIGH, allowing the 4 I bits to be shared with other devices.

- Accepts 8 interrupt inputs
  Interrupts may be pulses or levels and are stored internally.
- Built-in mask register
  Six different operations can be performed on mask register.
- Built-in status register
  Status register holds code for lowest allowed interrupt.
- *Vectored* output
  Output is binary code for highest priority un-masked interrupt.
- Expandable
  Any number of TS2914's may be stacked for large interrupt systems.
- Microprogrammable
  Executes 16 different microinstructions. Instruction enable pin aids in vertical microprogramming.
- High-speed operation
  Delay from an interrupt clocked into the interrupt register to interrupt request output is typically 60 ns.

For applications information, see Chapter VI of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

VECTORED PRIORITY INTERRUPT CONTROLLER

CASE CB-182



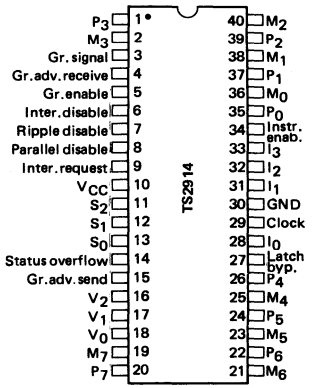
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX	E SUFFIX
CERDIP PACKAGE	CHIP CARRIER

Hi-Rel versions available - See chapter 4

PIN ASSIGNMENT



Ref. 01265-R1

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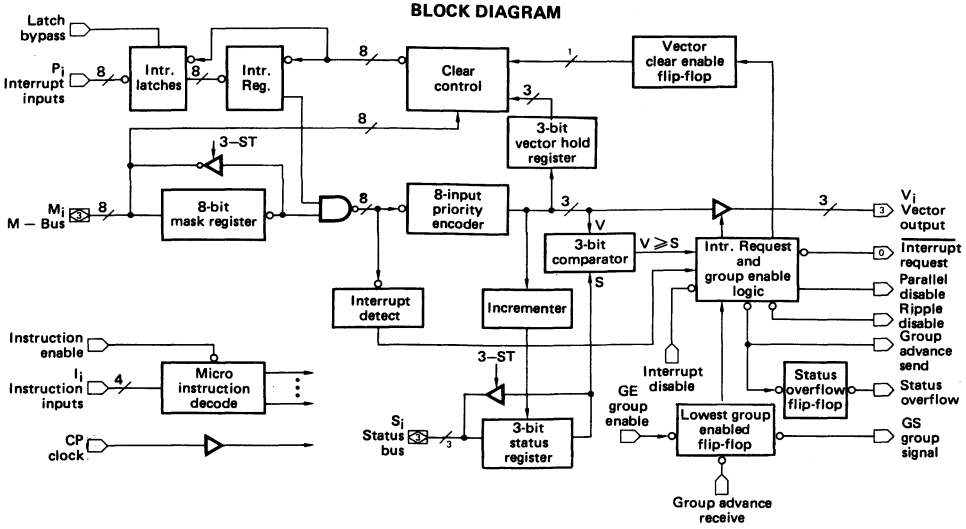
THOMSON COMPONENTS

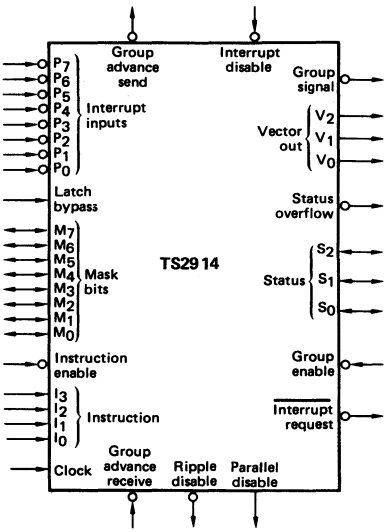
BLOCK DIAGRAM



PIN SYMBOLS

INPUT PIN	OPEN COLLECTOR OUTPUT
OUTPUT PIN	
BIDIRECTIONAL I/O	THREE-STATE OUTPUT

LOGIC SYMBOL



BLOCK DIAGRAM DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

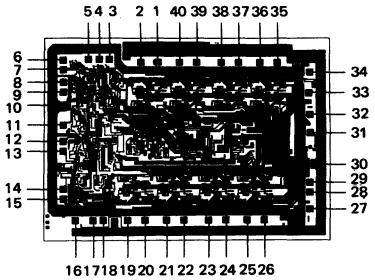
The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

Metallization and Pad Layout



Die size : 3.600 x 4.900

Numbers correspond to DIP pin-out.

TABLE I
MICROINSTRUCTION SET FOR 2914 PRIORITY INTERRUPT CIRCUIT

Decimal $I_3I_2I_1I_0$	Mnemonic	Instruction	Decimal $I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask Register Functions			**Vectored Output**
14	LDM	Load mask register from M bus	5	RDVC	Read vector output to V outputs, load V+1 into status register, load V into vector hold register and set vector clear enable flip-flop.
7	RDM	Read mask register to M bus			
12	CLRM	Clear mask register (enables all priorities)			
8	SETM	Set mask register (inhibits all interrupts)			**Priority Interrupt Register Clear**
10	BCLRM	Bit clear mask register from M bus	1	CLRIN	Clear all interrupts
11	BSETM	Bit set mask register from M bus	3	CLRMR	Clear interrupts from mask register data (uses the M bus)
		Status Register Functions	2	CLRMB	Clear interrupts from M bus data
9	LDSTA	Load status register from S bus and LGE flip-flop from GE input	4	CLRVC	Clear the individual interrupt associated with the last vector read
6	RDSTA	Read status register to S bus			
		Interrupt Request Control			**Master Clear**
15	ENIN	Enable interrupt request	0	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request.
13	DISIN	Disable interrupt request			

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +110°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	+0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Temperature	V_{CC}
C SUFFIX	0°C to +70°C	4.75V to 5.25V
M SUFFIX	−55°C to +110°C	4.50V to 5.50V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

C SUFFIX T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V
M SUFFIX T_C = −55°C to +110°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4			Volts
			COM'L, I_{OH} = −2.6mA		2.4			
I_{CEX}	Output Leakage Current for IR Output	V_{CC} = MIN., V_O = 5.5V					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	M_{0-7}				−0.15	mA
			S_{0-2}				−0.1	
			L. B.				−0.4	
			$\overline{I. D.}$				−2.0	
			$\overline{IE}$				−1.08	
			All Others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	M_{0-7}				150	µA
			S_{0-2}				100	
			$\overline{GE}$, $\overline{GAR}$				40	
			$\overline{IE}$				60	
			$\overline{I. D.}$				60	
			All Others				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZL}	Off-State Output Current	V_{CC} = MAX.	V_{OUT} = 0.5V	M_{0-7}			−150	µA
				S_{0-2}			−100	
				V_{0-2}			−50	
I_{OZH}			V_{OUT} = 2.4V	M_{0-7}			150	
				S_{0-2}			100	
				V_{0-2}			50	
I_{CC}	Power Supply Current	V_{CC} = 5.0V, 25°C				170	−	mA
		V_{CC} = MAX.	COM'L	0°C			305	
				70°C			250	
			MIL	−55°C			310	
				110°C			200	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA

Notes : 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS AT 25°C AND 5.0 VOLTS

Note : All outputs fully loaded. C_L = 50 pF. Measurements made at 1.5 V with input levels of 0V and 3.0V. All numbers are in ns.
For interrupt request output, R_L = 470Ω

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	GUARANTEED
Minimum Clock LOW Time	30
Minimum Clock HIGH Time	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	25
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	10

TABLE II. COMBINATIONAL PROPAGATION DELAYS (ns)

	TYPICAL						GUARANTEED					
To Output / From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	36	40	40	–	–	30	48	55	55	–	–	47
I_{0123}	36	40	40	–	–	30	48	55	55	–	–	47
Irpt. Disable	–	–	25	35	8	19	–	–	37	42	18	25

TABLE III. DELAYS FROM CLOCK TO OUTPUTS (ns)

Clock Path	TYPICAL							GUARANTEED						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Mask Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Status Register	45	55	28	31	37	–	–	59	74	57	57	58	–	–
Lowest Group Enabled Flip-Flop	–	–	22	25	–	–	17	–	–	42	45	–	–	32
Irpt Request Enable Flip-Flop	–	40	–	–	–	–	–	–	56	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	17	–	–	–	–	–	–	30	–

TABLE IV. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	GUARANTEED	
	Set-up Time	Hold Time
S-Bus	11	8
M-Bus	11	8
$\overline{P_0}$-$\overline{P_7}$	11	6
Latch Bypass	16	0
$\overline{IE}$ / I_{0123} (See Note)	46 / t_{pwL} + 29	0
$\overline{GE}$	11	11
$\overline{GAR}$	11	11
$\overline{Irpt\ Disable}$	35	0
P_0-P_7 Hold Time Relative to LB	–	21

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

All outputs fully loaded, C_L = 50pF. Measurements made at 1.5V with input levels of 0V and 3.0V. For Interrupt Request Output, R_L = 470Ω.

TABLE V. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	C SUFFIX T_A = 0°C to +70°C, 5V ± 5%	M SUFFIX T_C = –55°C to +110°C, 5V ± 10%
Minimum Clock LOW Time	30	30
Minimum Clock HIGH Time	30	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	40	40
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	8	8
Minimum Clock Period, $\overline{IE}$ = H on current cycle and previous cycle	50	55
Minimum Clock Period, $\overline{IE}$ = L on current cycle or previous cycle	100	110

TABLE VI. MAXIMUM COMBINATIONAL PROPAGATION DELAYS (ns)

	C SUFFIX T_A = 0°C to +70°C, 5V ± 5%						M SUFFIX T_C = –55°C to +110°C, 5V ± 10%					
To Output / From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	52	60	65	–	–	56	60	68	70	–	–	62
I_{0123}	52	60	65	–	–	56	60	68	70	–	–	62
Irpt. Disable	–	–	45	52	20	30	–	–	48	60	22	33

TABLE VII. MAXIMUM DELAYS FROM CLOCK TO OUTPUTS (ns)

Clock Path	C SUFFIX T_A = 0°C to +70°C, 5V ± 5%							M SUFFIX T_C = –55°C to +110°C, 5V ± 10%						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Mask Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Status Register	67	88	63	63	70	–	–	73	96	66	66	76	–	–
Lowest Group Enabled Flip-Flop	–	–	48	52	–	–	38	–	–	54	58	–	–	45
Irpt Request Enable Flip-Flop	–	62	–	–	–	–	–	–	66	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	35	–	–	–	–	–	–	40	–

BLOCK DIAGRAM DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

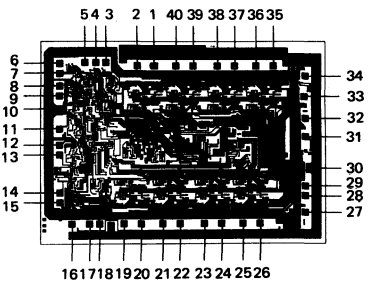
The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

Metallization and Pad Layout



Die size : 3.600 x 4.900

Numbers correspond to DIP pin-out.

TABLE I
MICROINSTRUCTION SET FOR 2914 PRIORITY INTERRUPT CIRCUIT

Decimal $I_3I_2I_1I_0$	Mnemonic	Instruction	Decimal $I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask Register Functions			**Vectored Output**
14	LDM	Load mask register from M bus	5	RDVC	Read vector output to V outputs, load V+1 into status register, load V into vector hold register and set vector clear enable flip-flop.
7	RDM	Read mask register to M bus			
12	CLRM	Clear mask register (enables all priorities)			
8	SETM	Set mask register (inhibits all interrupts)			**Priority Interrupt Register Clear**
10	BCLRM	Bit clear mask register from M bus	1	CLRIN	Clear all interrupts
11	BSETM	Bit set mask register from M bus	3	CLRMR	Clear interrupts from mask register data (uses the M bus)
		Status Register Functions	2	CLRMB	Clear interrupts from M bus data
9	LDSTA	Load status register from S bus and LGE flip-flop from GE input	4	CLRVC	Clear the individual interrupt associated with the last vector read
6	RDSTA	Read status register to S bus			**Master Clear**
		Interrupt Request Control	0	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request.
15	ENIN	Enable interrupt request			
13	DISIN	Disable interrupt request			

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +110°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	+0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Temperature	V_{CC}
C SUFFIX	0°C to +70°C	4.75V to 5.25V
M SUFFIX	−55°C to +110°C	4.50V to 5.50V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

C SUFFIX T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V
M SUFFIX T_C = −55°C to +110°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4			Volts
			COM'L, I_{OH} = −2.6mA		2.4			
I_{CEX}	Output Leakage Current for IR Output	V_{CC} = MIN., V_O = 5.5V					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	M_{0-7}				−0.15	mA
			S_{0-2}				−0.1	
			L. B.				−0.4	
			$\overline{I.D.}$				−2.0	
			$\overline{IE}$				−1.08	
			All Others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	M_{0-7}				150	µA
			S_{0-2}				100	
			$\overline{GE}$, $\overline{GAR}$				40	
			$\overline{IE}$				60	
			$\overline{I.D.}$				60	
			All Others				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZL}	Off-State Output Current	V_{CC} = MAX.	V_{OUT} = 0.5V	M_{0-7}			−150	µA
				S_{0-2}			−100	
				V_{0-2}			−50	
I_{OZH}			V_{OUT} = 2.4V	M_{0-7}			150	
				S_{0-2}			100	
				V_{0-2}			50	
I_{CC}	Power Supply Current	V_{CC} = 5.0V, 25°C				170	−	mA
		V_{CC} = MAX.	COM'L	0°C			305	
				70°C			250	
			MIL	−55°C			310	
				110°C			200	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA

Notes : 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS AT 25°C AND 5.0 VOLTS

Note : All outputs fully loaded. C_L = 50 pF. Measurements made at 1.5 V with input levels of 0V and 3.0V. All numbers are in ns.
For interrupt request output, $R_L = 470\Omega$

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	GUARANTEED
Minimum Clock LOW Time	30
Minimum Clock HIGH Time	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	25
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	10

TABLE II. COMBINATIONAL PROPAGATION DELAYS (ns)

	TYPICAL						GUARANTEED					
To Output / From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	36	40	40	–	–	30	48	55	55	–	–	47
I_{0123}	36	40	40	–	–	30	48	55	55	–	–	47
Irpt. Disable	–	–	25	35	8	19	–	–	37	42	18	25

TABLE III. DELAYS FROM CLOCK TO OUTPUTS (ns)

Clock Path	TYPICAL							GUARANTEED						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Mask Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Status Register	45	55	28	31	37	–	–	59	74	57	57	58	–	–
Lowest Group Enabled Flip-Flop	–	–	22	25	–	–	17	–	–	42	45	–	–	32
Irpt Request Enable Flip-Flop	–	40	–	–	–	–	–	–	56	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	17	–	–	–	–	–	–	30	–

TABLE IV. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	GUARANTEED	
	Set-up Time	Hold Time
S-Bus	11	8
M-Bus	11	8
$\overline{P_0}$-$\overline{P_7}$	11	6
Latch Bypass	16	0
$\overline{IE}$ / I_{0123} (See Note)	46 / t_{pwL} + 29	0
$\overline{GE}$	11	11
$\overline{GAR}$	11	11
$\overline{Irpt\ Disable}$	35	0
P_0-P_7 Hold Time Relative to LB	–	21

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

All outputs fully loaded, C_L = 50pF. Measurements made at 1.5V with input levels of 0V and 3.0V. For Interrupt Request Output, R_L = 470Ω.

TABLE V. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	C SUFFIX T_A = 0°C to +70°C, 5V ± 5%	M SUFFIX T_C = −55°C to +110°C, 5V ± 10%
Minimum Clock LOW Time	30	30
Minimum Clock HIGH Time	30	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	40	40
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	8	8
Minimum Clock Period, $\overline{IE}$ = H on current cycle and previous cycle	50	55
Minimum Clock Period, $\overline{IE}$ = L on current cycle or previous cycle	100	110

TABLE VI. MAXIMUM COMBINATIONAL PROPAGATION DELAYS (ns)

	C SUFFIX T_A = 0°C to +70°C, 5V ± 5%						M SUFFIX T_C = −55°C to +110°C, 5V ± 10%					
To Output / From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	52	60	65	–	–	56	60	68	70	–	–	62
I_{0123}	52	60	65	–	–	56	60	68	70	–	–	62
Irpt. Disable	–	–	45	52	20	30	–	–	48	60	22	33

TABLE VII. MAXIMUM DELAYS FROM CLOCK TO OUTPUTS (ns)

Clock Path	C SUFFIX T_A = 0°C to +70°C, 5V ± 5%							M SUFFIX T_C = −55°C to +110°C, 5V ± 10%						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Mask Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Status Register	67	88	63	63	70	–	–	73	96	66	66	76	–	–
Lowest Group Enabled Flip-Flop	–	–	48	52	–	–	38	–	–	54	58	–	–	45
Irpt Request Enable Flip-Flop	–	62	–	–	–	–	–	–	66	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	35	–	–	–	–	–	–	40	–

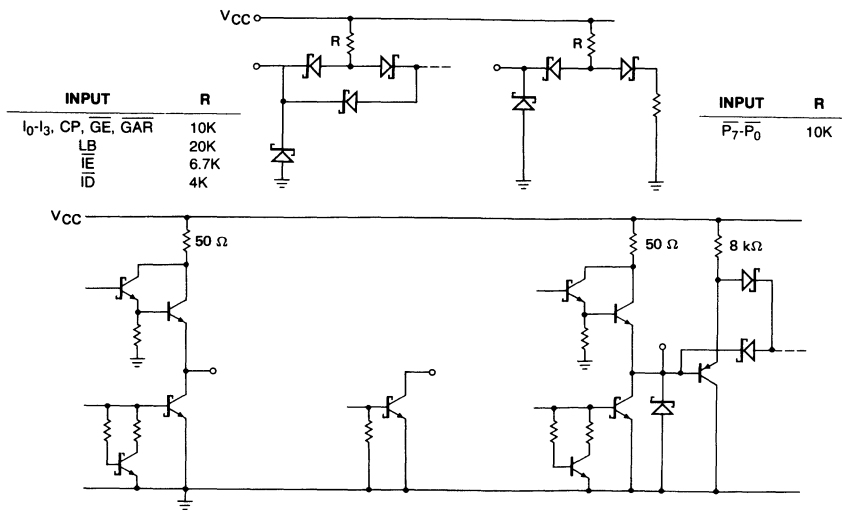
TABLE VIII. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	C SUFFIX T_A = 0°C to +70°C, 5V ± 5%		M SUFFIX T_C = –55°C to +110°C, 5V ± 10%	
	Set-Up Time	Hold Time	Set-Up Time	Hold Time
S-Bus	15	10	15	10
M-Bus	15	10	15	10
$\overline{P_0}$-$\overline{P_7}$	15	8	15	8
Latch Bypass	20	0	20	0
$\overline{IE}$ I_{0123} (See Note)	55 t_{pwL} + 33	0	55 t_{pwL} + 40	0
$\overline{GE}$	15	13	15	13
$\overline{GAR}$	15	13	15	13
$\overline{Irpt\ Disable}$	42	0	42	0
P_0-P_7 Hold Time Relative to LB	—	25	—	25

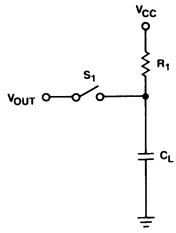
Note : t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

INPUT/OUTPUT CIRCUITS

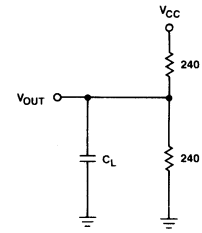


TEST OUTPUT LOAD CONFIGURATIONS FOR 2914

C. OPEN-COLLECTOR OUTPUTS



D. THREE-STATE OUTPUTS



Notes : 1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. C_L = 5.0 pF for output disable tests.

TEST OUTPUT LOADS FOR 2914

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
3	Group Signal	C	2K	–
4	Group Advance Receive	C	2K	–
7	Ripple Disable	C	2K	–
8	Parallel Disable	C	2K	–
9	Interrupt Request	C	330	–
13-11	S_{0-2}	D	240	240
14	Status Overflow	C	2K	–
18-16	V_{0-2}	D	240	240
–	M_{0-7}	D	240	240

A MICROPROGRAMMABLE, BIPOLAR, LSI INTERRRUPT STRUCTURE USING THE TS2914

INTRODUCTION

THOMSON SEMICONDUCTORS introduction of the TS2914 Vectored Priority Interrupt Controller now makes possible the structuring of a microprogrammable bipolar LSI interrupt system. The design engineer may use the 2914 to simplify his design process, dramatically reduce the system cost, size and package count, and increase the speed, capability and reliability of his interrupt system.

The 2914 is a modular, low cost, standard LSI component that may be microprogrammed to meet the requirements of specific applications. Today's engineer may utilize the 2914 microprogrammability to provide functional flexibility and ease of engineering change, while taking advantage of its modularity to provide hardware regularity and future expansion capability.

THE INTERRUPT CONCEPT

In any state machine, a requirement exists for the efficient synchronization and response to asynchronous events such as power failure, machine malfunctions, control panel service requests, external timer signals, supervisory calls, program errors, and input/output device service requests. The merit of such an "asynchronous event handler" may be measured in terms of response time, system throughput, real time overhead, hardware cost and memory space required.

The simplest approach to asynchronous event handling is the poll approach. A status indicator is associated with each possible asynchronous event. The processor tests each indicator in sequence and, in effect, "asks" if service is required. This program-driven method is inefficient for a number of reasons. Much time is consumed polling when no service is required; programs must have frequent test points to poll indicators, and since indicators are polled in sequence, considerable time may elapse before the processor responds to an event. Thus, system throughput is low; real time overhead and response time are high, and a large memory space is required.

The interrupt method is a much more efficient way of servicing asynchronous requests. An asynchronous event requiring service generates an interrupt request signal to the processor. When the processor receives the interrupt request, it may suspend the program it is currently executing, execute an interrupt service routine which services the asynchronous request, then resume the execution of the suspended program. In this system, the execution of the service routine is initiated by an interrupt request; thus, the system is interrupt driven and service routines are executed only when service is requested. Although hardware cost may be higher in this type of system, it is more efficient since system throughput is higher, response time is faster, real time overhead is lower and less memory space is required.

INTERRUPT SYSTEM FUNCTIONAL DEFINITION

A complete and clear functional definition is key to the design of a good interrupt system. The following features are useful.

Multiple Interrupt Request Handling: Since interrupt requests are generated from a number of different sources, the interrupt system's ability to handle interrupt requests from several sources is important.

Interrupt Request Prioritization: Since the processor can service only one interrupt request at a time, it is important that the interrupt system has the ability to prioritize the requests and determine which has the highest priority.

Interrupt Service Routine "Nesting": This feature allows an interrupt service routine for a given priority request to be interrupted in turn, but only by a higher priority interrupt request. The service routine for the higher priority request is executed, then the execution of the interrupted service routine is resumed. If there are "n" interrupt requests, an "n" deep "nest" is possible.

Dynamic Interrupt Enabling/Disabling: The ability to enable/disable all interrupts "on the fly" under microprogram control can be used to prevent interruption of certain processes.

Dynamic Interrupt Request Masking: The ability to selectively inhibit or "mask" individual interrupt requests under microprogram control is useful.

Interrupt Request Vectoring: Many times, a particular interrupt request requires the execution of a unique interrupt service routine. For this reason, the generation of a unique binary coded vector for each interrupt request is very helpful. This vector can be used as a pointer to the start of a unique service routine.

Interrupt Request Priority Threshold: The ability to establish a priority threshold is valuable. In this type of operation, only those interrupt requests which have higher priority than a specified threshold priority are accepted. The threshold priority can be defined by microprogram or can be automatically established by hardware at the interrupt currently being serviced plus one. This automatic threshold prevents multiple interrupts from the same source. Also useful is the ability to read the threshold priority under microprogram control. Thus, the interrupt request being serviced may be determined by the microprogram.

Interrupt Request Clearing Flexibility: Flexibility in the method of clearing interrupt requests allows different modes of interrupt system operation. Of particular value are the abilities to clear the interrupt currently being serviced, clear all interrupts, or clear interrupts via a programmable mask register or bus.

Microprogrammability: Microprogrammability permits the construction of a general purpose or "universal" interrupt structure which can be microprogrammed to meet a specific application's requirements. The universality of the structure allows standardization of the hardware and amortization of the hardware development costs across a much broader user base. The end result is a flexible, low cost interrupt structure.

Hardware Modularity: Modular interrupt system hardware is beneficial in two ways. First, hardware modularity provides expansion capability. Additional modules may be added as the need to service additional requests arises. Secondly, hardware modularity provides a structural regularity which simplifies the system structure and also reduces the number of hardware part numbers.

Fast Interrupt System Response Time: Quick interrupt system response provides more efficient system operation. Fast response reduces real time overhead and increases overall system throughput.

INTERRUPT SYSTEM IMPLEMENTATION USING THE TS2914

The 2914 provides all of the foregoing features on a single LSI chip. The 2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The 2914's high speed is ideal for use in 2900 Family microcomputer designs.

The 2914 receives interrupt requests on eight Interrupt Input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses (HIGH-LOW-HIGH) on these lines, or the latch may be bypassed so that the request lines drive the D-inputs to the edge-triggered Interrupt Register directly. An eight-bit Mask Register is used to mask individual interrupts. Considerable flexibility is provided for controlling the Mask Register. Requests in the Interrupt Register (P_0-P_7) are ANDed with the corresponding bits in the mask register (M_0-M_7) and the results are sent to an eight-input priority encoder, which produces a three-bit encoded vector representing the highest priority input which is not masked.

An internal Status Register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the Status Register are compared with the output of the priority encoder, and an Interrupt Request output will occur if the vector is greater than or equal to the contents of the Status Register. Whenever a vector is read from the 2914, the Status Register is automatically updated to point to one level higher than the vector read. (The Status Register can be loaded externally or read out at any time using the S-Bus.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A Status Overflow output indicates that an interrupt has been read at the highest priority.

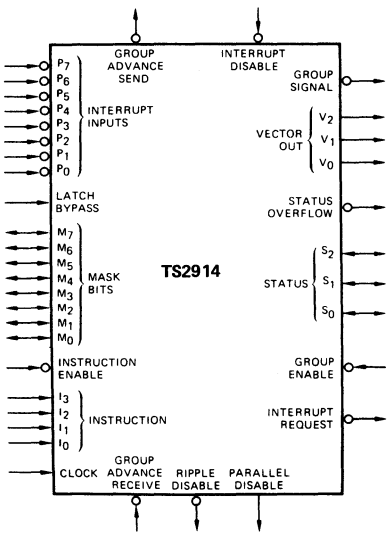


Figure 1. TS2914 Logic Symbol

The 2914 is controlled by a four-bit microinstruction field I_0-I_3. The microinstruction is executed if $\overline{IE}$ (Instruction Enable) is LOW and is ignored if $\overline{IE}$ is HIGH, allowing the four I bits to be shared with other functions. Sixteen different microinstructions are executed. Figure 2 shows the microinstructions and the microinstruction codes.

MICROINSTRUCTION DESCRIPTION	MICROINSTRUCTION CODE $I_3I_2I_1I_0$
MASTER CLEAR	0000
CLEAR ALL INTERRUPTS	0001
CLEAR INTERRUPTS FROM M-BUS	0010
CLEAR INTERRUPTS FROM MASK REGISTER	0011
CLEAR INTERRUPT, LAST VECTOR READ	0100
READ VECTOR	0101
READ STATUS REGISTER	0110
READ MASK REGISTER	0111
SET MASK REGISTER	1000
LOAD STATUS REGISTER	1001
BIT CLEAR MASK REGISTER	1010
BIT SET MASK REGISTER	1011
CLEAR MASK REGISTER	1100
DISABLE INTERRUPT REQUEST	1101
LOAD MASK REGISTER	1110
ENABLE INTERRUPT REQUEST	1111

Figure 2. TS2914 Microinstruction Set.

In this microinstruction set, the *Master Clear* microinstruction is selected as binary zero so that during a power up sequence, the microinstruction register in the microprogram control unit of the central processor can be cleared to all zeros. Thus, on the next clock cycle, the 2914 will execute the Master *Clear* function. This includes clearing the Interrupt Latches and Register as well as the Mask Register and Status Register. The LGE flip-flop of the least significant group is set LOW because the Group Advance Receive input is tied LOW. All other Group Advance Receive inputs are tied to Group Advance Send outputs and these are forced HIGH during this instruction. This clear instruction also sets the Interrupt Request Enable flip-flop so that a fully interrupt driven system can be easily initiated from any interrupt.

The *Clear All Interrupts* microinstruction clears the Interrupt Latches and Register.

The *Clear Interrupts from Mask Register* microinstruction clears those Interrupt Latches and Register bits which have corresponding Mask Register bits set equal to one. The M-Bus is used by the 2914 during the execution of this microinstruction and must be floating.

The *Clear Interrupts from M-Bus* microinstruction clears those Interrupt Latches and Register bits which have corresponding M-Bus bits set equal to one.

The *Clear Interrupt, Last Vector Read* microinstruction clears the Interrupt Latch and Register bit associated with the last vector read.

The *Read Vector* microinstruction is used to read the vector value of the highest priority request causing the interrupt. The vector outputs are three-state drivers that are enabled onto the $V_0V_1V_2$ bus during this instruction. This microinstruction also automatically loads the value "vector plus one" into the Status Register. In addition, this instruction sets the Vector Clear Enable flip-flop and loads the current vector value into the Vector Hold Register so that this value can be used by the *Clear Interrupt, Last Vector Read* microinstruction. This allows the user to read the vector associated with the interrupt, and at some later time clear the Interrupt Latch and Register bit associated with the vector read.

The *Load Status Register* microinstruction loads S-Bus data into the Status Register and also loads the LGE flip-flop from the Group Enable input.

During the *Read Status Register* microinstruction, the Status Register outputs are enabled onto the Status Bus (S_0-S_2). The Status Bus is a three-bit, bi-directional, three-state bus.

The *Load Mask Register* microinstruction loads data from the three-state, bi-directional M-Bus into the Mask Register.

The *Read Mask Register* microinstruction enables the Mask Register outputs onto the bi-directional, three-state M-Bus.

The *Set Mask Register* microinstruction sets all the bits in the Mask Register to one. This results in all interrupts being inhibited.

The entire Mask Register is cleared by the *Clear Mask Register* microinstruction. This enables all interrupts subject to the Interrupt Enable flip-flop and the Status Register.

The *Bit Clear Mask Register* microinstruction may be used to selectively clear individual Mask Register bits. This microinstruction clears those Mask Register bits which have corresponding M-Bus bits equal to one. Mask Register bits with corresponding M-Bus bits equal to zero are not affected.

The *Bit Set Mask Register* microinstruction sets those Mask Register bits which have corresponding M-Bus bits equal to one. Other Mask Register bits are not affected.

All Interrupt Requests may be disabled by execution of the *Disable Interrupt Request* microinstruction. This microinstruction resets an Interrupt Request Enable flip-flop on the chip.

The *Enable Interrupt Request* microinstruction sets the Interrupt Enable flip-flop. Thus, Interrupt Requests are enabled subject to the contents of the Mask and Status Registers.

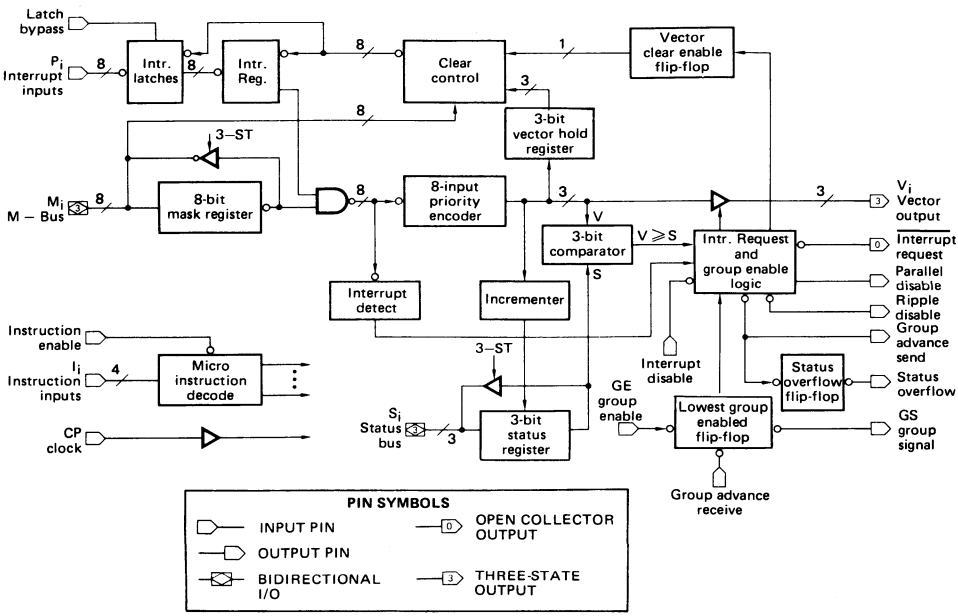


Figure 3. TS2914 Block Diagram

2914 BLOCK DIAGRAM DESCRIPTION

The 2914 block diagram is shown in Figure 3. The Micro-instruction Decode circuitry decodes the Interrupt Micro-instructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal if the Interrupt Input is LOW.

The Interrupt latches are set/reset latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M-Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector can be used later for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S-Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus, the Status Register points to a level one greater than the vector just read.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this chip. When it is set it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

The 2914 can be microprogrammed in many different ways. Figure 4 shows an example interrupt sequence. The *Read Vector* microinstruction is necessary in order to read the interrupt priority level. Since vector plus one is automatically loaded into the Status Register when a *Read Vector* microinstruction is executed, the Status Register possibly will overflow and disable all interrupts. For this reason, the Status Register must be reloaded periodically. The other 2914 microinstructions are optional.

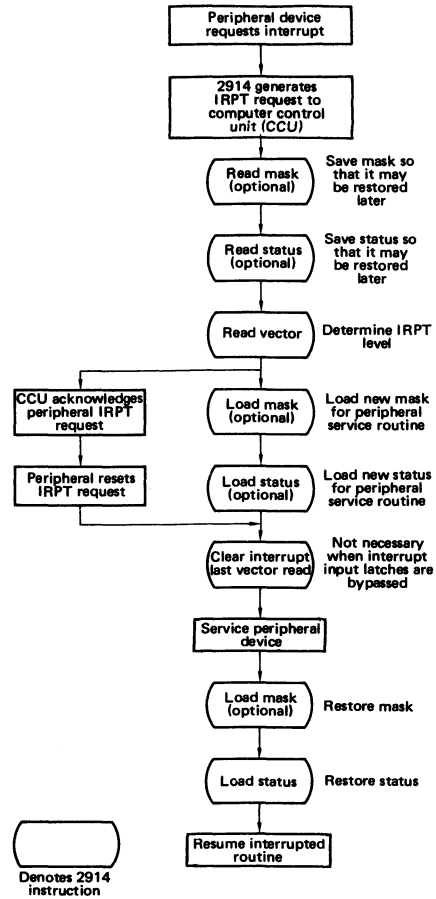


Figure 4. Example Interrupt Sequence.

CASCADING THE 2914

A number of input/output signals are provided for cascading the 2914 Vectored Priority Interrupt Encoder. A definition of these I/O signals and their required connections follows:

Group Signal ($\overline{GS}$) – This signal is the output of the Lowest Group Enabled flip-flop and during a Read Status microinstruction is used to generate the high order bits of the Status word.

Group Enable ($\overline{GE}$) – This signal is one of the inputs to the Lowest Group Enable flip-flop and is used to load the flip-flop during the Load Status microinstruction.

Group Advance Send ($\overline{GAS}$) – During a Read Vector microinstruction, this output signal is LOW when the highest priority vector (vector seven) of the group is being read. In a cascaded system Group Advance Send must be tied to the Group Advance Receive input of the next higher group in order to transfer status information.

Group Advance Receive ($\overline{GAR}$) – During a Master Clear or Read Vector microinstruction, this input signal is used with other internal signals to load the Lowest Group Enabled flip-flop. The Group Advance Receive input of the lowest priority group must be tied to ground.

Status Overflow ($\overline{SV}$) – This output signal becomes LOW after the highest priority vector (vector seven) of the group has been read and indicates the Status Register has overflowed. It stays LOW until a Master Clear or Load Status microinstruction is executed. The Status Overflow output of the highest priority group should be connected to the Interrupt Disable input of the same group and serves to disable all interrupts until new status is loaded or the system is master cleared. The Status Overflow outputs of lower priority groups should be left open (see Figure 7).

Interrupt Disable ($\overline{ID}$) – When LOW, this input signal inhibits the Interrupt Request output from the chip and also generates a Ripple Disable output.

Ripple Disable ($\overline{RD}$) – This output signal is used only in the Ripple Cascade Mode (see below). The Ripple Disable output is LOW when the Interrupt Disable input is LOW, the Lowest Group Enabled flip-flop is LOW, or an Interrupt Request is generated in the group. In the ripple cascade mode, the

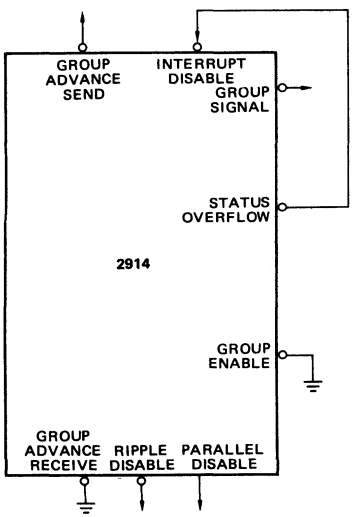


Figure 5. Cascade Lines Connection for Single Chip System.

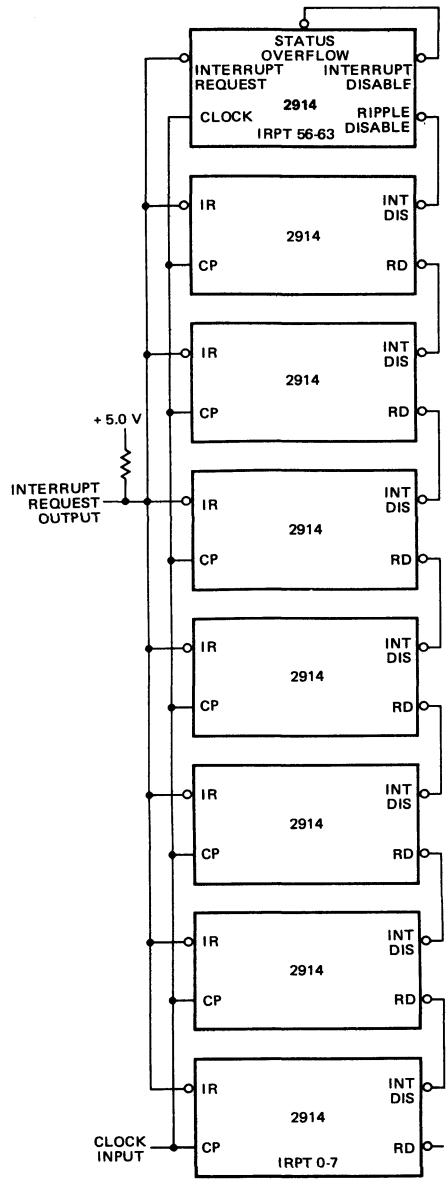


Figure 6. Interrupt Disable Connections for Ripple Cascade Mode.

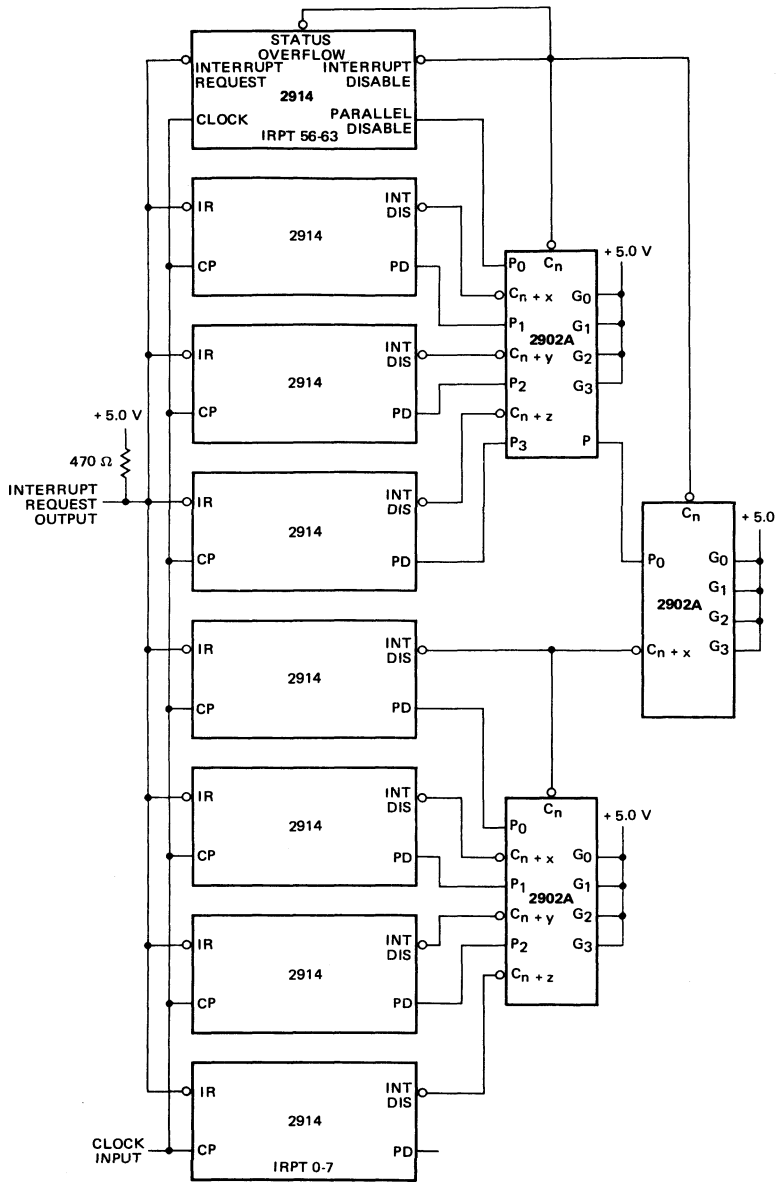


Figure 7. Interrupt Disable Connections for Parallel Cascade Mode.

Ripple Disable output is tied to the Interrupt Disable input of the next lower priority group (see Figure 6).

Parallel Disable (PD) – This output is used only in the parallel cascade mode (see below). It is HIGH when the Lowest Group Enabled flip-flop is LOW or an Interrupt Request is generated in the group. It is not affected by the Interrupt Disable input.

A single 2914 chip may be used to proritize and encode up to eight interrupt inputs. Figure 5 shows how the above cascade lines should be connected in such a single chip system.

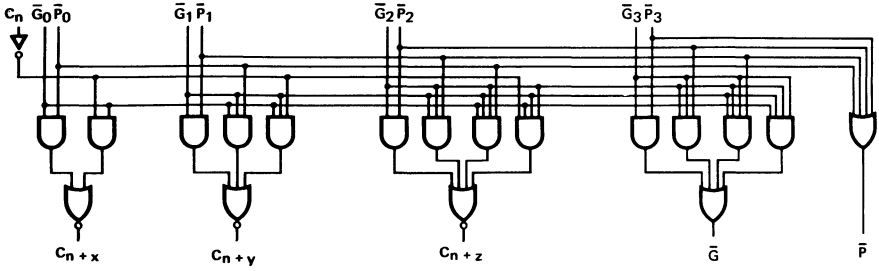
The Group Advance Receive and Group Enable inputs should be connected to ground so that the Lowest Group Enabled flip-flop is forced LOW during a *Master Clear* or *Load Status* microinstruction. Status Overflow should be connected to Interrupt Disable in order to disable interrupts when vector seven is read. The Group Advance Send, Ripple Disable, Group Signal and Parallel Disable pins should be left open.

The 2914 may be cascaded in either a Ripple Cascade Mode or a Parallel Cascade Mode. In the Ripple Cascade Mode, the Interrupt Disable signal, which disables lower priority interrupts, is allowed to ripple through lower priority groups. Figures 6, 9 and 11 show the cascade connections required for a ripple cascade 64 input interrupt system.

In the parallel cascade mode, a parallel lookahead scheme is employed using the high-speed 2902A Lookahead Carry Generator. Figures 7, 9 and 10 show the cascade connections required for a parallel cascade 64-input interrupt system. For this application, the 2902A is used as a lookahead interrupt disable generator. A Parallel Disable output from any group results in the disab'ing of all lower priority groups in parallel. Figure 8 shows the 2902A logic diagram and equations.

In Figures 9 and 10, the 2913 Priority Interrupt Expander is shown forming the high order bits of the vector and status, respectively. The 2913 is an eight-line to three-line priority encoder with three-state outputs which are enabled by the five output control signals G1, G2, $\overline{G3}$, $\overline{G4}$, and $\overline{G5}$. In Figure 9, the 2913 is connected so that its outputs are enabled during a Read Vector instruction, and in Figure 10 the 2913 is connected so that its outputs are enabled during a Read Status instruction. The 2913 logic diagram and truth table are shown in Figure 11.

The Am25LS138 three-line to eight-line Decoder also is shown in Figure 10. It is used to decode the three high order status bits during a Load Status instruction. The Am25LS138 logic diagram and truth table are shown in Figure 12.



$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

Figure 8. 2902A Carry Lookahead Generator Logic Diagram and Equations.

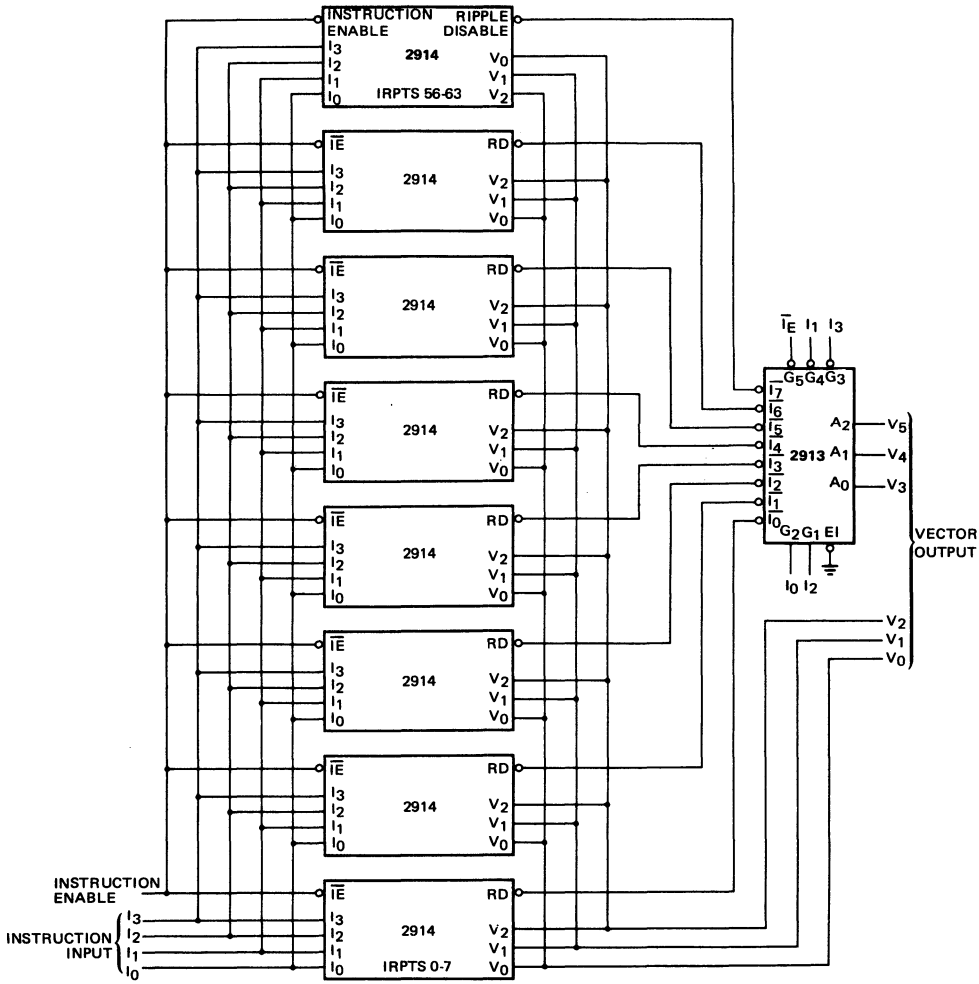


Figure 9. Vector Connections for both the Parallel and Ripple Cascade Modes.

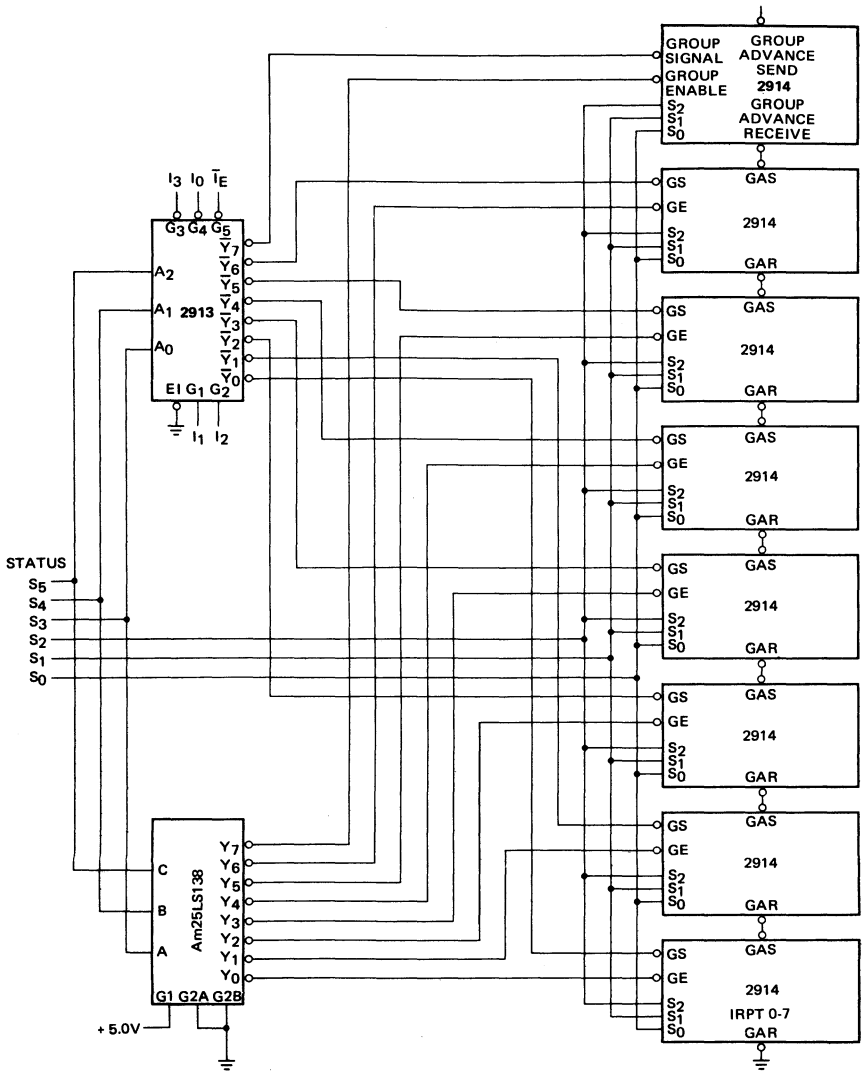
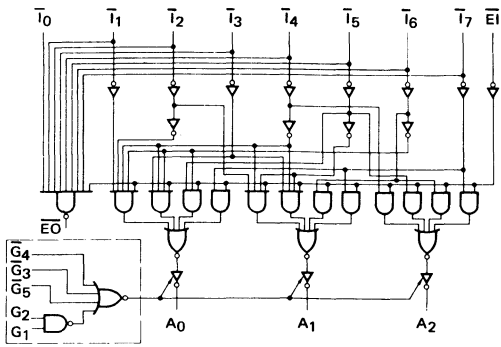


Figure 10. Group Signal, Group Enable, Group Advance Send, Group Advance Receive and Status Connections for Both the Parallel and Ripple Cascade Modes.



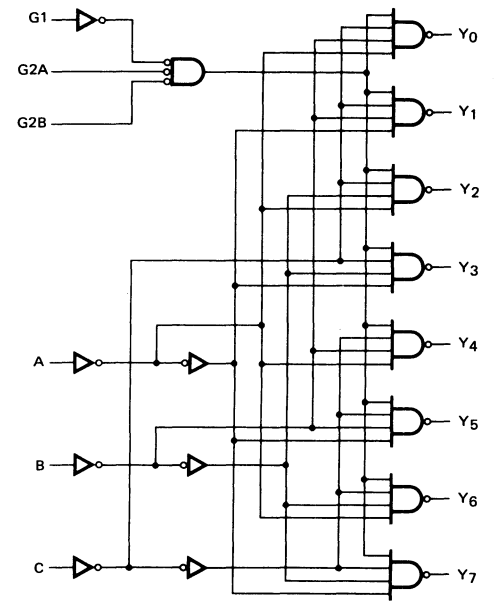
Inputs									Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care
For G1 = H, G2 = H,
G3 = L, G4 = L, G5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

Z = HIGH impedance

Figure 11. 2913 Priority Interrupt Expander Logic Diagram and Truth Table.



Inputs						Outputs							
Enable			Select										
G1	G2A	G2B	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't Care

Figure 12. Am25LS138 3 to 8 Line Decoder Logic Diagram and Truth Table.

EXAMPLE INTERRUPT SYSTEMS DESIGNS FOR A 2900 SYSTEM

A classical computer architecture is shown in Figure 13. The Computer Control Unit controls the internal busses and subsystems of the processor, synchronizes internal and external events and grants or denies permission to external systems. The data bus is commonly used by all of the subsystems in the computer. Information, instructions, address operands, data and sometimes control signals are transmitted down the data bus under control of a microprogram. The microprogram selects the source of the data as well as the destination(s) of the data. The Address Bus is typically used to select a word in memory for an internal computer function or to select an input/output port for an external subsystem or peripheral function. The source of the data for the address bus, also selected by microprogram commands, may be the program counter, the memory address register, a direct memory address controller, an interface controller, etc.

The arithmetic/logic unit (ALU) is that portion of the processor that computes. Under control of the microprogram, the ALU performs a number of different arithmetic and logic functions on data in the working registers or from the data bus. The ALU also provides a set of condition codes as a result of the current arithmetic or logic operation. The condition codes, along with other computer status information, are stored in a register for later use by the programmer or computer control unit.

The program counter and the memory address register are the two main sources of memory word and I/O address select data on the address bus. The program counter contains the address of the next instruction or instruction operand that is to be fetched from main memory, and the memory address register contains instruction address operands which are necessary to fetch the data required for the execution of the current instruction.

A subroutine address stack is provided to allow the return address linkage to be handled easily when exiting a subroutine. The address stack is a last-in, first-out stack that is controlled by a jump-to-subroutine, PUSH, or a return-from-subroutine, POP, instruction from the CCU microinstruction word.

The next microprogram address control (NMAC) circuitry controls the generation of microinstruction addresses. Based on microprogram control, interrupt requests, test conditions and commands from a control panel or other processor, the NMAC determines the address of the next microinstruction to be executed.

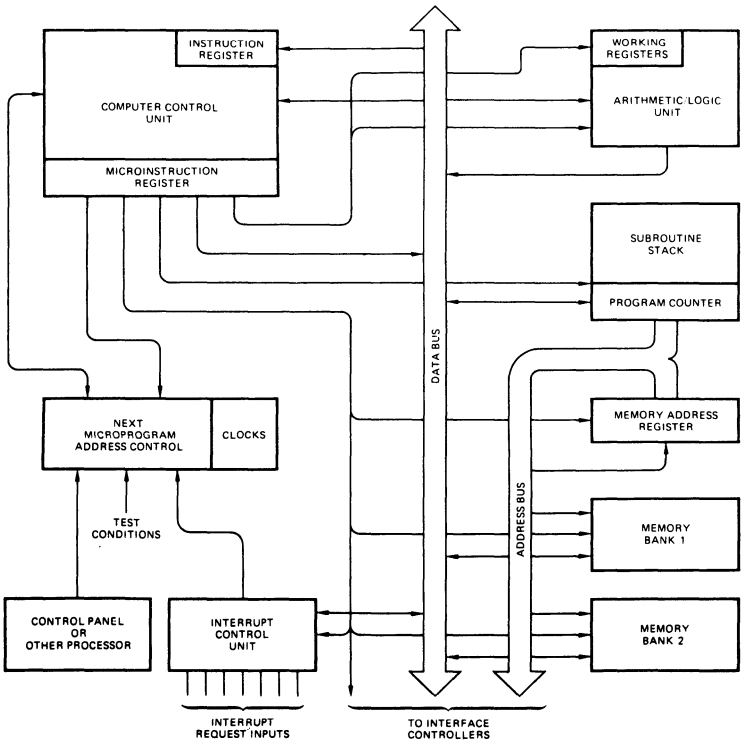


Figure 13. Generalized Computer Architecture.

TS2914 PRIORITY INTERRUPT ENCODER DETAILED LOGIC DESCRIPTION

INTRODUCTION

A clear understanding of the 2914 Priority Interrupt controller's operation facilitates its efficient use. With that idea in mind, a detailed logic description of the 2914 is presented here. A detailed logic diagram and control signal truth table are shown, and significant aspects of the 2914 design are described verbally.

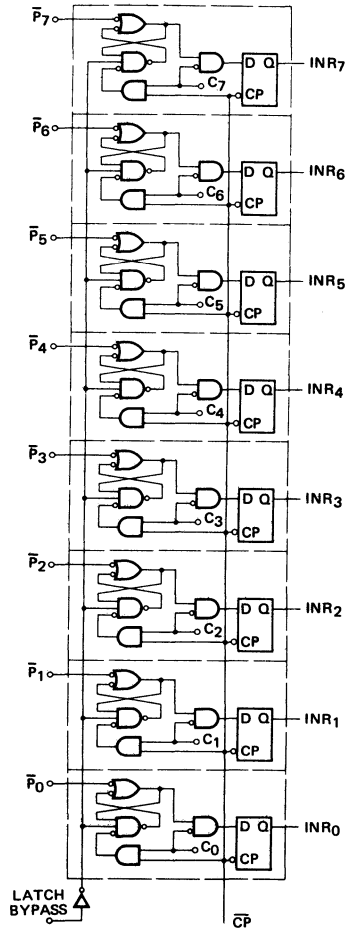


Figure 1. Interrupt Latches and Register.

LOGIC DIAGRAM DESCRIPTION

The Interrupt Latches and Register are shown in Figure 1. The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent. The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register. It is updated on the LOW-to-HIGH transition of the clock pulse (HIGH-to-LOW transition of the $\overline{CP}$ signal) as are all of the flip-flops on the chip.

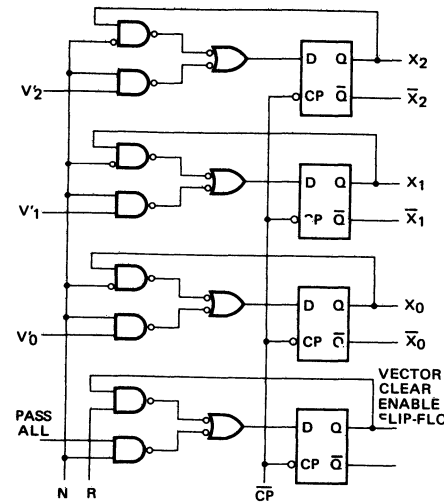


Figure 2. Vector Hold Register

When a Read Vector instruction is executed, the binary coded vector is loaded into the Vector Hold Register of Figure 2. This stored vector can be used later for clearing the interrupt associated with the last vector that was read. The Vector Clear Enable Flip-Flop of Figure 2 is set when a Read Vector instruction is executed and the PASS ALL signal is HIGH. A HIGH PASS ALL signal level indicates that this group is enabled and that an interrupt request in this group was detected and passed priority. The Vector Hold Register and the Vector Clear Enable Flip-Flop are cleared when a Master Clear, Clear All Interrupts, or Clear Interrupt Last Vector Read is executed. Table 1 shows the generation of the "N and R" control signals for each of these operations.

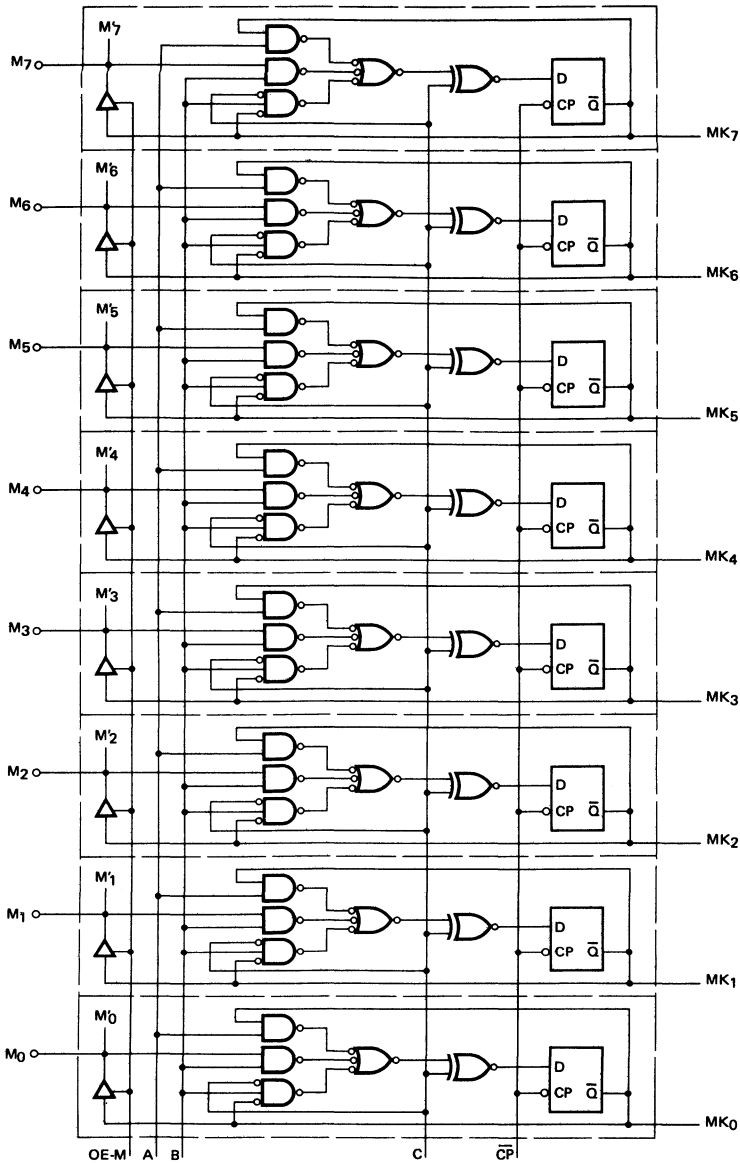


Figure 3. Mask Register.

The Mask Register shown in Figure 3 holds the eight mask bits associated with the eight interrupt levels. The register may be set or cleared, bit set or bit cleared from the "M" bus, or loaded or read to the "M" bus. Table 1 shows the generation of the "A", "B", "C" and "OE-M" control signals for each of these operations.

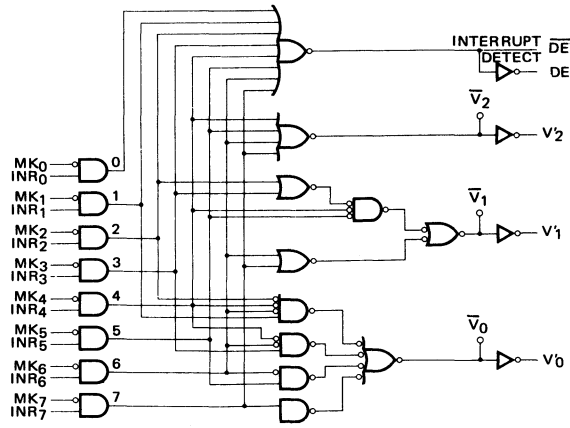


Figure 4. Interrupt Request Detect and Priority Decoder.

The Interrupt Request Detect and Priority Encode circuitry are shown in Figure 4. The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector, V_0-V_2.

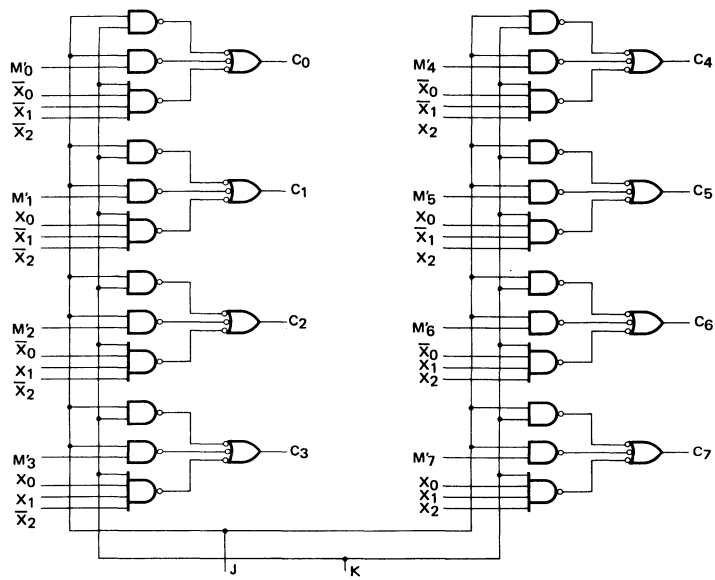


Figure 5. Clear Control.

The Clear Control logic of Figure 5 generates the eight individual clear signals for the eight Interrupt Register bits. Under microinstruction control, all interrupts, interrupts with corresponding mask register bits set, interrupts with corresponding mask bus bits equal to one, or the interrupt associated with the last vector read may be cleared. Table 1 shows the generation of the "J" and "K" control signals for each of these operations.

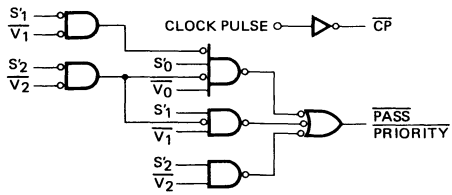


Figure 6. Three-Bit comparator.

The three-bit Comparator of Figure 6 compares the interrupt vector with the contents of the Status Register. A LOW signal level at the PASS PRIORITY output indicates that the interrupt vector is greater than or equal to the contents of the Status Register.

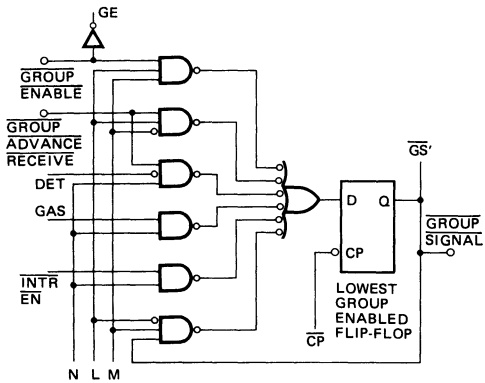


Figure 7. Group Enable Logic.

The Lowest Group Enabled Flip-Flop, Figure 7, is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the group which contains the lowest priority interrupt which will be accepted and is used to form the high order status bits. When a Load Status instruction is executed, the flip-flop is loaded from the GROUP ENABLE input. When a Master Clear instruction is executed, it is loaded from the GROUP ADVANCE RECEIVE input. The flip-flop is set HIGH when a Read Vector instruction is executed if a Group Advance is not received and no interrupt in this group is detected, if a Group Advance is sent from this group, or if interrupts from this group are disabled. For all other instructions, the flip-flop remains the same. Table 1 shows the generation of the "N", "L" and "M" control signals for these operations.

The Status Register holds the status bits and may be loaded from or read to the "S" bus as shown in Figure 8. Note that when a Load Status instruction is executed, status from the "S" bus is loaded into the Status Register only if the $\overline{\text{GROUP ENABLE}}$ input is LOW; if the $\overline{\text{GROUP ENABLE}}$ input is HIGH, the Status Register is cleared. Also note that during a Read Status instruction, the Status Register outputs are enabled onto the "S" bus only if the Lowest Group Enabled Flip-Flop of this group is LOW. When a Read Vector instruction is executed, the incrementer increases the vector by one and the result is loaded into the Status Register. Thus, the Status Register always points to the lowest level at which an interrupt will be accepted. Table 1 shows the generation of the "F", "G" and "$\overline{\text{OE-S}}$" control signals for Status Register operations.

The Interrupt Request Logic, shown in Figure 9, generates the $\overline{\text{RIPPLE DISABLE}}$, PARALLEL DISABLE, $\overline{\text{INTERRUPT REQUEST}}$, GROUP ADVANCE SEND, and $\overline{\text{STATUS OVERFLOW}}$ output signals. The PARALLEL DISABLE signal is generated when the Lowest Group Enabled signal is LOW or an interrupt request in this group is detected and passes priority. The $\overline{\text{RIPPLE DISABLE}}$ signal is generated when the PARALLEL DISABLE signal is generated and also when the $\overline{\text{INTERRUPT DISABLE}}$ input signal is LOW. The $\overline{\text{INTERRUPT REQUEST}}$ output signal is generated when interrupt requests in this group are enabled and a request is detected and passes priority. The $\overline{\text{GROUP ADVANCE SEND}}$ output signal is generated when a vector of value seven is being read. The Status Overflow Flip-Flop is set LOW when a vector of value seven is read and indicates the Status Register has overflowed. The Interrupt Request Enable Flip-Flop is either set or reset by the Enable Request or Disable Request microinstructions respectively, and is used to enable or disable the $\overline{\text{INTERRUPT REQUEST}}$ output. Table 1 shows the generation of control signals "D", "E", "S" and "H".

Note that the vector outputs are enabled only when a Read Vector is being executed. Also note that when a Read Vector instruction is executed, the vector outputs will be disabled after the execution of the instruction since the Status Register is loaded with V+1, and the $\overline{\text{INTERRUPT REQUEST}}$ will no longer be generated.

The Microinstruction Decode circuitry, Figure 10, decodes the 2914 microinstructions and generates the required internal control signals. Table 1 shows the truth table for these functions and Figure 11 shows the function tables.

Table 1. 2914 Control Signal Truth Table.
0 = LOW, 1 = HIGH

Microinstruction						Function	Mask Register				Status Register			Group Enable		Clear Control		Irpt Request Enable		Vector Hold Register		Other	
Decimal	$\overline{I_E}$	I_3	I_2	I_1	I_0	Description	A	B	C	OE-M	F	G	$\overline{OE\text{-}S}$	L	M	J	K	D	E	N	R	S	H
0	0	0	0	0	0	Master Clear	0	0	1	0	0	0	1	1	0	1	1	0	1	0	0	1	1
1	0	0	0	0	1	Clear All Interrupts	1	0	1	0	0	1	1	0	1	1	1	1	X	0	0	1	0
2	0	0	0	1	0	Clear Intr Via M Bus	1	0	1	0	0	1	1	0	1	1	0	1	X	0	1	1	0
3	0	0	0	1	1	Clear Intr Via M Reg	1	0	1	1	0	1	1	0	1	1	0	1	X	0	1	1	0
4	0	0	1	0	0	Clear Intr, Last Vector	1	0	1	0	0	1	1	0	1	0	1/0	1	X	0	0	1	0
5	0	0	1	0	1	Read Vector	1	0	1	0	0/1	0	1	0	0	0	0	1	X	1	0	0	1
6	0	0	1	1	0	Read Status Reg	1	0	1	0	0	1	0	0	1	0	0	1	X	0	1	1	0
7	0	0	1	1	1	Read Mask Reg	1	0	1	1	0	1	1	0	1	0	0	1	X	0	1	1	0
8	0	1	0	0	0	Set Mask Reg	0	0	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
9	0	1	0	0	1	Load Status Reg	1	0	1	0	1	1	1	1	1	0	0	1	X	0	1	1	1
10	0	1	0	1	0	Bit Clear Mask Reg	0	1	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
11	0	1	0	1	1	Bit Set Mask Reg	1	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
12	0	1	1	0	0	Clear Mask Reg	0	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
13	0	1	1	0	1	Disable Request	1	0	1	0	0	1	1	0	1	0	0	0	0	0	1	1	0
14	0	1	1	1	0	Load Mask Reg	0	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
15	0	1	1	1	1	Enable Request	1	0	1	0	0	1	1	0	1	0	0	0	1	0	1	1	0
X	1	X	X	X	X	Instruction Disable	1	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0

Notes : 1. Control line "F" during "READ VECTOR" instruction is 0 when "PASS ALL" is LOW and 1 when "PASS ALL' is HIGH.
2. Control line "K"during "Clear Intr, Last Vector" instruction is 0 when "Vector Clear Enable" is LOW and 1 when "Vector Clear Enable" is HIGH.

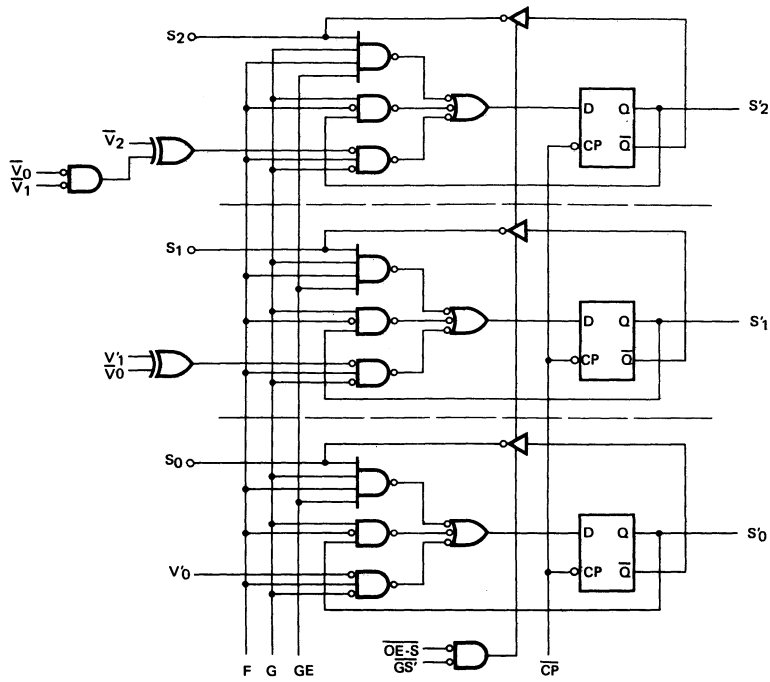


Figure 8. Incrementer and Status Register.

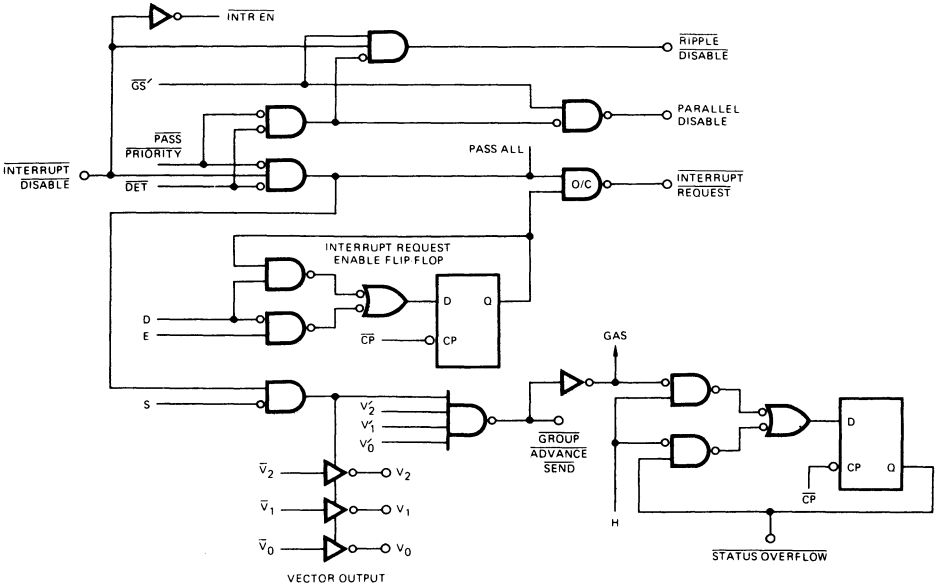


Figure 9. Interrupt Request Logic.

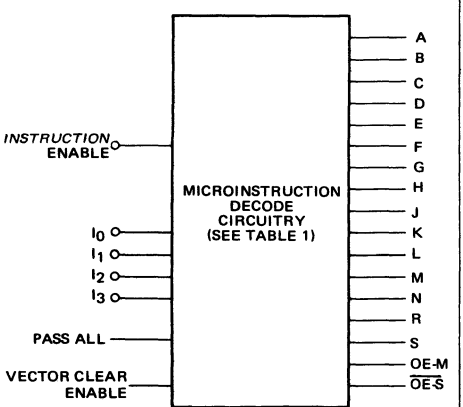


Figure 10.

MASK REGISTER

A	B	C	FUNCTION
0	0	0	SET
0	0	1	CLEAR
0	1	0	BIT CLEAR
0	1	1	LOAD
1	0	1	HOLD
1	1	1	BIT SET

CLEAR CONTROL

J	K	FUNCTION
0	0	NO CLEAR
0	1	CLEAR IRPT. VECTOR
1	0	CLEAR IRPTS VIA M
1	1	CLEAR ALL IRPTS

VECTOR HOLD REGISTER

N	FUNCTION
0	HOLD
1	LOAD

LOWEST GROUP ENABLED FLIP-FLOP

L	M	FUNCTION
0	0	UPDATE
0	1	HOLD
1	0	LOAD VIA GROUP ADVANCE RECEIVE
1	1	LOAD VIA GROUP ENABLE

STATUS REGISTER

F	G	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD VECTOR + 1
1	1	LOAD VIA "S" BUS

INTERRUPT REQUEST ENABLE FLIP-FLOP

D	E	FUNCTION
0	0	DISABLE IRPTS
0	1	ENABLE IRPTS
1	X	HOLD

VECTOR CLEAR ENABLE FLIP-FLOP

N	R	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD

STATUS OVERFLOW FLIP-FLOP

H	FUNCTION
0	HOLD
1	LOAD

Figure 11. Control Function Tables.

ORDERING INFORMATION

TS2914 | M | J | B/B

- TS2914: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

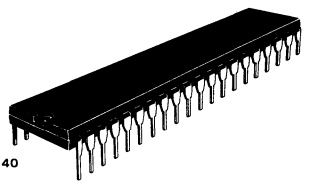
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2914	●		●	●			●	●		
		●		●	●	●	●		●	●

Examples : TS2914CP, TS2914CP-D, TS2914CJ, TS2914CJ-D
TS2914MJ, TS2914MJG/B, TS2914MJB/B,...

Oper. temp. : **C** : 0°C to + 70°C, **M** : – 55°C to + 125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

CASE CB-182

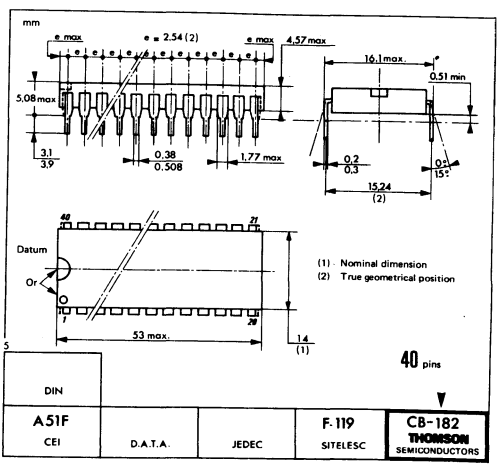


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTEURS

TS2915A

QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

The TS2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

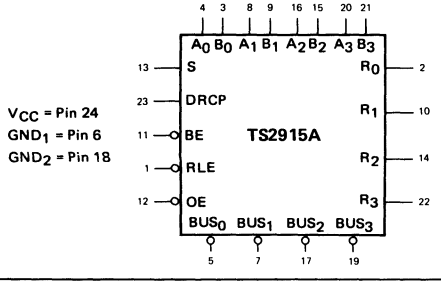
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48 mA at 0.5 V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

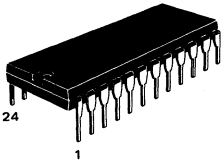
- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48 mA at 0.5 V max
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 3.5 V minimum output high voltage for direct interface to MOS microprocessors.

LOGIC SYMBOL



QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

CASE CB-68



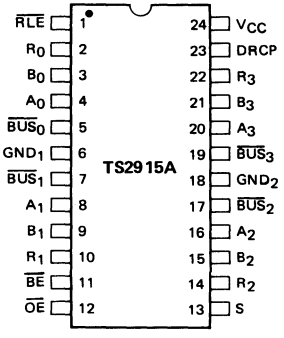
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX	E SUFFIX
CERDIP PACKAGE	CHIP-CARRIER

Hi-Rel versions available - See chapter 4

PIN ASSIGNMENT



Ref. 01270-R1

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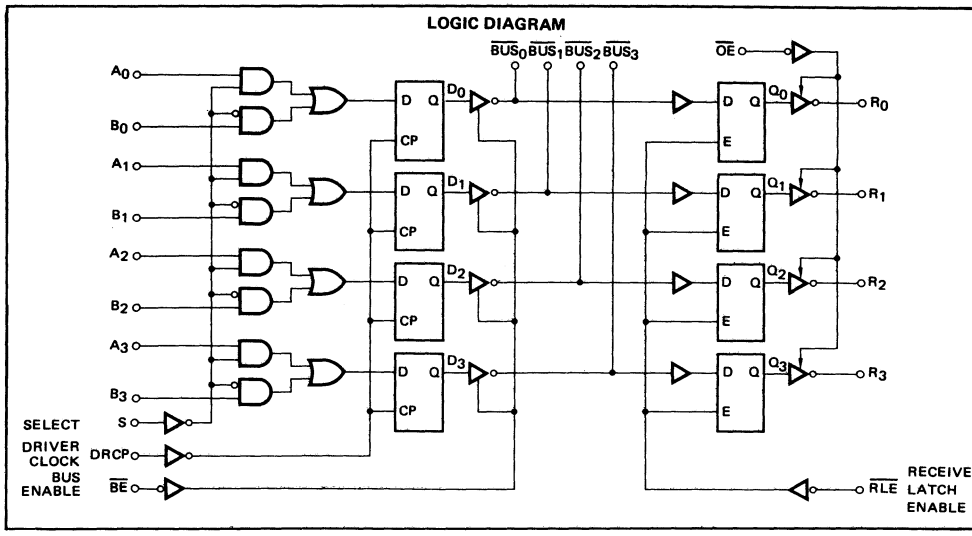
THOMSON COMPONENTS



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted :

C SUFFIX $T_A = 0°C$ to $+70°C$ V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
M SUFFIX $T_A = -55°C$ to $+125°C$ V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted :

C SUFFIX $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
M SUFFIX $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

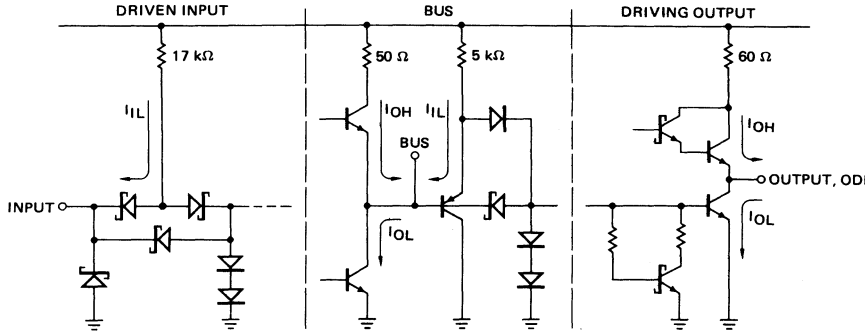
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		$V_{CC} = 5.0$V, $I_{OH} = -100\mu$A		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0$mA		0.27	0.4	Volts
			$I_{OL} = 8.0$mA		0.32	0.45	
			$I_{OL} = 12$mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0$V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$V			50	μA
			$V_O = 0.4$V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	M SUFFIX Min.	M SUFFIX Typ. (Note 2)	M SUFFIX Max.	C SUFFIX Min.	C SUFFIX Typ. (Note 2)	C SUFFIX Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	C_L = 15pF R_L = 2.0kΩ	15			12			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output	C_L = 5pF, R_L = 2.0kΩ		14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

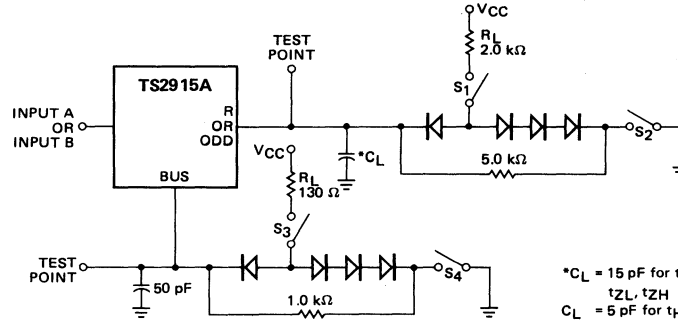
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

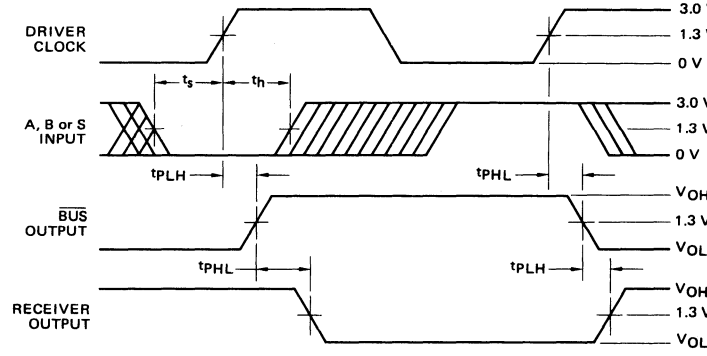


Note : Actual current flow direction shown.

SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



Note . Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

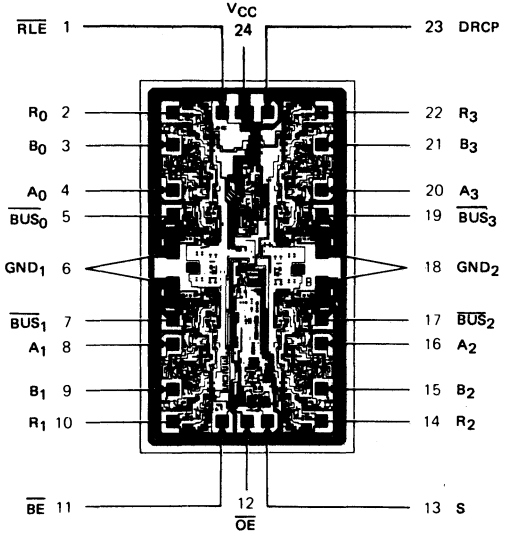
$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

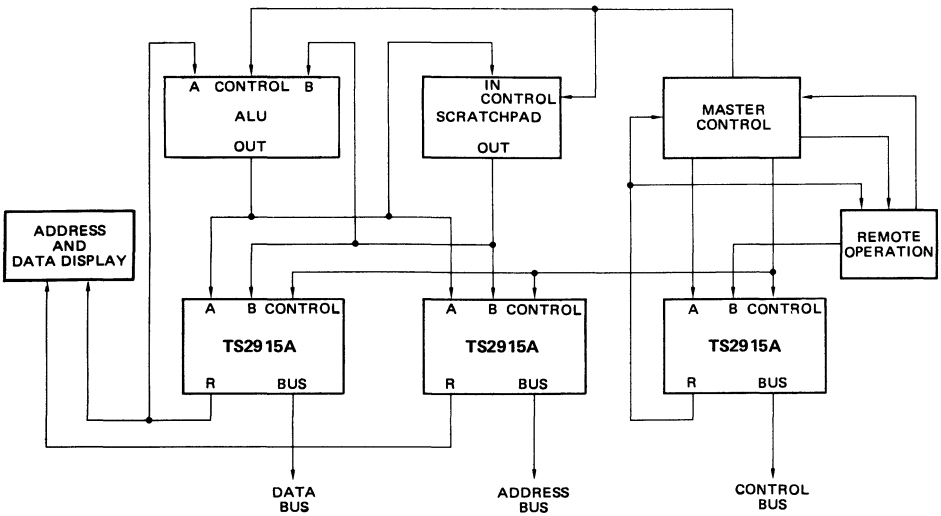
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

Metallization and Pad Layout



Die size : 2.020 x 3.440 mm

APPLICATIONS



The TS2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

ORDERING INFORMATION

TS2915A | M | J | B/B

- TS2915A: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

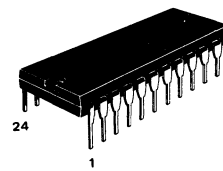
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2915A	●		●	●			●	●		
		●	●	●	●	●	●		●	●

Examples :TS2915ACP, TS2915ACP-D, TS2915ACJ, TS2915ACJ-D
TS2915AMJ, TS2915AMJG/B, TS2915AMJB/B,...

Oper. temp. : **C** : 0°C to + 70°C, **M** : −55°C to +125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

CASE CB-68

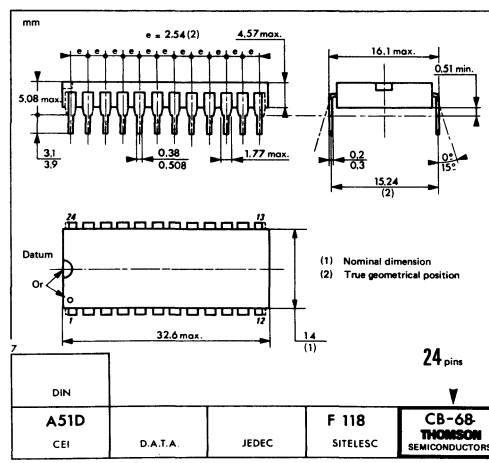


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP-CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTEURS

TS2917A

QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

The TS2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48 mA at 0.5 V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

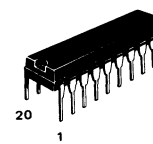
Data from the A input is inverted at the BUS output. Like-wise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The TS2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- *D-type register on driver*
- Bus driver output can sink 48 mA at 0.5 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 3.5 V minimum output high voltage for direct interface to MOS microprocessors.

QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

CASE CB-194



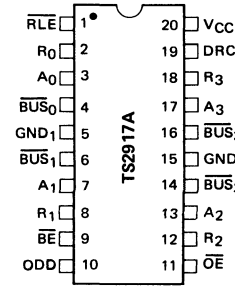
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX	E SUFFIX
CERDIP PACKAGE	CHIP CARRIER

Hi-Rel versions available - See chapter 4

PIN ASSIGNMENT



Ref. 01275-R1

THOMSON SEMICONDUCTEURS
Sales headquarters
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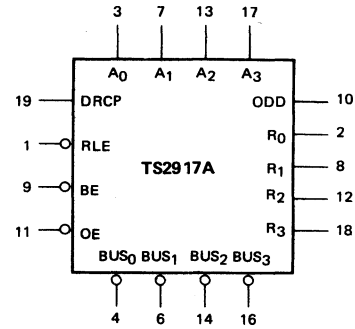
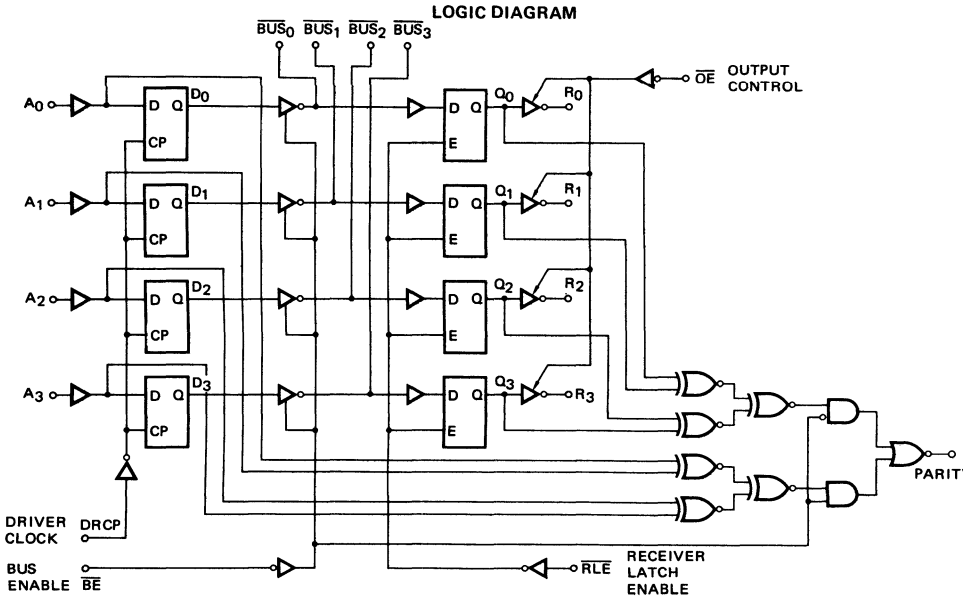
THOMSON COMPONENTS

LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

C SUFFIX (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
M SUFFIX (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 48 mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20 mA	2.4			Volts
			MIL, I_{OH} = −15 mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5 V, V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX., V_O = 0 V		−50	−120	−225	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: I_{OH} = −1.0 mA	2.4	3.4		Volts
			COM'L: I_{OH} = −2.6 mA	2.4	3.4		
		V_{CC} = 5.0 V, I_{OH} = −100 μA		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −660 μA, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	*Input Clamp* Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

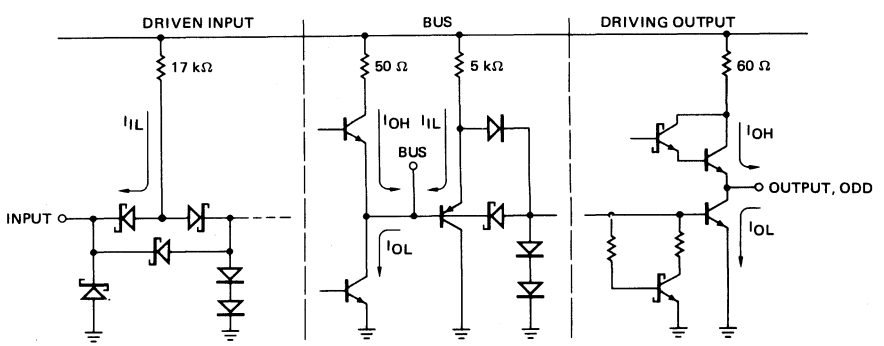
C SUFFIX	(COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC} MIN. = 4.75 V	V_{CC} MAX. = 5.25 V
M SUFFIX	(MIL)	$T_A = -55°C$ to $+125°C$	V_{CC} MIN. = 4.50 V	V_{CC} MAX. = 5.50 V

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	M SUFFIX Min.	M SUFFIX Typ. (Note 2)	M SUFFIX Max.	C SUFFIX Min.	C SUFFIX Typ. (Note 2)	C SUFFIX Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	A Data Inputs	C_L = 15pF, R_L = 2.0kΩ	15			12			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		C_L = 5pF, R_L = 2.0kΩ		14	26		14	23	

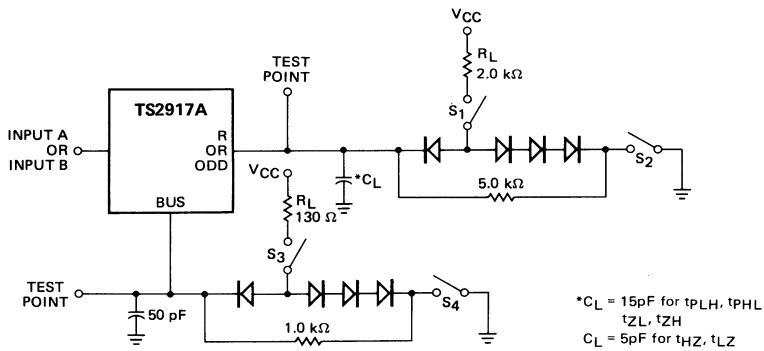
Notes :
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25° C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

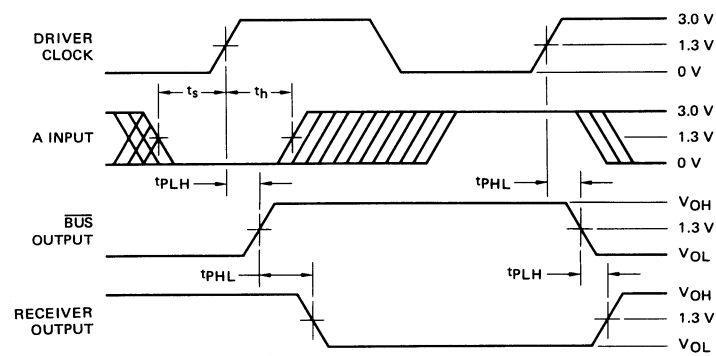


Note : Actual current flow direction shown.

SWITCHING TEST CIRCUIT

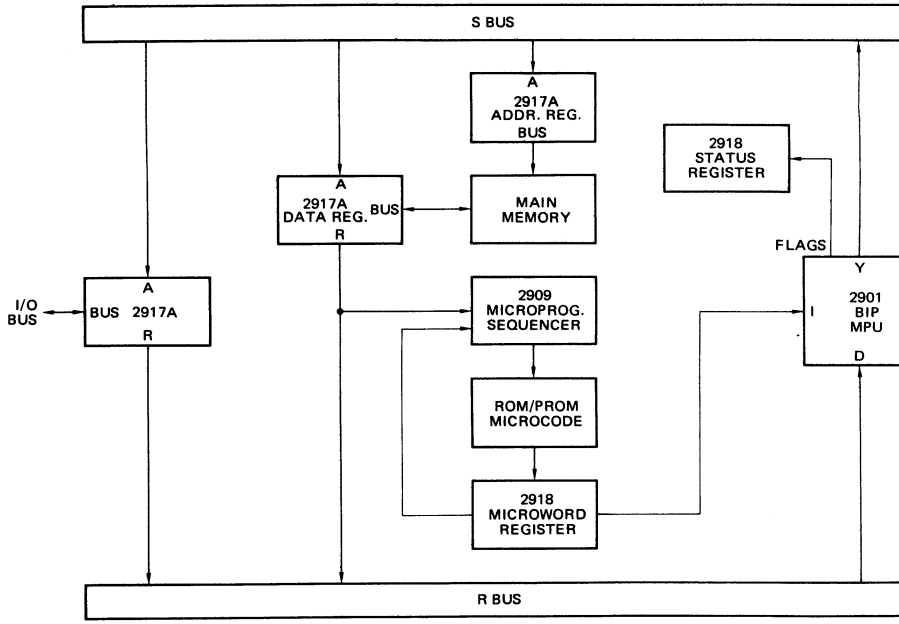


SWITCHING WAVEFORMS



Note : Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

APPLICATIONS



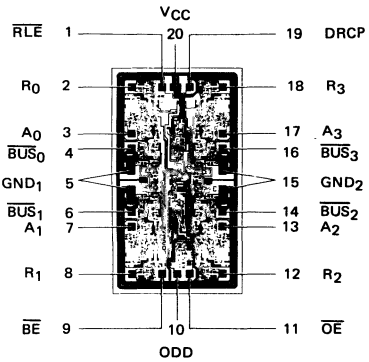
The TS2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high speed Microprocessor Systems.

FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



Die size : 1.880 x 3.300 mm

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

ORDERING INFORMATION

TS2917A | M | J | B/B

- TS2917A: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

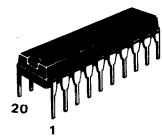
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2917A	●		●	●			●	●		
		●		●	●	●	●		●	●

Examples :TS2917ACP, TS2917ACP-D, TS2917ACJ, TS2917ACJ-D
TS2917AMJ, TS2917AMJG/B, TS2917AMJB/B,...

Oper. temp. : **C** : 0°C to + 70°C, **M** : –55°C to +125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

CASE CB-194

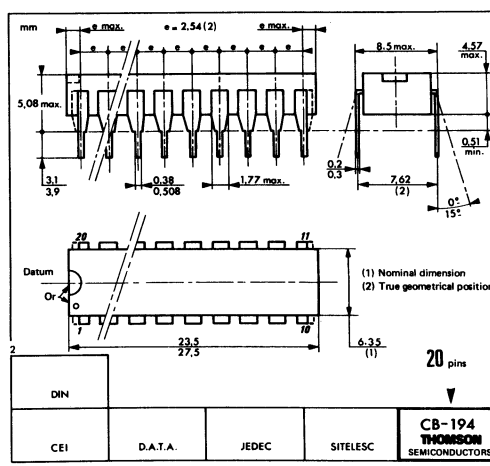


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

THOMSON SEMICONDUCTEURS

TS2918

QUAD D REGISTER WITH STANDARD AND THREE-STATE OUTPUTS

New Schottky circuits such as the TS2918 register provide the design engineer with additional flexibility in system configuration – especially with regard to bus structure, organization and speed. The TS2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

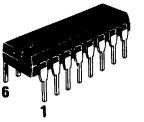
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The TS2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the TS2918 register. Other applications of TS2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency.

QUAD D REGISTER WITH STANDARD AND THREE-STATE OUTPUTS

CASE CB-79



P SUFFIX
PLASTIC PACKAGE

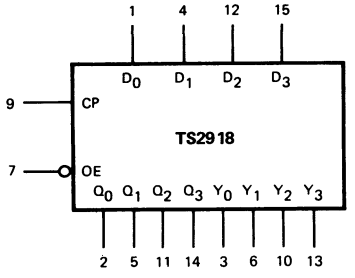
ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER

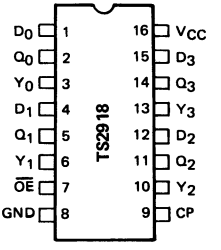
Hi-Rel versions available - See chapter 4

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN ASSIGNMENT



Ref.01280

THOMSON SEMICONDUCTEURS
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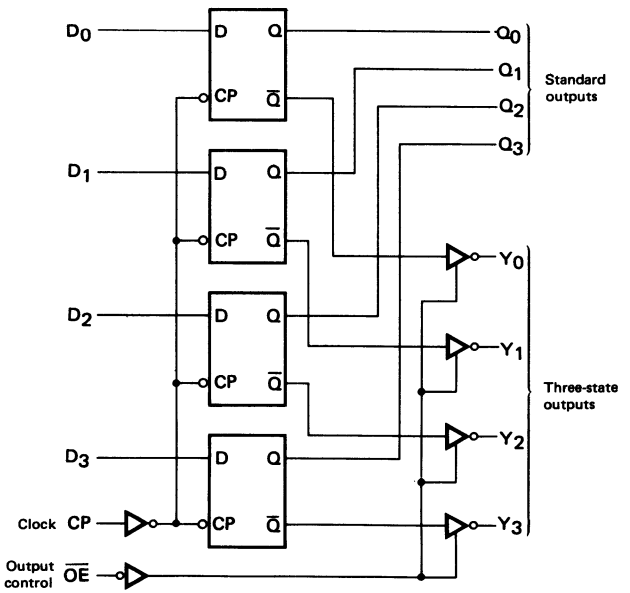
Tel. : (1) 39.46.97.19 / Telex : 204780F

THOMSON COMPONENTS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

C SUFFIX $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (COM'L) MIN. = 4.75V MAX. = 5.25V
M SUFFIX $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q	$I_{OH} = -1mA$ MIL	2.5	3.4		Volts
				$I_{OH} = -1mA$ COM'L	2.7	3.4		
			Y	XM, $I_{OH} = -2mA$	2.4	3.4		
				XC, $I_{OH} = -6.5mA$	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., $I_{OL} = 20mA$ $V_{IN} = V_{IH}$ or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.5V$					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5V$					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		$V_O = 2.4V$			50	µA
				$V_O = 0.4V$			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, $T_A = 25°C$ ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics ($T_A = +25°C$, $V_{CC} = 5.0V$, $R_L = 280\Omega$)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)				6.0	9.0	ns
t_{PHL}					8.5	13	
t_{ZH}	Output Control to Output		C_L = 15 pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0 pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

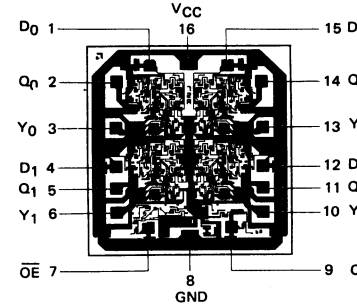
Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

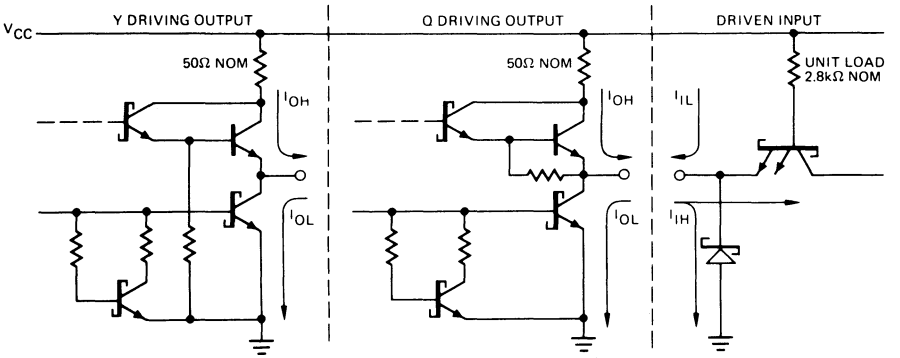
$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

METALLIZATION AND PAD LAYOUT



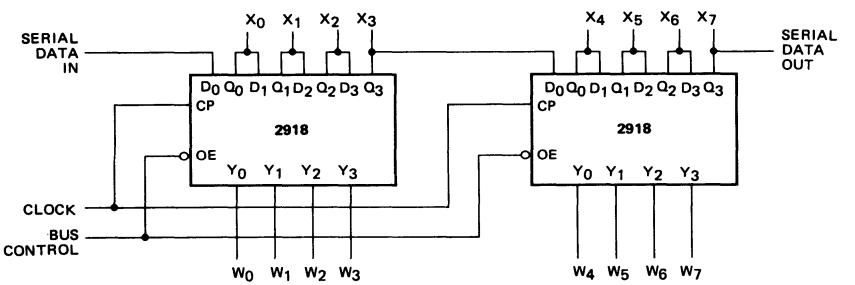
Die size : 2.010 x 1.960 mm

SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS



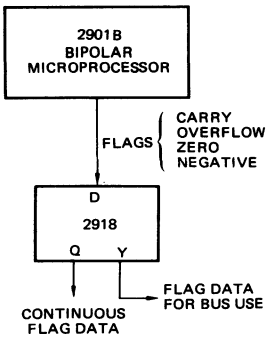
Note : Actual current flow direction shown.

APPLICATIONS

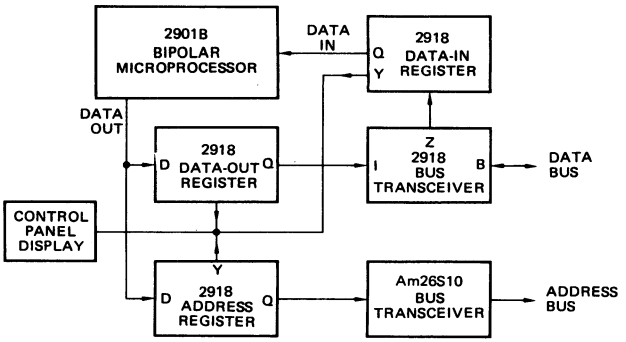


8-bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

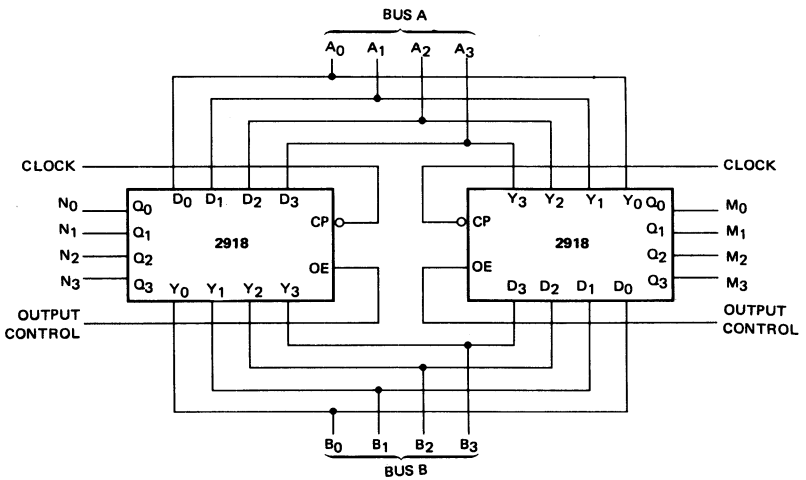
APPLICATIONS



The TS2918 as a 4-bit status register.



The TS2918 used as data-in, data-out and address registers.



The TS2918 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.

ORDERING INFORMATION

TS2918 | M | J | B/B

- TS2918: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

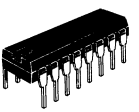
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2918	●		●	●			●	●		
		●		●	●	●	●		●	●

Examples : TS2918CP, TS2918CP-D, TS2918CJ, TS2918CJ-D
TS2918MJ, TS2918MJG/B, TS2918MJB/B,...

Oper. temp. : **C** : 0°C to + 70°C, **M** : – 55°C to + 125°C.
Package : **P** : Plastic DIL, **J** : Cerdip DIL, **C** : Ceramic DIL, **E** : Ceramic LCC.
Screening classes : **Std** (no end-suffix), **–D** : NFC 96883 level D.
G/B : NFC 96883 level G, **B/B** : MIL-STD-883 level B and NFC 96883 level B.

CASE CB-79

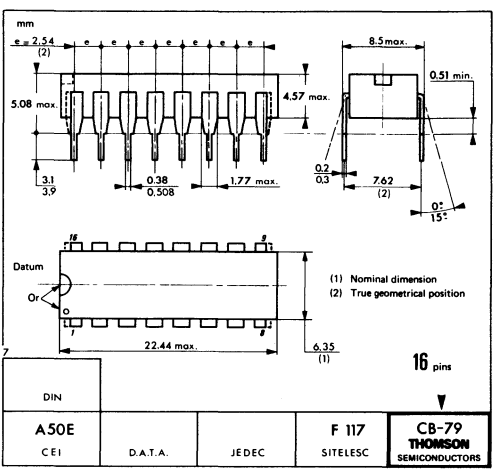


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

NOTES

THOMSON SEMICONDUCTEURS

TS2919

QUAD REGISTER WITH DUAL THREE-STATE OUTPUTS

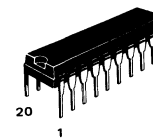
The TS2919 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The TS2919 is packaged in a space-saving 20-pin package.

- Two sets of three-state outputs
- Four D-type flip-flops
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs.

QUAD REGISTER WITH DUAL THREE-STATE OUTPUTS

CASE CB-194



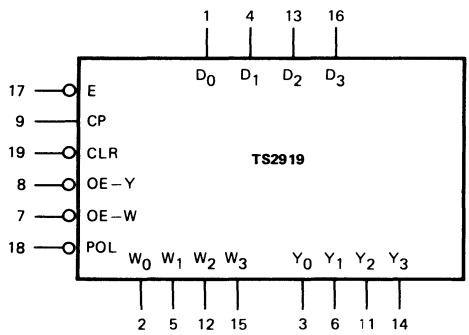
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

J SUFFIX	E SUFFIX
CERDIP PACKAGE	CHIP CARRIER

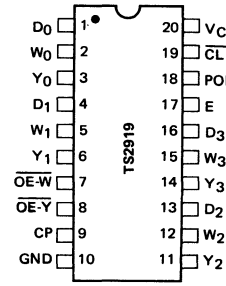
Hi-Rel versions available - See chapter 4

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

PIN ASSIGNMENT



Ref. 01285 R-1

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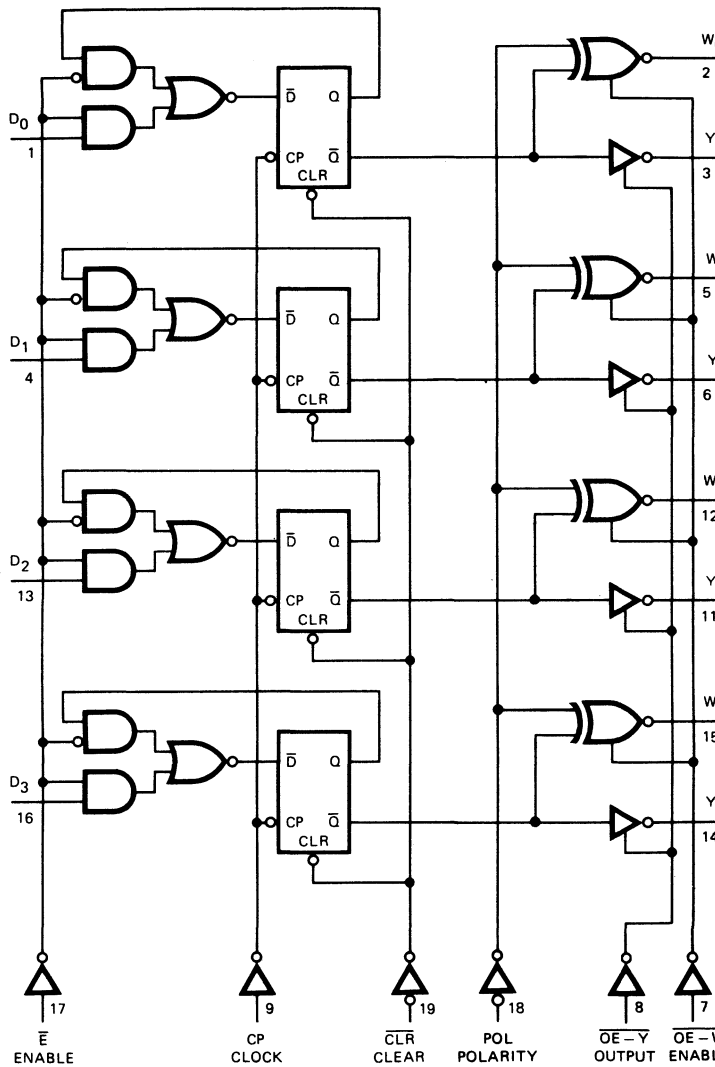
THOMSON COMPONENTS

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0\,V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\,V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4\,V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7\,V$				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0\,V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4\,V$			−20	µA
			$V_O = 2.4\,V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		-15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.	MIL		24	36	mA
			COM'L		24	39	

Notes :
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0\,V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded ; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

FUNCTION TABLE

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE\text{-}W}$	$\overline{OE\text{-}Y}$	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L = LOW H = HIGH Z = High Impedance NC = No Change X = Don't Care ↑ = LOW-to-HIGH Transition

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

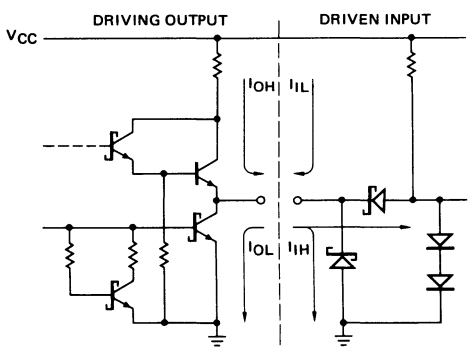
Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PHL}	Clock to Y_i			22	33	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}				20	30		
t_{PLH}	Clock to W_i (Either Polarity)			24	36	ns	
t_{PHL}				24	36		
t_{PHL}	Clear to Y_i			29	43	ns	
t_{PLH}	Clear to W_i			25	37	ns	
t_{PHL}				30	45		
t_{PLH}	Polarity to W_i			23	34	ns	
t_{PHL}				25	37		
t_{pw}	Clear		18			ns	
t_{pw}	Clock Pulse Width	LOW	15			ns	
		HIGH	18				
t_s	Data		15			ns	
t_h	Data		5			ns	
t_s	Data Enable		20			ns	
t_h	Data Enable		0			ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		20	15		ns	
t_{ZH}	Output Enable to W or Y			11	17	ns	
t_{ZL}				13	20		
t_{HZ}	Output Enable to W or Y			13	20	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}				11	17		
f_{max}	Maximum Clock Frequency (Note 1)		35	45		MHz	C_L = 15pF R_L = 2.0kΩ

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

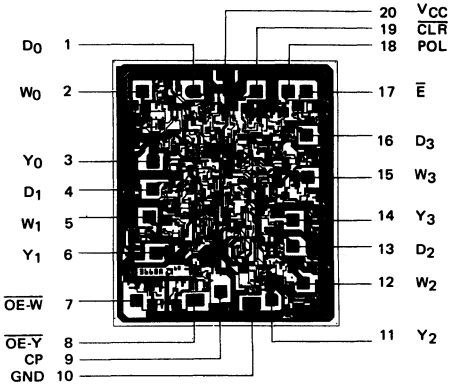
Parameters	Description		TS2919CP, CJ T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	TS2919CP, CJ Max.	TS2919 MJ, ME T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	TS2919 MJ, ME Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i			39		42	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}				39		45		
t_{PLH}	Clock to W_i (Either Polarity)			41		43	ns	
t_{PHL}				44		48		
t_{PHL}	Clear to Y_i			52		58	ns	
t_{PLH}	Clear to W_i			42		43	ns	
t_{PHL}				51		53		
t_{PLH}	Polarity to W_i			41		45	ns	
t_{PHL}				42		44		
t_{pw}	Clear		20		20		ns	
t_{pw}	Clock	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		10		10		ns	
t_s	Data Enable		25		25		ns	
t_h	Data Enable		0		0		ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		23		24		ns	
t_{ZH}	Output Enable to W_i or Y_i			24		27	ns	
t_{ZL}				29		35		
t_{HZ}	Output Enable to W_i or Y_i			33		45	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}				22		26		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	C_L = 50pF R_L = 2.0kΩ

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



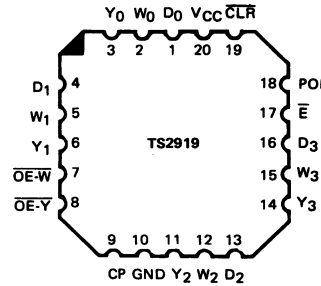
Note : Actual current flow direction shown.

METALLIZATION AND PAD LAYOUT



Die size : 2.515 x 2.108 mm

CHIP CARRIER



DEFINITION OF FUNCTIONAL TERMS

D_i — Any of the four D flip-flop data lines.

$\overline{E}$ — Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.

CP — Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.

$\overline{OE\text{-}W}$, $\overline{OE\text{-}Y}$ — Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE\text{-}W}$ controls the W set of outputs, and $\overline{OE\text{-}Y}$ controls the Y set.

Y_i — Any of the four non-inverting three-state output lines.

W_i — Any of the four three-state outputs with polarity control.

POL — Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.

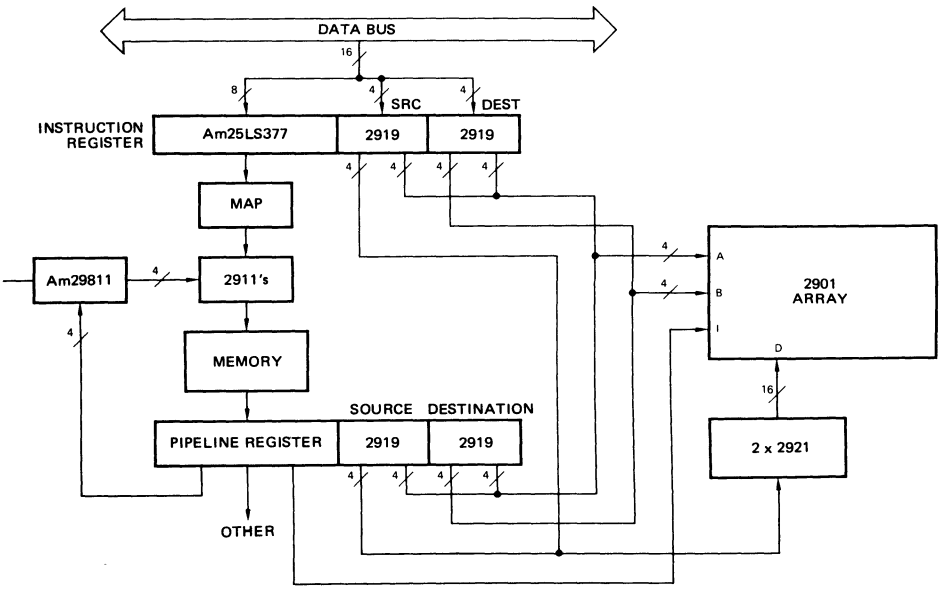
$\overline{CLR}$ — Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

		Input	Output HIGH		Output LOW	
Pin No.'s	Input/Output	Load	MIL	COM'L	MIL	COM'L
1	D_0	1.0	–	–	–	–
2	W_0	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	D_1	1.0	–	–	–	–
5	W_1	–	50	130	33	33
6	Y_1	–	50	130	33	33
7	$\overline{OE\text{-}W}$	1.0	–	–	–	–
8	$\overline{OE\text{-}Y}$	1.0	–	–	–	–
9	CP	1.0	–	–	–	–
10	GND	–	–	–	–	–
11	Y_2		50	130	33	33
12	W_2		50	130	33	33
13	D_2	1.0	–	–	–	–
14	Y_3	–	50	130	33	33
15	W_3	–	50	130	33	33
16	D_3	1.0	–	–	–	–
17	$\overline{E}$	1.0	–	–	–	–
18	POL	1.0	–	–	–	–
19	$\overline{CLR}$	1.0	–	–	–	–
20	V_{CC}	–	–	–	–	–

APPLICATION



The 2919 provides for easy control of the selection of source and destination register addresses for the 2901. These controls can emanate from both the instruction register and the pipeline register. The control is accomplished by three-state action at the 2919 outputs. Four different register outputs can be selected by the B address which is the destination register in the 2901. Two registers can be selected for the 2901 A input which is a second RAM source.

The other pair of three-state outputs can be used for function control select as shown with the 2921. Here, bit set, bit clear, bit toggle and bit test on any of the 16 bits can be performed.

ORDERING INFORMATION

TS2919 | M | J | B/B

- TS2919: Part number
- M: Oper. temp.
- J: Package
- B/B: Screening class

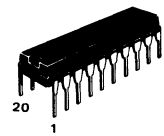
The table below horizontally shows all available suffix combinations for package, operating temperature and quality level. Other possibilities on request.

PART NUMBER	OPER. TEMP.		PACKAGE				SCREENING CLASS			
	C	M	P	J	C	E	Std	–D	G/B	B/B
TS2919	●		●	●			●	●		
		●		●	●	●	●		●	●

Examples : TS2919CP, TS2919CP-D, TS2919CJ, TS2919CJ-D
TS2919MJ, TS2919MJG/B, TS2919MJB/B,...

Oper. temp. : C : 0°C to + 70°C, **M :** – 55°C to + 125°C.
Package : P : Plastic DIL, **J :** Cerdip DIL, **C :** Ceramic LCC, **E :** Ceramic LCC.
Screening classes : Std (no end-suffix), **– D :** NFC 96883 level D.
G/B : NFC 96883 level G, **B/B :** MIL-STD-883 level B and NFC 96883 level B.

CASE CB-194

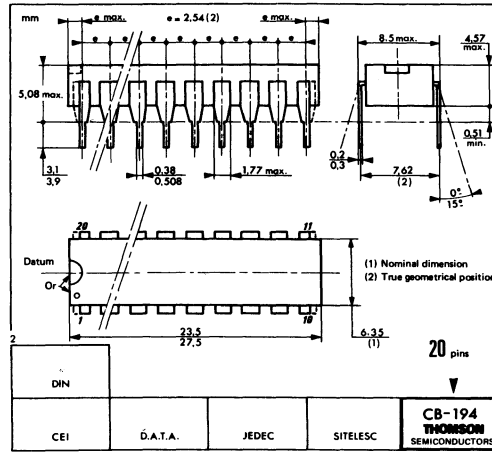


P SUFFIX
PLASTIC PACKAGE

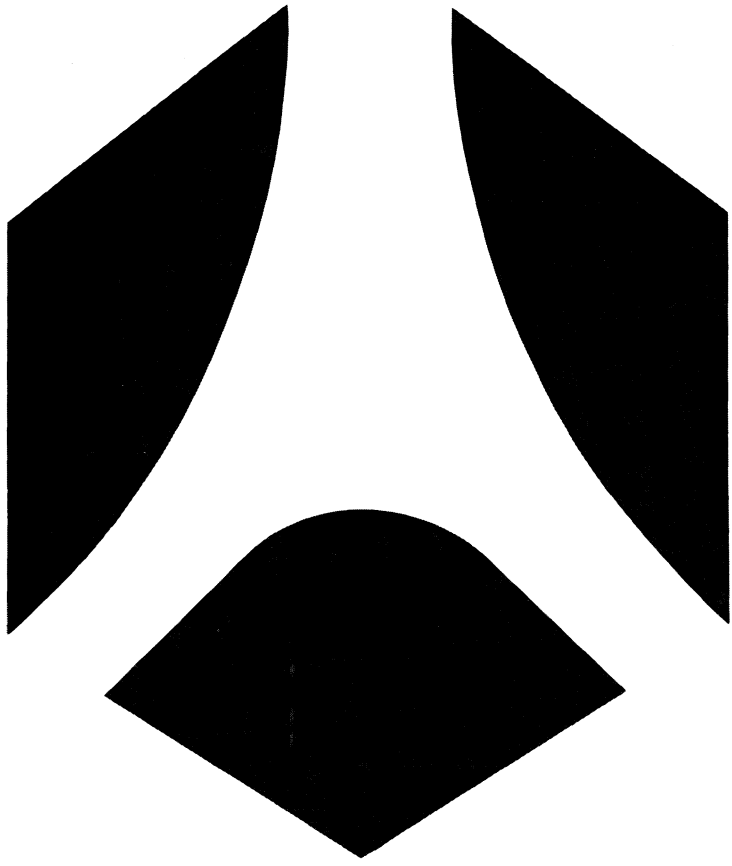
ALSO AVAILABLE

J SUFFIX
CERDIP PACKAGE

E SUFFIX
CHIP CARRIER



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.



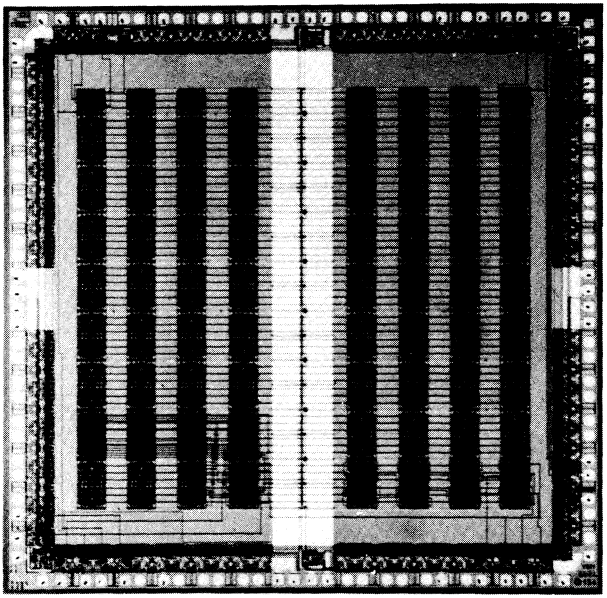
3

Semi-custom ICs

THOMSON SEMICONDUCTEURS

TSC06
TSC12
TSC17

ADVANCE INFORMATION



BIPOLAR MACRO ARRAYS

Two standard electrical interface environments have evolved for digital integrated circuits, TTL and ECL. TTL compatible products such as LS, FAST, CMOS, NMOS, etc., represent the majority of digital ICs in use today. However, ECL products are necessary for applications requiring the highest available switching performance. Interfacing these two incompatible environments has usually required dedicated level translation circuits as few logic ICs can operate in both environments simultaneously.

The TSC Bipolar MACRO ARRAYS exceed present offerings in compatibility, user friendliness, flexibility and performance. One comprehensive macro library and one set of industry standard CAD software tools support the entire family of arrays. The user may input a design in a variety of ways, from submitting a logic schematic to inputting a complete CAD design file via a remote terminal. Each array can be configured to operate in a TTL and/or ECL environment and all array pins can be configured as inputs or outputs providing maximum design flexibility. The internal macro logic is implemented with high performance series gated ECL circuits. These MACRO ARRAY features give the user a custom design solution with lower risk, lower cost and shorter design cycle than a full custom integrated circuit.

- TSC06 : 748 gates, TSC12 : 1338 gates, TSC17 : 1712 gates
- Typical internal equivalent gate delay : 0.8 ns
- Typical ECL I/O buffer pair delay : 2.0 ns
- Typical TTL I/O buffer pair delay : 8.0 ns
- All I/O cells may be configured as input, output, or bidirectional pins.
- True 10K ECL compatible interface
- Optional 2 kΩ on-chip pulldown resistor for direct wiring of ECL.
- True LS-TTL compatible interface including 8 mA or 16 mA outputs and three-state or open collector output options.
- High performance, oxide-isolated, 2 layer metalization process technology.
- Temperature range : −55 to + 125°C
- Identical macro library for all three arrays.
- Complete set of VAX/VMS and workstation CAD tools for the entire family.
- Commercial, Industrial and full MIL-STD-883C level B screening available.

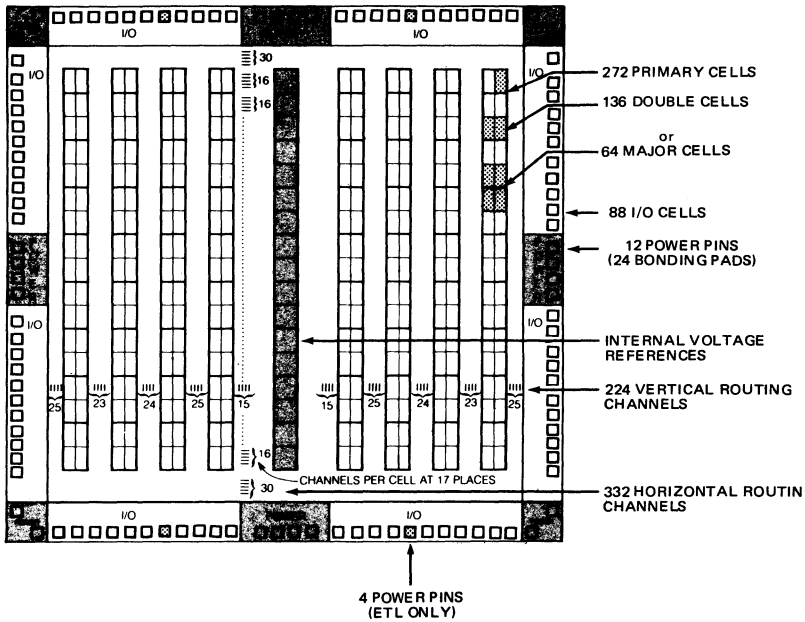
3

Ref. 04825

THOMSON SEMICONDUCTEURS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (1) 39.46.97.19 / Telex : 204780F

THOMSON COMPONENTS

FIGURE 1



INTERFACE MODE

Each bipolar MACRO ARRAY can be designed to operate in either a TTL, ECL or combined TTL and ECL interface environment. Prior to generating a custom logic design on the arrays, the user selects the array size and the array interface mode. Selection of the interface mode determines the fixed metal pattern for all power busing and the assignment of supply voltages to package pins. The mode selection also determines which group of I/O Macros will be used. Selection of macros for primary, double, or major macro functions is not affected by the interface mode or array size. The ECL and TTL modes do not restrict the number of I/O's available or location. The ETL mode is restricted in that ECL I/O's and TTL I/O's are available on two sides respectively. In addition, four ECL I/O locations are eliminated because additional power pins are necessary. The number of available I/O's for each mode is listed below.

POWER

The power supply pins are located at the corners and centers of array periphery. Each power pin ties to two adjacent building pads. The number and assignment of supply voltages to the power pins depends on the interface mode. The power buses for internal array and I/O buffers are separated. This allows for improved array and system performance. The internal ARRAY is referenced to ECL power supply levels in both the ECL and DUAL interface mode and to *TTL power* levels in the TTL interface mode.

Interface mode	Number of I/O's		
	TSC06	TSC12	TSC17
ECL	52	72	88
TTL	52	72	88
DUAL		ECL 32 TTL 30	ECL 40 TTL 44

Mode	4–5.2 V	0 V	5.0 V
ECL	X	X	
TTL		X	X
DUAL	X	X	X

THE TSC BIPOLAR MACRO ARRAYS

	TSC06	TSC12	TSC17
Primary cells	108	210	272
I/O cells	52	72	88
Max. Equivalent Gates (1)	748	1338	1712
Typical Array power	750 mW	1.5 mW	2.0 mW

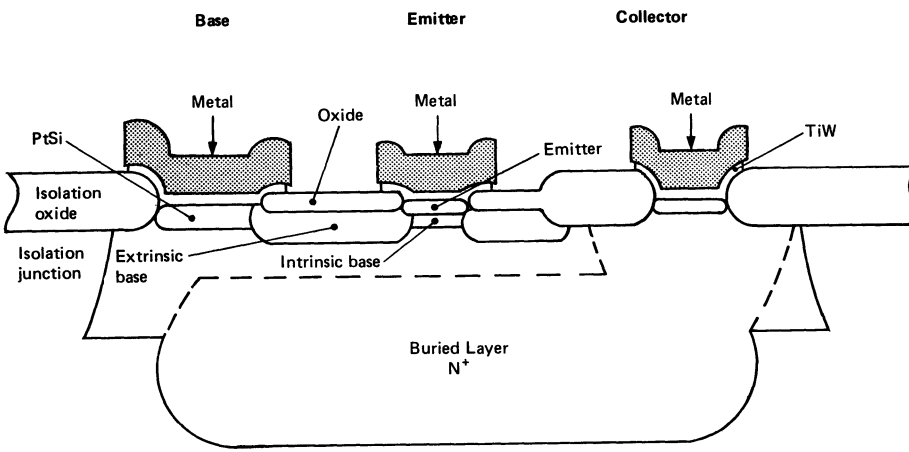
(1) - Assumes that all array cells are utilized at an average of 5 equivalent, 2-input gates per primary cell and 4 equivalent gates per I/O cell.

3

PROCESS DESCRIPTION

The TSC bipolar MACRO ARRAYS are fabricated on THOMSON SEMICONDUCTEURS' HBIP2 high performance two metal process.

This technology provides improved speed power products over convention junction isolated product.

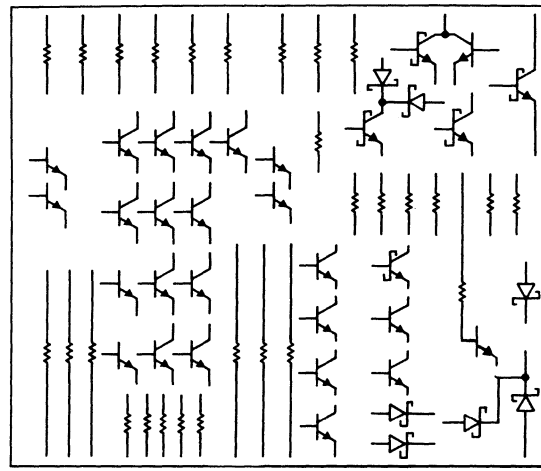


I/O MACRO CELLS

I/O macro cells are located around the periphery of the array. Each I/O cell has the required components to operate in either a ECL or TTL mode as an input or output. The I/O cell contains 28 transistors, 7 schottky diodes and 28 resistors. A schematic representation is shown in figure 2.

All signals to and from array must pass through an I/O cell for level translation and/or current drive capability. Each I/O location has a fixed bonding pad location allowing for single input and single output macros.

FIGURE 2



PRIMARY CELLS

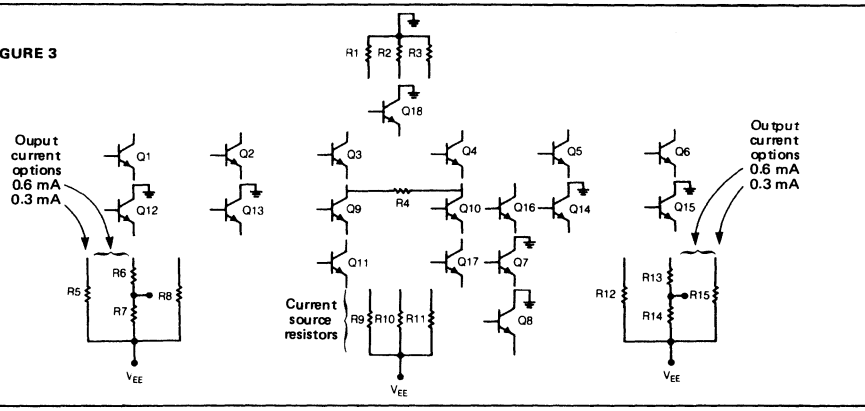
A primary cell is the basic logic building block in the internal array. Each primary cell contains 18 transistors and 15 resistors. A schematic representation is shown in figure 3. Logic functions are formed using first level metal interconnects. To incorporate more complex functions, adjacent cells are combined to form double cell or four symmetrical cells are combined to form a major cell.

All internal logic is configured with ECL logic structures using series gating. Other internal signals use one set of ECL logic levels. Some competing products use upper and lower logic levels which increases design risk.

The primary cell inputs can only be driven by an I/O cell or another primary cell and not from the external environment. Three drive levels are available from each primary output by paralleling resistors on the emitter follower : 0.300 mA and 0.600 mA. The outputs cannot be used as off-chip output drivers.

This primary cell has an increased component density over competing array product. This allows for more efficient utilisation of available cell locations.

FIGURE 3



PRIMARY CELL

4/7

CELL LIBRARY

I/O MACROS : to assist the designer in secreting the appropriate I/O macro, they have been given symbolic names which indicates logic function, fanout capability and interface mode :

First character : I for Input macro
O for Ouput macro
Second character : A number indicating logic function
Third character : Fanout capability (N-Normal, F-Fast)
Fourth character : Interface mode
(E-ECL, T-TTL, D-DUAL)

I/O macro	Macro description
I 1ND	TTL input LATCH
I 1NE	ECL input LATCH
I 1NT	TTL input LATCH
I 2ND	TTL input buffer/converter
I 2NE	ECL input buffer/converter
I 2NT	TTL input buffer/converter
I 3ND	TTL chip enable
I 3NT	TTL chip enable
I 4NE	ECL latch clock input
O INT	TTL bidirectional buffer
O 2ND	TTL output with LATCH
O 2NE	ECL output with LATCH
O 2NT	TTL output with LATCH
O 3ND	3 input OR with TTL output
O 3NE	3 input OR with ECL output
O 3NT	3 input OR with TTL output
O 4ND	3 input NOR with TTL output
O 4NE	4 input NOR with ECL output
O 4NT	4 input NOR with ECL output
O 5ND	2 input AND with TTL output
O 5NE	2 input AND with ECL output
O 5NT	2 input AND with TTL output
O 6ND	2 input NAND with TTL output
O 6NE	2 input NAND with ECL output
O 6NT	2 input NAND with TTL output

INTERNAL MACROS : The designer uses the same internal macros regardless of the interface mode. These macros have mnemonic names to assist the designer in the selection of macro function.

First character : define the logic function
- **AR** - combined AND/OR
- **D** - D Flip Flop
- **L** - Latch
- **M** - Mux
- **N** - Inverter
- **R** - OR
- **X** - Exclusive OR

Second character : Inverter specifics about logic function.
Last character : Defines fanout ability.
N-Fanout up to 6 (0.3 mA)
F-Fanout up to 10 (0.6 mA).

Logic macro	Macro description
AR1N	3 input OR-AND
AR2N	2 wide 3-input active low AND-OR/NOR
AR3N	3 input OR-AND/NAND with 3 active low enable
AR4N	3 wide active low AND-OR/NOR
F1N	Positive edge D flip-flop with asynchronous reset
F2N	Positive edge D flip-flop with asynchronous set and reset
L1N	Negative clock transparent LATCH with reset
L2N	Positive clock transparent LATCH with reset
L3N	2 bit LATCH with asynchronous reset and active low enable
M1N	2 to 1 MUX with OR select and active low enable
M2N	2 to 1 MUX with OR select and active high enable
M3N	4 to 1 MUX
M4N	4 to 1 MUX with active low enable
M5N	DUAL 2 to 1 MUX
M7N	DUAL 2 to 1 MUX with common select
NR2N	4 input OR/NOR
NR2N	DUAL 3 input OR - 3 input NOR
NR4N	6 input OR/NOR
NR5N	DUAL 3 input NOR with 2 common input
NR7N	7 input OR-NOR
NR8N	12 input OR-NOR
R1N	DUAL 3 input OR
R2N	DUAL 3 input OR with 2 common inputs
X1N	3 input OR-exclusive OR/NOR
X2N	2 input OR-exclusive OR with active low
X3N	4 input ODD parity checker
X4N	4 input exclusive OR/NOR
X5N	2 input NOR-exclusive OR/NOR.

3

A.C. PERFORMANCE

The cell library provides the maximum delay time for worst case technology, 25°C ambient and $V_{CC} = -5.2$ V. Worst case performance can be calculated using the formula provided in the design manual or the CAD system.

The CAD system provides the designer with both a prerouting and routed A.C performance simulation. The prerouting simulation is based upon statistical loading estimates based upon fanout.

The designer can also calculate the typical and best case performance by multiplying worst case performance by 0.5 and 0.7 respectively.

The designer will be able to select the speed power products of an internal macro. Each function, where possible, will be released using a 0.300 mA and 0.600 mA source current. By doubling the power, the designer is able to obtain a 30 % performance improvement.

Table 1 provides a summary of typical performances for selected internal and I/O logic functions. The internal macros performance does not vary based upon interface mode.

TABLE 1 – TYPICAL TIMING DELAYS

INTERNAL MACRO (1)	TYPICAL DELAY
3 Input gate	1.8 ns
3 Input AND/OR	2.0 ns
Flip-flop	2.7 ns
Latch	2.2 ns
Mux	2.0 ns
INPUT MACRO (1)	
Latch (ECL)	3.9 ns
Latch (TTL)	4.2 ns
Buffer (ECL)	2.2 ns
Buffer (TTL)	2.7 ns
OUTPUT MACRO (2)	
Latch (ECL)	3.5 ns
Latch (TTL)	8.4 ns
Buffer (ECL)	2.1 ns
Buffer (TTL)	8.1 ns

(1) FANOUT = 3, routing metal 2.5 mm
(2) ECL load 50 Ω to – 2 V,
TTL load = 300 Ω.

PACKAGING OPTIONS

Package Type	Leads	TSC06	TSC12	TSC17
Ceramic DIP	28	X		
	40	X	X	
	48	X	X	
	64	X	X	X
Plastic DIP	28	X		
	40	X		
	48	X		
	64	X		
Leadless Ceramic Chip Carrier	68	X	X	X
	84		X	X
Pin Grid Array	68	X	X	X
	84		X	X

Other packages available on request.

QUALITY LEVELS

In addition to the standard quality procedures for commercial grade product, THOMSON SEMICONDUCTEURS offers a variety of extended temperature ranges and high reliability screening levels for the TSC MACRO Arrays. All extended screening is performed at THOMSON SEMICONDUCTEURS' Military and Spatial Division facility in France, which is completely equipped with state-of-the-art assembly, electrical test and environmental stress equipment. The Military and Spatial Division is dedicated to performing quality control and reliability assurance for all THOMSON SEMICONDUCTEURS integrated circuits for military and space applications.

AVAILABLE SCREENING LEVELS

Level	Description
Standard	Commercial Temp. Range 0° to + 70°C Industrial Temp. Range –40° to + 85°C Military Temp. Range –55° to + 125°C
D	Standard Level with Burn-in
B/B	Full MIL-STD-883C, Class B Screening
G/B	MIL-STD-883C Without Constant Acceleration or Temp. Test, PDA < 10 %.

CAD SYSTEM

All of the THOMSON SEMICONDUCTEURS Array Products are supported by a fully automated VAX/VMS based CAD System. The CAD System provides a complete set of industry standard design, layout and verification tools to ensure fast, error-free design of the TSC MACRO ARRAYS. The CAD System resides at THOMSON SEMICONDUCTEURS Design Center and is accessed with a Tektronix 4109 (or equivalent) graphics terminal.

The CAD System can also accept verified netlists from a variety of popular engineering workstations, including Daisy®, Valid®, Mentor®, and IBM PC-XT®-based workstations that are equipped with the TSC Series Macro library. The key components of the THOMSON SEMICONDUCTEURS CAD System are :

Schematic Capture	SDS®
Netlist Extraction	SDS®
Logic Simulation	HILO®
Timing Analysis	HILO®
Fault Grading	HILO®
Tester Program Interface	HILO®
Automatic Placement and Routing	GARDS®
Interactive Placement and Routing	GARDS®
Design Rule Checking	GARDS®
Automatic Mask Generation	GARDS®

®SDS and GARDS are trademarks of SilvarLisco. HILO is a trademark of GenRad Inc. VAX and VMS are trademarks of Digital Equipment Corp. IBM and PC-XT are trademarks of the IBM Corporation. Daisy is a trademark of Daisy Systems Corp. Mentor is a trademark of Mentor Graphics Corp. Valid is a trademark of Valid Logic Systems Inc.

Design entry is easily accomplished with the SDS menu driven software and a graphics terminal (Tek 4109). The SDS generated logic schematic is converted to a netlist and checked for logic design rule violations (excessive fanout, for instance). The netlist is then automatically converted to HILO simulation format.

The HILO simulation program performs logic simulation based on the user defined input test pattern and timing analysis using pre-routing statistical load capacitances for delay calculations. HILO also can be used to perform fault grade analysis of the input test pattern.

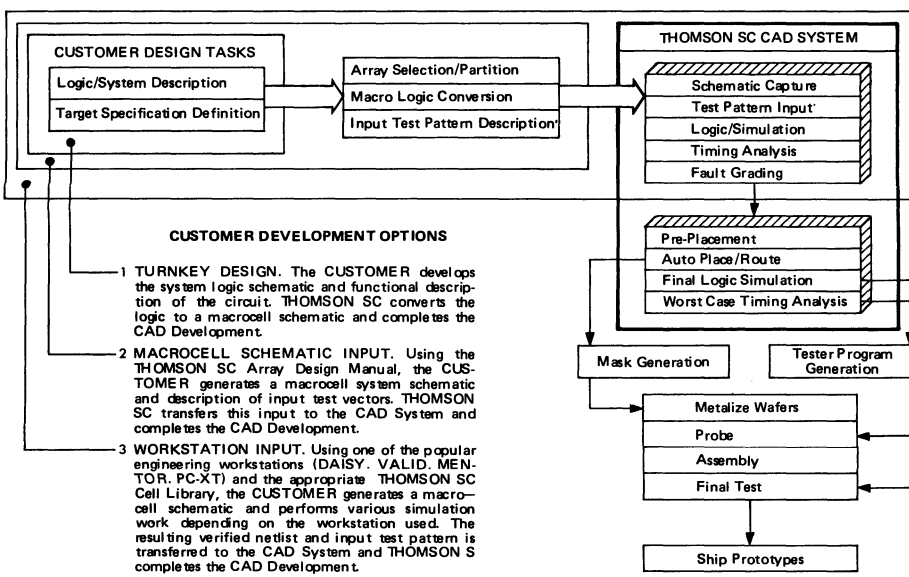
The GARDS program is used to automatically place and route the array's cell logic as described in the SDS netlist. GARDS also has an interactive mode that allows cell or I/O preplacement and manual routing to optimize critical paths if necessary. After placement and routing is completed, HILO timing analysis can be performed again to determine worst case critical path delays using the actual interconnect length and fanout capacitances.

When the array design work is completed on the CAD System, the HILO simulation output is automatically converted to a tester program tape and the GARDS place and route file is converted to a graphics data base for mask generation. These two data bases are then sent to the factory for prototype generation.

3

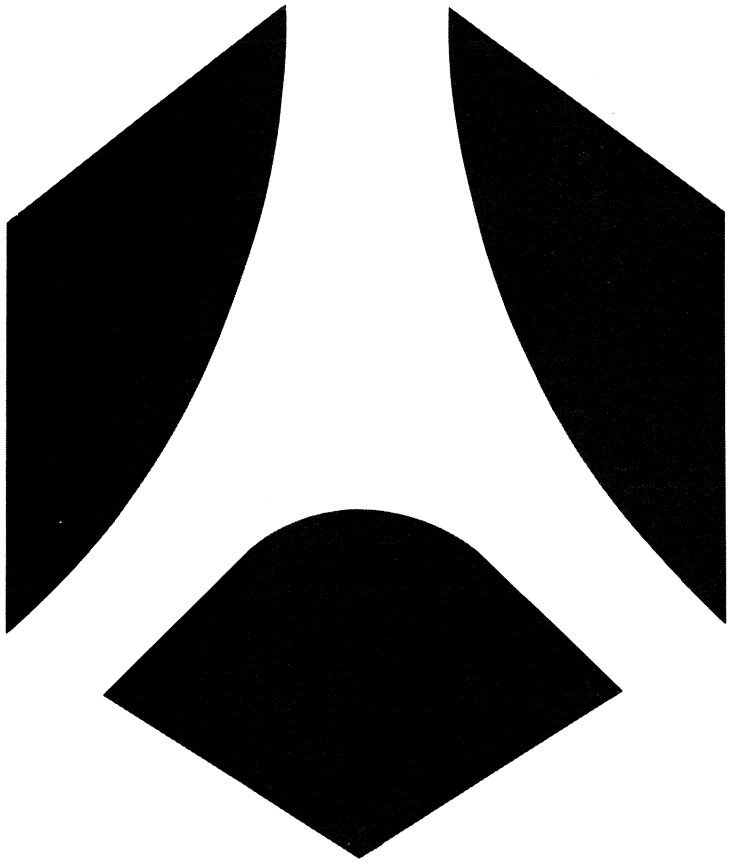
DESIGN DEVELOPMENT PROCEDURE

The design of an array option is a joint development effort involving THOMSON SEMICONDUCTEURS and the CUSTOMER. THOMSON SEMICONDUCTEURS offers a very flexible interface to the CAD System, providing the CUSTOMER with several options in performing the various CAD Development Procedures as shown below :



NOTES

This is advance information and specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.



4

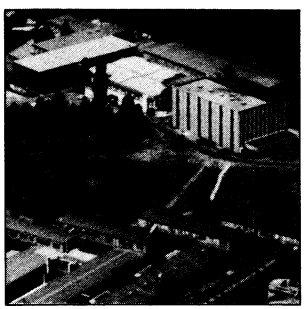
Military and Hi-Rel ICs

MILITARY AND SPACE PROGRAM

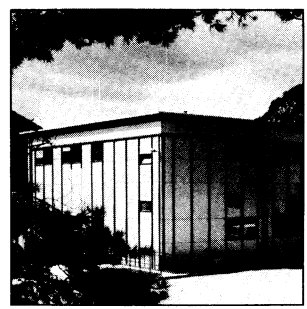
To meet increasing worldwide demand for high-quality high-reliability semiconductors, THOMSON SEMICONDUCTEURS has created a Military and Space Division specialized in these products.

The division is wholly responsible for strategy, design and manufacture of semiconductor products for military and space applications, and has the expertise and the resources to satisfy the most demanding requirements:

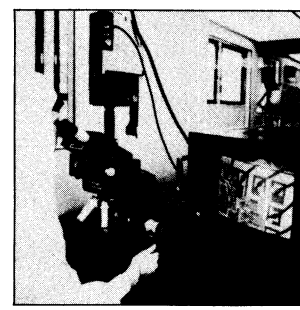
- a 3,000 m² plant exclusively assigned to the design and manufacture of military and space products,
- equipment carefully selected to guarantee the highest possible standards in terms of quality,
- staff fully trained in the strictest possible quality assurance and reliability procedures,
- large known-bow based on active participation in outstanding programs including ARIANE, AIRBUS, MIRAGE 2000, METEOSAT, etc.



THOMSON SEMICONDUCTEURS' Military and Space Division is located at the Company's and manufacturing facility in Grenoble.



3,000 m² Military and Space Division plant on the St Egreve complex.



The most sophisticated quality control and reliability methods and resources are employed by expert staff who *ensure that quality assu*rance procedures are strictly complied with.

SEMICONDUCTORS FOR A VARIED RANGE OF PRESTIGE PROGRAMS

THOMSON SEMICONDUCTEURS has been involved in components development for weapons and avionics systems, space vehicles and ballistic missiles for nearly 20 years. A selection of examples is listed below:

Military

- RITA telecommunication network
- EXOCET missile
- CROTALE missile
- SHAHINE missile

Civil and military aviation

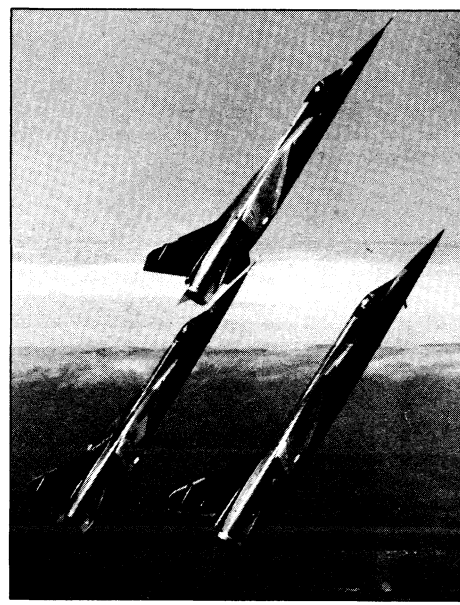
- AIRBUS aircraft
- MIRAGE 2000 air-fighter
- Airport guidance systems

Space

- ARIANE launch vehicle
- METEOSAT satellite
- TV-SAT satellite

Other

- TGV (High-speed inter-urbain transport)



QUALITY CONTROL: a tailored service

The market for high-reliability components is characterized by its highly individual requirements, with which THOMSON SEMICONDUCTEURS is more than able to cope:

● By offering quality levels compatible with the leading international standards:

— MIL-STD-883/class B,
— ESA/SCC 9000, classes B and C, LA1, 2 and 3,
— CECC 90000, selection classes B or D and quality assurance level Y,
— NFC 96883, selection classes B, G or D,
— NFC 96020, Quality Assessment Standard, level Y.

● By ensuring that its semiconductor products appear on as many Preferential Product Lists (GAMT1, MUAHAG, etc.) and Qualified Product Lists as possible.

● By deploying the most advanced technology: in the ongoing search for improved performance (speed, power consumption, integration, immunity to radiation, etc.), military equipment design demands the use of the most modern technologies. These technologies are deployed by THOMSON SEMICONDUCTEURS in respect of its standard products as well as its custom activities:

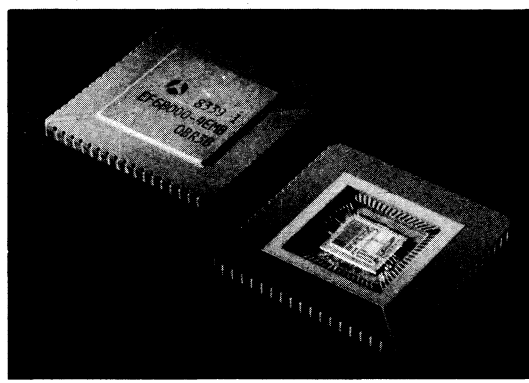
Processes

— HMOS1 (3μ) and HMOS2 (2μ),
— HCMOS (2μ) double-layer,
— HCMOS/SOS,
— High-speed linear bipolar (4 GHz),
— High-speed digital bipolar (ECL): HBIP2 (2μ).

Encapsulation technologies

— Metal can (linear),
— Cerdip,
— Ceramic,
— Chip-carrier,
— Pin grid array,
— Dice (for hybrids).

● By providing a tailor-made service: special requirements in respect of quality, product life and quantities are a characteristic feature of this market sector. In all these areas, THOMSON SEMICONDUCTEURS offers the optimum cost/performance trade-off for the problem in hand.



FIVE SELECTION LEVELS

The THOMSON SEMICONDUCTEURS Military and Space Division offers five selection classes compatible with international standards. For a more complete explanation of each class refer to the "Quality Information" section of this data book. The essential features of each class are outlined below:

Level S:

Space applications: the methods applied conform to specification ESA/SCC 9000/classes B and C, LAT1, 2 and 3.

Level B/B and G/B:

Class B/B conforms strictly to MIL-STD-883/class B.
The classes are schematically represented in the flowchart (next page), illustrating the differences between them. The selection methods for classes B/B and G/B are those of MIL-STD-883, class B, which are in turn identical to those of standards NFC 96883/class B and CECC 90,000/class B.

Level G/B, offered by very few manufacturers, is an alternative particularly appreciated by users for its quality/price trade-off.

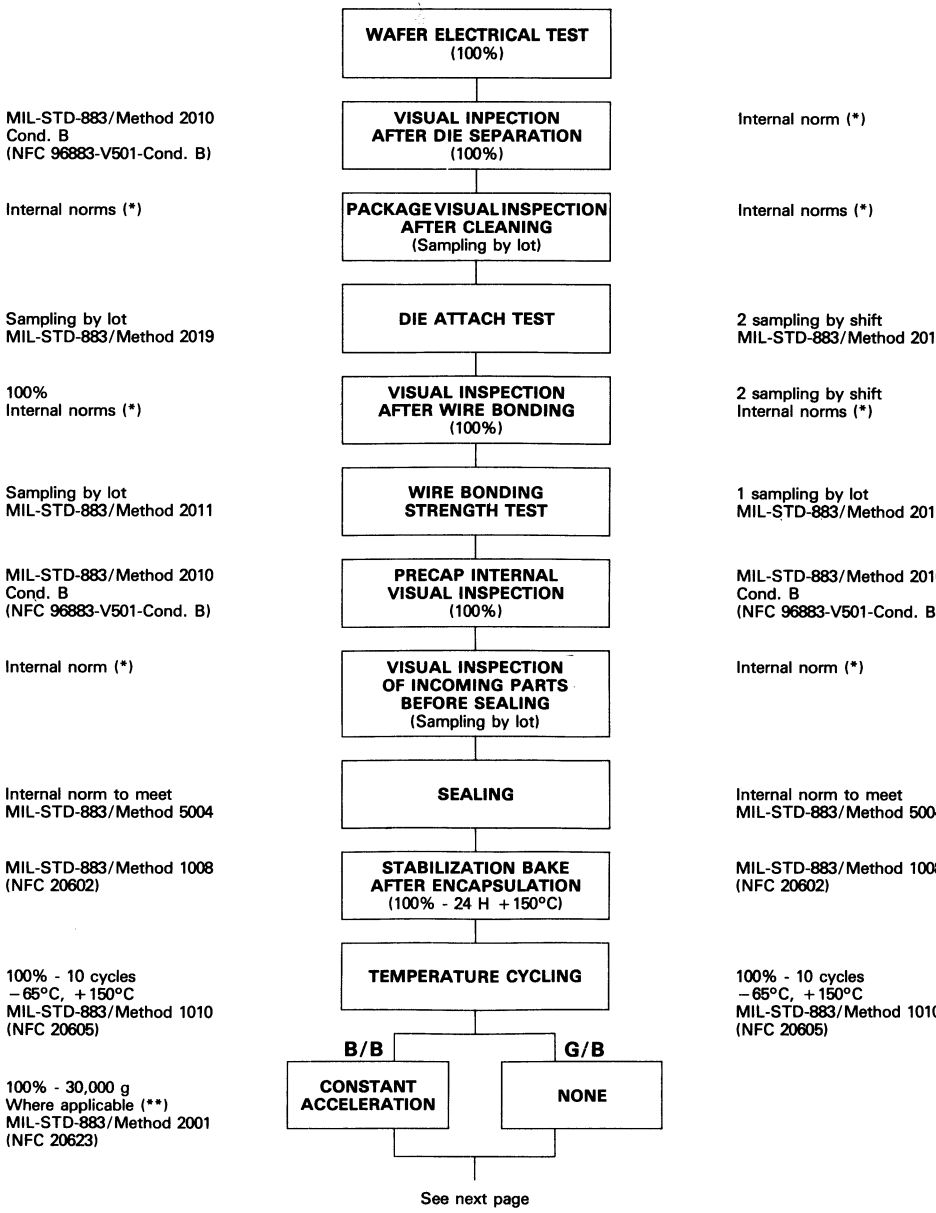
Levels D and Standard:

In the "Standard" class, the Military and Space Division offers a range of products in ceramic, cerdip and metal packages, for operation in the following temperature ranges:

- Extended: −40°C to +85°C,
- Military: −55°C to +125°C.

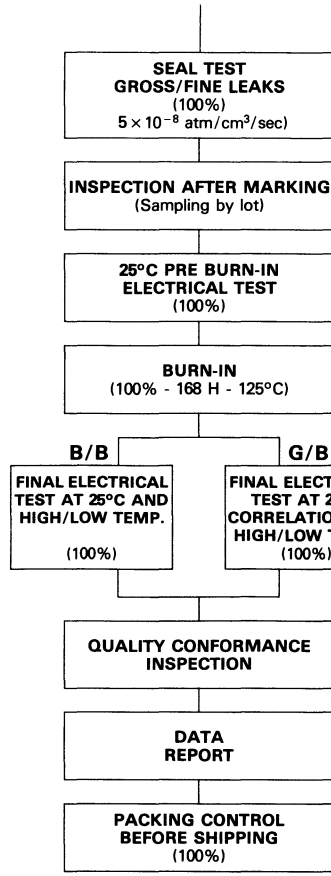
The **"D"** level is the standard level with additional burn-in only.

B/B AND G/B CLASS QUALITY ASSURANCE AND SCREENING PROCEDURES



(*) Not specified in MIL-STD-883: THOMSON SEMICONDUCTEURS norms.
(**) For TO-3 and large DIL: contact manufacturing.

B/B and G/B SCREENINGS(continued)



(***) On customer requests selection between AQL (NFC 96883) and LTPD (MIL-STD-883/Method 5005) will be sent.

THE RESOURCES TO ENSURE RIGOROUS QUALITY CONTROL

The strictest possible quality control at all levels of the manufacturing process offers the user the best guarantee of reliability.

Wafer processing

The diffusion workshops are covered by extremely rigorous specifications in respect of cleanliness and the precision with which the various operations are carried out. Production is continuously sampled for the purpose of reliability testing. The most stringent requirements are imposed to wafers intended for military and space applications.

Assembly

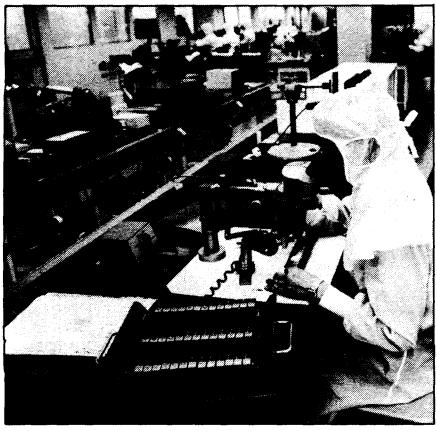
Assembly is carried out in a clean room environment by highly skilled staff using the most sophisticated automated equipment. There are a number of possible test and inspection levels:

- 100% visual inspection (PRECAP),
- Wire bonding test,
- Die attach test,
- Stabilization bake,
- Temperature cycling,
- Constant acceleration,
- Particle impact noise detection test (Pind-test),
- Seal test.

Quality assurance and selection

Electrical tests are performed on 100% of devices after selection operations. Apart from sorting parts, this test is used to determine the proportion of circuits defective after burn-in . Application of the 5% PDA procedure enables the entire production to be rejected where lots show a potential for failures after shipping considered excessive.

Following the selection operations, the Quality Assurance staff applies standardized quality monitoring procedures in accordance with standard CECC 90,000, level Y.



BIPOLAR MICROPROCESSOR SERIES

Part number	Characteristic	Package	Processed or qualified according to:						Page
			MIL-STD-883 level B	NFC 96883 level B	NFC 96883 level G	NFC 96883 level D	CECC 90000	ESA/SCC 9000	
TS2901BMCB/B MCG/B	4-bit microprocessor	Ceramic DIL 40	●	●	●	Contact our sales offices	Contact our sales offices	Contact our sales offices	33
MEB/B MEG/B		44-pad LCC	●	●	●				
MJB/B MJG/B		Cerdip DIL 40	●	●	●				
TS2901CMCB/B MCG/B		Ceramic DIL 40	●	●	●				59
MEB/B MEG/B		44-pad LCC	●	●	●				
MJB/B MJG/B		Cerdip DIL 40	●	●	●				
TS2902AMCB/B MCG/B	High speed look-ahead carry generator	Ceramic DIL 16	●	●	●				83
MEB/B MEG/B		20-pad LCC	●	●	●				
MJB/B MJG/B		Cerdip DIL 16	●	●	●				
TS2909AMCB/B MCG/B	Microprogram sequencer	Ceramic DIL 28	●	●	●				89
MEB/B MEG/B		28-pad LCC	●	●	●				
MJB/B MJG/B		Cerdip DIL 28	●	●	●				
TS2910 MCB/B MCG/B	Microprogram controller	Ceramic DIL 40	●	●	●				105
MEB/B MEG/B		44-pad LCC	●	●	●				
MJB/B MJG/B		Cerdip DIL 40	●	●	●				
TS2911AMCB/B MCG/B	Microprogram sequencer	Ceramic DIL 20	●	●	●				89
MEB/B MEG/B		20-pad LCC	●	●	●				
MJB/B MJG/B		Cerdip DIL 20	●	●	●				
TS2914 MCB/B MCG/B	Vectored priority interrupt controller	Ceramic DIL 40	●	●	●				*121*
MEB/B MEG/B		44-pad LCC	●	●	●				
MJB/B MJG/B		Cerdip DIL 40	●	●	●				
TS2915AMCB/B MCG/B	Quad three-state bus transceiver with interface logic	Ceramic DIL 24	●	●	●				147
MEB/B MEG/B		28-pad LCC	●	●	●				
MJB/B MJG/B		Cerdip DIL 24	●	●	●				

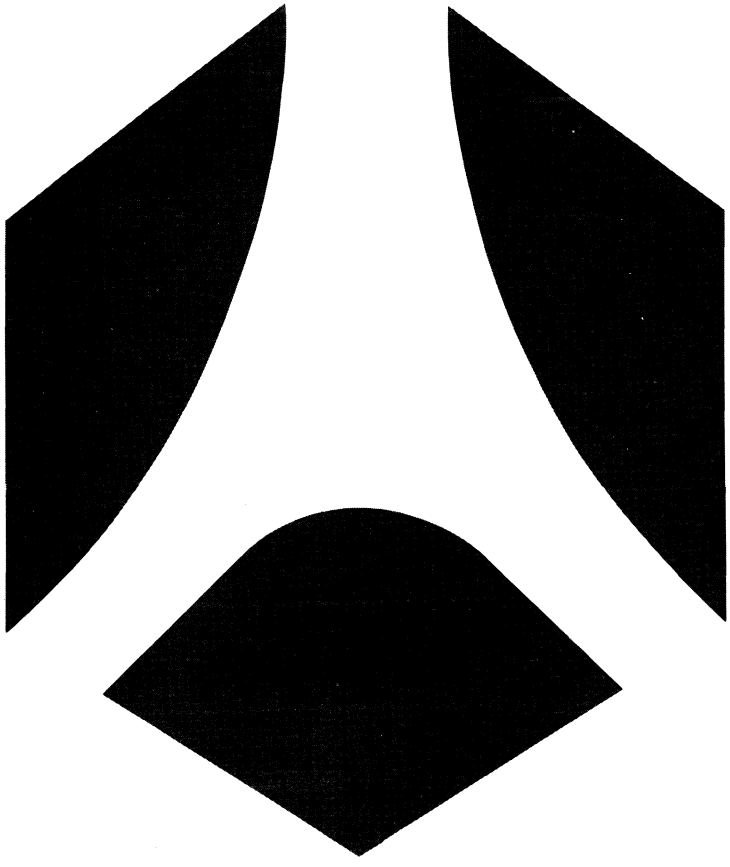
BIPOLAR MICROPROCESSOR SERIES (continued)

Part number	Characteristic	Package	Processed or qualified according to:						Page
			MIL-STD-883 level B	NFC 96883 level B	NFC 96883 level G	NFC 96883 level D	CECC 90000	ESA/SCC 9000	
TS2917AMCB/B MCG/B MEB/B MEG/B MJB/B MJG/B	Quad three-state bus transceiver with interface logic	Ceramic DIL 20	●	●	●	Contact our sales offices	Contact our sales offices	Contact our sales offices	155
		20-pad LCC	●	●	●				
		Cerdip DIL 20	●	●	●				
TS2918 MCB/B MCG/B MEB/B MEG/B MJB/B MJG/B	Quad D-register with standard and three-state outputs	Ceramic DIL 16	●	●	●				163
		20-pad LCC	●	●	●				
		Cerdip DIL 16	●	●	●				
TS2919 MCB/B MCG/B MEB/B MEG/B MJB/B MJG/B	Quad register with dual three-state outputs	Ceramic DIL 20	●	●	●				171
		20-pad LCC	●	●	●				
		Cerdip DIL 20	●	●	●				

4

BIPOLAR MEMORIES

TS71191 MCB/B MCG/B MEB/B MEG/B MJG/B	2K×8 PROM (80 ns)	Ceramic DIL 24	●	●	●	Contact our sales offices	Contact our sales offices	Contact our sales offices	15
		28-pad LCC	●	●	●				
		Cerdip DIL 24			●				
TS71191AMCB/B MCG/B MEB/B MEG/B MJG/B	2K×8 PROM (60 ns)	Ceramic DIL 24	●	●	●				15
		28-pad LCC	●	●	●				
		Cerdip DIL 24			●				
TS71191BMCB/B MCG/B MEB/B MEG/B MJG/B	2K×8 PROM (45 ns)	Ceramic DIL 24	●	●	●				15
		28-pad LCC	●	●	●				
		Cerdip DIL 24			●				
TS71191CMCB/B MCG/B MEB/B MEG/B MJG/B	2K×8 PROM (35 ns)	Ceramic DIL 24	●	●	●				15
		28-pad LCC	●	●	●				
		Cerdip DIL 24			●				
TS71291CMCB/B MCG/B MJG/B	16K PROM Slim-line	Ceramic DIL 24	●	●	●				15
		Cerdip DIL 24			●				



5

Quality information

SCREENING CLASSES

Different screening classes are available from THOMSON SEMICONDUCTEURS for customers desirous to use a same product in different environmental conditions. Consequently, screening classes choice is the customer's responsibility.
Screening classes for packaged circuits, and quality levels for dice are indicated below.

PACKAGED PRODUCTS

S space screening class:
In accordance with ESA/SCC 9000, B or C class with LA1, LA2 or LA3 on customer's resquest.

B/B screening class:
Strictly equivalent to the US MIL-STD-883 class B (or French NFC 96883/class B or European CECC 9000/class B). This is suitable for products used in severe environmental conditions and when low maintenance cost is required.

G/B screening class:
Same as B/B but:
- No constant acceleration test,
- Full range temperature test through +25°C correlated measurement.

Only available with THOMSON SEMICONDUCTEURS , this screening class, which refers to the MIL-STD-883, is a cost effective alternative for customers wishing to buy HI-REL devices at lower cost. This screening is strictly conform to the French NFC 96883/class G.

D SCREENING CLASS:
In accordance with French NFC 96883/class D (and European CECC 9000/class D), this level corresponds to "standard screening" products submitted only to an additional burn-in.

STANDARD QUALITY CLASS:
Guaranteed level when no specific screening class is required by the customer.

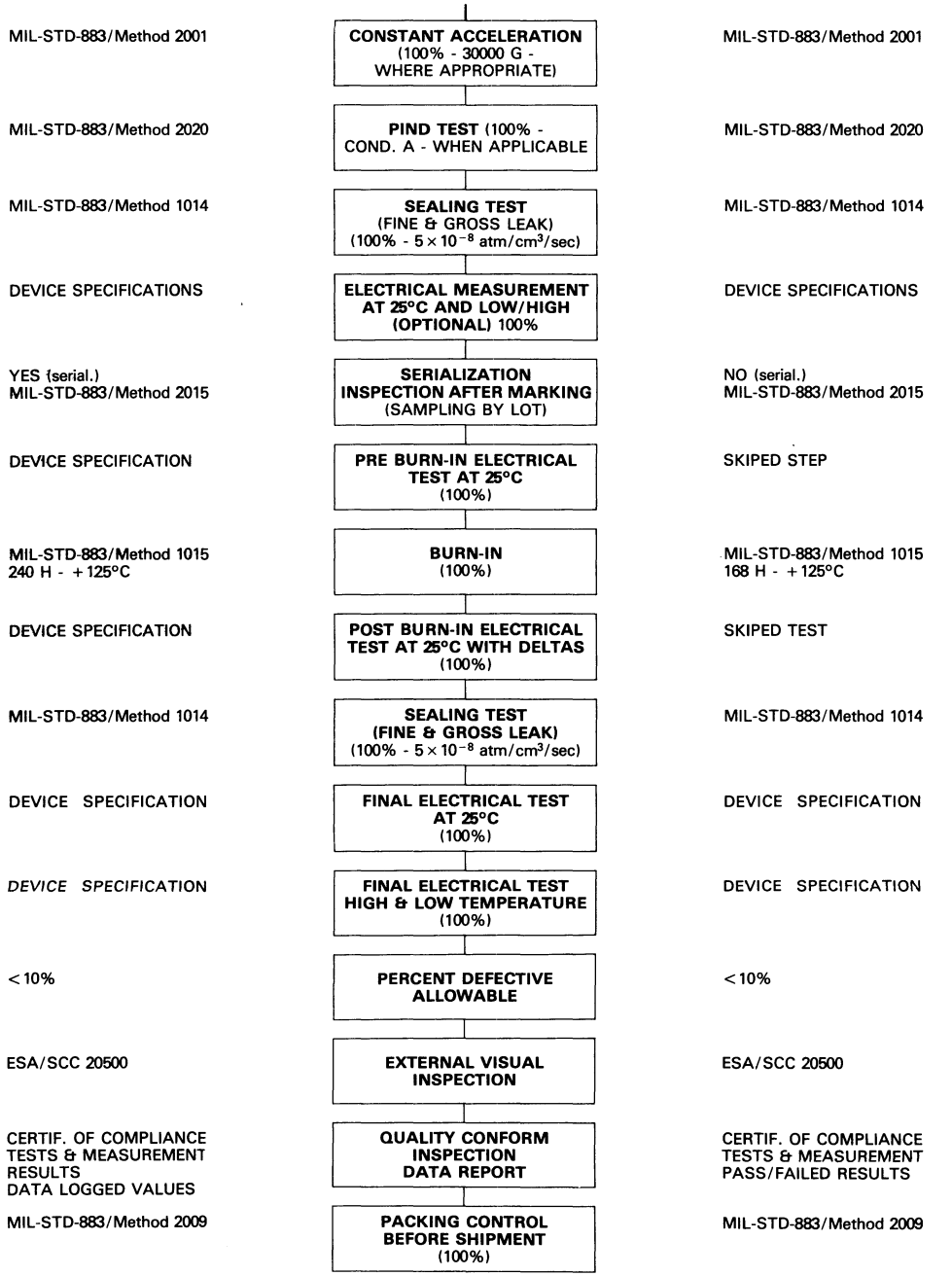
S space screening

Specifications class B		Specifications class C
Internal norm (*) ESA/SCC 21400	**WAFER LOT ACCEPTANCE** (100%)	Internal norm (*)
Internal norm (*)	**WAFER ELECTRICAL TEST** (100%)	Internal norm (*)
MIL-STD-883/Method 2010 Cond. A	**VISUAL INSPECTION AFTER DIE SEPARATION** (100%)	MIL-STD-883/Method 2010 Cond. B
Internal norm (*)	**VISUAL INSPECTION OF PACKAGE AFTER CLEANING** (100%)	Internal norm (*)
MIL-STD-883/Method 2019	**DIE ATTACH TEST** (SAMPLING BY SHIFT & LOT)	MIL-STD-883/Method 2019
Internal norm (*)	**VISUAL INPECTION AFTER WIRE BONDING** (100%)	Internal norm (*)
MIL-STD-883/Method 2011	**WIRE BONDING STRENGTH TEST** (SAMPLING BY SHIFT & LOT)	MIL-STD-883/Method 2011
MIL-STD-883/Method 2010 Cond. A	**PRECAP INTERNAL VISUAL INSPECTION** (100%)	MIL-STD-883/Method 2010 Cond. B
Internal norm (*)	**VISUAL INSPECTION OF INCOMING PARTS BEFORE SEALING** (100%)	Internal norm (*)
MIL-STD-883/Method 1008	**STABILIZATION BAKE AFTER ENCAPSULATION** (100% - 48 H - 150°C)	MIL-STD-883/Method 1008
MIL-STD-883/Method 1010	**TEMPERATURE CYCLING** (100% - 10 cycles −65°C ; +150°C)	MIL-STD-883/Method 1010

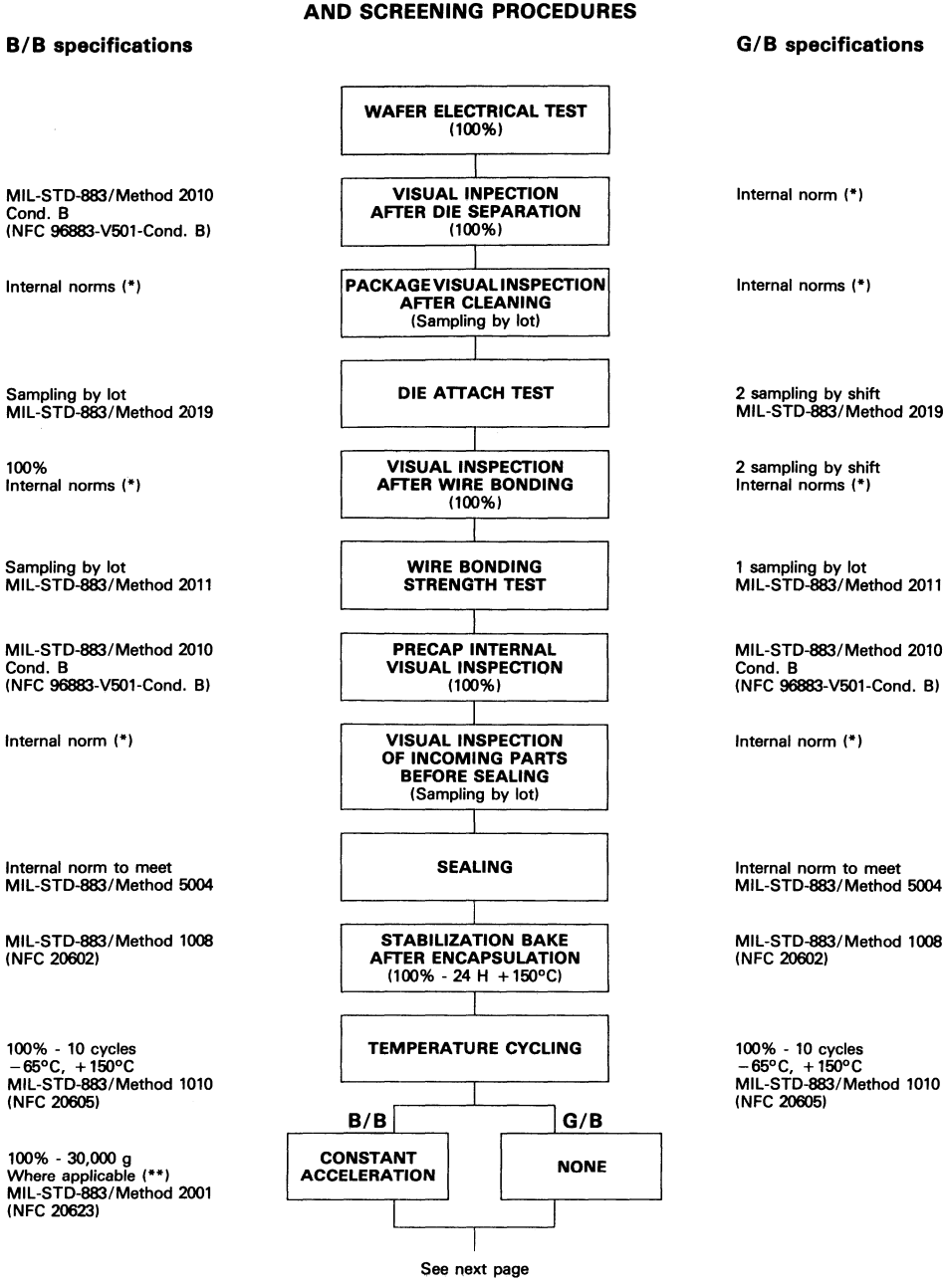
See next page

(*) Not specified in ESA/SCC 9000: THOMSON SEMICONDUCTEURS norms.

S space screening (continued)

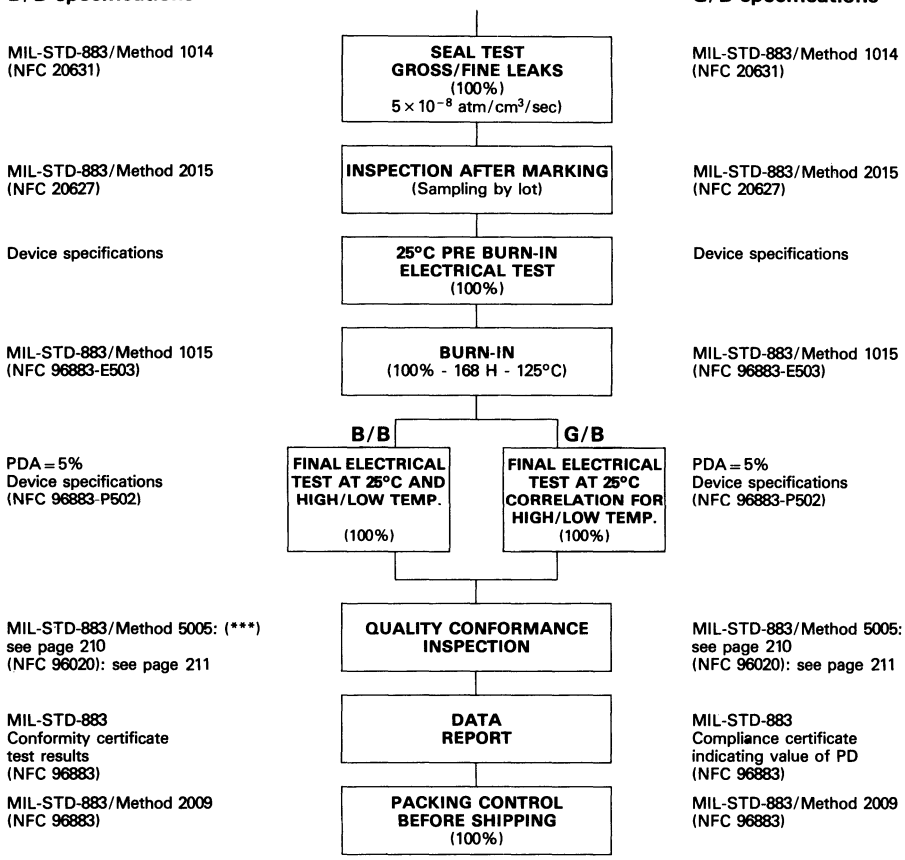


B/B AND G/B CLASS QUALITY ASSURANCE AND SCREENING PROCEDURES



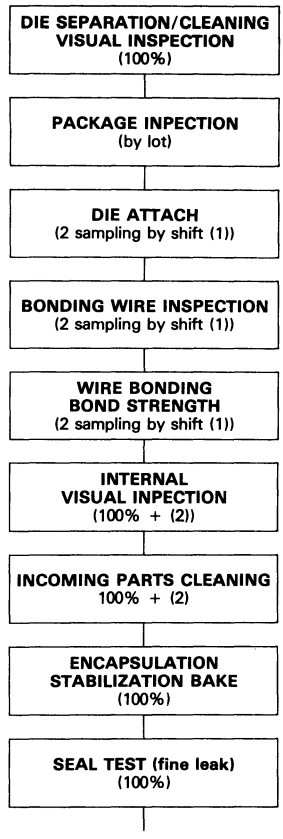
(*) *Not specified* in MIL-STD-883: THOMSON SEMICONDUCTEURS norms.
(**) For TO-3 and large DIL: contact manufacturing.

B/B and G/B SCREENINGS (continued)



(***) On customer request selection between AQL (NFC 96883) and LTPD (MIL-STD-883/Method 5005) will be sent.

D and STANDARD SCREENINGS



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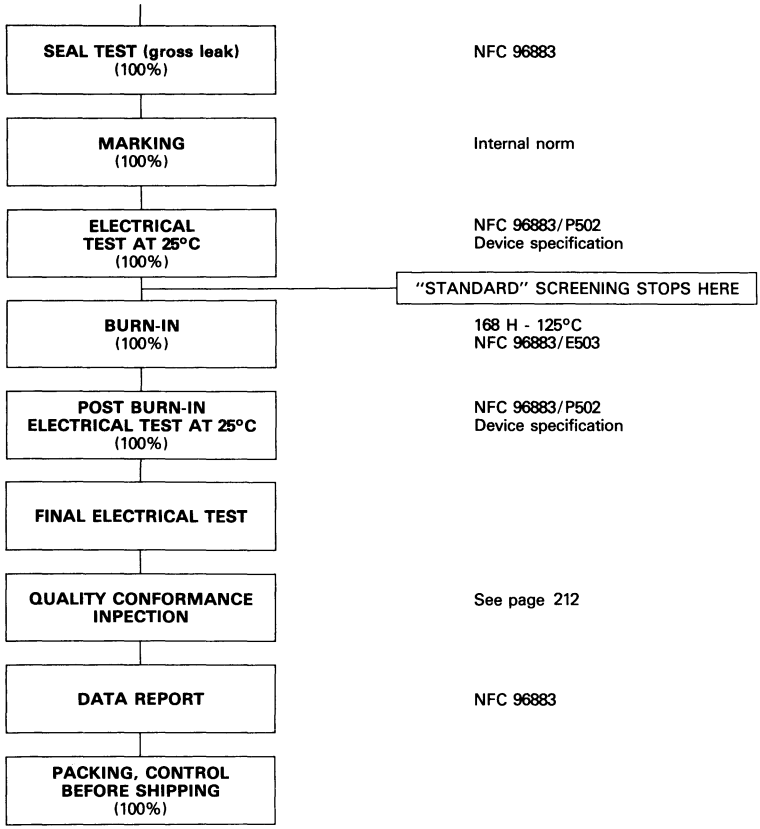
D and STANDARD SCREENINGS (continued)



(1) Minimum sample quantity by shift
(2) Lot sampling

B/B QUALITY CONFORMANCE INSPECTION

GROUP A TESTS
(performed on each lot)

	DEVICES	ANALOG B/B LEVEL MIL-STD-883 Method 5005		LOGIC B/B LEVEL MIL-STD-883 Method 5005	
	CLASS				
TESTS	**MIL-STD-883 Method**	**LTPD**	**Accept. number**	**LTPD**	**Accept. number**
External visual inspection Marking conformance	2009	3	2	3	2
Mechanical inoperatives		3	1	3	1
Functional test at 25°C	Subgroups 4 and 7	2	0	2	0
Main static tests and complementary static tests at 25°C	Subgroup 1				
Functional and main static tests at maximum rated operating temperature	Subgroups 2, 5 and 8	3	1	3	1
Functional and main static tests at minimum rated operating temperature	Subgroups 3, 6 and 8	5	2	5	2
Switching tests at 25°C	Subgroup 9	2	0	2	0
Switching tests at maximum rated operating temperature	Subgroup 10	3	0	3	0
Switching tests at minimum rated operating temperature	Subgroup 11	5	0	5	0

GROUP B TESTS
(by lot or weekly by package type and by lead finish)
MIL-STD-883/Method 5005

Group B tests	Method	Quantity/(Accept. no.) or LTPD
Subgroup 1 (a) Physical dimensions	2016	2 devices (no failures)
Subgroup 2 (a) Resistance to solvents	2015	4 devices (no failures)
Subgroup 3 (a) Solderability	2003	15
Subgroup 4 (a) Internal visual and mechanical	2014	1 device (no failures)
Subgroup 5 (a) Bond strength	2011	15
Subgroup 6 (1) (a) Internal water-vapor content	1018	No test (Packages contain no dessicant)
Subgroup 7 (1) (a) Seal	1014	5
Subgroup 8 (a) Electrical parameters (b) Electrical discharge sensitivity classification (c) Electrical parameters	3015	No test (Performed for initial qualification and product redesign)

GROUP C TESTS
(Every 3 months)
MIL-STD-883/Method 5005

Group C tests	Method	Quantity/(Accept. no.) or LTPD
Subgroup 1 (a) Steady state life test (1000 H - 125°C) (b) End-point electrical parameters	1005	5
Subgroup 2 (a) Temperature cycling (b) Constant acceleration Y1 orientation (c) Seal (1) Fine (2) Gross (d) Visual examination (e) End-point electrical parameters	1010 2001 1014	15

GROUP D TESTS
(Every 6 months)
MIL-STD-883/Method 5005

Group D tests	Method	Quantity/(Accept. no.) or LTPD
Subgroup 1 (a) Physical dimensions	2016	15
Subgroup 2 (a) Lead integrity (b) Seal (1) (1) Fine (2) Gross	2004 1014	15
Subgroup 3 (a) Thermal shock (b) Temperature cycling (c) Moisture resistance (d) Seal (1) Fine (2) Gross (e) Visual examination (f) End-point electrical parameters	1011 1010 1004 1014	15
Subgroup 4 (1) (a) Mechanical shock (b) Vibration, variable frequency (c) Constant acceleration (d) Seal (1) Fine (2) Gross (e) Visual examination (f) End-point electrical parameters	2002 2007 2001 1014	15
Subgroup 5 (a) Salt atmosphere (2) (3) (b) Seal (1) (1) Fine (2) Gross (c) Visual examination	1009 1014	15
Subgroup 6 (1) (a) Internal water-vapor content	1018	3 devices (0) failures or 5 devices (1 failure)
Subgroup 7 (1) (a) Adhesion of lead finish (2)	2025	15
Subgroup 8 (a) Lid torque (2)	2024	5 (0)

(1) For cavity packages only.
(2) No test for leadless chip carrier packages.
(3) According to package.

G/B QUALITY CONFORMANCE INSPECTION

The following tables comply with the NFC 96020 norms. This norm is quite similar to the MIL-STD-883 quality conformance *inspection from which it differs only on minor points.*

Lot acceptance test
The group A and B tests are performed on each lot (NFC 96020-Y level)

Quality conformance inspection for assembly process and technologies
These tests are accomplished with a periodicity of 3 or 6 months.
We perform practically all the tests of group C, as defined in the French standard NFC 96020, adopting methods compatible with book VII of methodic documentation of the CCT (UTE COO-192).

Tests of groups A and B (Y level) of the French Standard NFC 96020 performed on each lot

		DEVICES	ANALOG		LOGIC	
		CLASS	G/B LEVEL		G/B LEVEL	
Sub-group	TESTS	NFC96020 reference §	Inspection level	AQL %	Inspection level	AQL %
A1a	External visual inspection Marking conformance	6.1 6.1.1	II	0.4	II	0.4
A1b	Mechanical inoperatives	6.2	II	0.15	II	0.15
A2	Functional test at 25°C or at T° max (*)	Device specification	II	0.15	II	0.25
A3a	Main static tests at 25°C		II	0.4		
A3b	Complementary static tests at 25°C					
A4a	Functional and main static tests at maximum rated operating temperature		S4	1		
A4b	Functional and main static tests at minimum rated operating temperature				S4	1
A5	Main dynamic tests at 25°C or at T° max (*)		S4	1.5	II	0.25

		DEVICES	ANALOG and LOGIC	
			G/B LEVEL	
Sub-group	TESTS	NFC96020 reference §	Sample sizes or inspection levels	Acceptance criteria or AQL %
B1	Physical dimensions	6.3	11	0/1
B2	Solderability	M302	32	1/2
B3	Seal test (For cavity packages)	M303	I	1 %

Periodical test table

Sub-group	Tests	NFC 96020 reference §	Sample sizes	Accep. criteria
C1	Secondary physical dimensions weight	6.3	11	0
C2	Marking resistance to solvents	M 306	18	1
C3	Terminal strength	M 304	18	1
C4	- Resistance to soldering heating - Thermal shocks	M 301 C 203	25	1
(1)	- Accelerated damp heat	C 205		
C5 (2)	- Mechanical shocks - Vibrations - bumps - Constant acceleration	M 307 M 308 M 305	18	1
C6	Damp heat (steady state) (3)	C 204	18	1
C8	Life test 1000 H at high temperature (4)	E 401 or E 403 and device spec.	25	1
C9	High temperature storage	E 402	18	1
C13	Salt atmosphere (5)	C 202	8	1

These tests are accomplished with a periodicity of 3 or 6 months.
They regroup practically all the tests of group C, as defined in the French standard NFC 96020, adopting methods compatible with book VII of the CCT methodic documentation (UTE C00-192).

(1) For plastic packages
(2) For ceramic and metal glass packages
(3) 10 days for gold plated leads
56 days for tin plated leads or tin dipped leads
(4) Max junction temperature : 150°C for cavity packages
130°C for plastic packages
(5) According to package (once a year).

5

D and STANDARD QUALITY CONFORMANCE INSPECTIONS

The following tables comply with the NFC 96020 norms. This norm is quite similar to the MIL-STD-883 quality conformance inspection from which it differs only on minor points.

Lot acceptance test
The group A and B tests are performed on each lot (NFC 96020-Y level)

Quality conformance inspection for assembly process and technologies
These tests are accomplished with a periodicity of 3 or 6 months.
We perform practically all the tests of group C, as defined in the French standard NFC 96020, adopting methods compatible with book VII of methodic documentation of the CCT (UTE COO-192).

Tests of groups A and B (Y level) of the French Standard NFC 96020 performed on each lot

		DEVICES	ANALOG		LOGIC	
		CLASS	STANDARD & D LEVELS		STANDARD & D LEVELS	
Sub-group	TESTS	NFC96020 reference §	Inspection level	AQL %	LTPD	Accept. criteria
A1a	External visual inspection Marking conformance	6.1 6.1.1	II	0.4	3	2/3
A1b	Mechanical inoperatives	6.2	II	0.25	3	1/2
A2	Functional test at 25°C or at T° max (*)	Device specification	II	0.15	3(*) @ T°max.	1/2
A3a	Main static tests at 25°C		II	0.4		
A3b	Complementary static tests at 25°C					
A4a	Functional and main static tests at maximum rated operating temperature		S4	1		
A4b	Functional and main static tests at minimum rated operating temperature				No test	No test
A5	Main dynamic tests at 25°C or at T° max (*)		No test	No test	5(*) @ T°max.	3/4

		DEVICES	ANALOG and LOGIC	
			STANDARD/D LEVELS	
Sub-group	TESTS	NFC96020 reference §	Sample sizes or inspection levels	Acceptance criteria or AQL %
B1	Physical dimensions	6.3	11	0/1
B2	Solderability	M302	32	1/2
B3	Seal test (For cavity packages)	M303	I	1 %

Periodical test table

Sub-group	Tests	NFC 96020 reference §	Sample sizes	Accep. criteria
C1	Secondary physical dimensions weight	6.3	11	0
C2	Marking resistance to solvents	M 306	18	1
C3	Terminal strength	M 304	18	1
C4	- Resistance to soldering heating - Thermal shocks	M 301 C 203	25	1
(1)	- Accelerated damp heat	C 205		
C5 (2)	- Mechanical shocks - Vibrations - bumps - Constant acceleration	M 307 M 308 M 305	18	1
C6	Damp heat (steady state) (3)	C 204	18	1
C8	Life test 1000 H at high temperature (4)	E 401 or E 403 and device spec.	25	1
C9	High temperature storage	E 402	18	1
C13	Salt atmosphere (5)	C 202	8	1

These tests are accomplished with a periodicity of 3 or 6 months.
They regroup practically all the tests of group C, as defined in the French standard NFC 96020, adopting methods compatible with book VII of the CCT methodic documentation (UTE C00-192).

(1) For plastic packages
(2) For ceramic and metal glass packages
(3) 10 days for gold plated leads
56 days for tin plated leads or tin dipped leads
(4) Max junction temperature : 150°C for cavity packages
130°C for plastic packages
(5) According to package (once a year).

DICE QUALITY LEVELS

Eight different quality levels are available for dice (*)

LEVEL A

- Wafer selection
- Wafer probe at room temperature
- Wafer inspection
- Packing
- Final acceptance (AQL: 1.5 - level 2)
- Shipment

LEVEL P

- Wafer selection
- Wafer probe at room temperature
- Wafer inspection
- Partial scribing
- Packing
- Final acceptance (AQL: 1.5 - level 2)
- Shipment

(*) Please inquire with our sales offices for the availability of the product you are interested in.

LEVEL S

- Wafer selection
- Wafer probe at room temperature
- Wafer inspection
- Scribing
- Packing
- Final acceptance (AQL: 1.5 - level 2)
- Shipment

LEVEL E

- Wafer selection
- Wafer probe at room temperature
- Wafer inspection
- Scribing
- Waffle packing of good dice
- Final acceptance (AQL: 2.5 - level 2)
- Shipment

LEVEL V

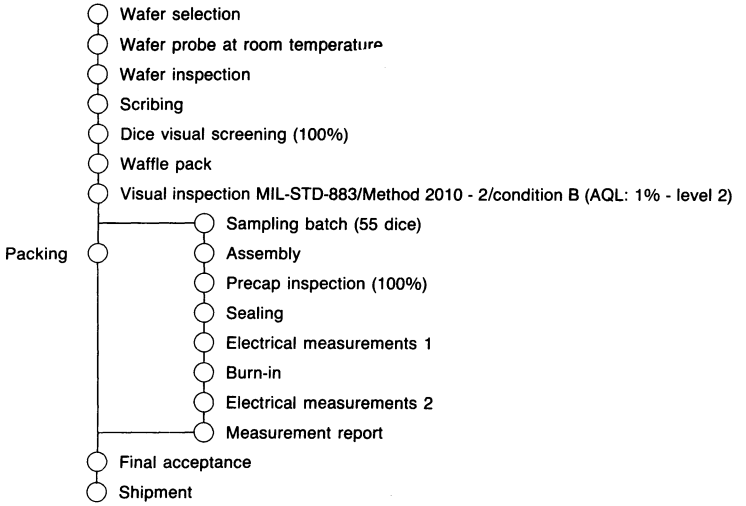
- Wafer selection
- Wafer probe at room temperature
- Wafer inspection
- Scribing
- Dice visual screening (100%) according to MIL-STD-883/Method 2010
- Waffle pack
- Visual inspection (sampling) MIL-STD-883/Method 2010 - 2/condition B
- Packing
- Final acceptance (AQL: 1.5 - level 2)
- Shipment

LEVEL N

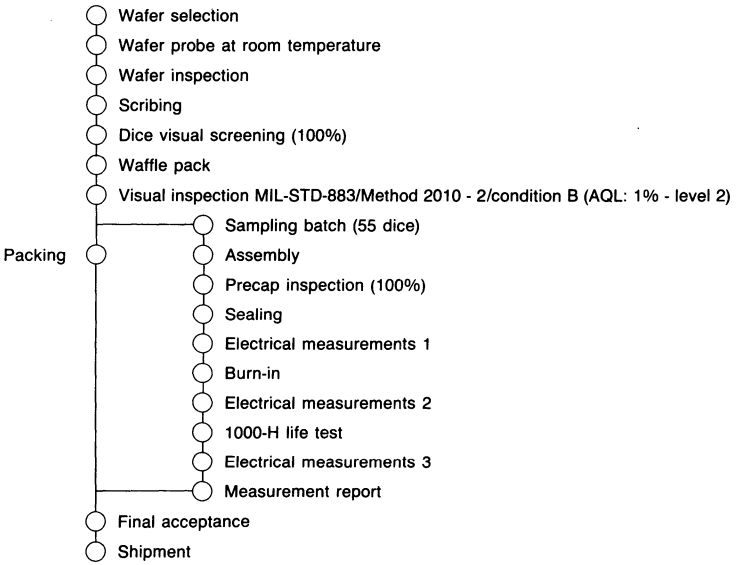
- Wafer selection
- Wafer selection at room temperature
- Wafer inspection
- Scribing
- Dice visual screening (100%)
- Waffle pack
- Visual inspection MIL-STD-883/Method 2010 - 2/condidion B (AQL: 1% - level 2)
- Packing
  - Sampling batch (55 dice)
  - Assembly
  - Precap inspection (100%)
  - Sealing
  - Electrical measurements
  - Measurement report
- Final acceptance
- Shipment

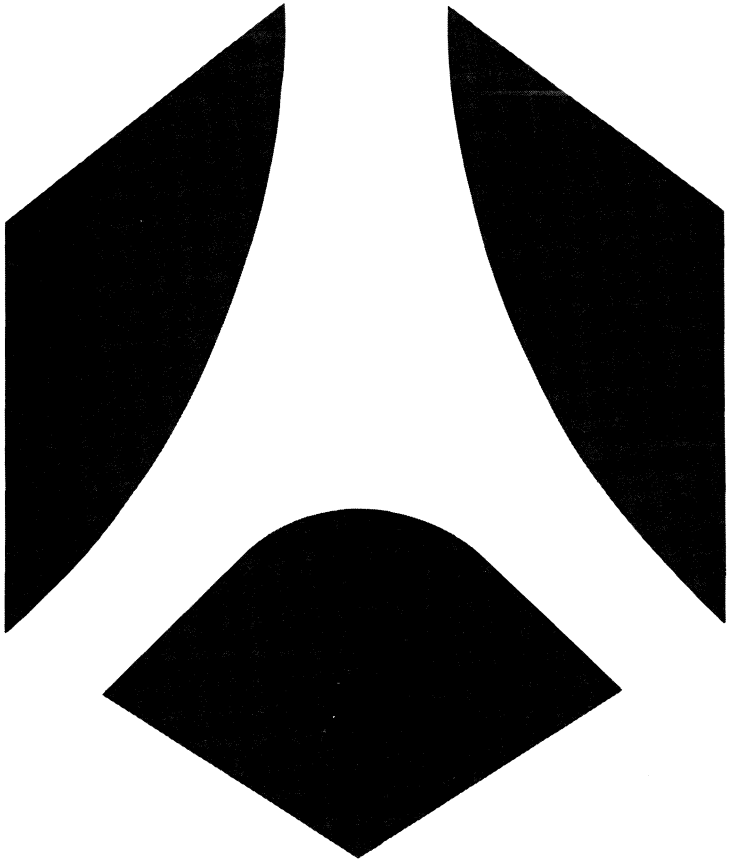
5

LEVEL T



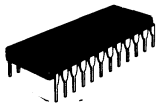
LEVEL Z

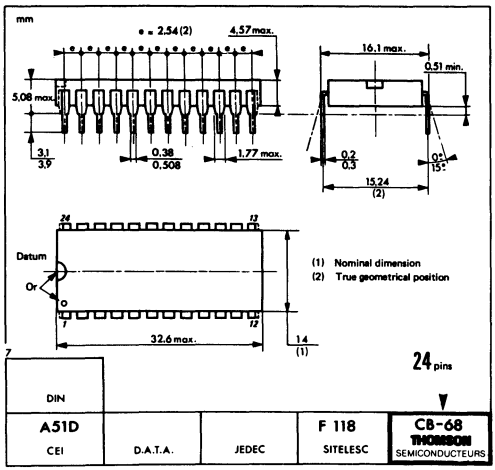




6

Package dimensions

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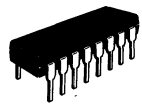
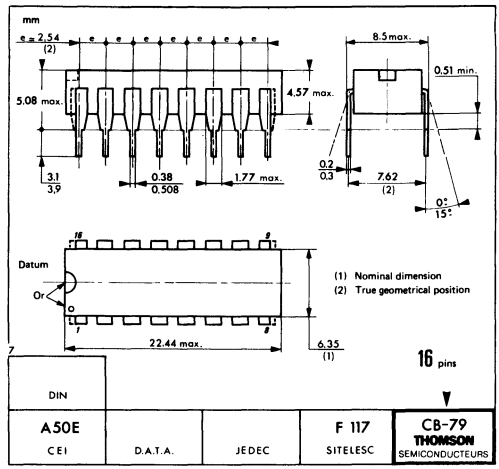
4.57 max.
16.1 max.
0.51 min.
5.08 max.
3.1
3.9
0.38
0.508
1.77 max.
0.2
0.3
0°
15°
15.24
(2)
Datum
Or
(1) Nominal dimension
(2) True geometrical position
32.6 max.
1.4
(1)
24 pins
DIN
A51D
CEI
D.A.T.A.
JEDEC
F 118
SITELESC
CB-68
THOMSON
SEMICONDUCTEURS

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(2)
8.5 max.
0.51 min.
4.57 max.
5.08 max.
3.1
3.9
0.38
0.508
1.77 max.
0.2
0.3
7.62
(2)
0°
15°
Datum
Or
(1) Nominal dimension
(2) True geometrical position
22.44 max.
6.35
(1)
16 pins
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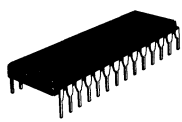
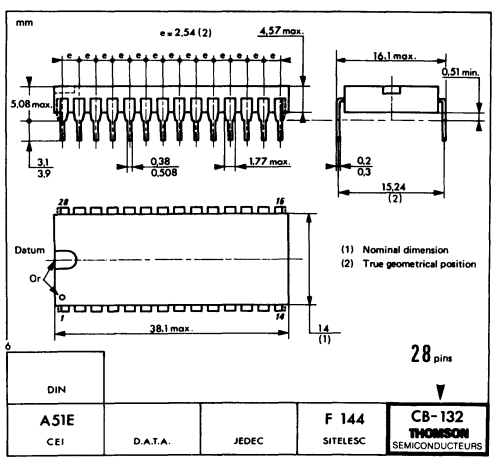
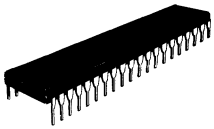
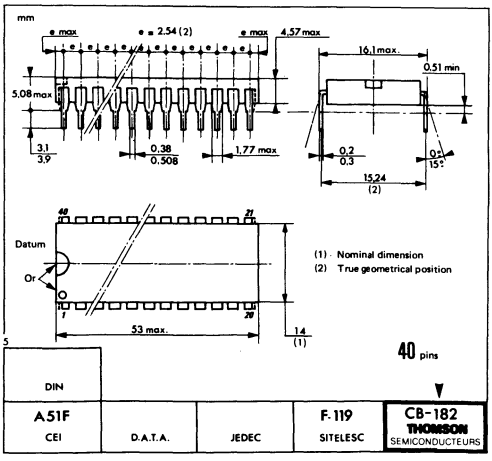
A50E
CEI
D.A.T.A.
JEDEC
F 117
SITELESC
CB-79
THOMSON
SEMICONDUCTEURS




mm
e = 2.54 (2)
4.57 max.
16.1 max.
0.51 min.
5.08 max.
3.1
3.9
0.38
0.508
1.77 max.
0.2
0.3
15.24
(2)
Datum
Or
(1) Nominal dimension
(2) True geometrical position
38.1 max.
1.4
(1)
28 pins
DIN
A51E
CEI
D.A.T.A.
JEDEC
F 144
SITELESC
CB-132
THOMSON
SEMICONDUCTEURS

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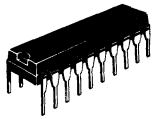
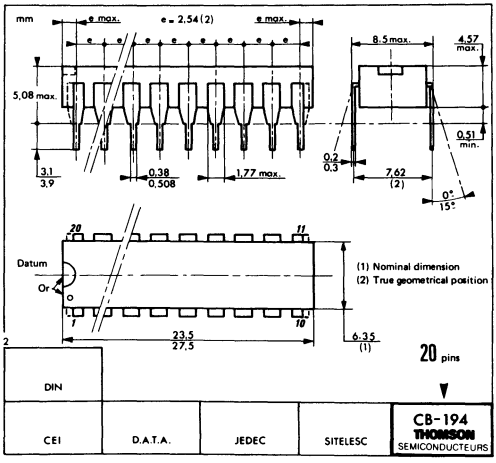
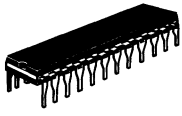
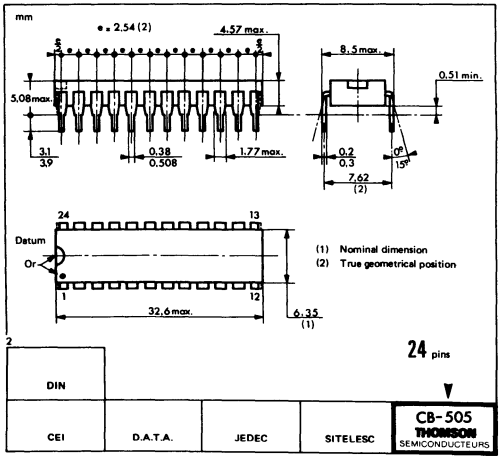
e max
e = 2.54 (2)
e max
4,57 max
5,08 max
16,1 max.
0,51 min
3,1
3,9
0,38
0,508
1,77 max
0,2
0,3
0°
15°
15,24
(2)
40
21
Datum
Or
1
20
53 max.
14
(1)
(1) Nominal dimension
(2) True geometrical position
5
40 pins
DIN
A51F
CEI
D.A.T.A.
JEDEC
F-119
SITELESC
CB-182
THOMSON
SEMICONDUCTEURS

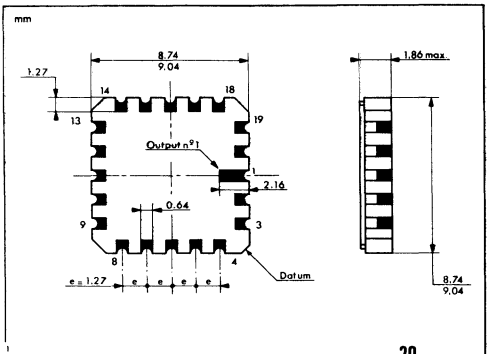



mm
e max.
e = 2.54 (2)
e max.
8,5 max.
4,57
max.
5,08 max.
0,51
min.
3,1
3,9
0,38
0,508
1,77 max.
0,2
0,3
7,62
(2)
0°
15°
20
11
Datum
Or
1
10
23,5
27,5
6,35
(1)
(1) Nominal dimension
(2) True geometrical position
2
20 pins
DIN
CEI
D.A.T.A.
JEDEC
SITELESC
CB-194
THOMSON
SEMICONDUCTEURS



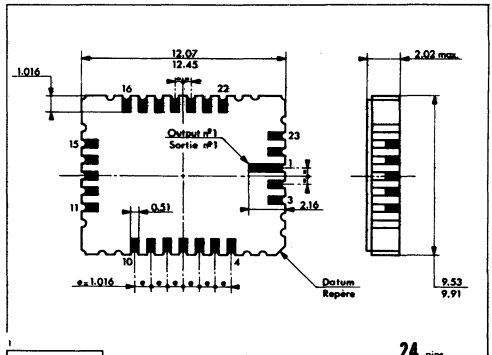

mm
e = 2.54 (2)
4,57 max.
8,5 max.
0,51 min.
5,08 max.
3,1
3,9
0,38
0,508
1,77 max.
0,2
0,3
0°
15°
7,62
(2)
24
13
Datum
Or
1
12
32,6 max.
6,35
(1)
(1) Nominal dimension
(2) True geometrical position
2
24 pins
DIN
CEI
D.A.T.A.
JEDEC
SITELESC
CB-505
THOMSON
SEMICONDUCTEURS

6



DIN				
MS004 CB		TMS004 CB		CB-705 THOMSON SEMICONDUCTEURS
CEI	D.A.T.A.	JEDEC	SITELESC	

20 pins



DIN				
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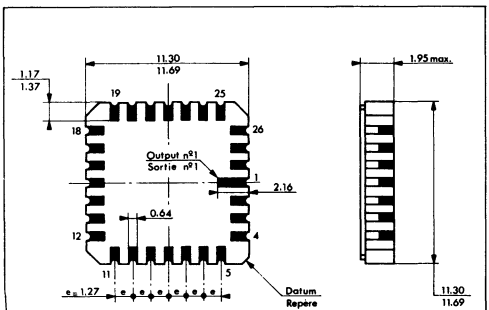
24 pins



DIN				
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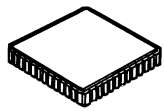
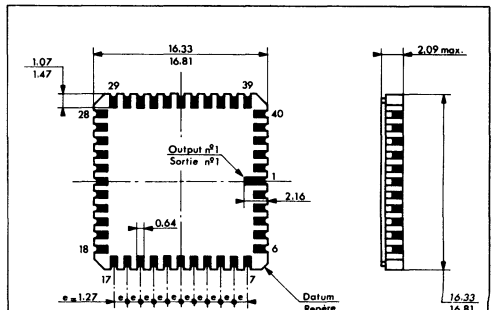
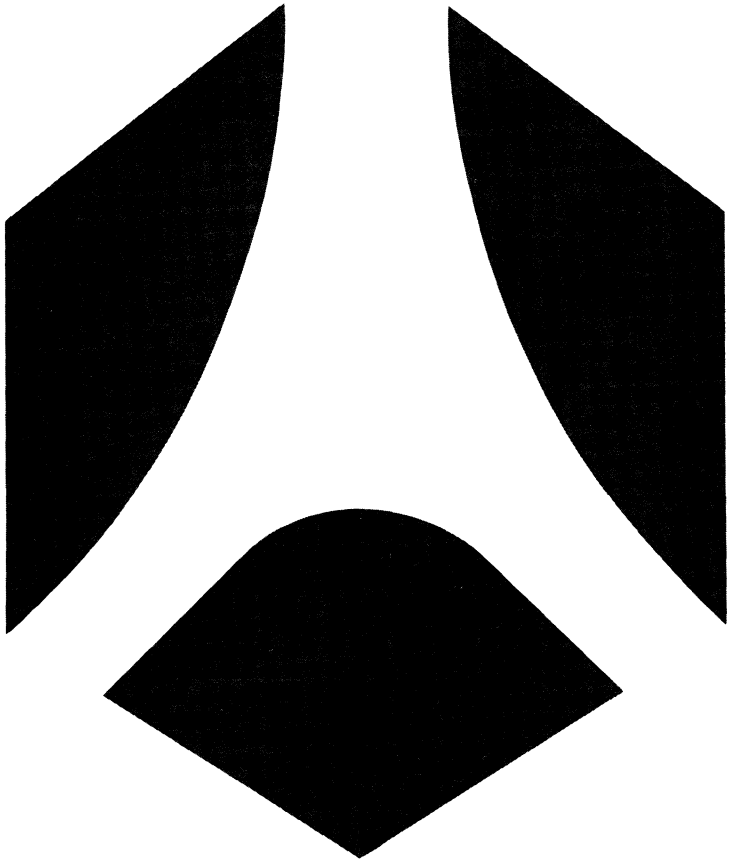
28 pins





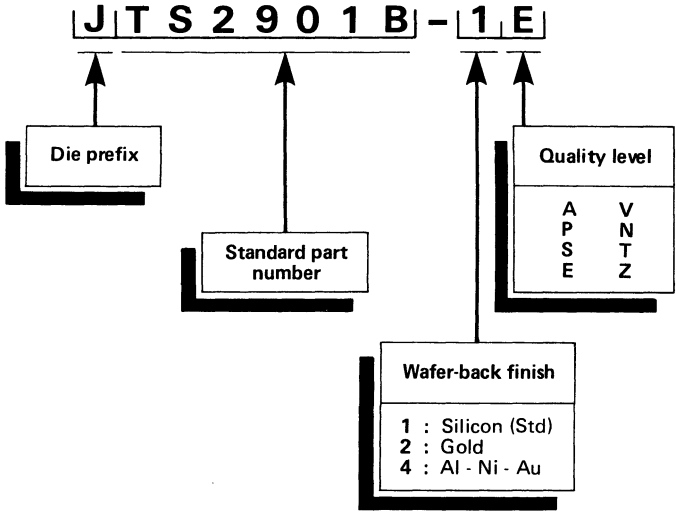
DIN				
CEI	D.A.T.A.	JEDEC	SITELESC	CB-708 THOMSON SEMICONDUCTEURS

44 pins



Ordering information

DICE ORDERING INFORMATION



Each THOMSON SEMICONDUCTEURS linear circuit supplied in chip or wafer form has a special ordering code divided as follows:

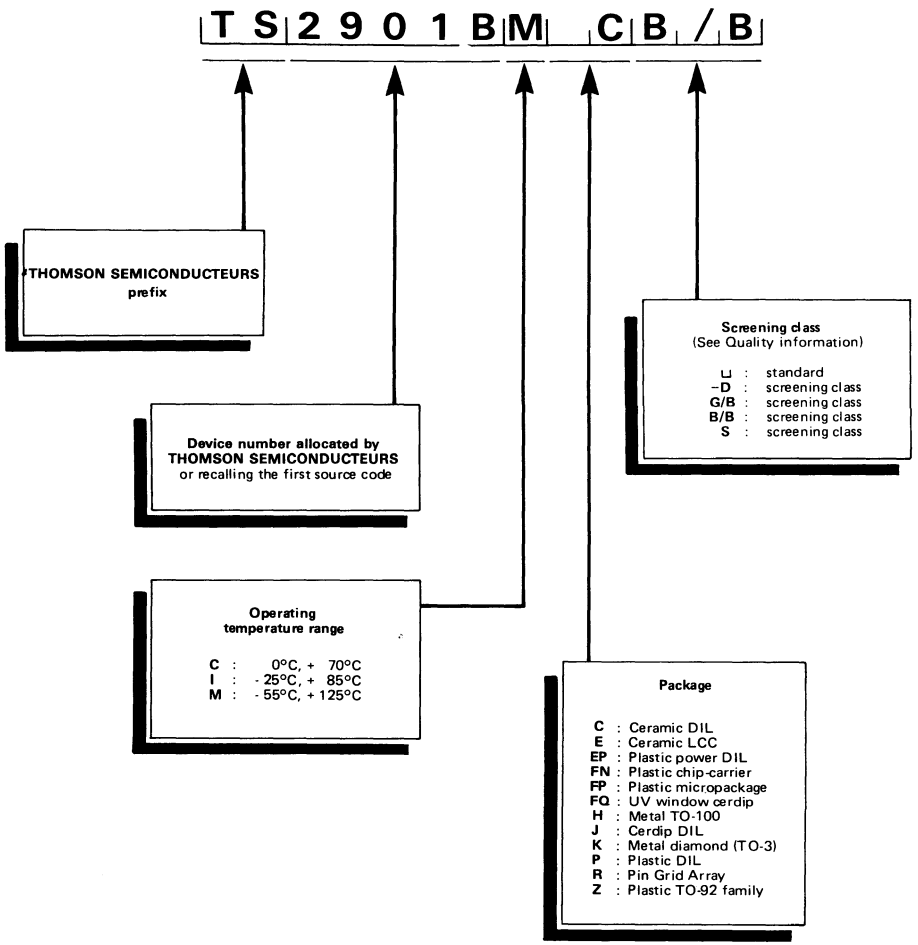
MAIN CODE (Device specification)

- beginning with **J** (Common to all devices)
- followed by the part number of the equivalent packaged device

COMPLEMENTARY CODE (Wafer-back finish and quality level)

After a dash, two characters are used
- a figure indicating the choice of wafer-back finish
- a letter to specify the quality level

A : Wafer
P : Scribed wafer
S : Wafer on adhesive tape with separated chips
E : Chips in waffle pack without visual inspection
V : Chips in waffle pack with 100 % visual inspection according to MIL - STD - 883 / Method 2010
N : V level plus sampling batch of 55 packaged ICs
T : N level plus burn-in on sampling batch of 55 packaged ICs
Z : T level plus 1000 H life test on sampling batch of 55 packaged ICs


T S 2 9 0 1 B M C B / B
THOMSON SEMICONDUCTEURS
prefix
Device number allocated by
THOMSON SEMICONDUCTEURS
or recalling the first source code
Operating
temperature range
C : 0°C, + 70°C
I : - 25°C, + 85°C
M : - 55°C, + 125°C
Package
C : Ceramic DIL
E : Ceramic LCC
EP : Plastic power DIL
FN : Plastic chip-carrier
FP : Plastic micropackage
FQ : UV window cerdip
H : Metal TO-100
J : Cerdip DIL
K : Metal diamond (TO-3)
P : Plastic DIL
R : Pin Grid Array
Z : Plastic TO-92 family
Screening class
(See Quality information)
␣ : standard
-D : screening class
G/B : screening class
B/B : screening class
S : screening class

THOMSON SEMICONDUCTEURS

SALES HEADQUARTERS
43-45, AVENUE DE L'EUROPE
78140 VELIZY-VILLACOUBLAY
TEL. (1)39.46.97.19 / TELEX : TCSF 204 780 F

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SUBSIDIARIES (March 1985)

AUSTRIA

THOMSON-CSF Elektronische Anlagen GmbH
Lützowgasse 12-14
1140 WIEN
Tel. (222) 94.62.82 Telex : 135572 TCSF WA

BELGIUM and The NETHERLANDS

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363 Avenue Louise B.P. 10
B-1050 BRUXELLES
Tel. (2) 648.64.85 Telex 23113 THBXL B

BRAZIL

THOMSON-CSF Componentes do Brasil
Avenida Roque Petroni JR S-N Brooklin
SAO PAULO CEP 04707
Tel. (55 11) 542.47.22 Telex 1124226 TCSF BR

CANADA

THOMSON-CSF Canada Ltd
Departement Semiconducteurs
1000 Sherbrooke ouest
suite 2105
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Dépôt légal : Octobre 1985

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